

DC-DC Converters with High Efficiency over Wide Load Ranges

by

Joshua Harlen Bretz

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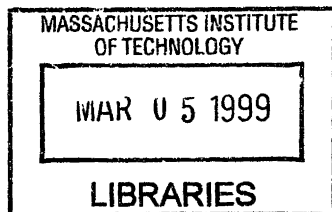
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Signature of Author:
Department of Electrical Engineering
January 30, 1999

Certified by:
Anantha P. Chandrakasan
Associate Professor of Electrical Engineering
Thesis Supervisor

Accepted by:
Arthur Clarke Smith
Professor of Electrical Engineering
Chairman, Committee for Graduate Students



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Joshua Harlen Bretz

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Abstract

An integrated switching regulator is presented, including theory of operation, circuit design, and test results. This DC-DC converter introduces several novel circuits which enable more efficient operation at output powers from $100\mu\text{W}$ to 1W . Efficiency above 80% is achieved from $500\mu\text{W}$ to 500mW . Specifically, depending on the load current, the regulator automatically switches between Pulse Frequency Modulation (PFM) and Pulse Width Modulation (PWM), and also automatically selects the optimum switching MOSFET. The current sensing is done without an additional current sense resistor. PFM mode operation is synchronous to allow sampled data systems to avoid sampling on switching transitions. In all modes of operation, the regulator output voltage is digitally programmable. This enables variable voltage architectures, in which the power supply of a digital system is dynamically changed depending on the throughput requirements, resulting in significant power reductions.

Thesis Supervisor: Anantha P. Chandrakasan
Title: Associate Professor of Electrical Engineering

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1 Problem Statement and Solution

1.1 Improved Battery Life

Switching regulators are often used in battery powered system to create a constant output voltage even as the battery open circuit voltage diminishes over time. This yields longer battery life than if the system were powered directly from the battery [1,2]. Since the battery voltage goes down over time, the system would have to be designed to operate at the battery open circuit voltage corresponding to a reasonably large depth of discharge. But, this implies that for the majority of time, the system is operating at a higher supply voltage than its minimum. This leads to a significant battery life reduction since the power of digital circuitry is roughly proportional to the square of the supply voltage. A switching regulator allows operation much nearer to the minimum system supply voltage for a larger portion of the battery discharge cycle. In this manner, the addition of a switching regulator typically adds at least 20% to the system battery lifetime.

1.2 Variable Voltage Systems

In digital systems, the minimum required supply voltage is reduced if the computation can take a longer time [3,4]. Given a workload 50% of the maximum throughput, there are two ways to reduce power. (See Figure 1) First, the computation can be done at speed with the nominal supply voltage, and the system can be powered down for the second half of the given time. Alternatively, the supply voltage could be reduced by about a factor of two, causing the computation time to extend to fill the given time. The second method requires approximately one quarter as much power as the first

method. As the power supply approaches the transistor threshold voltage (V_t), the increases are not as dramatic since the circuit delay is no longer linearly proportional to V_{dd} .

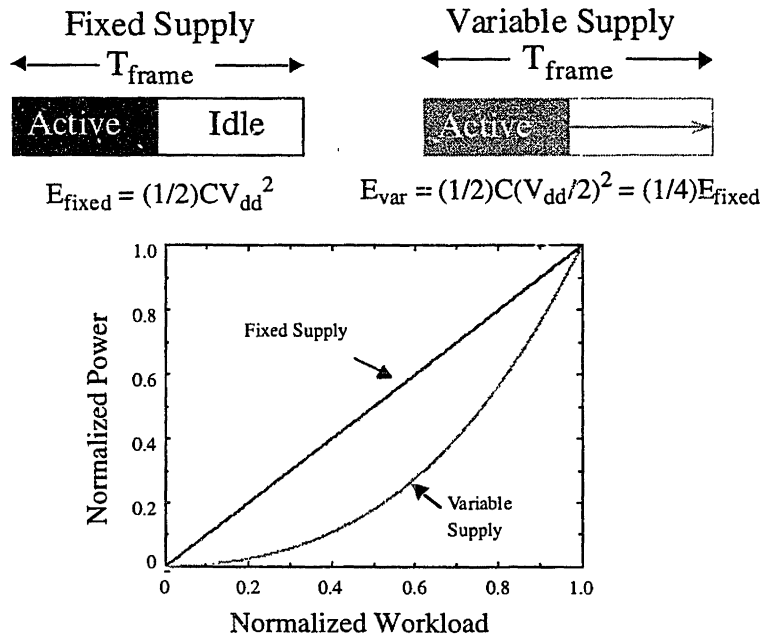


Figure 1: Variable Voltage Power Supply

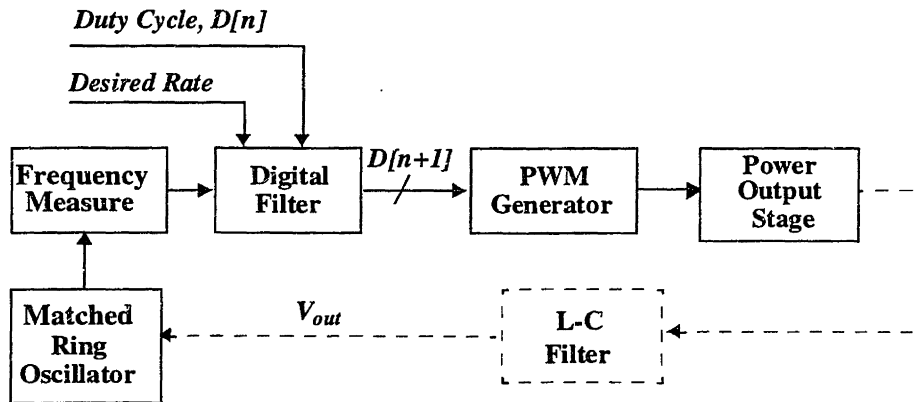


Figure 2: Variable Voltage Feedback Control

A feedback loop can be made to generate the minimum valid supply voltage by measuring a performance indicator of the system [5]. (See Figure 2) A ring oscillator

can be constructed from components identical to the calculated critical path of the digital system. The rest of the system is clocked at the ring oscillator frequency. This frequency can be measured and used to control the supply voltage. If the frequency and therefore system throughput is too low, the supply voltage can be raised, and vice-versa. An added advantage is that the system does not need to be designed with an additional built in timing margin to account for process and temperature variations. A constant timing margin can be automatically generated by adding an additional delay to the ring oscillator.

1.3 Widely Variable System Power

Many battery powered systems have widely changing power requirements over time. A good example is a wireless video camera, in which video is captured digitally at a variable resolution, and then compressed and encrypted before transmission over a radio channel. (See Figure 3)

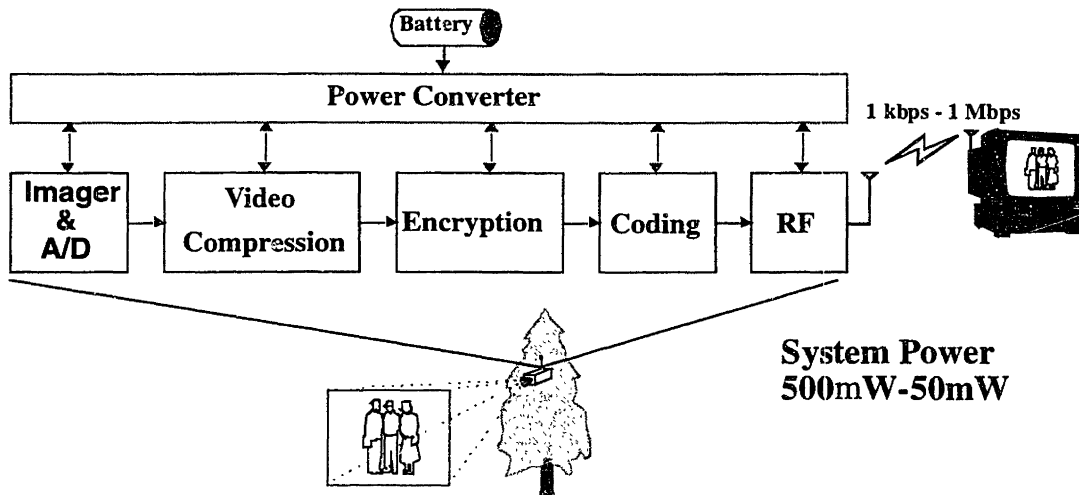


Figure 3: A Wireless Digital Video Camera

When there is no motion in the field of vision of the camera, the image sensor can lower its resolution and there is a very low data rate through the compression, encryption,

and radio channel. Therefore, the standby power can be very low, on the order of $500\mu\text{W}$. However, when there is quick motion, successive frames are less correlated, and a large amount of data must be transmitted. Therefore, the active power can be relatively high, on the order of 50mW . In a surveillance application, the times with motion are very valuable. While in standby, the camera must know when to activate and capture these moments. Circuit functionality in both the low and high power regimes is necessary for success.

Often, the system is in standby mode for the vast majority of the time. If this is the case, then the power converter efficiency in standby mode could determine the overall battery life as much as the efficiency in the active mode. The power converter must have high efficiency over a large range of output power, in this case, all the way from $500\mu\text{W}$ to 50mW . Conventional switching regulator architectures do not achieve this.

1.4 Noise Suppression

Switching regulators can generate a significant amount of conducted and radiated noise. This noise is concentrated at the times when switching events take place. One way to reduce noise in sampled data systems is to synchronize the system to the switching frequency of the regulator, so that sampling never takes place near a switching event. As will become evident in Chapter 2, synchronization is simple in Pulse Width Modulation (PWM) mode. However, in conventional implementations of Pulse Frequency Modulation (PFM) mode, switching events are not synchronous.

1.5 Solutions

An integrated circuit was fabricated which contains all elements of a switching regulator except the filter inductor and capacitor. It is designed for output powers from $100\mu\text{W}$ to 1W . Higher efficiency than conventional converters is maintained at the power extremes by automatically switching to Pulse Frequency Modulation (PFM) mode at low powers, and Low Switch Resistance (LSR) mode at high powers. Switching events are synchronous even in PFM mode. In all modes, the output voltage can be dynamically controlled for use in variable voltage systems.

2 Circuit Theory of Operation

2.1 Buck Regulator Circuit Background

The switched mode power converter is inherently more efficient than a linear power regulator. A typical linear regulator circuit is shown in Figure 4. The voltage drop across M1 is maintained as the difference between the input and output voltages. This voltage drop translates into a large power loss since all the output current goes through M1. Neglecting the power overhead of the amplifier, reference, and voltage divider, the efficiency is limited to:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} \cdot I_L}{V_{in} \cdot I_L} = \frac{V_{out}}{V_{in}}$$

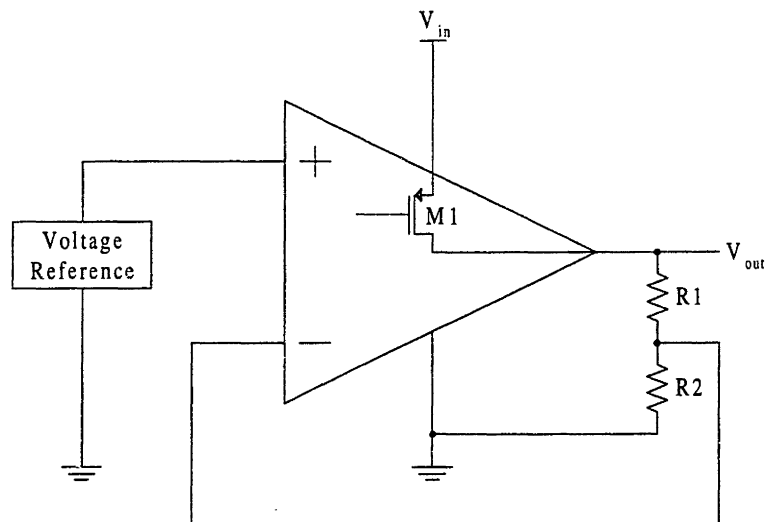


Figure 4: A representative linear regulator circuit

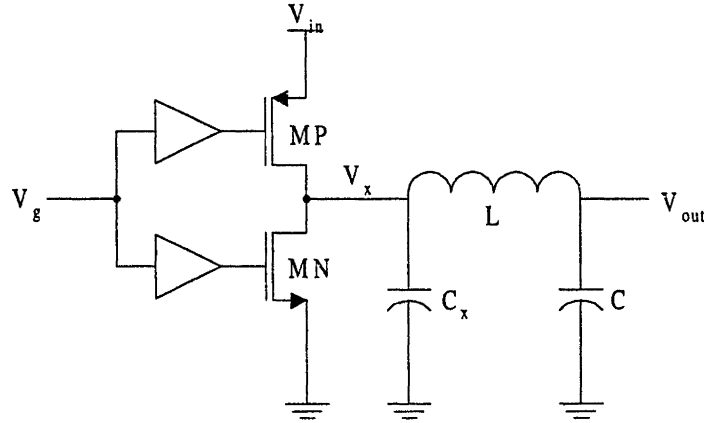


Figure 5: The Buck switching regulator circuit

In a switched mode power supply, there is never a large voltage drop across the switching transistors. The transistor channel widths are made very large, and they are either fully on or fully off. The "buck converter" topology is shown in Figure 5. It is configured to convert a higher voltage to a lower voltage. There are many other possible configurations. For instance, a boost converter creates a higher voltage, and a buck-boost converter creates a negative voltage, which can be larger or smaller in magnitude than the input voltage [6]. The buck converter works by creating a pulse-width modulated (PWM) waveform at the node V_x , as shown in Figure 7. The inductor and capacitor act together as a second order low-pass filter. They are selected to have a low cutoff frequency with respect to the switching frequency (f_{sw}). Thus, the output of the filter, V_{out} , is approximately the DC value of the V_x waveform. As the duty cycle (D) of this waveform is increased, the average value of V_x increases, so V_{out} increases.

Alternatively, in the steady state, the current in the inductor must return to the same value after each cycle, and the current increase while the p MOSFET is conducting must equal the current decrease while the n MOSFET is conducting:

$$\begin{aligned} \left[\left(\frac{di_L}{dt} \right) (\Delta t) \right]_{PMOS-on} + \left[\left(\frac{di_L}{dt} \right) (\Delta t) \right]_{NMOS-on} &= 0 \\ \left[\left(\frac{V_{in} - V_{out}}{L} \right) (Dt_s) \right] + \left[\left(\frac{-V_{out}}{L} \right) ((1-D)t_s) \right] &= 0 \\ V_{out} &= DV_{in} \end{aligned}$$

2.1.1 Ripple Current and Voltage

In addition to a DC value, V_{out} also has a small AC ripple component. This is since the filter does not completely reject the V_x signal at the switching frequency. Higher harmonics are filtered out more, so they are not as important as the fundamental frequency. The output voltage ripple is the integral of the current ripple in the inductor. Both depend on the duty cycle, with the maximum ripple at 50% duty cycle. The inductor current ripple is larger if the switching period is larger, or the inductor is smaller.

$$\begin{aligned} \Delta i_L &= \left[\frac{V_{out}}{V_{in}} (V_{in} - V_{out}) \right] \frac{t_s}{L} = [V_{in} (D - D^2)] \frac{t_s}{L} \\ \Delta i_L^{\max} &= \frac{V_{in} t_s}{4L} \\ \Delta V_{out} &= \Delta i_L \frac{t_s}{8} \\ \Delta V_{out}^{\max} &= \frac{V_{in} t_s^2}{32LC} \end{aligned}$$

Where t_s is the inverse of the switching frequency. The inductor current ripple increases as the switching frequency decreases, or the inductor value decreases. The voltage ripple is inversely proportional to the square of the switching frequency. Figure 6 shows an actual oscilloscope trace of the output voltage ripple.

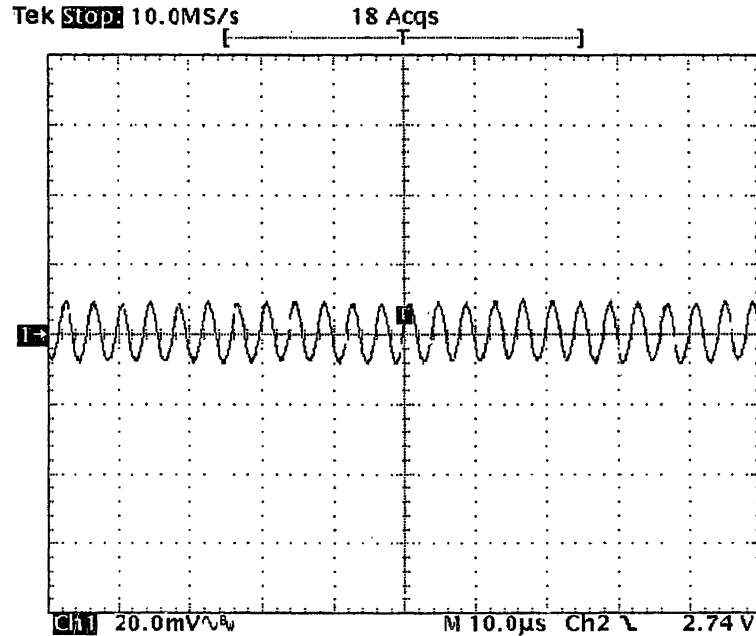


Figure 6: Output voltage ripple in PWM mode

2.1.2 Sources of Loss

With ideal components, the switching converter has 100% efficiency. However, MOSFETs are not ideal switches. Power is lost in three areas. First, switching the gates and the V_x capacitance at the frequency f_{sw} costs:

$$P_{sw} = \alpha (C_{gs}^n + C_{gs}^p) V_{in}^2 f_{sw}$$

Where C_{gs} is the gate to source capacitance of the n and p channel MOSFETs. α is a number larger than 1, which represents the total switched capacitance including the additional capacitance of the gate driver circuits. For instance, if the total gate capacitance of the driver circuits were 30% as large as the gate capacitance of the output switch itself, then α would be equal to 1.30.

Second, resistance in the switches and inductor costs:

$$P_{res} = \left(I_{L,av}^2 + \frac{\Delta i_L^2}{12} \right) \left[R_{ind} + R_{sw}^n D + R_{sw}^p (1 - D) \right]$$

Where Δi_L is the inductor current ripple (See section 2.1.1) The duty cycle (D) factors in since the high and low output switches trade off conducting the output current. R_{ind} is not related to the duty cycle since the output current always flows through the inductor.

When the average load current is high, the resistive power loss is high. Even when the average load current is low, there remains a resistive power loss due to the constant inductor ripple current.

R_{sw} is the channel resistance of the n and p MOSFET switches in the linear region:

$$R_{sw} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{gs} - V_t)}$$

Where μ is the electron or hole mobility, C_{ox} is the gate oxide capacitance per unit area, W and L are the dimensions of the gate, V_t is the absolute value of the threshold voltage, and V_{gs} is the gate to source voltage applied to the MOSFET when it is on.

Third, there is power lost in the circuits for feedback control and pulse generation. Put together, the gate switching, resistive, and overhead losses typically place the peak efficiency of a switching regulator above 90%. However, switching losses dominate at low output currents, and resistive losses dominate at high output currents. Thus, the peak efficiency is generally only maintained over a relatively narrow window of load current.

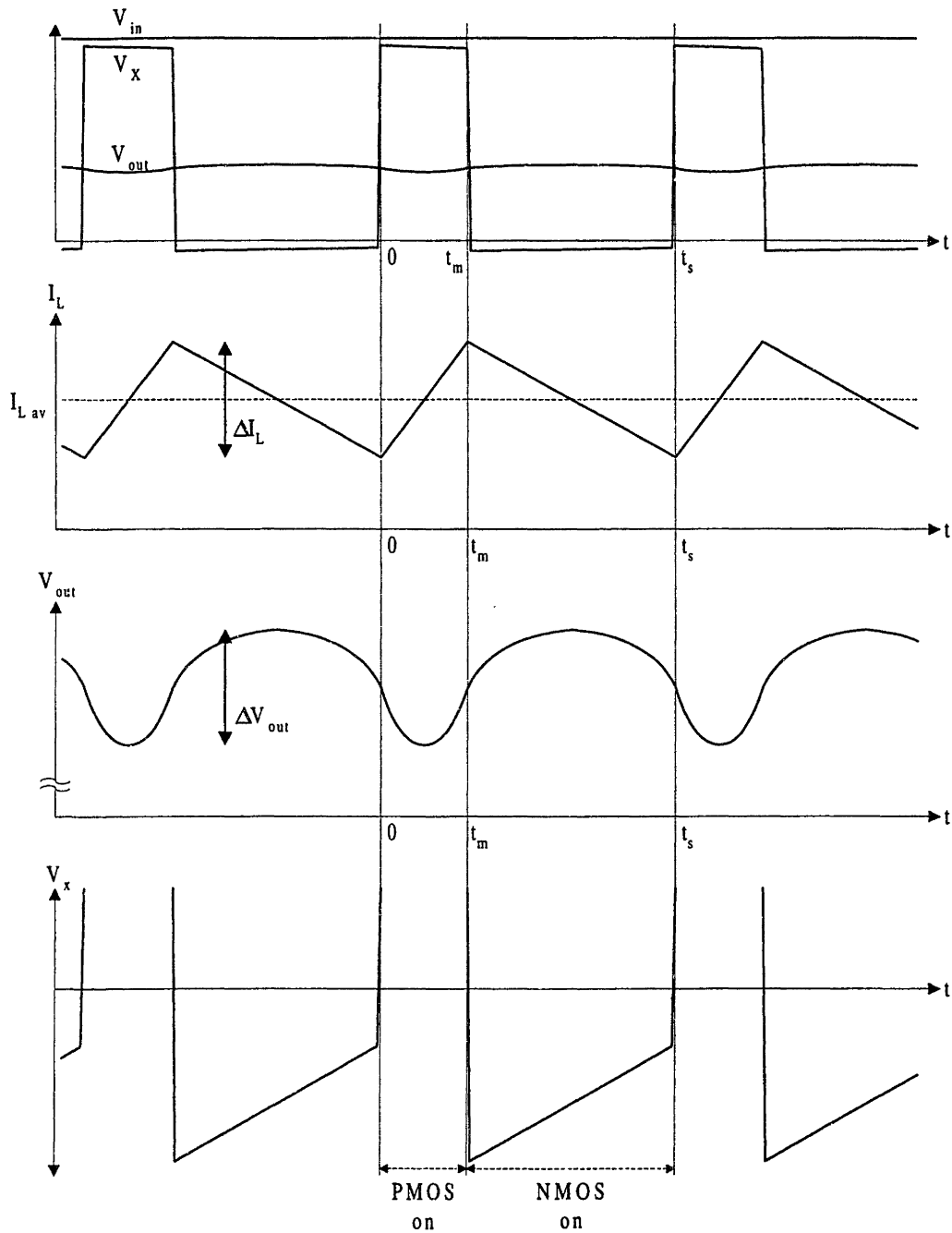


Figure 7: Buck converter waveforms

2.1.3 Closed Loop Feedback Control

Closed loop feedback control is implemented to synthesize the correct duty cycle for the desired output voltage. Feedback control improves transient response to changes

in load current and input voltage. The best controller is constructed using full state feedback, where both the filter inductor current and filter capacitor voltage are monitored. However, measuring the inductor current accurately in continuous time requires a relatively high gain and bandwidth amplifier, which uses a lot of power. The gain must be high because the current sense resistor inserted in series with the filter inductor must be small for low power loss. The bandwidth must be relatively high to minimize tracking error of the inductor current. Therefore, for low power converters usually only the capacitor voltage is used in the feedback loop.

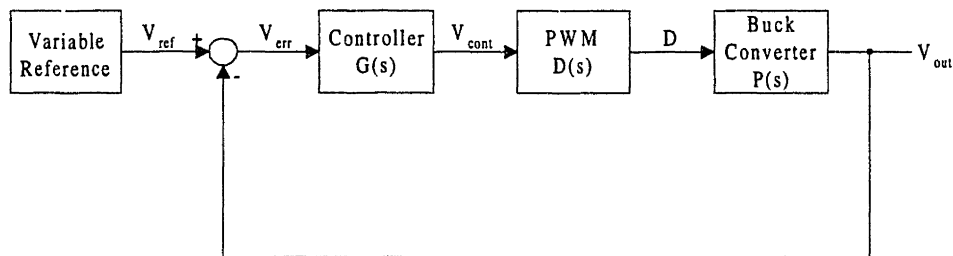


Figure 8: Feedback Block Diagram

A block diagram of the feedback loop is shown in Figure 8. The system transfer function $P(s)$ from small signal changes in commanded duty cycle to small changes in output voltage exhibits several important features.

$$P(s) = \frac{\tilde{V}_{out}}{\tilde{D}} \cong \frac{V_{in}}{LCs^2 + \frac{L}{R_L}s + 1}$$

Since the average value at V_x depends linearly on V_{in} , $P(s)$ depends linearly on V_{in} . Stability of the closed loop system must be guaranteed for the highest V_{in} possible since this represents the highest possible gain and therefore the highest unity gain crossover frequency. The transfer function also has a peak at the resonant frequency of the filter. In the closed loop system, this peak can cause oscillations if the loop gain is greater than

one that the resonant frequency, assuming integral control. The height of the peak depends on the damping provided by the load resistance and the switch resistance. As the output current goes down, the equivalent output resistance goes up, and less damping is provided. Higher switch resistance also reduces the height of the resonant peak. Stability of the closed loop system must be guaranteed for the highest resonant peak possible.

The transfer function $D(s)$ models delays in the control system. There is always a delay in the pulse generation circuit, which can be modeled as one half of a switching period. There is also a delay if the output is sampled discretely, equal to the sampling frequency.

$$D(s) = \frac{\tilde{D}}{\tilde{V}_{cont}} \equiv e^{-st_{delay}}$$

One possible control law is a simple gain and integrator:

$$G(s) = \frac{\tilde{V}_{cont}}{\tilde{V}_{err}} = \frac{K}{s}$$

It is possible to use more aggressive control to increase the loop bandwidth, but it comes at the cost of much higher control power overhead [7]. In a low power converter, the unity gain crossover frequency is typically placed low enough so that there is adequate phase margin, and so that the highest possible resonant peak does not also have above unity gain.

2.2 Alternative Modes of Operation

Different loss mechanisms become dominant in PWM mode as the load current changes. As load current increases, the power lost due to channel resistance goes up. Therefore, at high output currents this loss dominates, and at low output currents it is

negligible. In contrast, the gate switching losses and control losses are constant with load current. Therefore, these losses dominate at low output currents, and are negligible at high output currents. (See Figure 9)

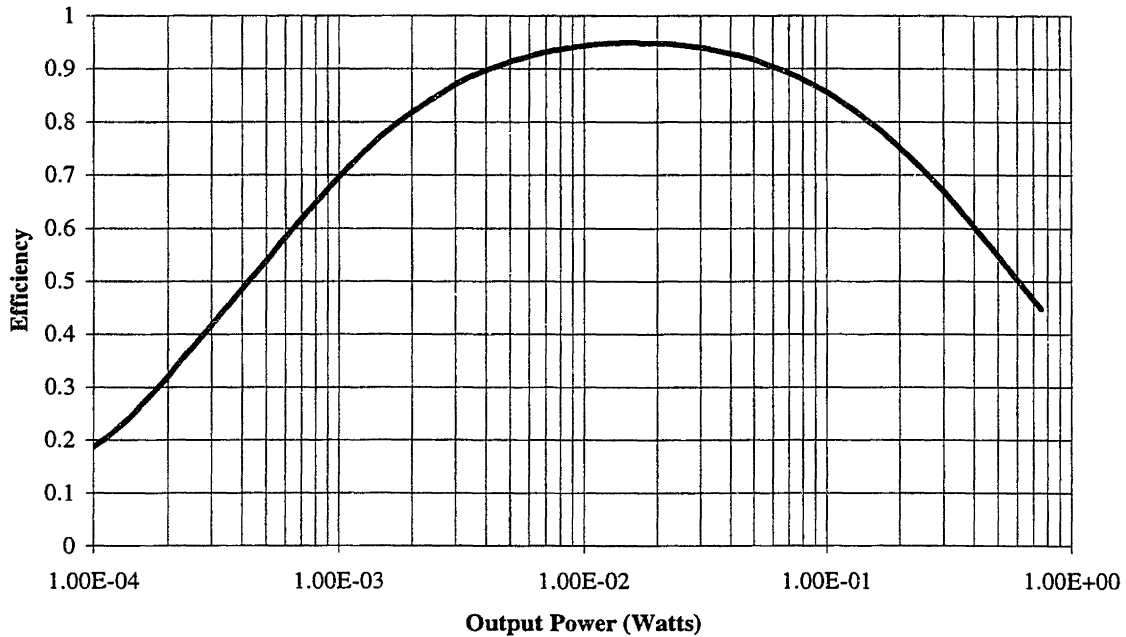


Figure 9: Simulated PWM Efficiency (Semilog)

To appreciably increase efficiency at the load current extremes, it is necessary to address the corresponding dominant loss mechanisms in architecture decisions. At low load, it is possible to vary the switching frequency. This makes the gate switching losses scale linearly with load current instead of being constant. This technique is called Pulse Frequency Modulation (PFM), and will be explained in the next section. At medium load, traditional Pulse Width Modulation (PWM) mode can be used. At high load it is possible to add larger switches in parallel with the smaller ones to reduce channel losses. This technique will be called Low Switch Resistance mode (LSR), and it uses fixed

frequency PWM control. Section 3.3 will show how it is possible to automatically select the optimal mode for the current output load.

2.2.1 Pulse Frequency Modulation Mode (PFM)

If both output switches were to be turned off when the load current is light, it would take a long time to discharge the output capacitor voltage by tens of millivolts, the size of the current ripple in PWM mode. For instance, at 100 μ A and 1V output, a 1 μ F capacitor discharging by 10mV takes 100 μ s.

$$dt = dV \frac{C}{I} = 100\mu s$$

This is much longer than a switching period in PWM mode, which is typically 1 μ s to 5 μ s. Therefore, it is possible to operate in a mode called Pulse Frequency Modulation (PFM). When it is detected that the voltage is below a given threshold, a single pulse raises the output voltage again. (See Figure 10 and Figure 11)

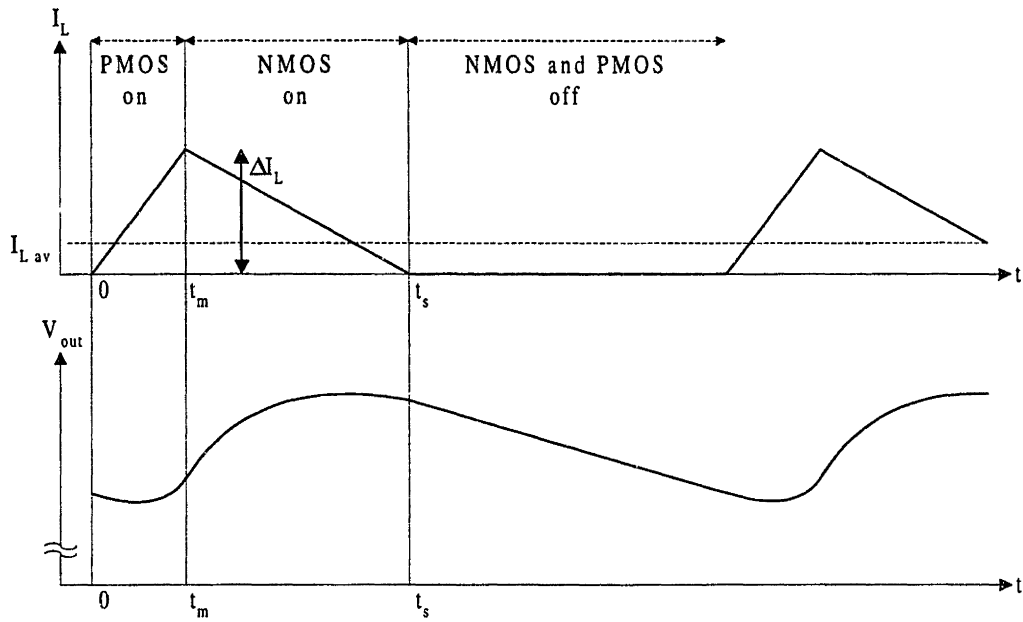


Figure 10: Example PFM waveforms

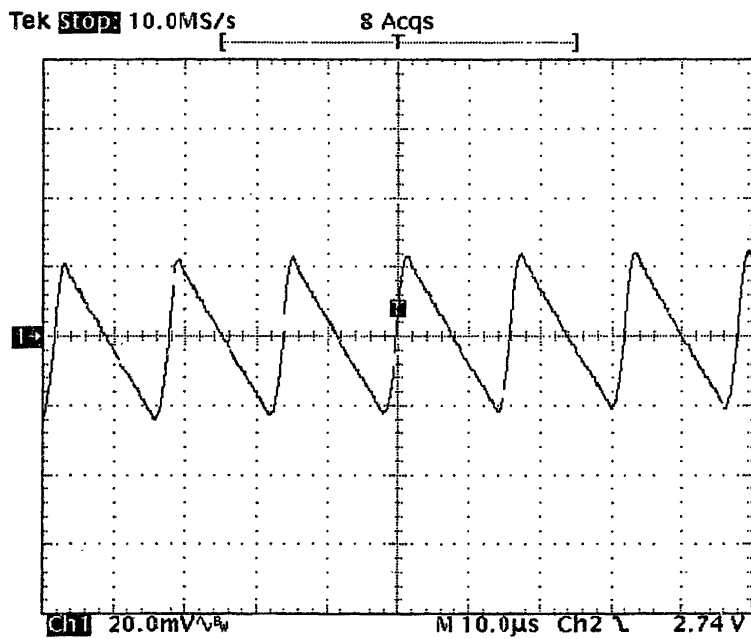


Figure 11: Output voltage ripple in PFM mode

In order to maintain peak efficiency, the inductor current (I_L) must be near zero at the end of a PFM pulse when both switches are turned off (t_s in Figure 10). If it is not,

then the inductor will either charge or discharge the small node V_x capacitance (C_x), until one of the switch body diodes conducts. The body diode will stop conducting when the inductor current ramps down to zero. If t_s is too late, then I_L will have gone negative, charging up C_x until the high side switch body diode turns on (See Figure 12). If t_s is too early, then I_L will still be positive, discharging C_x until the low side switch body diode turns on (See Figure 13). Either way, the entire power stored in the inductor at the time t_s will be dissipated in a body diode. However, this stored power decreases as the square of the inductor current. I_L is decreasing linearly in the region of t_s , so if t_s is slightly misplaced, then the power stored in the inductor will be small. But, if t_s is badly misplaced, then power loss could be high.

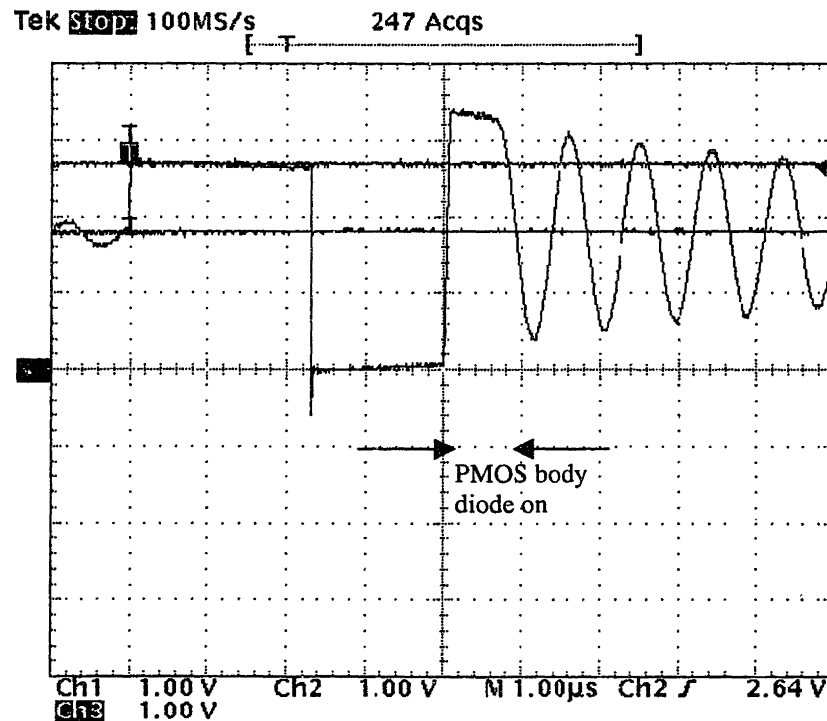


Figure 12: Late NMOS turnoff

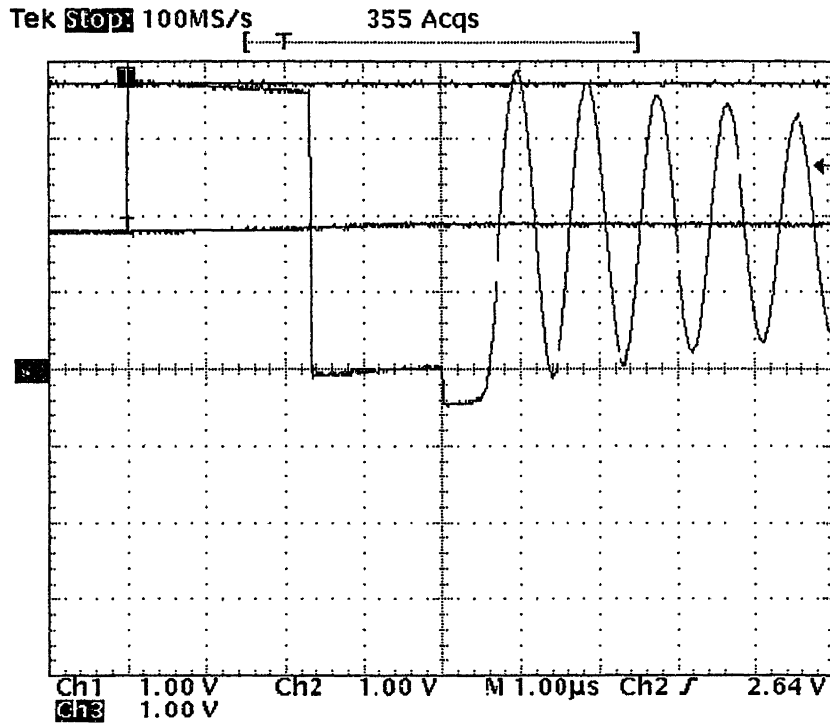


Figure 13: Early NMOS turnoff

The correct t_s is a function of V_{in} , V_{out} and t_m (The time during a pulse when the low side switch takes over for the high side switch):

$$t_s = t_m \frac{V_{in}}{V_{out}}$$

Alternatively, given a fixed t_s , the correct t_m can be derived. In the implementation of this timing, it is easiest to make t_s exactly equal a PWM switching period. Then, duty cycle can be inherited from the steady state duty cycle in PWM mode. If it is possible for V_{in} to change while in PFM mode, then the proper duty cycle can be calculated given a measurement of V_{in} . A division is required, but since relatively low accuracy is necessary, it can be implemented with a small lookup table.

One disadvantage with the traditional implementation of PFM is that the switching events are not synchronous, as they are in PWM mode. Many times, switched

capacitor analog circuits are phase locked to the switching frequency so that sampling does not take place at the same time as a switching event, at which time there is elevated levels of radiated and conducted noise. If PFM is implemented so that a simple comparator initiates each switching pulse, then the overall frequency cannot be predicted, and thus noise cannot always be cancelled. However, it is possible to operate in synchronous PFM mode, where each pulse can start only at a discrete time. As in fixed frequency control, the PFM pulse can be locked to a reference clock. This clock can often be shared with the circuit under power and so therefore represents a negligible power overhead if the circuit under power is in the same package.

In synchronous PFM mode, the correspondence between pulse duration and output voltage ripple is different than PWM mode. If the pulse width is the same in PFM mode as in PWM mode, then the output voltage change over one pulse will actually be larger in PFM mode. The total inductor current ripple is unchanged:

$$\Delta i_L = \left[\frac{V_{out}}{V_{in}} (V_{in} - V_{out}) \right] \frac{t_s}{L} = [V_{in} (D - D^2)] \frac{t_s}{L}$$

But, at zero output current, the inductor ripple current goes both positive and negative in PWM mode. In PFM mode, it is strictly positive, which means that the peak value is twice as high. Therefore, at zero output current, the output voltage ripple will be four times as large. As the output current increases, the output voltage ripple across one pulse is reduced since the capacitor is being drained during the pulse:

$$\Delta V_{out}^{PFM} = \Delta i_L \frac{t_s}{2} - \frac{I_L t_s}{C}$$

However, at the same time, a dithering effect occurs since the output voltage is measured at discrete times. An example of this behavior is shown in Figure 14. This dithering effect effectively negates the reduction in ripple due to output current.

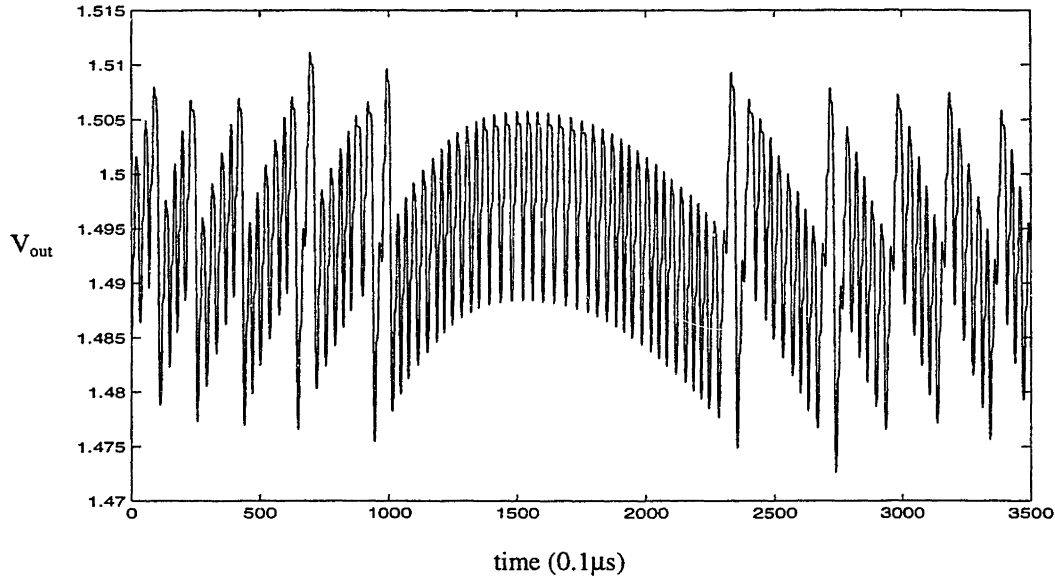


Figure 14: Limit cycles in PFM mode as the output current increases

If the ripple in PFM mode is desired to be smaller, it is possible to make each pulse shorter. This would imply that the time t_m would have to be scaled by the same amount. Since the pulse generator is implemented digitally, it is trivial to do such operations. If each pulse is shorter, then pulses will be spaced closer together, resulting in slightly lower efficiency. However, the ultimate efficiency at low output currents is limited by the ADC and clock circuitry overhead, and therefore will not change.

If the output voltage is measured at discrete times, it must be sampled immediately before the beginning of a candidate pulse. If the measurement is made earlier in the preceding cycle, then the output voltage ripple will be larger. And, if this

delay is larger than a pulse duration, then will be limit cycles in the output voltage.

However, the delay does not need to be zero, because the output voltage changes slowly near the end of a pulse. This is since the inductor current is near zero at this time. (See Figure 10) A reasonable delay allows ample time to make a measurement and decide whether to generate a pulse on the subsequent cycle.

2.2.2 Low Switch Resistance (LSR) Mode

For a given output load, there is an optimal switch size which minimizes the combined losses from gate switching and channel conduction. As the switches are made wider, the gate capacitance goes up, and the channel resistance goes down. The minimum power loss is achieved when the width is selected as follows:

$$W_n^{opt} = \sqrt{\frac{D \left(I_{Lav}^2 + \frac{\Delta i_L^2}{12} \right)}{\alpha \mu_n C_{ox}^2 V_{gs}^2 (V_{gs} - V_t) f_{sw}}}$$

$$W_p^{opt} = \sqrt{\frac{(1-D) \left(I_{Lav}^2 + \frac{\Delta i_L^2}{12} \right)}{\alpha \mu_p C_{ox}^2 V_{gs}^2 (V_{gs} - V_t) f_{sw}}}$$

Where α is a constant accounting for the additional switched capacitance of the gate drivers (See section 2.1.2), and Δi_L is the peak to peak inductor current ripple (See section 2.1.1). V_{gs} is the gate to source voltage that a transistor has while it is on. It is a fairly broad minimum, as can be seen in Figure 16, and so it is reasonable to have two discrete switch sizes to choose from. ><Figure>< shows the optimum NMOS gate width given typical parameters.

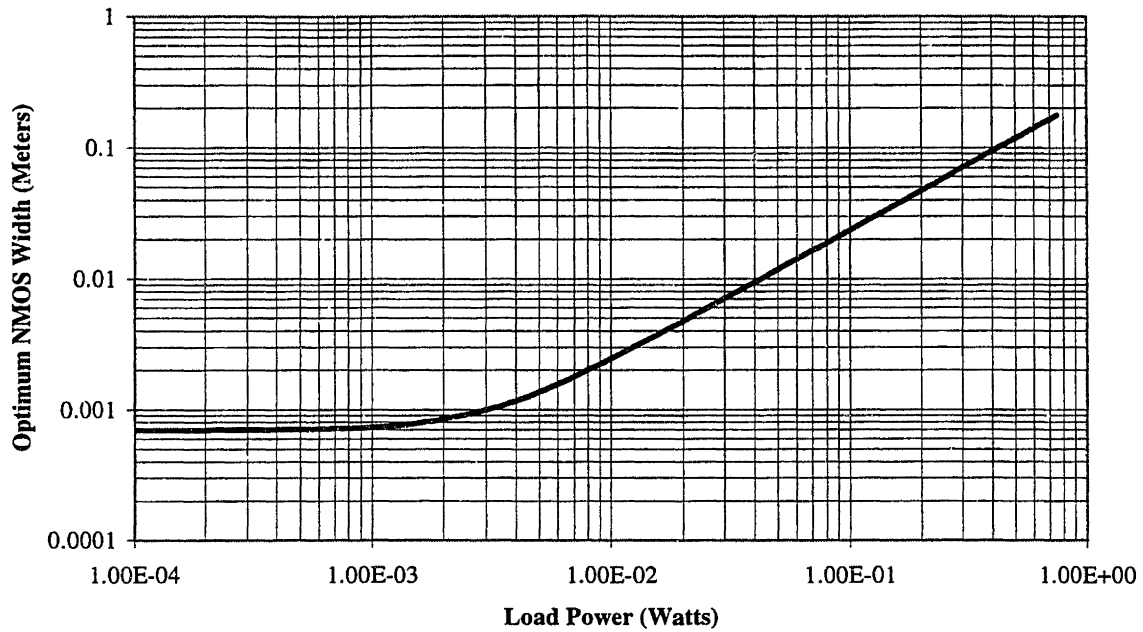


Figure 15: Optimum NMOS gate width

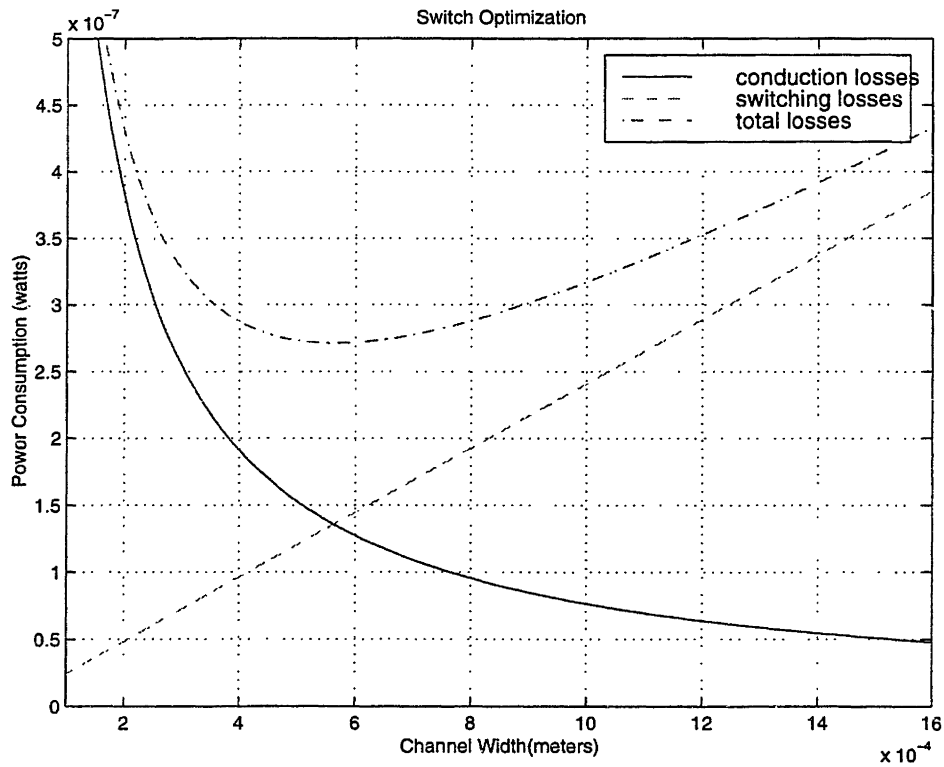


Figure 16: Power Losses vs NMOS gate width

2.3 Optimal Mode Selection

The optimum of three different modes is automatically selected in real time: PFM mode, PWM mode, and PWM mode with wider switches (LSR). This can be done reliably with a low power overhead, without using an external current sense resistor. Implementation details of each mode transition will be described, along with suggestions for further improvements.

Conventionally, an external current sense resistor and amplifier are used to measure current. In a novel approach, the channel resistance of the NMOS switch itself can be used to measure the output current. When the inductor current is positive (flowing into the filter capacitor), the node V_x will be negative while the NMOS switch is conducting. See Figure 7 for switching waveforms. The output current is the average of the inductor current, and the inductor current has a fixed sawtooth ripple amplitude. Therefore, when the output current goes below one half of the inductor ripple current amplitude, the inductor current goes negative near the time t_s . In turn, V_x would be positive immediately before t_s . Immediately after t_s , the PMOS switch begins conducting, and V_x swings near the input voltage. There is a direct relationship between the voltage at V_x immediately before t_s , and the average output current. Given the inductor ripple amplitude (ΔI_L):

$$\Delta i_L = \left[\frac{V_{out}}{V_{in}} (V_{in} - V_{out}) \right] \frac{t_s}{L} = [V_{in} (D - D^2)] \frac{t_s}{L}$$

$$\langle i_o \rangle_{PFM_{thresh}} = \frac{V_x|_{t=t_s}}{R_{sw}^n} + \frac{\Delta i_L}{2}$$

where R_{sw} is the resistance of the NMOS switch. Figure 17 shows an oscilloscope trace of V_x while in PWM mode.

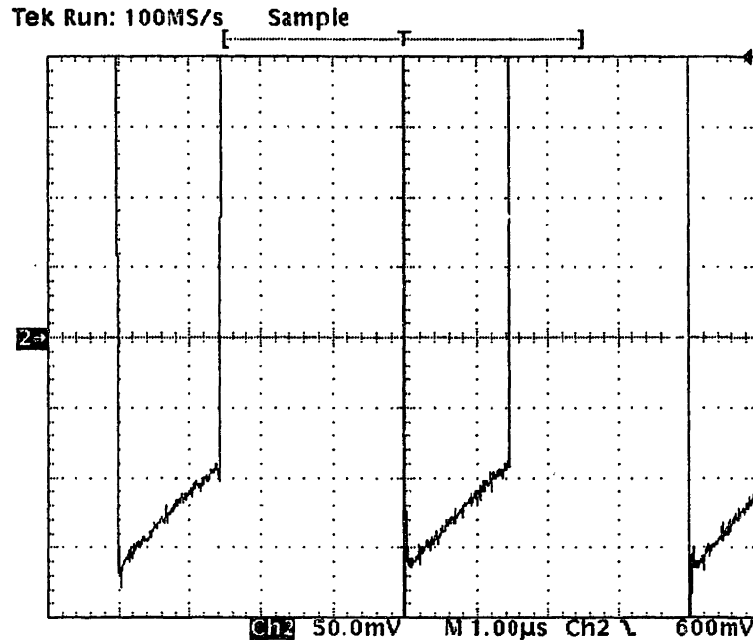


Figure 17: V_x magnified in PWM mode

V_x can be sampled immediately before t_s , from which $\langle i_o \rangle$ can be deduced. A programmable offset can be introduced to the measurement circuit to put $\langle i_o \rangle$ inside a range of currents, which then is used to set the proper operating mode. This circuit remains low power because it can be shut down between measurements. The levels at V_x are relatively small, which makes the circuit design non-trivial. However, since the measurement of V_x always takes place immediately before a switching event, there is no switching noise interference in the measurement. With no external current sense resistor, the differential sense wires can remain on the die, where they are less susceptible to noise. And, the resistance of the NMOS switch is high compared to that of a sense resistor, making the signal level at V_x higher, which also reduces noise sensitivity. If the current sense resistance were as large as the NMOS switch, then comparable power would be dissipated in the sense resistor, reducing overall efficiency.

When the converter is operating in PFM mode, the transition to PWM control must be made when the output current goes above the threshold:

$$I_{PFMthresh}^+ = \frac{\Delta i_L}{2}$$

This is because above this threshold, the inductor current never goes to zero, so there is no opportunity to turn off both switches. Figure 18 shows the switching voltage V_x in PWM mode when the output voltage is just above the PFM threshold.

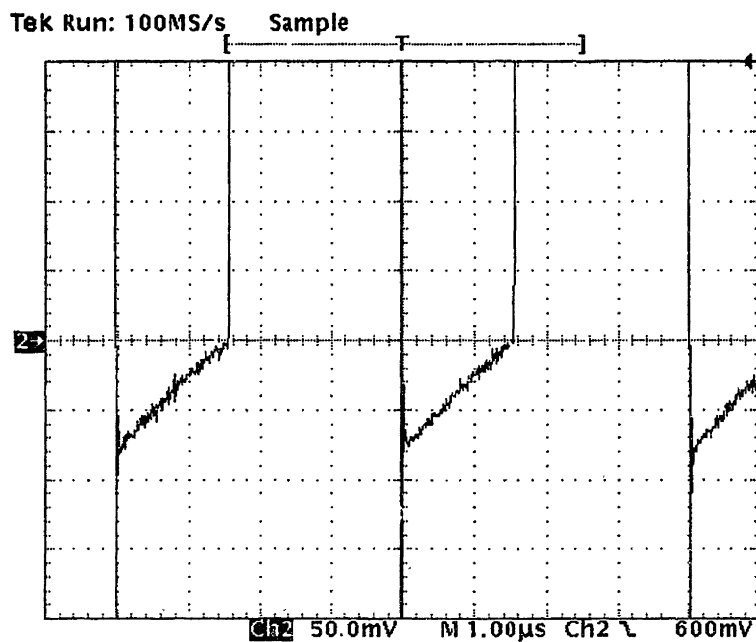


Figure 18: V_x magnified in PWM mode near PFM transition

If PFM mode control is maintained at high current, there may be instability as the output voltage oscillates above and below the voltage reference. There are two ways to detect the PWM current threshold. First, the node V_x can be measured at the end of a pulse to see whether it is above a certain value. The pulse should be the first following a period when both switches are off, to insure that the inductor current starts the pulse period at zero current. This method does not appreciably lower efficiency at low output

currents because no measurements are made when there are no pulses. Secondly, the number of consecutive pulses can be monitored. If there are too many pulses in a row, then the output current is approaching the threshold. The second method is susceptible to output voltage oscillation than the first method. Also, as the number of pulses in a row gets larger, oscillation can take place at lower frequencies, and thus becomes more likely. The first method guarantees that the output current is below the threshold, thus preventing oscillation.

When the converter is operating in PWM mode, the transition to PFM control must be made when the output current is below $I_{PFMthresh}$. V_x is monitored at a set interval to detect the output current. Current does not have to be measured every cycle, to save a small amount of power. To add hysteresis to the transition, the current set point is slightly lower than in the reverse direction. This prevents limit cycles when the output current is very near the set point. If PFM mode control is set up to inherit the duty cycle of the PWM mode, then the PWM controller must be near steady state before the transition is made. To insure this, there is a delay on startup and on returning to PWM mode before PFM mode can be activated. The duty cycle can leave steady state when a load transient occurs. But, this is not an issue since PFM mode would only be activated after a step from steady state high current to low current, at which time the duty cycle would not change much since the control bandwidth is low compared to the measurement frequency. And, any small error in duty cycle does not appreciably reduce the efficiency in PFM mode. (See section 3.3)

If the output current goes above a higher threshold ($I_{LSRthresh+}$), then wider switches are activated (Low Switch Resistance Mode or LSR). This threshold should be at the point where the big switches are equally as efficient as the small switches:

$$P_{sw}^{sml} + P_{res}^{sml} = P_{sw}^{big} + P_{res}^{big}$$

$$I_{LSRthresh}^+ = \sqrt{\frac{W_{big}^2 (C_{gs}^{sml-n} + C_{gs}^{sml-p}) V_{in}^2 f_{sw}}{W_{sml} R_{sw}^{sml-n} D + R_{sw}^{sml-p} (1-D)} - \frac{\Delta i_L^2}{12}}$$

Where C_{gs} is the gate to source capacitance of the small n and p channel MOSFETs, R_{sw} is the corresponding channel resistance, and Δi_L is the inductor current ripple. (See Sections 2.1.1 and 2.1.2) Measurements of PFM and LSR thresholds can be interleaved so that two comparator circuits are not needed.

Once in LSR mode, the resistance of the NMOS power FET changes according to its width, and therefore the reverse threshold $I_{LSRthresh-}$ must be scaled to compensate. In addition, some hysteresis should be added to prevent oscillation in and out of LSR mode near the threshold.

3 Circuit Design

3.1 System Reconfiguration

The control logic is reconfigured in two different ways for PWM and PFM modes. Figure 19 shows how each element is used in the two regimes. The control logic is implemented digitally. This makes it possible to program loop parameters in real time. In both modes, the output voltage can be changed by the device being powered, which saves significant power. In PWM mode, the loop gain can also be changed, which is useful since the gain margin changes linearly with duty cycle [8].

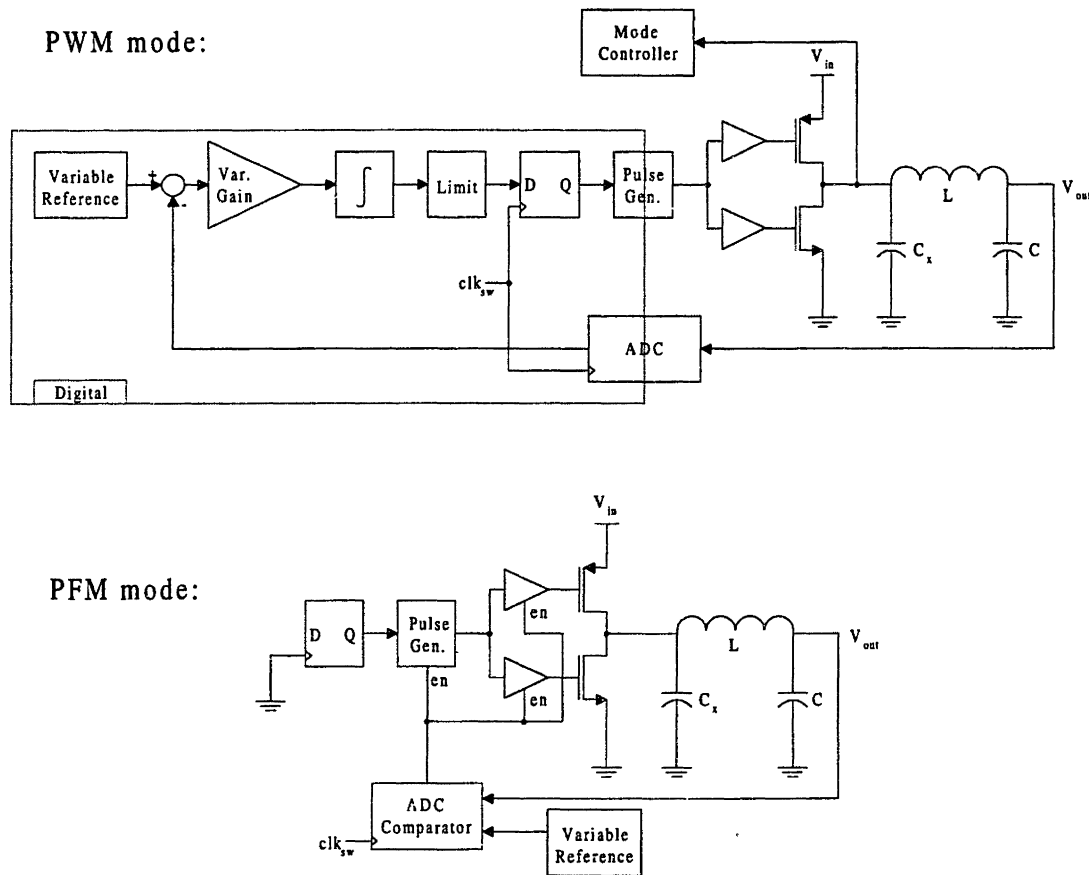


Figure 19: System block diagram showing reconfiguration in PFM and PWM modes

In PFM mode, the complexity of the control loop is minimized to reduce the power overhead. The duty cycle is fixed at the last value while in PWM mode. For this method to be work, the input voltage must remain relatively constant while in PFM mode. This assumption is valid for battery powered systems, since the battery voltage is unlikely to change quickly, especially under low load conditions in PFM mode. The pulse generator and gate drivers are only enabled during a pulse. The Analog to Digital Converter (ADC) is reconfigured to operate as a variable threshold comparator. In this configuration, the ADC is faster and consumes less power.

3.2 Analog to Digital Conversion

An Analog to Digital Converter (ADC) is needed to measure the output voltage so that it can be compared to the desired value. Seven bit precision is reasonable to make the error smaller than 1% of the input voltage. (The Pulse Generator has eight bit precision, to prevent limit cycles.) Very low power operation is required at a sampling rate of about 100kHz. The charge redistribution ADC is well suited to this application [9]. It consumes no static current, and the dynamic power consumption is low.

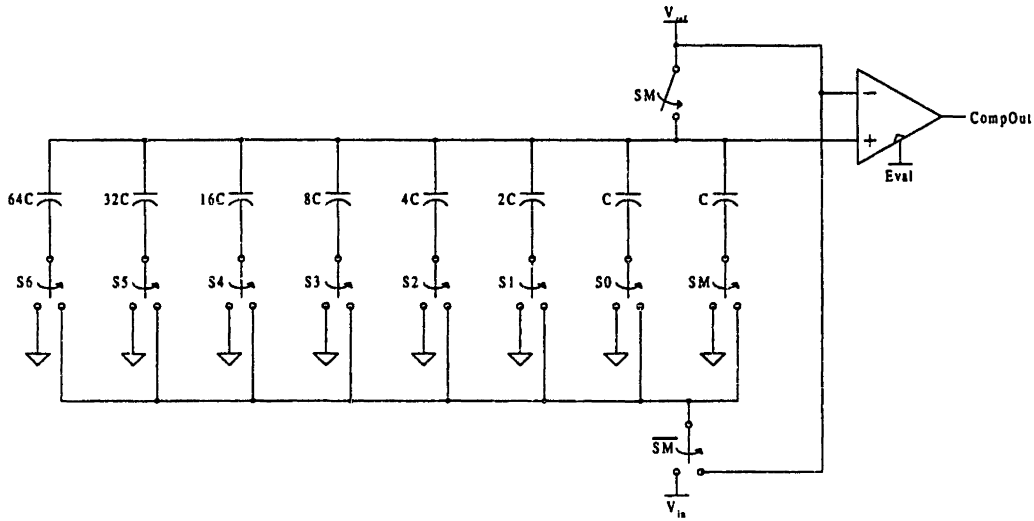


Figure 20: A charge redistribution ADC

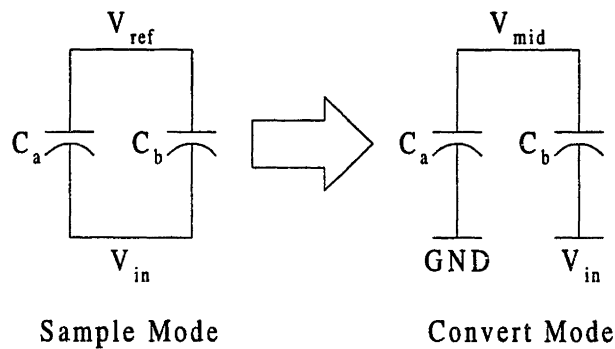


Figure 21: Charge redistribution configurations

Figure 20 shows a representative circuit diagram of the ADC. First, the input voltage is sampled. The node V_{mid} is connected to V_{ref} , and the bottom plates of all capacitors are connected to V_{in} . Then, the conversion begins. The node V_{mid} is left floating while the bottom plates of some capacitors are grounded, and others are connected to V_{ref} . Figure 21 shows this process in a simplified form. A finite state machine monitors the output of the comparator, and does a binary search by connecting different sets of capacitors C_a and C_b to find the closest approximation to the input voltage. By conservation of charge, the value of V_{mid} can be derived:

$$Q_{vmid}^{sample} = Q_{vmid}^{convert} = \sum_i C_i V_i$$

$$(C_a + C_b)(V_{ref} - V_{in}) = (C_a + C_b)V_{mid} - C_b V_{ref}$$

$$V_{mid} = \frac{C_a + 2C_b}{C_a + C_b} V_{ref} - V_{in}$$

The comparator output will change state when V_{mid} is equal to V_{ref} . This is the final configuration of the converter after the binary search has completed. The ratio of V_{in} to V_{ref} is linearly related to the portion of the total capacitance in the bank that was switched to C_b :

$$V_{ref} = V_{mid} = \frac{C_a + 2C_b}{C_a + C_b} V_{ref} - V_{in}$$

$$\frac{V_{in}}{V_{ref}} = \frac{C_b}{C_a + C_b}$$

In this manner, a linear conversion is performed, even though the value of V_{mid} is not linear with V_{in} .

The total conversion takes eight cycles. The first cycle is when the input voltage is sampled. The subsequent seven cycles comprise the binary search, which establishes a seven bit result. In Pulse Frequency Modulation (PFM) mode, the requirements are slightly different. The result needed is only one bit, which signifies whether the output voltage is higher or lower than the reference voltage. Also, the result is needed very quickly since it determines the subsequent pulse. It is possible to reconfigure the ADC to meet both these conditions. The sampling takes place in the same manner, but only one comparison is done. The switches S0-S6 are simply connected to reflect the digital voltage reference. If V_{in} is greater than this reference, then at the input to the comparator, V_{mid} will be smaller than V_{ref} .

In the full conversion mode, there can be a loss of accuracy for small input voltages. The problem is that V_{mid} can exceed V_{ref} during the conversion. If the voltage difference is greater than about 0.6 volts, then the body diode of the MOSFET connected from V_{mid} to V_{ref} can begin conducting. This will change the charge distribution on all the capacitors, and will therefore make the conversion nonlinear. One solution would be to bias the substrate of this MOSFET at a higher voltage. Alternatively, the voltage reference could be lowered. Or, the binary search algorithm could be altered so that V_{mid} never gets too high. This would make the conversion slightly longer, but would relax restrictions on the reference voltage. Two extra conversion cycles would occur before the other seven, comparing V_{in} to $V_{\text{ref}}/8$ and then $V_{\text{ref}}/4$ instead of $V_{\text{ref}}/2$ immediately. Yet another solution would be to connect two p channel MOSFETs in series, with the body of the MOSFET next to V_{mid} connected to its own source terminal. This would put two body diodes in series, raising the tolerable voltage difference between V_{mid} to V_{ref} to about 1.2 volts.

3.3 Pulse Generator

A pulse generator circuit is needed to precisely place a signal edge within the switching period, given a digital duty cycle command value. This edge is used to create the gate waveforms of the output power MOSFETs. The pulse generator circuit subdivides the switching period into 2^M sections, where M is the number of bits in the duty cycle command value. The nature of this process is power intensive, and therefore the circuit requires optimization for power. First, two common approaches will be presented: a fast clocked counter, and a delay line. Then, a power saving alternative will be discussed: a hybrid of these two approaches.

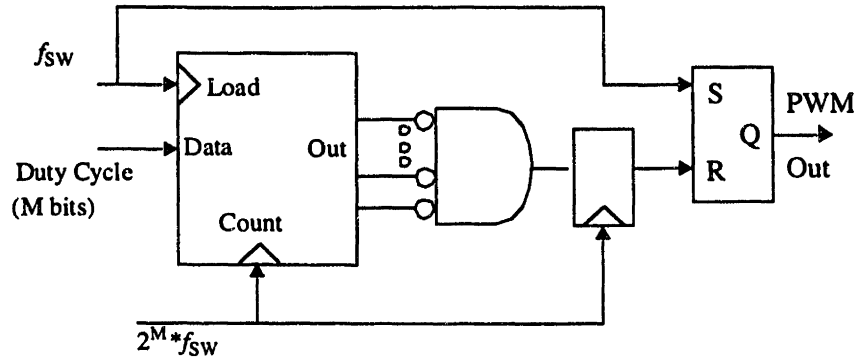


Figure 22: A fast clocked pulse generator

3.3.1 Fast Clocked Counter Pulse Generator

In the fast clocked counter approach, the desired duty cycle is loaded in to a down-counter clocked at a frequency $f_{sw}2^M$ where f_{sw} is the switching frequency. (See Figure 22) When the counter reaches zero, the edge is created. The power of this circuit is at least proportional to 2^M . The amount of capacitance switched in one cycle increases as 2^M . Furthermore, as the clocking frequency increases, the power supply of the counter must be increased to satisfy timing requirements. Therefore, if the circuit operates at the power converter input voltage, then there is a limit to the accuracy.

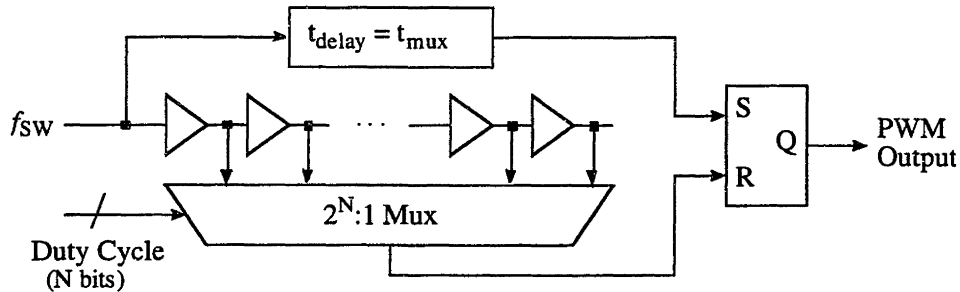


Figure 23: A delay line pulse generator

3.3.2 Delay Line Pulse Generator

In the delay line approach, a delay line is constructed with 2^N elements. (See Figure 23) The total delay is made exactly equal to a switching period. The desired duty cycle selects one of the delay element outputs, creating the timing edge. The power of this circuit is at least proportional to 2^N . This is because there are 2^N elements which switch during one switching period. Furthermore, as the delay through a single element decreases, the minimum supply voltage increases. However, this minimum supply voltage is lower than with the fast clocked counter approach, since the critical timing path in the counter is much longer. The disadvantage of the delay line approach is that the multiplexer takes up a large area.

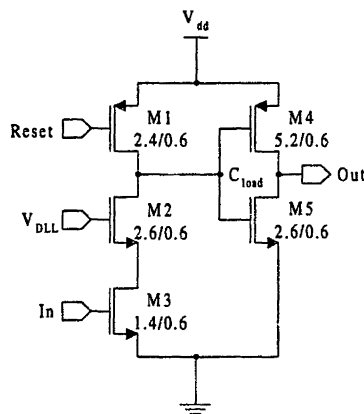


Figure 24: A delay line element

3.3.2.1 Delay Line Element

An individual delay element is made from a current starved inverter, followed by a simple inverter. (See Figure 24) After each use, the Reset input is pulled low, which recharges the inverter input capacitance C_{load} . When a rising edge goes in to the delay

element, C_{load} is discharged. The speed of this discharge is controlled by the voltage V_{DLL} . In this manner, the delay through the element can be programmed.

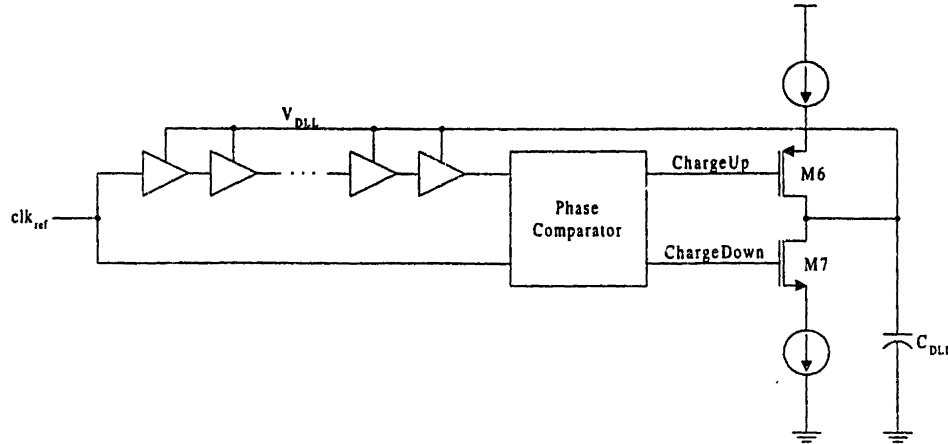


Figure 25: Delay Locked Loop (DLL) feedback

3.3.2.2 Delay Locked Loop Operation

Closed loop feedback is implemented in a Delay Locked Loop (DLL) structure to dynamically control V_{DLL} so that the length of the delay line is exactly equal to a switching period. (See Figure 25) The output of the delay line is compared to the reference clock by a phase comparator. If the output arrives too late, then V_{DLL} is charged up by a small current source. If the output arrives too early, then V_{DLL} is charged down. The duration of the charging is proportional to the error in the output arrival time. If the output arrives at exactly the same time as the reference clock, then V_{DLL} is not changed. Stability of the loop is trivial, since there is only a 90° phase shift in the loop transfer function. V_{DLL} is stored on the capacitor C_{DLL} , which is relatively large. If C_{DLL} were too small, then the voltage V_{DLL} would change as the edge propagated through the delay line since there is a small amount of charge sharing between C_{DLL} and C_{load} through

C_{gd} of M3. Also, V_{DLL} would be discharged by leakage current through M6 and M7 if the delay line were inactive for a long time.

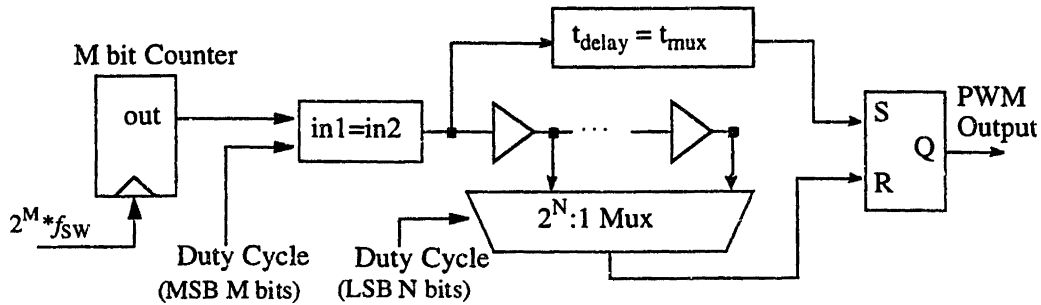


Figure 26: A hybrid pulse generator

3.3.3 Hybrid Pulse Generator

The hybrid pulse generator approach combines coarse accuracy versions of a fast clocked counter and a delay line. (See Figure 26) The counter divides the switching period into 2^M sections, and the delay line further subdivides one of these sections into 2^N subsections. The delay line only needs to be active during one section since only one edge needs to be generated. The total power is reduced since the individual power of the counter and delay line scales better than exponentially with M and N.

$$2^M + 2^N \ll 2^{(M+N)}$$

The area is also reduced compared to the delay line approach since the multiplexer is much smaller.

3.4 V_x Comparator

An accurate comparator is needed to measure the output current indirectly by sampling V_x immediately before the end of a switching cycle. Very good offset characteristics are needed since the resistance of the output NMOS switch may be very

low. Therefore, a differential preamplifier is required. The input voltages to this amplifier are always near ground, and are often negative. Therefore, input sampling capacitors are required to shift the input levels into the active region of the amplifier. High speed is not necessary since the waveform at V_x has a very low slope. But, at the end of the switching cycle, when the PMOS switch turns on again, V_x makes a fast transition to a voltage near V_{in} . Therefore, the output of the differential preamplifier must be sampled and held before this transition. This scheme affords very good noise immunity, since the sensitive differential preamplifier never operates during a switching event.

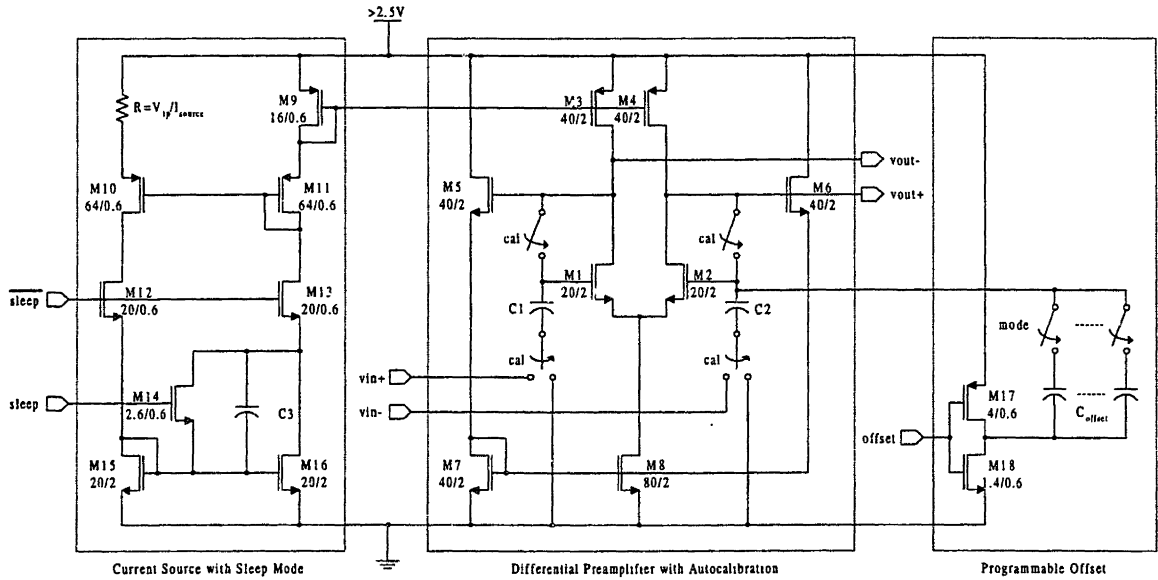


Figure 27: Differential preamplifier

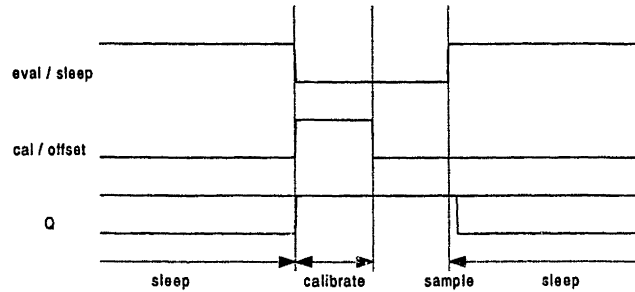


Figure 28: Differential preamplifier and comparator waveforms

3.4.1 Differential Preamplifier

The preamplifier schematic is shown in Figure 27, and example waveforms are shown in Figure 28 [10]. Before each measurement, the preamplifier is autozeroed. When the "cal" signal is asserted, the input transistors M1 and M2 are diode connected along with one plate of the corresponding input capacitor. The other plate of each input capacitor is connected to ground. In this manner, any input common mode level near ground can be accommodated. Transistor lengths are wider than minimum to increase the equivalent resistance in the saturation region.

3.4.1.1 Programmable Offset

The configuration of the input capacitors also makes it simple to add a programmable offset to the amplifier. This offset is changed on the fly to decide which mode is optimal. To create the offset, a certain amount of charge is asymmetrically injected on one of the capacitors. A bank of very small capacitors (C_{offset}) is connected to C2, and then the negative plate V_{trans} of C_{offset} is switched by M17 and M18. If V_{trans} is switched from ground to V_{cc} , then the voltage on C2 is increased, and a negative offset is introduced at the input of the amplifier. When V_{trans} is switched from V_{cc} to ground, then

a positive offset is introduced. The magnitude of the offset depends on the relative size of C_2 and C_{offset} :

$$|V_{offset}| = \frac{V_{cc}}{\left(1 + \frac{C_2}{C_{offset}}\right)}$$

The magnitude of the offset does not depend on the absolute value of any capacitor, and is therefore not as sensitive to process variations. C_2 does not need to be exactly matched to C_{offset} , since any shift will affect all offsets equally, and any hysteresis will be maintained. Since the capacitors in C_{offset} are near minimum size, and the desired offset is very small, C_1 and C_2 are large compared to the gate capacitance of M1 and M2. Therefore, C_1 and C_2 do not need to be exactly matched for good accuracy.

3.4.1.2 Common Mode Feedback

The differential pair is kept in its active region through common mode feedback created by M5, M6, M7, and M8. If the common mode voltage at V_{out}^+ or V_{out}^- goes up, then M5 and M6 pass more current. This raises the voltage at the diode connected gate of M7, which is connected to the gate of M8. Thus, M8 will pass more current, which is split between M3 and M4. This additional current across the equivalent resistance of M3 and M4 lowers the common mode voltage at V_{out}^+ and V_{out}^- , thus closing the loop with negative feedback. The feedback is nonlinear since it depends on the quadratic dependence of drain current on V_{gs} . However, in a comparator this does not matter since the only important thing is whether V_{out}^+ is larger than V_{out}^- .

3.4.1.3 Current Source with Sleep Mode

The current source, created by M9-M16, is referenced to V_{tp} , since the voltage across the resistor is V_{tp} . The current source does not need to be especially stable or accurate for the comparator to perform well. If ΔV_i is defined as $V_{gsi} - V_t$, then:

$$\begin{aligned} V_{cc} - V_{d9} &= V_{tp} + \Delta V_9 \\ V_{cc} - V_{d11} &= V_{d9} + \Delta V_{11} \\ V_{cc} - V_{s10} &= V_{d11} - \Delta V_{10} \\ V_{cc} - V_{s10} &= V_{tp} + \Delta V_9 - \Delta V_{10} + \Delta V_{11} \end{aligned}$$

M15 and M16 form a mirror so that roughly the same current I_{source} flows through M9, M10, and M11.

$$\begin{aligned} I_{source} &= \frac{W}{L} k_p (\Delta V_i)^2 = \frac{64}{0.6} k_p (\Delta V_9)^2 = \frac{16}{0.6} k_p (\Delta V_{10})^2 = \frac{64}{0.6} k_p (\Delta V_{11})^2 \\ V_{cc} - V_{s10} &= V_{tp} + \Delta V_9 - \frac{8}{4} \Delta V_9 + \frac{4}{4} \Delta V_9 = V_{tp} \end{aligned}$$

To save power, the current source can go into a sleep mode when the amplifier is not being used. When the signal "sleep" is asserted, M12 and M13 interrupt all current paths, and the capacitor C3 is shorted by M14. When it is time to wake up, M12 and M13 are closed, and M14 is opened. Since the voltage across C3 is zero at this time, V_{g10} is pulled lower, and V_{g16} is pulled higher. So, M9, M10, M11, M15, and M16 are all forced on, guaranteeing that the current source will start up. The power lost in the charging and discharging of C3 is negligible. C3 only needs to be several times larger than the sum of the gate capacitances of M9, M10, M11, M15, and M16 to turn these transistors on.

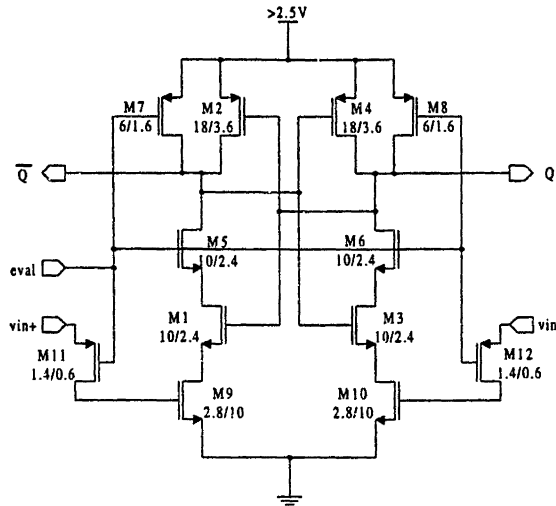


Figure 29: Dynamic comparator (input from preamplifier)

3.4.2 Dynamic Comparator

The output of the preamplifier is connected to a positive feedback dynamic comparator stage. The schematic for this stage is shown in Figure 29 [11]. When the signal E_{val} is low, both M5 and M6 are off, and both M7 and M8 are on, so both V_{out} and $_V_{out}$ are high. When E_{val} goes high, these conditions are reversed. If one preamplifier output is higher than the other, there will be a current imbalance between M9 and M10. Then, the cross-coupled inverter pair formed from M1, M2, M3, and M4 begins positive feedback action, and the final state depends on the current imbalance. There is no static power regardless of the level of E_{val} . M9 and M10 are sized to reduce the current during the positive feedback transition time. This makes the comparator slower, but reduces the input voltage offset.

The transistors M11 and M12 sample and hold the preamplifier output so that any subsequent disturbance does not affect the cross-coupled inverters while they switch.

This disturbance could either be the preamplifier entering sleep mode or a switching event at V_x

4 Results from Fabricated IC

4.1 Measured Efficiency

The efficiency was measured, and showed marked improvement at the load extremes. (See Figure 30) For comparison, the predicted efficiency of a PWM-only converter is shown in Figure 31. In the multi-mode converter, the efficiency is near 90% for load powers ranging over more than two orders of magnitude. However, there is still a falloff at the load extremes. Both Figure 30 and Figure 31 were created with $V_{in}=3V$, $V_{out}=1.7V$, and $f_{sw}=250kHz$

At high output power, the efficiency falloff is primarily due to bond wire resistance. Out of convenience for the bonding technician, a very small bond wire diameter was used. The bond pads are large enough to support a bond wire three times thicker, which would reduce the resistance by a factor of nine.

At low output power, the efficiency falloff is primarily due to digital control circuit overhead. The reference clock is divided by eight to make the switching clock, and this divider represents more than half the control circuit power overhead. Currently, the digital circuits run at the input voltage. However, they work down to 1.7V at a switching frequency of 500kHz. Therefore, a linear regulator could be used to reduce the digital supply voltage. This would result in an approximately linear decrease in digital circuit power with power supply reduction.

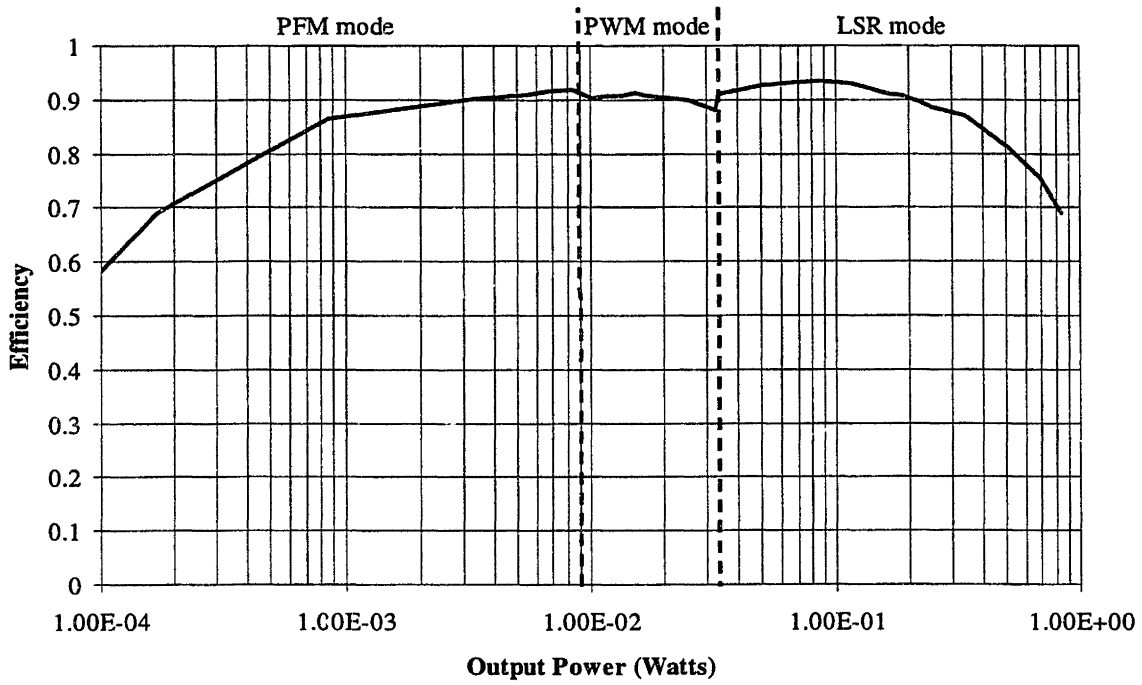


Figure 30: Multi-mode measured efficiency vs. output power (Semilog)

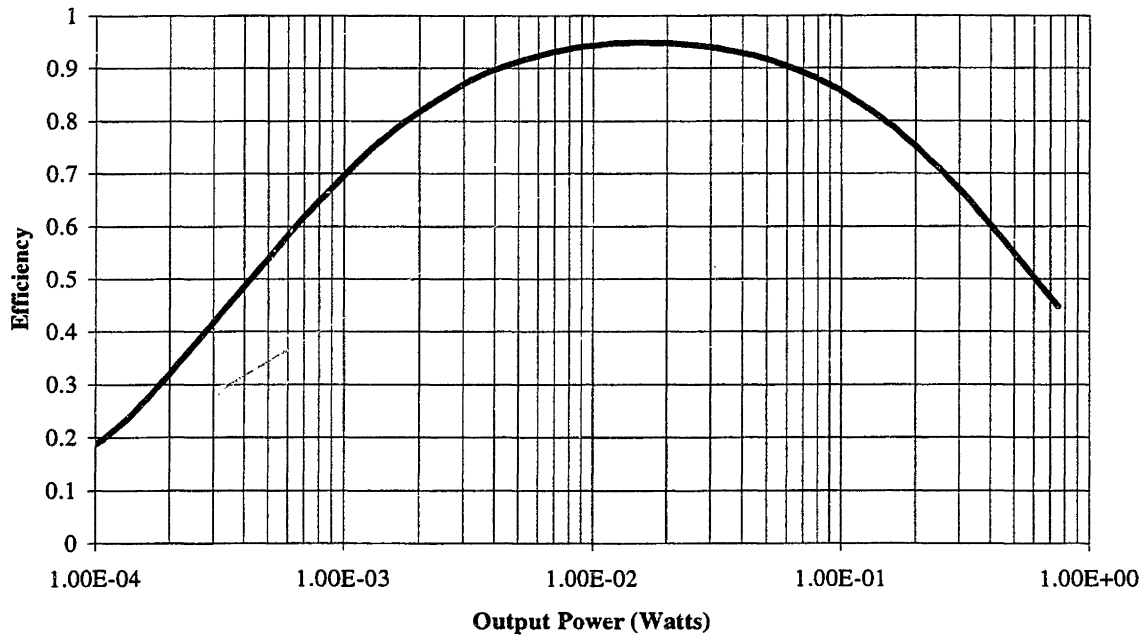


Figure 31: PWM-only mode simulated efficiency vs. output power (Semilog)

4.2 PFM operation

Figure 3 shows the input voltage, output voltage, and switching node V_x , while in PFM mode. Oscillation at V_x is expected when both switches are off, since the filter inductor and capacitor together form a nearly lossless resonator. At the end of each PFM pulse, the Voltage at V_x rises to $2V_{out}$, and then proceeds to resonate, slowly losing energy to the inductor series resistance. Note that the time between PFM pulses is not always the same, even for a constant output current. This is because the pulses are made to start at discrete times, and therefore some dithering must take place. When the output current is zero, the PFM pulses become widely separated.

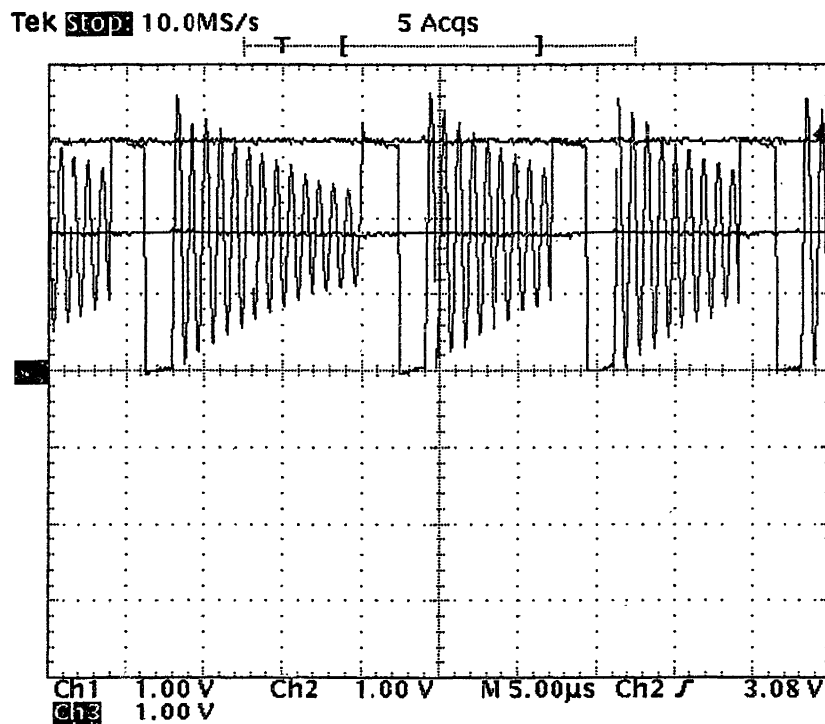


Figure 32: V_{in} , V_{out} , and V_x in PFM mode

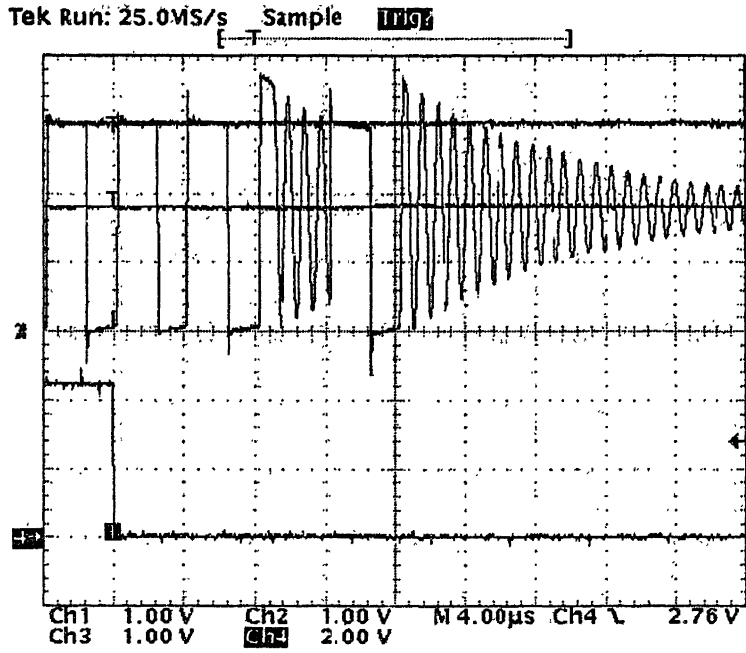


Figure 33: Transition from PWM to PFM mode

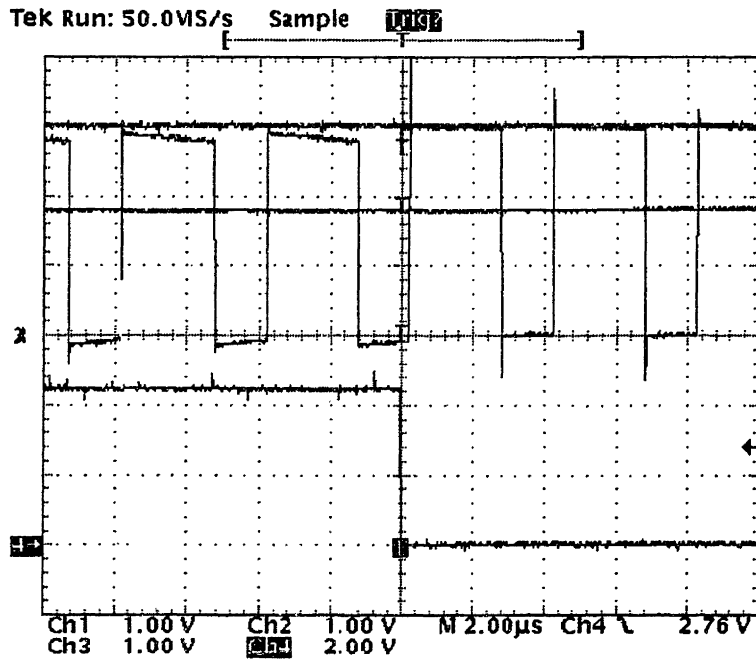


Figure 34: Transition to Low Switch Resistance (LSR) mode

4.3 Mode Transitions

Figure 33 shows a transition from PWM to PFM mode. Note that the p MOSFET body diode turns on for one cycle. This brings the inductor current down to exactly zero, and subsequent PFM pulses return the inductor current to exactly zero.

Figure 34 shows a transition into LSR mode. Note that the voltage drop across the switches is reduced dramatically. This makes the average voltage at V_x slightly higher, and therefore the output voltage will rise slightly until the voltage feedback loop brings it back to the reference level.

4.4 Control Power

The control power overhead is directly proportional to the switching frequency since almost all the power is due to switched capacitance. At a switching frequency of 250kHz and a power supply of 3.00V, the control power in PWM mode is 179 μ W. The control power in PFM mode ranges from 60.9 μ W to 80.7 μ W, depending on the pulse separation. The difference in power is attributed to the pulse generator along with control logic, both of which idle between PFM pulses. The 60 μ W overhead is split between the ADC and digital logic such as the reference clock divider, both of which are always active.

4.5 Layout Plot

Figure 35 shows the layout of the IC. Note that the ADC and Pulse Generator take up much less die area than the control logic. This suggests that the converter could be made much smaller with a feature size of 0.25 μ m, instead of the implemented 0.6 μ m

length. This change would also greatly improve the efficiency at low output currents, since the control overhead is dominated by switched capacitance losses.

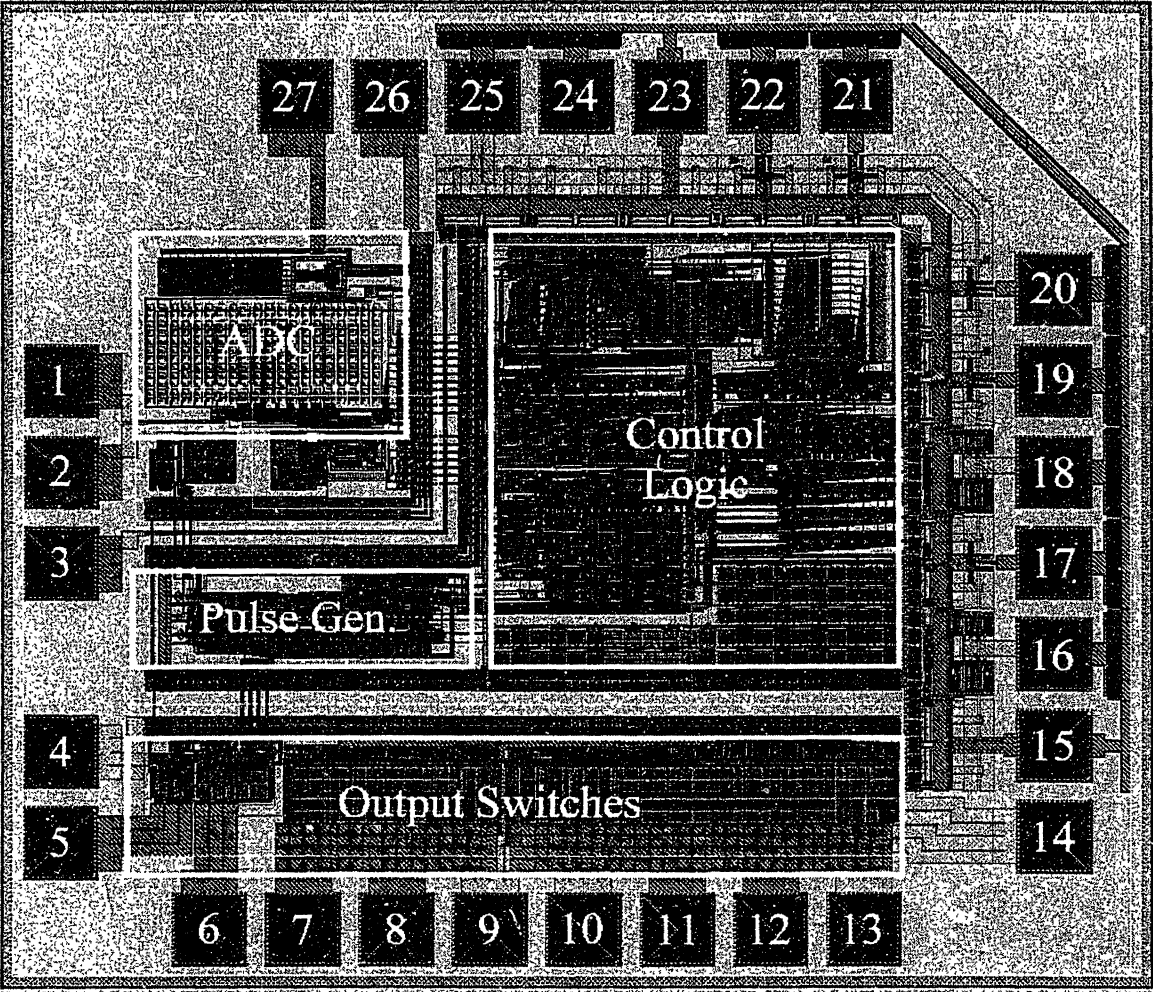


Figure 35: Layout Plot

5 Conclusions and Future Work

5.1 Future Work

5.1.1 PFM-PWM Transition

In the present integrated circuit (IC), there are several areas where the implementation could be easily improved. First, transition from PFM to PWM mode is currently detected by counting a certain number of sequential pulses. If the pulse threshold is too high, instability is possible, as the voltage oscillates above and below the reference voltage. Instead, detection could be done by measuring current in the same manner as the PWM to PFM mode transition. The differential preamplifier and comparator could be activated at the end of each pulse, or at the end of two sequential pulses. In this manner, a direct measurement of the output current could be made. By using the programmable offset in the differential preamplifier, hysteresis on PWM-PFM transition could be added. Alternatively, the current threshold for PWM to PFM mode transition could be lowered, so that hysteresis would be present even with a low pulse count threshold in the PFM to PWM transition.

5.1.2 Digital Reference Loading in PFM mode

In the present IC, the digital voltage reference is loaded via the serial port interface. In PWM mode, this reference is an integral part of the control loop. However, on transition to PFM mode, the last valid PWM duty cycle is latched and held constant until PWM mode returns. This means that a change in the voltage reference while in

PFM mode will indeed change the output voltage, but will imbalance the inductor current so that it no longer equals zero at the end of a pulse. This will incur additional power loss. One simple workaround would be to override the duty cycle if the voltage reference is changed while in PFM mode. An external status pin could be used to determine whether the converter is currently in PFM or PWM mode. However, to exactly determine the correct duty cycle requires knowledge of the input voltage. This is not always exactly known in battery powered systems. A fix might involve scaling the duty cycle to match the reference voltage changes while in PFM mode. Or, the ADC could be connected to measure the input voltage, and this could be used directly to set the proper duty cycle for a given reference voltage.

5.1.3 LSR threshold

In the present IC, the Low Switch Resistance (LSR) mode threshold is fixed. Since the optimum threshold depends on input voltage, switching frequency, duty cycle, and ripple current, the threshold should be programmable. This would allow optimization for the expected variables. Adding a bank of offset capacitors to the differential preamplifier is a trivial circuit addition. For programmability, the bank of capacitors could be interfaced to a serial port register. In this manner, the PFM-PWM threshold could also be changed, and the level of hysteresis could be altered.

5.1.4 Small switch deactivation in LSR mode

In the present IC, when the supplementary switch mode is activated, the smaller pair of switches are used in parallel with the larger pair. If the gate timing is not exactly the same between the two gate drivers, then the smaller pair of switches could

conduct a large current for a short time until the large switches are activated. This could cause undue stress on the smaller switches. Therefore, the smaller switches should be deactivated when the larger switches are activated.

5.1.5 Load Transient Improvement

In the present IC, when there is a large load transient in PWM mode, the voltage feedback loop can take a relatively long time to respond. This leaves a glitch at the output as the output capacitor either charges or discharges given the disparity between the new output current and the old inductor current. One common method to reduce the severity of this glitch is to add a window comparator on the output voltage. If it strays too far from the reference voltage, then the duty cycle is forced to either 0% or 100%. This can lead to a large buildup in inductor current, so it should only be done for a limited amount of time. It would be trivial to implement in the present digital controller, since the output voltage is in digital form. Another method avoids inductor current buildup and the associated time lag. This method connects an additional pair of switches directly to the output capacitor. If the window comparator is triggered, then one of the switches shunts current directly to the output. Again, it would be trivial to implement this feature given the present digital controller architecture.

5.2 Conclusions

A fully operational DC-DC converter has been presented, which has the potential to greatly increase the battery life of portable systems which consume very low power (down to $100\mu\text{W}$) for long periods, and high power (up to 1W) for short periods. Novel low power, high accuracy circuits have been presented for inductor current

detection without an additional current sense resistor. The future of this architecture is even brighter in light of the possibilities for future work.

Appendix: Technical Documentation

Serial Port Interface

A unidirectional three wire serial port is used to provide external programmability of various chip functions. The interface consists of clock, data, and an active low enable. Data is sent in 16 bit packets, where the first 8 bits correspond to a register address, and the second 8 bits are the data to be loaded into that register. All data is sent Most Significant Bit (MSB) first, and should be valid with the positive edge of the serial port clock. The serial port will only be active when the enable pin is low. Multiple registers can be written to sequentially while the enable pin is low. Multiple registers can be loaded with the same data simultaneously by using the OR of both addresses. See Figure 36 for timing. Each register may serve more than one function, being divided into several fields. The location, definition, and default value of each field is listed in Table 1.

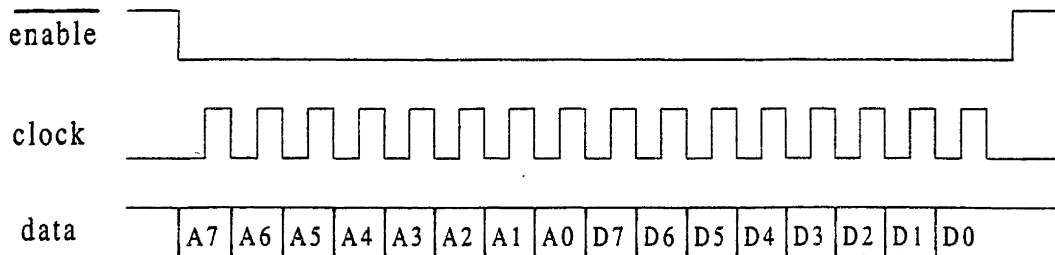


Figure 36: Serial port timing

Address	Data Default Value & Field Number
00X0001X	00000100 1234<-5>
00X0010X	10110100 <---6-->
00X0100X	XX011010 XX<7><8>
00X1000X	00010011 <-9><10>
01X0000X	000000XX <-11->
10X0000X	XXXXXX00 12

Field Number	Definition
1	Low R _{sw} Mode Lock
2	High R _{sw} Mode Lock
3	PWM Mode Lock
4	PFM Mode Lock
5	PFM Pulse Threshold
6	Digital Voltage Reference
7	PFM Measure Frequency
8	PFM Measure Delay
9	PWM Feedback Frequency
10	PWM Feedback Gain
11	Duty Cycle <5:0>
12	Duty Cycle <7:6>

Table 1: Serial Port Registers and Field Definitions

Low R_{sw} Mode Lock (1 bit)

If this bit is high, then the wider set of output switches are always enabled.

High R_{sw} Mode Lock (1 bit)

If this bit is high, then the wider set of output switches are always disabled.

PWM Mode Lock (1 bit)

If this bit is high, then the converter always operates in Pulse Width Modulation (PWM) mode.

PFM Mode Lock (1 bit)

If this bit is high, then the converter always operates in Pulse Frequency Modulation (PFM) mode.

PFM Pulse Threshold (4 bits)

This field sets the number of consecutive pulses in PFM mode which will trigger the return to PWM mode. An entry of zero corresponds to two pulses in a row.

Digital Voltage Reference (8 bits)

This field sets the desired output voltage level, as a fraction of the analog reference voltage supplied to the Analog to Digital Converter (ADC). It is entered in 2s complement form, with the MSB always high. For example, if the ADC reference were 3V, and the desired output voltage were 2V, then the bits "10101011" would be entered into this field. The precompiled C program "pfmb" automatically does this calculation, so the input to this program would simply be a number from 0 to 127.

PFM Measure Frequency (3 bits)

This field sets the frequency at which the differential comparator evaluates the output current. The result is used to determine whether to switch into PFM or Low R_{sw} modes. An entry of zero corresponds to evaluation every other cycle, with interleaving of measurements for PFM and Low R_{sw} modes. Higher entries set frequencies equal to 2^N+2 . For instance, an entry of five corresponds to evaluation every 34 cycles.

PFM Measure Delay (3 bits)

This field defines a time period during which the converter is locked into PWM mode operation. The time period begins when the converter is powered up, and also when the converter switches from PFM mode back to PWM mode. The time is a multiple of the PFM Measure Frequency. If N is the value entered into the PFM Measure Frequency field, then the PFM Measure Delay is equal to:

PWM Feedback Frequency (4 bits)

This field sets the frequency at which both the output voltage is sampled by the ADC and the digital error integrator is updated. The frequency is equal to 2^M+2 . An entry of 1 corresponds to a measurement every third cycle. An entry of zero is illegal.

PWM Feedback Gain (4 bits)

This field sets the gain of the PWM feedback controller, as it is directly connected to a 4x8 bit multiplier in the feedback loop. Thus, an entry of zero is illegal.

Duty Cycle (8 bits)

The Duty Cycle is split into two fields since it is internally a 12 bit number to eliminate rounding errors from multiplication. When either of the two fields is written to, the PWM feedback controller is deactivated until the serial port enable pin is deasserted. The PFM mode feedback controller is not affected. If the reference voltage is changed in PFM mode, then the Duty Cycle should be updated as well to insure that the inductor current returns to zero at the end of a pulse.

Die Pad Signals

Die pads are numbered from 1 to 28 counterclockwise, starting on the upper left hand side, where there are three pads separated from the other pads. Descriptions of each pad signal follow.

Vref (Pad 1)

This is the reference to the ADC, which should be attached to a quiet reference voltage. Digital reference voltage commands from the serial port will be interpreted as a fraction of this reference voltage. If the output voltage is desired to be always a fixed fraction of the input voltage, then the reference voltage could be connected to the input voltage.

VfilterCap (Pad 2)

This is the input to the ADC, which should be attached to the converter output at the filter capacitor.

ShieldGnd (Pad 3)

This is a substrate connection between the digital logic and the analog circuitry. It should be grounded.

VxSmall (Pad 4)

This is the drain connection for the small output transistor pair. It should be connected to the filter inductor.

Vddp (Pads 5, 11, and 12)

This is the source connection to the PMOS output transistors. Pad 6 connects to the small transistor, and Pads 11 and 12 connect to the large transistor.

Gndp (Pads 5, 7, and 8)

This is the source connection to the NMOS output transistors. Pad 5 connects to the small transistor, and Pads 7 and 8 connect to the large transistor.

VxLarge (Pads 9, 10, 13, and 14)

This is the drain connection for the large output transistor pair. It should be connected to VxSmall if Low Switch Resistance (LSR) mode is used.

Gnnd (Pads 15 and 23)

This is the digital power supply ground.

LSRmode (Pad 16)

This status bit is high when the converter is operating in Low Switch Resistance (LSR) mode.

Mclk (Pad 17)

This is the reference clock, at eight times the switching frequency. The NMOS-PMOS switching transition will always take place near a falling edge. The PMOS-NMOS switching transition is determined by the duty cycle.

PFMmode (Pad 18)

This status bit is high when the converter is operating in Pulse Frequency Modulation (PFM) mode.

SerData (Pad 19)

This is the serial address and data input. See Figure 36 for serial port timing.

SerClk (Pad 20)

This is the clock for the serial port interface. Data is registered on the rising edge.

_SerEn (Pad 21)

This is an active low enable for the serial port interface. If they duty cycle register is written to, then the feedback controller will be deactivated until the enable is pulled high.

Reset (Pad 22)

This is an active high reset for all digital registers.

Vhh (Pad 24)

This is the power supply for the pad ring. It should be 5V for a 3V digital logic supply.

Vddd (Pad 25)

This is the digital power supply. Values from 1.5V to 5V are valid at a switching frequency of 250kHz.

Gnda (Pad 26)

This is the analog power supply ground.

Vdda (Pad 27)

This is the analog power supply. Values from 2.5V to 5V are valid.

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