III-V Compositionally Graded Buffers for Heterostructure Integration

By

Adam Christopher Jandl

B.S. in Engineering Physics
University of Wisconsin – Madison, 2008

M.S. in Materials Science and Engineering
University of Wisconsin – Madison, 2009

Submitted to the Department of Materials Science and Engineering in Partial Fulfillment of the Requirements for the Degree of

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Signature of Author: Signature redacted
Department of Materials Science and Engineering
December 22, 2014

Certified by: Signature redacted
Eugene A. Fitzgerald
Merton C. Flemings-SMA professor of Materials Science and Engineering
Thesis Supervisor

Accepted by: Signature redacted
Donald Sadoway
Chair, Departmental Committee on Graduate Students

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ABSTRACT

$In_yGa_{1-y}As$ alloys are critical in commercial applications such as high speed transistors, light emitting diodes, solid state lasers, photovoltaics, and photo-detectors. However, the range of compositions used in these applications is often limited to the range of $In_yGa_{1-y}As$ compositions which are lattice matched to elementary or binary semiconductor substrates. Additionally, the integration of $In_yGa_{1-y}As$ based devices on silicon substrates has been limited by complicated processing procedures. In order to resolve these issues we developed two compositionally graded buffer systems to integrate $In_yGa_{1-y}As$ devices on InP and Si substrates. The development of $In_yGa_{1-y}As$ devices on Si substrates also used the direct growth of Ge on Si offcut substrates.

$InAs_xP_{1-x}$ compositionally graded buffers were investigated for the growth of $In_yGa_{1-y}As$ compositions with lattice constants greater than InP. We report the effects of strain gradient, growth temperature, and strain initiation sequence (gradual or abrupt strain introduction) on threading dislocation density, surface roughness, epi-layer relaxation, and tilt. We find that gradual introduction of strain causes increased dislocation densities ($>10^6$ cm^{-2}) and tilt of the epi-layer ($> 0.1^o$). A method of abrupt strain initiation is proposed which can result in dislocation densities as low as $1.0x10^5$ cm^{-2} for films graded from the InP lattice constant to $InAs_{0.15}P_{0.85}$. A model for a two-energy level dislocation nucleation system is proposed based on our results.

We demonstrate a method for the growth of $In_yGa_{1-y}As$ devices on Si substrates in a single process run. Two epitaxial layers were used to change the lattice constant from the Si substrate to the $In_yGa_{1-y}As$ lattice constant. The first layer was a Ge layer grown directly on Si. To reduce the threading dislocation density to $< 10^8$ cm^{-2} we investigated the most efficient thermal cycle annealing procedure. The second layer was an $In_vAl_{1-v}As$ compositionally graded buffer. $In_{0.3}Ga_{0.7}As$ quantum well devices grown on $In_vAl_{1-v}As$/Ge/Si virtual substrates had threading dislocation density of 2×10^7 cm^{-2}, mobility of 6400 cm^2/Vs, and sheet carrier concentration of 1.1×10^{12} cm^{-2}.

Thesis Supervisor: Eugene A. Fitzgerald
Title: Merton C. Flemings-SMA Professor of Materials Science and Engineering

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1. Introduction

The ternary alloy semiconductor $In_yGa_{1-y}As$ has many current and potential applications in high speed transistors, light emitting diodes, solid state lasers, photovoltaics, and photo-detectors [1]–[7]. These applications all rely on the low band gap and high electron mobility of $In_yGa_{1-y}As$ alloys. However, only one composition of $In_yGa_{1-y}As$ is lattice matched to InP (Figure 1). Any device which requires an $In_yGa_{1-y}As$ composition not closely latticed matched to InP will have to manage the epitaxial misfit strain created by the difference in the lattice constant between the film and the substrate. Since the thickness of most of these devices will be greater than the critical thickness, the films will relax by the nucleation and glide of dislocations. Given the nature of the epitaxial process, this means that segments of these dislocations will pass through the device layers. Due to the electronic states associated with the dislocations [8], the mobility and lifetime of charge carriers will be reduced as a function of the density of dislocations in the device layer. Therefore, in order to prevent severe reduction of the device performance a method to manage the strain and associated defects is required in many applications.

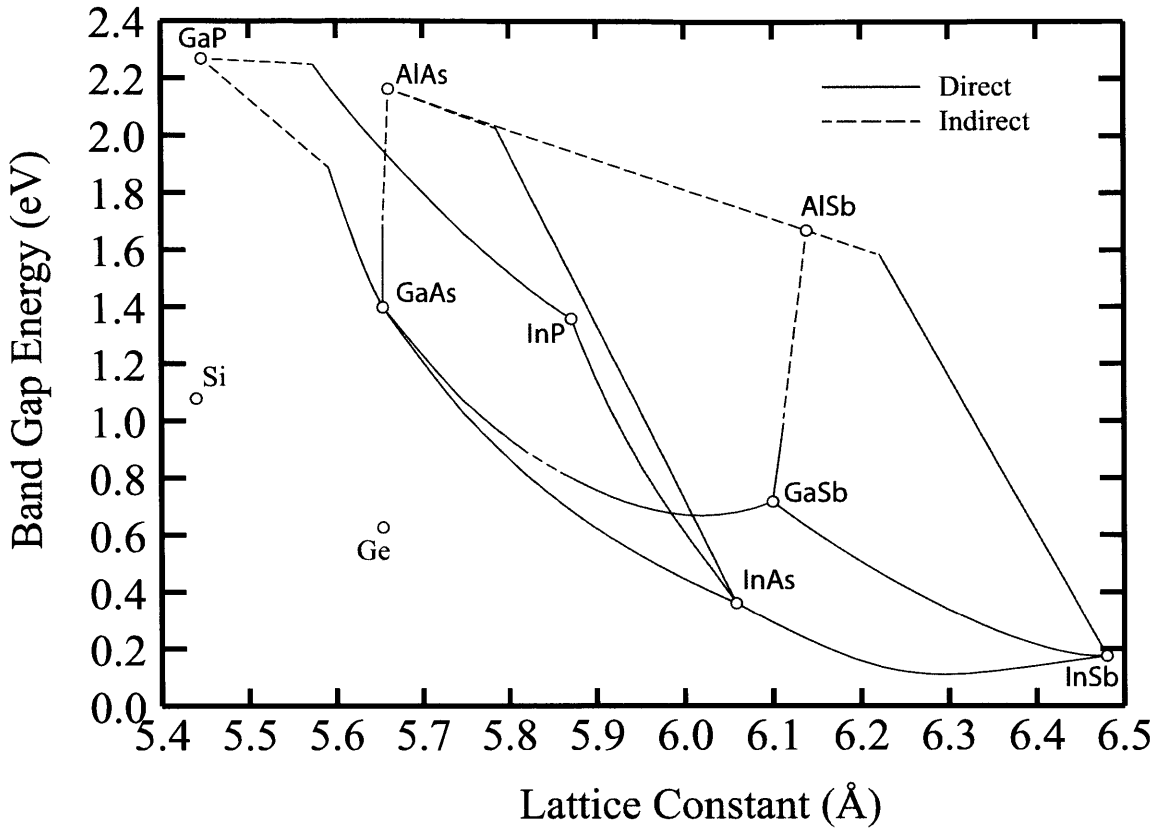


Figure 1: Band gap energy of select III-V and IV semiconductor alloys. Binary alloys are represented as open circles and ternary alloys are shown as solid or dashed lines and are composed of a solid solution of the binary alloy end points. The alignment of the Γ points and the conduction band minimum are indicated in the legend. Materials where these locations coincide are labelled as "direct" band gap semiconductors.

One method to accommodate the lattice mismatch is to grow a compositionally graded buffer which allows for the misfit strain to be slowly incorporated into the film. The more gradual introduction of the strain permits the existing dislocations to relax the film without the need to nucleate additional dislocations.

This thesis discusses the development of two compositionally graded buffer systems for two different $In_yGa_{1-y}As$ devices on InP and Si substrates. In addition, the growth of germanium films directly on silicon substrates in a metal-organic chemical vapor deposition reactor (MOCVD) is presented as an alternative to SiGe compositionally graded buffers for majority carrier devices..

1.1. Lattice mismatched materials and devices

Compositionally graded buffers of various alloys have allowed for low defect density lattice-mismatched devices to be integrated on a variety of substrates [2], [9]–[11]. For the $In_yGa_{1-y}As$ alloy system, multiple graded buffer materials have been developed: $In_yGa_{1-y}As$ [12], $In_vAl_{1-v}As$ [13], $GaAs_zSb_{1-z}$ (for GaAs or Ge substrates) [2], or $InAs_xP_{1-x}$ (for InP substrates) [14], [15] graded buffers are used to create low defect density virtual substrates for $In_yGa_{1-y}As$ device structures. For GaAs substrates, many studies have developed lattice mismatched $In_yGa_{1-y}As$ devices for telecommunication and high speed electronic applications [1]–[3]. On InP substrates, the $In_yGa_{1-y}As$ material system as been used for thermophotovoltaics (TPV), infrared photodetectors, and high-speed electronics [4], [14], [16]. This thesis is primarily focused on the development for compositionally graded buffers for use with TPV, photodiode, and HEMT, or more generally quantum well (QW), applications of $In_yGa_{1-y}As$.

The remainder of this chapter will give a brief overview of the methods for lattice mismatched epitaxy used in this thesis. A review of the range of $In_yGa_{1-y}As$ compositions of interest, the methods of previous studies, and those employed here will be discussed. Finally, the objectives of this research will be established.

1.2. Lattice mismatched epitaxy

Compositionally graded buffers are not the only way to accommodate lattice mismatch while maintaining a low defect density. Layer transfer allows for high quality semiconducting layers to be transferred to a variety of substrates [17] or to remove the graded layer from the final device structure [18], [19]. Epitaxial necking [20] techniques exploit the nature of the 60° dislocations in zinc-blende crystals (see Secton 2.1.1.) to trap nucleated dislocations in narrow channels or wells before the selective growth on the larger, surrounding regions. Both of these techniques require additional processing steps prior to or subsequent to the epitaxial growth. Compositionally graded buffers and thermal cycle annealing of highly strained and defective layers can be grown and annealed in the same CVD reactor and process run as the devices layers and require no additional pre- or post-growth processing. A brief introduction to both of these layer structures is provide here and a more thorough discussion is given in Sections 2.1. and 2.2.

1.2.1. Compositionally graded buffers

Compositionally graded buffers are created by changing the composition of the deposited film continuously (linearly graded) or in small increments (step graded) varying the flows of the reactant gasses. The change in composition, and therefore the lattice constant, creates misfit strain between the epi-layer and sub-layer. Once sufficient strain energy has accumulated, dislocations in the structure will glide creating increased dislocation length along the interface which reduces the misfit strain. The process of compositional grading promotes the glide of existing dislocations over the nucleation of new dislocations in order to relax the film (see Section 2.1.) Since the dislocation density in the substrates is often lower than the dislocation density threading through the film, nucleation of additional dislocations must take place during compositional grading. However, if all of the misfit strain was incorporated into a single change in the lattice constant (i.e. a uniform layer), the strain energy would increase so rapidly that the glide of dislocations would be kinetically limited and dislocation nucleation is activated. Therefore, the advantage of the graded layers allow for much lower dislocation densities to be achieved than if only a single strained layer is grown.

The rate at which strain is incorporated in a graded buffer is determined by the strain gradient which has units of strain, or percent strain, per film thickness (%ε/μm). Typical strain gradients are between 0.2 %ε/μm and 2.0 %ε/μm, with lower strain gradients producing lower threading dislocation densities (see Section 2.1.). The total thickness of the graded layers depends on the total misfit between the substrate and final alloy composition and the tolerable threading dislocation as determined by the strain gradient. The strain field produced by the many misfit dislocations introduced in the graded region can cause spatial variations in the growth rate at the surface of the film, which results in surface roughness and the characteristic cross-hatch morphology [9]. The magnitude of the surface roughness is related to the proximity of the growing surface to the misfit dislocation arrays and is therefore related to the strain gradients. The surface roughness created during the growth of the graded layers can affect the dislocation glide velocity and therefore can cause increases in the TDD values [21] (since new dislocations are nucleated if too much strain accumulates). The morphology produced by the graded layers must be engineered in order to meet the requirements of the particular application of the epitaxial structure.

1.2.2. Two-step growth

A two-step growth process for the deposition of Ge [22], [23] or GaAs [24] on Si and InP [25] on GaAs followed by thermal cycle annealing can create layers with threading dislocation densities as low as 10^7 #/cm^2, which can be suitable for majority carrier devices. The two-step growth refers to the initiation of a thin layer at low temperature followed by a thicker layer grown at higher temperatures. The low temperature initiation is used to create a coalesced planar but defective layer [26], [27] at a small thickness. Threading dislocation interaction close to the interface results in dislocation annihilation, lowering threading dislocation density. The film still has a relatively high density of threading dislocations but the TDD can be reduced by increasing the probability for further dislocation-dislocation reactions which can result in annihilation or coalescence.

There are two methods for increasing the probability of dislocation-dislocation interactions. The first method is to increase the thickness of the epi-layer. As threading dislocations increase in length with film thickness, and since in (001) systems the threading dislocations line direction is along <110> directions, increased film thickness increases the chance for interaction with other threading dislocations. The second method is thermal cycling to create stress due to the difference in thermal expansion coefficient between the film and substrate. Typically the temperature is cycled between 600 °C - 650 °C at the low temperature to 750 °C to 850 °C at the high temperature. The thermal stresses act on the dislocations to cause lateral glide and thereby increases the chance for dislocation-dislocation reactions. By cycling the temperature the dislocations can be repeatedly moved which increases the probability for them to react. Traditionally, increasing either the film thickness or the number of temperature cycles has been used to reduce the TDD.

1.3. InGaAs system

1.3.1. Applications in TPV, photodiodes, and HEMT devices

Much of the development of TPV devices have relied on the $InAs_xP_{1-x}$ graded buffer platform for low defect density virtual substrates [4]–[6], [28], [29]. These devices use $In_yGa_{1-y}As$ photovoltaic cells to convert the black body radiation from a heated emitter to low voltage electrical power. The appropriate band gaps are in the range of 0.5 – 0.8 eV, so $InAs_xP_{1-x}$ graded buffers are a good choice of material for the buffer layer since $InAs_xP_{1-x}$ generally has a larger band gap (Figure 1) than the active materials. This allows for the $InAs_xP_{1-x}$ to act a back-surface-field and window layer in the device structure [4]. Since TPV devices, like photovoltaic devices in general, require long minority carrier lifetimes, it is necessary to eliminate the recombination centers associated with the threading dislocations created in these lattice mismatched devices in order to maximize the efficiency. This thesis will develop a novel method for the growth of low threading dislocation density $InAs_xP_{1-x}$ compositionally graded buffers on InP and will also present a model of a two energy level dislocation nulceation process.

$In_yGa_{1-y}As$ alloys have been widely investigated for use as the channel material in high electron mobility transistors (HEMTs). Much of the previous work has focused on metamorphic HEMTs (m-HEMTs) which consist of a lattice mismatched channel and substrate [7], [30]–[34]. $In_yGa_{1-y}As$ m-HEMTs are commonly developed on GaAs or InP substrates using $In_yGa_{1-y}As$ [30]–[32] or $In_vAl_{1-v}As$ [7], [13], [32]–[34] graded buffers to reduce the threading dislocation densities. Some work has also been done to integrate $In_yGa_{1-y}As$ HEMTs on Ge or Si substrates [35]–[40]. Indium compositions of 30 – 50 % have been identified as the optimal compositions for high power (due to the large band off sets between $In_yGa_{1-y}As$ and $In_vAl_{1-v}As$, Figure 1) or high frequency applications [7], [33], [34]. This thesis investigates a method for the growth of $In_yGa_{1-y}As$ device layers onto 150 mm silicon substrates with an intermediate germanium layer. The presence of the germanium allows for the future development of high mobility hole devices which has been identified as a crucial, and so far lacking, component of complimentary III-V devices [41].

1.3.2. Previous methods for fabricating lattice mismatched $In_yGa_{1-y}As$ devices on InP substrates

Three material systems have previously been reported for the development of $In_yGa_{1-y}As$ device structures with lattice constants between InP and InAs: $In_yGa_{1-y}As$ ($0.53 < y < 1$), $In_vAl_{1-v}As$ ($0.53 < v < 1$), and $InAs_xP_{1-x}$ ($0 < x < 1$) [42], [43]. However, both $In_yGa_{1-y}As$ and $In_vAl_{1-v}As$ alloys suffer from issues of phase separation (resulting from the solution of In with Ga or Al on the group-III sub-lattice) which make it more difficult to the fabricate the high quality buffers required [42]. $InAs_xP_{1-x}$ does not phase separate since it is a mixed group-V alloy. Many previous studies have employed $InAs_xP_{1-x}$ graded buffers [4], [14], [29], [42] but only a few have discussed the quality and defect densities produced by these structures [14], [42]

1.3.3. Previous methods for fabricating lattice mismatched $In_yGa_{1-y}As$ devices on GaAs substrates

Most previous studies have used $In_yGa_{1-y}As$ or $In_vAl_{1-v}As$ graded buffers for the growth of lattice mismatched $In_yGa_{1-y}As$ devices on GaAs substrates [7], [12], [44]–[50]. Since many of the intended applications in these studies were $In_yGa_{1-y}As$ HEMT devices, $In_vAl_{1-v}As$ graded buffers were preferred since the larger band gap of the $In_vAl_{1-v}As$ provides better electrical isolation between the device layers and the substrate. In both of these material systems phase separation is possible. Investigations into $In_nGa_{1-n}P$ and $GaAs_zSb_{1-z}$ compositionally graded buffers to avoid the phase separation have been reported [2], [3], but the quality of these material systems has not progressed sufficiently for broad use in device platforms.

1.4. Research Objectives

Two ranges of $In_yGa_{1-y}As$ compositions are considered in this thesis. The first composition range is for $0.53 < y < 1$ on InP substrates where the low bandgap of the $In_yGa_{1-y}As$ can be used as an active layer in thermophotovoltaic devices. The second composition range is $0 < y \leq 0.53$ where the high electron mobility two dimensional electron gas (2DEG) formed between $In_yGa_{1-y}As$ and delta-doped $In_vAl_{1-v}As$ layers is used for high frequency or high power devices. Two compositionally graded buffer material systems were developed to address the different requirements for each of these types of devices.

1.4.1. Describe the relaxation process of InAsP graded buffers

$InAs_xP_{1-x}$ compositionally graded buffers on InP substrates were developed as a platform for thermophotovoltaic devices, which are minority carrier devices and therefore require threading dislocations densities between $10^5 - 10^6$ #/cm^2. In order to obtain TDD values this low, the strain gradients in the graded buffer layers are limited to ~0.8 %ε/μm or less and dislocation nucleation must be minimized. The first part of this thesis discusses and analyzes the relaxation process in $InAs_xP_{1-x}$ linearly graded buffers on InP. Early result showed evidence of asymmetric relaxation in the low As ($x < 0.2$), initial layers of the graded buffer and suggested that additional dislocation nucleation processes were present. To investigate these nucleation processes, strain in the graded buffers was abruptly initiated. Measurements of the epitaxial tilt, strain relaxation, surface roughness, and TDD were used to study the dislocation nucleation and strain relaxation processes in the $InAs_xP_{1-x}$ graded buffer. It will be shown that strain initiation plays a critical role in the final threading dislocations density (TDD) of the compositionally graded buffers. A method to suppress nucleation from these additional sources is reported and a model for the relaxation process is discussed. This method results in lower TDD and surface roughness of the final graded buffer cap layer.

1.4.2. Develop a method for the integration of InGaAs quantum well devices on Si

For the development of $In_yGa_{1-y}As$ ($0 < y \leq 0.53$) devices on Si, two misfit accommodating layers were investigated. The first layer was the direct growth of Ge onto Si by initiating at low temperatures followed by growth at higher temperatures. This layer accommodates the 4 % strain between the Ge and Si lattice constants. After the growth of the Ge layer, thermal cycle annealing was used to reduce the TDD in the film. $In_vAl_{1-v}As$ compositionally graded buffers were grown on the Ge surface in the same process run. The $In_vAl_{1-v}As$ graded buffers accommodated the lattice misfit between GaAs and InP (up to 3.6 % strain for $In_{0.52}Al_{0.48}As$ lattice matched).

The process times for the thermal cycle annealing of the germanium on silicon can be relatively long compared to the process times for the rest of the epitaxial structure. Minimizing the total process time is important if this technology is to be transferred to an industrial semiconductor foundry, where the throughput of wafers is closely related to the operating costs. Since the intended application of the Ge/Si virtual substrates is for majority carrier devices, TDD values as high as 10^8 #/cm^2 can be tolerated without significant detrimental effects on the device performance [51]. Therefore, the minimum necessary processing for the thermal cycle annealing has been determined while maintaining acceptable levels of TDD ($< 3\times10^7$ #/cm^2) and surface roughness (< 10 nm RMS roughness).

$In_vAl_{1-v}As$ graded buffers provided a method for the integration $In_yGa_{1-y}As$ QW integration on GaAs or Ge substrates, but previous research did not indicate how these devices would perform. Since the intended application for the QW devices was for millimeter-wave power devices and high frequency devices, the 2DEG electron mobility and sheet carrier concentration were the materials properties which need to be maximized for optimal device performance. Previous research showed that the range of indium compositions best suited for these applications was between 30 and 50% In [7], [33], [34].

Usually the goal of research regarding graded buffers is to determine a grading strategy which will minimize the defects nucleated in the graded layer. In this thesis the goal was slightly different since the virtual Ge/Si substrate always had a threading dislocation density of at least 10^7 #/cm^2. Instead the goal was to determine the greatest strain gradient in the $In_vAl_{1-v}As$ compositionally graded buffer which would not significantly increase the threading dislocation density above the density of the virtual substrate. Maximizing the allowed strain gradient also permitted the growth of the thinnest tolerable graded buffer. Minimizing the thickness of the graded buffer layer was necessary to prevent the accumulation of thermally induced strains due to the difference in thermal expansion between the $In_vAl_{1-v}As$ and the silicon substrate. The electron mobility of these devices was measured for various process parameters in order to determine the optimal $In_vAl_{1-v}As$/Ge/Si integration strategy.

The threading dislocation density and buffer thickness were not the only parameters which had to be optimized. $In_vAl_{1-v}As$ alloys are known to phase separate [52]–[54] during heteroepitaxial growth. However, changing the growth temperature also affects the adatom mobility on the surface. By growing at low temperatures, it is possible to kinetically suppress phase separation. Conversely, by growing at elevated temperatures the phase separation can be prevented since it will no longer be thermodynamically favored. Since growing at elevated temperatures increases the dislocation glide velocity (Equation 2 in Section 2.1.2.) the latter approach was preferred. Besides phase separation, surface roughening due to the formation of cross-hatch morphology [9] or dislocations piles-ups [21] was possible as with any compositionally graded buffer. In general the process of surface roughening was controlled by the proximity of the misfit dislocations to the growing surface. Therefore, the extent of surface roughness was related to the strain gradient in the graded buffer.

2. Methods

2.1. Compositionally graded buffers

2.1.1. Dislocations in zincblende materials

Strain relaxation in zincblende materials occurs by the glide of dislocations in the lattice mismatched layers in order to increase the dislocation length at the interface between the mismatched epi-layers. In lattice mismatched epitaxy, glissile dislocations are either introduced by the substrate or heterogeneously nucleated at the surface of the film. The typical density of dislocations in the substrate are on the order of 10^3 cm^{-2} and the final density in lattice mismatched films with strains greater than about 0.5 % are $10^4 - 10^9$ cm^{-2}. Therefore, a majority of the dislocations found in epitaxial films are nucleated during the growth. The relaxation of strain in the lattice mismatched films is provided by the glide of dislocations in the epitaxial layer.

The portion of the dislocation's length laying at the interface is known as the misfit segment and relieves the strain between the mismatched layers (Figure 2). Portions of the dislocation's length extending away from the interface towards the surface are known as threading, or thread, segments. Glissile dislocations in zincblende are of the form $\frac{1}{2}a_c\langle 110\rangle\{111\}$. This means that the Burgers vectors are $\frac{1}{2}a_c\langle 110\rangle$ and lay on the $\{111\}$ planes. When growth occurs in the [001] direction the misfit line direction of dislocations which can relieve strain are in either the [110] or $[1\bar{1}0]$ directions. Therefore there are eight possible Burgers vectors which can relieve lattice mismatch strain. Half of these 8 Burgers vectors can relieve compressive strains and the other half can relieve tensile strains.

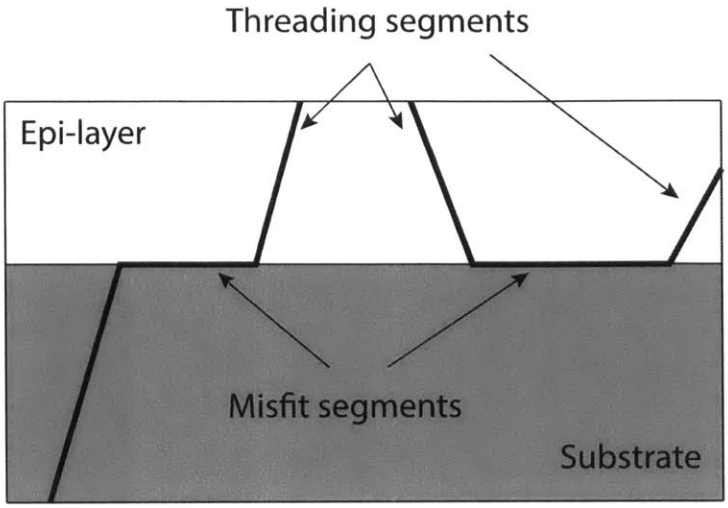


Figure 2: Drawing of the type of dislocations found in the lattice mismatched epitaxy of zincblende materials. The substrate is represented by the gray region and the epi-layer, or film, by the unfilled region. Dislocations are shown as thick black lines.

The angle between the Burgers vector and the misfit line direction of these 8 strain relieving and glissile dislocations is 60°. Therefore, the misfit dislocations are of mixed behavior and the total Burgers vector can be decomposed into edge, screw, and tilt componenets (Figure 3). The edge component locally relieves strain between the lattice mismatched layers. The screw component creates a local rotation of the epi-layer about the [001] direction, known as twist. The tilt component creates a tilt about the [110] or $[1\bar{1}0]$ directions. The sign of the strain imposes restrictions on the possible edge segments since misfit dislocations which cannot relieve strain will not be created by nucleation events. The same restrictions do not apply to the screw and tilt components. Therefore all possible varieties of these latter components can exist and if the population of each is equal, then no global tilt or twist will be observed. If there is a population imbalance then tilt or twist will be observed. All of the possible screw components cause rotation about a single [001] axis. Tilt creates a rotation about two possible axis, [110] or $[1\bar{1}0]$, due to the two possible line directions of the misfit dislocations so the magnitude of the tilt in two orthogonal directions can be measured independently.

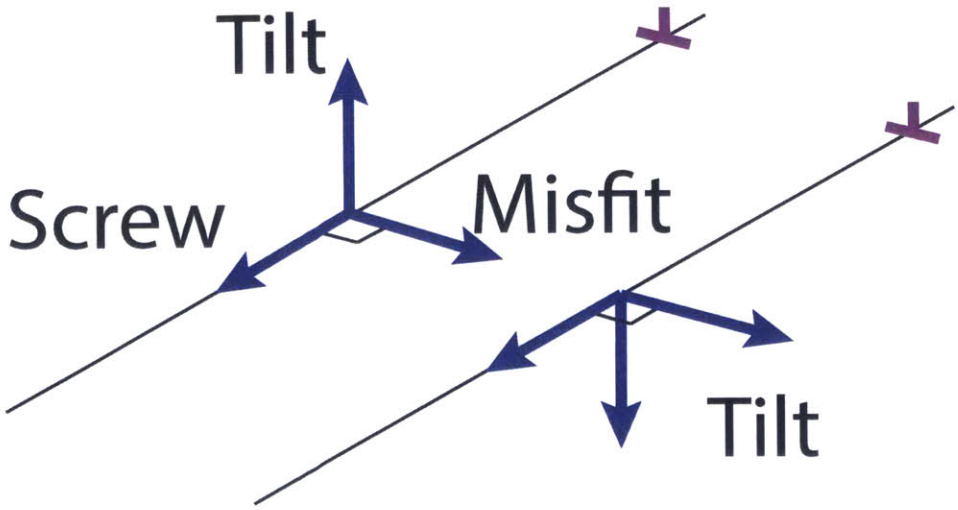


Figure 3: Drawing showing the decomposition of two possible Burgers vectors into the misfit, tilt, and screw components. The black lines represent the line directions of misfit dislocations and lay in the plane defined by the screw and misfit components. The substrate lies below this plane and epi-layer is above. The two possible orientations of the tilt component are shown. Only one of the possible screw components is shown, the other possible orientation has the negative sign of the orientation shown in the figure. The orientation of the misfit component is dependent on the sign of the strain in the epi-layer.

2.1.2. Relaxation process

Graded buffers allow for the management of strain and defects in lattice mismatched epitaxy by preventing the interaction of threading dislocations during the relaxation process. When a sufficient number of threading dislocations are free to glide, the film is able to relax at the same rate that strain is incorporated. The number of required dislocations was derived by Yang *et al.* and Fitzgerald *et al.* [2], [55]. Their theory predicts the number of threading dislocations which must be nucleated in a graded buffer for a constant growth rate, strain gradient, and glide velocity. Since the growth rate and strain gradient are both experimental parameters, a proportionality between the dislocation density and glide velocity is given by:

$$\rho = \frac{2C_f g_r}{bv} \tag{1}$$

where ρ is the threading dislocation density, C_f is the strain gradient, g_r is the growth rate and v is the dislocation glide velocity. The in-plane Burgers vector is represented by b and is equivalent to $0.707a$, (a being the relaxed lattice constant). Glide velocity is a temperature dependent quantity so Equation 1 can be written as:

$$\rho = \frac{2C_f g_r}{b v_o \left(\frac{\sigma_{eff}}{\sigma_o}\right)^m e^{\frac{-E_a}{k_b T}}} \tag{2}$$

where v_o is a constant, material dependent prefactor, m is a power factor which depends on the material system, σ_{eff} is the effective shear stress acting on the dislocations, σ_o is a constant to remove the stress dimensions from the equation, E_a is the material's activation energy for dislocation glide, k_b is Boltzmann's constant, and T is the growth temperature.

Calculations using Equations 1 and 2 show that for any practical strain gradient and growth rate that the threading dislocation density will be between $10^4 - 10^9$ #/cm^2. In devices which depend on the motion of majority carriers (e.g. HEMT devices), the dislocation density can be as high as 10^8 #/cm^2 [51]. However, minority carrier devices can only tolerate densities up to about 10^5 or 10^6 #/cm^2 before the performance suffers [56]. Therefore, it is imperative that dislocation nucleation in the graded buffer be minimized when subsequent layers will contain minority carrier devices. Even though majority carrier devices are less sensitive to the dislocation density, other morphological effects (i.e. surface roughness) could still degrade the device performance and therefore must be minimized as well.

2.1.3. Measurement of threading dislocation density

Accurately measuring the TDD created by a compositionally graded buffer can be challenging since the possible densities cover a board range, $10^4 - 10^9$ cm^{-2}. Imaging the threading segments was done with direct imaging in plan-view TEM or with an optical microscope after etching with a defect highlighting etch. Imaging the defects in a TEM is the most reliable method, but at the lowest TDD values the distance between defects is so large that it is difficult to image enough threads to get a statistically significant result. Etching the defects and then imaging with an optical microscope is known as etch pit density (EPD). EPD measurements can improve the statistics for the lower TDD values but a reliable etch must be available and must be correlated with TEM measurements. To the author's knowledge reliable etches only exist for group IV semiconductors. At TDD values above 10^8 cm^{-2}, EPD measurements are less accurate since the pits start to merge and overlap, but this range of values is easily measured in a TEM.

2.2. Two-step germanium

The epitaxial growth of germanium directly on silicon has historically been grown in ultra-high vacuum chemical vapor deposition (UHVCVD) reactors [22], [57], [58] or with reduced pressure chemical vapor depositions (RPCVD) reactors [59]–[61]. Since the III-V materials will be grown by MOCVD, it is desirable that a single process run could be used to grow both the Ge and the III-V materials on bare Si substrates. Recently, and as a part of this thesis, direct growth of germanium on silicon has been achieved with MOCVD for the first time [23].

2.2.1. Low temperature initiation of Ge on Si

The initiation of germanium on silicon was done at relatively low growth temperatures in order to maintain a planar surface. Bean *et al.* found that planar germanium films could be deposited on silicon for temperatures below 550 °C [26]. Eaglesham and Cerullo showed that growth of germanium directly onto silicon at temperatures above 200 °C will avoid the formation of amorphous germanium layers [27]. These studies establish a temperature window for the initiation of germanium on silicon. Although the germanium is planar, the TDD was as high as 10^{12} cm^{-2}, but could be reduced with subsequent annealing steps [27]. Low temperature initiation was used to create a planar seed layer of germanium before a high temperature growth step followed by thermal cycle annealing to reduce the TDD.

2.2.2. High temperature growth and relaxation of Ge layer

Methods to reduce the TDD of the germanium layers include increasing the growth temperature from the initiation temperature, increasing the thickness of the layer, and cyclic annealing between a high and low temperature. Increasing the growth temperature has two effects. The first is that the growth of germanium at higher temperatures allows for faster growths rates [62]. The second is that the increased temperature increases the dislocation glide velocity (Equation 2) which allows the for the germanium layer to relax. Increasing the thickness of the germanium layers have been shown to decrease TDD [63]–[65] and allows for greater stress to develop during the thermal cycle annealing step. Yamaguchi (for GaAs on silicon) [66] and Luan *et al.* (for germanium on silicon) [22] have shown that thermal cycle annealing can reduce the TDD from 10^9 cm^{-2} to 10^7 cm^{-2}. In this process the temperature is alternated between a low and a high value with brief annealing times at both temperatures. Yamaguchi showed that the high temperature value and the number of annealing cycles was the dominate factors in reducing the TDD through a process of dislocation coalescence and annihilation [66]. The cycling of the temperature creates stress due to the difference in the coefficient of thermal expansion between the substrate and epi-layer. These stresses then act on the threading dislocations causing them to glide and thereby increasing the misfit dislocation length which relieves the strain between the epi-layer and substrate. During this glide process there is a high probability for threading dislocation-dislocation reactions to take place due to the high density. The interactions of these dislocation-dislocation reactions have been described by Romanov *et al.* and Speck *et al.* [67], [68]. Eventually, enough annihilation reactions have occurred to reduce the TDD to a level that cannot be reduced any further due to the wide separation of remaining threading dislocations. In germanium this lower limit is near $\sim 10^7$ cm^{-2}.

2.3. MOCVD Growth

Epitaxial growth was done in a Aixtron close-coupled showerhead metal-organic chemical vapor deposition (MOCVD) reactor. Chemical reactants were trimethyl-indium (TMIn), trimethyl-aluminum (TMAl), trimethyl-gallium (TMGa), arsine (AsH_3), and phosphine (PH_3) and germane (GeH_4). The growth of all III-V alloys was conducted with N_2 as the carrier gas and ambient while the growth of Ge used H_2 as the ambient and carrier gas. The growth pressure was 100 Torr for all material systems except for the initiation of GaAs on Ge which used a pressure of 250 Torr in order to increase the partial pressure of AsH_3. A brief description of the growth techniques and experimental parameters used for the different materials systems is given here and a more thorough discussion of the growth conditions is given at the beginning of each chapter corresponding to the material system discussed therein.

2.3.1. Growth of InAsP compositionally graded buffers

Two methods of compositional grading were used for the growth of $In_yGa_{1-y}As$ compositionally graded buffers. In linearly graded buffers the $InAs_xP_{1-x}$ composition was continually graded from InP towards InAs by computer-controlled reactant flow changes. In step-graded buffers the composition was incremented in 2 %As steps and the thickness of these layers determined the average strain gradient. The strain gradient for all structures was approximately 0.5% strain/μm (except where noted otherwise). The final layer in the structure was a 1μm layer of $InAs_xP_{1-x}$ with a composition matching the last layer in the graded buffer. This capping layer allowed additional time for the structure to attain equilibrium and makes the observation of threading dislocations in plan-view transmission electron microscopy (TEM) easier since it prevents misfit dislocations from obscuring the field of view.

In our experiments three design parameters were varied: the growth temperature, the strain gradient, and the misfit initiation. Each of these parameters was changed individually across a series of samples. For the growth temperature experiment, we used temperatures of 650 °C, 675 °C, 700 °C, and 725 °C. It was found that for growth temperatures of 675 °C and above that it was necessary to increase the ratio of group V species flow to group III species flow (known as the V/III ratio) in order to get smooth epitaxial growth. However, at 725 °C it was found that the highest V/III ratio available in our reactor was still insufficient for high quality epitaxial growth. For the strain gradient experiment, the thickness of the graded layer was changed without changing the final composition. Therefore thinner graded buffer layers experienced higher strain gradients and thicker layers experienced lower strain gradients. In our experiments the strain gradient was changed between 0.33 %ε/μm and 1.37 %ε/μm with nominal final compositions of $InAs_{0.4}P_{0.6}$. For the misfit initiation experiments, the composition of the first layer of the graded layer was changed. After the initial layer was grown a compositionally graded layer starting at the composition of the initial layer and finishing at $InAs_{0.15}P_{0.85}$ was grown. The thickness of the initial layer was chosen to ensure that the total thickness of the epitaxial growth was equal between samples. This allows for all of the samples to experience the same amount of time for relaxation.

2.3.2. Overview of InGaAs quantum well devices on silicon

The full structure of the $In_yGa_{1-y}As$ QW devices on silicon is shown in Figure 4. The lattice mismatch between silicon and the $In_yGa_{1-y}As$ compositions which were used in this thesis were between 5.5 % and 8 %. Two strain relieving layers were used to accommodate this lattice mismatch while maintaining a TDD low enough for majority carrier devices. The first strain relieving layer was germanium grown directly on silicon. Germanium has a 4 % lattice mismatch with silicon so $In_vAl_{1-v}As$ compositionally graded buffers were used to relieve the remaining strain. Figure 5 shows the *in-situ* relative reflectivity of an MOCVD process run starting with the growth of germanium on silicon, followed by thermal cycle annealing, and ending with an $In_vAl_{1-v}As$ compositionally graded buffer.

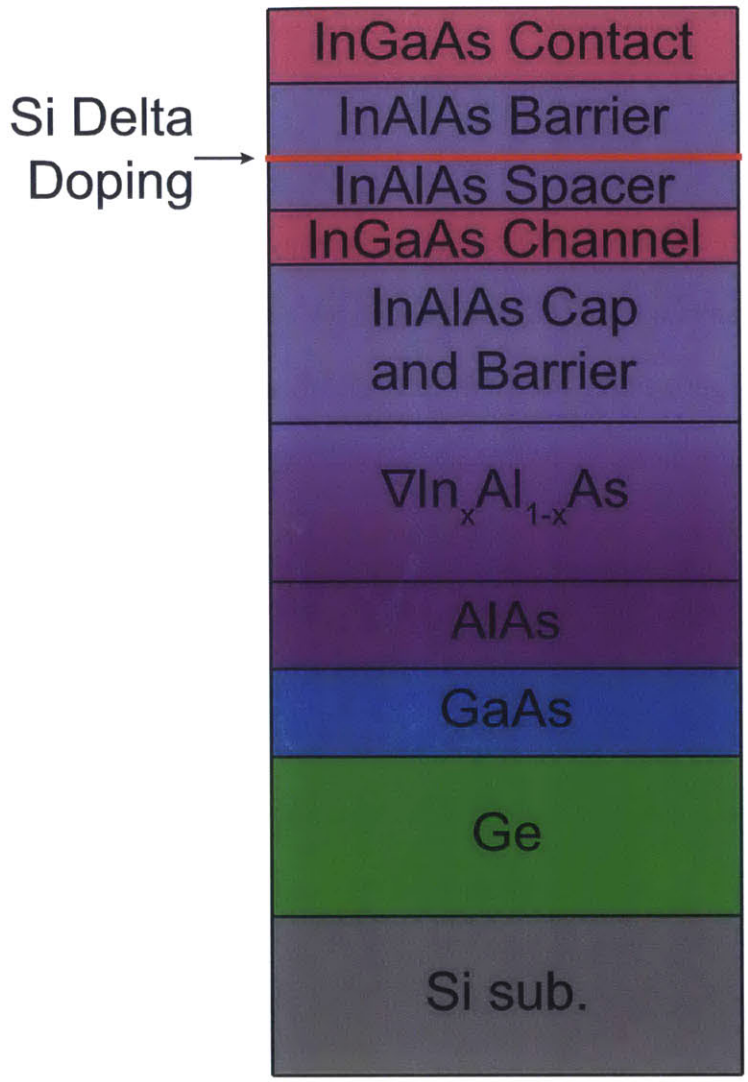


Figure 4: Diagram of final $In_yGa_{1-y}As$ QW device on silicon. The layer thicknesses are not to scale.

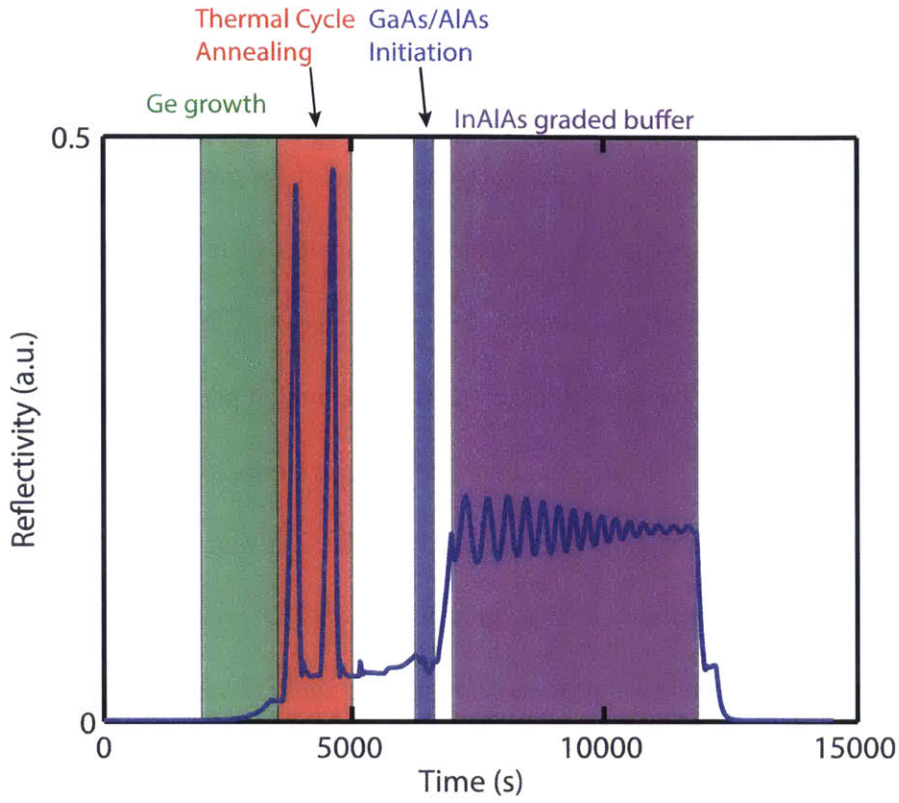


Figure 5: *In-situ* relative reflectivity of a typical $In_vAl_{1-v}As$/Ge/Si growth. When there is a difference in the refractive index of the film and underlying layer the conditions for constructive and destructive interference will be met in an alternating fashion as the thickness of the film is increased. The interference will cause the intensity of the reflectivity signal to oscillate and can be used to calculate the growth rate. Increases in temperature cause increases in the reflectivity. A few time periods have been shaded and labelled to indicate the different parts of the process.

2.3.3. Direct growth of germanium on silicon

The growth of germanium on silicon followed the methods described by Kwang *et al.* [23], [69]. The 150 mm silicon substrates were prepared for growth by a wet chemical cleaning process which results in an oxide free, hydrogen terminated surface. Germanium was initiated at 400 °C in a H_2 ambient to create a defective but planar layer. The growth temperature was then raised to 600 °C while flowing a small amount of GeH_4 which prevented contaminates from accumulating at the surface. At the elevated growth temperature the germanium layer was grown at a faster rate by increasing the GeH_4 flow. The final thickness of the germanium layer is 1 μm. Thermal cycle annealing was used to reduce the TDD. We varied the temperature ramp rate, annealing times, and number of thermal cycles to study how the TDD and surface roughness were affected. If III-V materials were to be grown on the Ge/Si virtual substrate, then the ambient was changed to N_2 and the growth temperature was changed to 650 °C for the initiation of GaAs.

2.3.4. Growth of InAlAs graded buffers

Growth of mixed group III alloys is more complicated than mixed group V alloys (such as $InAs_xP_{1-x}$), especially when used in compositionally graded buffers, since the growth rate and composition are both dependent on the group III flows. In order to simplify the calibration process, the growth rate and composition were left as dependent variables. Instead, the ratio of TMIn to TMAl flow was the controlled variable and the composition was calibrated as a function of this ratio. The growth rate was calibrated as a function of the total group III flow (TMIn and TMAl).

Substrates were either semi-insulating (001) GaAs with a 6° offcut towards the nearest <111>A, or two-step Ge/Si virtual substrates (the growth of these latter substrates is described in Section 0and Chapter 4.). Offcut wafers were used to prevent the formation of anti-phase domains when growing III-V materials on silicon or germanium substrates [70]. In this work, offcut substrates were always used for the growth of $In_vAl_{1-v}As$ graded buffers to ensure consistency between the different substrate materials.

A linear grading strategy was used for all graded buffer layers and was followed by 1μm of constant composition $In_vAl_{1-v}As$. To determine the thinnest allowable graded layer, an experimental set of three buffer with different thicknesses were grown on GaAs substrates. Once a method for grading $In_vAl_{1-v}As$ with a suitable TDD and surface roughness had been established, the structures were reproduced on Ge/Si virtual substrates. The final composition of the graded buffers grown on GaAs substrate was $In_{0.40}Al_{0.60}As$. Due to issues of phase separation, the final composition of the $In_vAl_{1-v}As$ graded buffers on Ge/Si virtual substrates was $In_{0.30}Al_{0.70}As$. The composition and thickness off all samples was confirmed by post-growth analysis.

2.3.5. Growth of InGaAs quantum well devices

Growth of the $In_yGa_{1-y}As$ QW layers immediately followed the growth of the $In_vAl_{1-v}As$ graded buffer described in Section 2.3.4. Two temperatures, 650 °C and 725 °C, were used for the growth of the QW layers. If the growth temperature was 725 °C, the same as the $In_vAl_{1-v}As$ growth temperature, then a separate buffer layer between the channel and virtual substrate was not needed since the graded buffer was capped with a 1 μm constant composition layer. For QWs grown at 650 °C, a short $In_vAl_{1-v}As$ buffer layer, lattice matched to the cap, was grown. This buffer was used to ensure that the delta doping layer above the channel had a greater effect on the Fermi level in the QW then the unintentional contaminate dopants deposited during the growth pause and temperature change. Intrinsic $In_yGa_{1-y}As$ QWs were deposited and followed by $In_vAl_{1-v}As$ barrier layer with a silicon delta doping layer placed a few nanometers above the QW. The delta doping pins the Fermi level near the conduction band in the $In_vAl_{1-v}As$ barrier and, due to the band offsets between the $In_vAl_{1-v}As$ and $In_yGa_{1-y}As$, bends the conduction band edge of the $In_yGa_{1-y}As$ below the Fermi level. This creates a high concentration of electrons in the $In_yGa_{1-y}As$ which in the ideal scenario will have a high mobility since there will be very few scattering mechanisms present in the QW.

2.4. Characterization

Samples were analyzed by transmission electron microscopy (TEM), high resolution x-ray diffraction (HRXRD), and atomic force microscopy (AFM) to measure the material properties (lattice constant, composition, residual strain, crystallographic tilt, dislocation density, and surface roughness) and experimental variables (thickness and lattice mismatch). Van der Pauw Hall effect measurements were used to measure the electrical properties of the $In_yGa_{1-y}As$ QW devices.

2.4.1. Transmission electron microscopy

Cross-section TEM (XTEM) was used to measure the layer thicknesses and plan-view TEM (PVTEM) was used to directly count the number of threading dislocations per unit area. TEM samples were prepared by manual mechanical grinding and polishing followed by Ar^+ ion milling. Since the films contain indium, it was necessary to use two milling steps at 3 kV and 2 kV or less. The latter step helps to remove the indium rich droplets that form during the former step. Images were collected with a JOEL 2011 microscope operating at 200 kV. It should be noted that XTEM cannot provide an accurate value for the TDD since only a very small area of the sample is observed compared to the observable areas in PVTEM.

2.4.2. X-ray diffraction

Symmetric (004) and asymmetric (224) HRXRD reciprocal space maps (RSM) were used to calculate the composition and residual strain in the cap layers and the crystallographic tilt which may have developed during the growth of the graded buffer. A Bruker D8 diffractometer using radiation from the Cu $K_{\alpha 1}$ transition and a linear array detector were used to create the RSMs. To calculate the strain in the [100] and [010] directions, two sets of RSMs were collected with the (110) and $(1\bar{1}0)$ diffraction planes, respectively. The reciprocal space coordinates in this thesis are defined such that:

$$q_x^{(004)} = 0 \text{ Å}^{-1}$$

$$q_z^{(004)} = \frac{40}{a_{(001)}} \text{ Å}^{-1} \tag{3}$$

where $a_{(001)}$ is plane spacing between the (001) planes, which will be denoted as a_3, and is the plane spacing for the planes nearly perpendicular to the wafer's surface normal direction (neglecting the change in orientation due to epi-layer tilt, substrate offcut, or unintentional miscut of the substrate). Additionally, a_1 and a_2 will indicate the plane spacing of the (100) and (010) planes as determined by the reciprocal lattice maps along the $[1\bar{1}0]$ or [110] directions.

Correction of the position of the reciprocal lattice points due to tilt and substrate mis-alignment (due to any offcut or goniometer configuration) followed the methods of Roesener *et al.* [71] The lattice constants of the epi-layers can be determined from the RSM peak positions by:

$$a_{1,2} = a_s\left(1 - \frac{\Delta q_x^{\{224\}}}{\frac{20\sqrt{2}}{a_s} + \Delta q_x^{\{224\}}}\right)$$
$$a_3 = a_s\left(1 - \frac{\Delta q_z^{(004)}}{\frac{40}{a_s} + \Delta q_z^{(004)}}\right) \quad (4)$$

where a_s is the relaxed lattice constant of the substrate and Δq_i is the difference between the film peak and substrate peak for the referenced coordinate. Note that in the first equation, two orthogonal {224} planes are needed to determine a_1 and a_2 independently.

Once the lattice constants are known, three independent strains can be determined by:

$$\varepsilon_i = \frac{a_R - a_i}{a_R} \; ; i = 1, 2, 3 \quad (5)$$

By using Hooke's law under plane stress conditions, $\sigma_3 = 0$, the relaxed lattice constant, a_R, can be found with:

$$a_R = \frac{c_{11}}{c_{11} + 2c_{12}} a_3 + \frac{c_{12}}{c_{11} + 2c_{12}}(a_1 + a_2) \quad (6)$$

and the elastic constants, c_{ij}, are determined by the epi-layer properties. The relaxation of the epi-layer is then defined as:

$$R_i = \frac{a_i - a_s}{a_R - a_s} \; ; i = 1,2 \tag{7}$$

The average relaxation of the epi-layer can be calculated as the geometric average of the relaxations found in Equation 7 as shown by Roesener *et al.* [71]:

$$\bar{R} = \frac{1}{2}(R_1 + R_2) \tag{8}$$

The relaxed lattice constant and relaxation of the films were determined by processing the 004 and 224 RSM data with a MATLAB script to calculate the center of mass of the two dimensional peaks, a second script then corrected the peak positions for substrate offcut and epitaxial tilt, finally a spreadsheet was used to iteratively solve for the relaxed lattice constant based on the corrected peak positons of the epitaxial layer and substrate. An iterative approach was used to solve for the relaxed lattice constant since the elastic constants in Equation 6 are functions of the epi-layer composition which itself cannot be determined until the relaxed lattice constant is known. The rest of this section describes the computations done by the MATLAB scripts and the spreadsheet.

The MATLAB function *PeakSelector.mat* (Appendix 7.2. 7.1.) reads RSM data into matrices for plotting and coordinate vectors. Multiple RSMs can be combined into the same figure which is often necessary since the detector scan range is often not large enough to collect all of the diffracted signals in a single scan. After plotting the data the user is asked to select a region of the reciprocal space data surrounding an individual peak. The center of mass of the top half of the peak in the sub-region is then calculated as the peak location and the user is asked if the peak location is valid (invalid detection of a peak position happens when the shoulder of an adjacent peak is captured in the sub-region). When the calculated position is not valid the user is allowed to pick the peak location manually. This process of selecting a sub-region and peak location is then repeated for every peak in the RSM and the user indicates which of the selected peaks corresponds to the substrate reciprocal lattice point (RLP). The (q_x, q_z) values are then returned to the *XRD_analysis.mat* (Appendix 7.1.) script.

The *XRD_analysis.mat* script is used to call the *PeakSelector.mat* function for both the 004 and 224 RSM. After the peak locations for the both of the RSMs have been returned to the *XRD_analysis.mat* script, the rotation of the 004 substrate RLP about the origin is calculated as:

$$\tan(\Omega) = \frac{q_{x,sub}^{(004)}}{q_{z,sub}^{(004)}} \tag{9}$$

where $q_{x,sub}^{(004)}$ and $q_{z,sub}^{(004)}$ are the observed reciprocal space coordinates of the substrates 004 RLP and Ω is the rotation of the 004 substrate RLP due to misalignment of the substrate on the goniometer or substrate offcut, intentional or otherwise (Figure 6a-b). Since the rotation of the substrate RLP does not contain any structural information and should be zero (Equation 3), a rotation matrix is used to rotate all of the observed RLP coordinates (from both the 004 and 224 scans) by $-\Omega$:

$$\begin{pmatrix} q_x \\ q_z \end{pmatrix}_{corrected} = \begin{pmatrix} \cos(\Omega) & -\sin(\Omega) \\ \sin(\Omega) & \cos(\Omega) \end{pmatrix} \begin{pmatrix} q_x \\ q_z \end{pmatrix}_{misaligned} \tag{10}$$

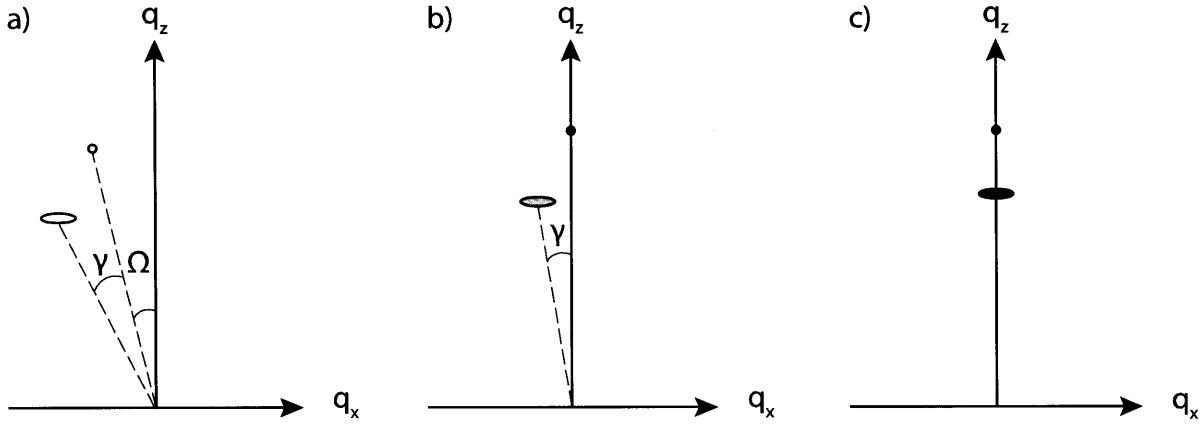


Figure 6: Schematics of reciprocal space maps. The substrate peak is represented by a circle and the film peak is represented by an oval. a) The raw data collected by the diffractometer includes rotations of substrate and film peaks by Ω and $\Omega + \gamma$ respectively. b) Correcting for the Ω rotation. c) Correcting only the film peak for the epitaxial tilt γ.

Once the RLP coordinates have been corrected for the misalignment or substrate orientation then the RLP coordinates of the epi-layers need to be corrected for tilt. The epitaxial tilt of each peak was calculated by

$$\tan(\gamma) = \frac{q_{x,corrected}^{(004)}}{q_{z,corrected}^{(004)}} \tag{11}$$

where $(q^{(004)}_{x,corrected}, q^{(004)}_{z,corrected})$ are the RLP coordinates of epi-layer as calculated by Equation 10 and γ is the epitaxial tilt of the layer (Figure 6a-b). Once the tilt of each epi-layer is known, the true RLP coordinates for each layer can be calculated with an equation similar to Equation 10 except with γ substituted for Ω (Figure 6c). The true RLP coordinates are then used in Equation 4 to calculate the lattice constants of the epi-layer.

2.4.3. Atomic force microscopy

A Nanoscope IV AFM measured the root-mean-square (RMS) roughness of the samples. Two scan sizes were used, 5 x 5 μm and 25 x 25 μm. The former can image the bunching of atomic steps at the surface while the latter images the cross-hatch morphology. The cross-hatch morphology is a result of dislocation pile-ups - which create deep trenches - or the strain fields emanating from the misfit arrays in the graded buffer - which create small amplitude ripples [9], [21].

2.4.4. Van der Pauw and Hall effect

Van der Pauw and Hall effect measurements at room temperature were used to measure the 2DEG electron mobility and sheet carrier concentration. Indium contacts were created by melting indium metal directly onto the $In_yGa_{1-y}As$ contact layer with a hot plate at 250 °C. The contacts were placed in the corners of approximately 1 cm x 1 cm pieces cleaved from the larger sample. The indium contacts were 1-2 mm in diameter. After the indium contacts were in place, the $In_yGa_{1-y}As$ contact layer was selectively etched with a citric acid and hydrogen peroxide solution [72] to remove the secondary conduction pathway.

3. InAsP Compositionally Graded Buffers

We grew $InAs_xP_{1-x}$ compositionally graded buffers to investigate how the layers relaxed by dislocation nucleation and glide. We varied the strain gradient, growth temperature, and the amount of misfit strain initiated at the $InAs_xP_{1-x}$/InP interface. Each parameter was varied independently. Our observations of the TDD, relaxation, epi-taxial tilt, and surface roughness allowed us for formulate a model which we used to explain the dislocation nucleation and glide processes in the compositionally graded layers.

3.1. Experimental Procedure

The MOCVD growth of $InAs_xP_{1-x}$ layers was done with an excess over-pressure of group V precursors. The group V to group III reactant (V/III) ratio was 160 or 320. The substrates were semi-insulating (001) on-axis InP purchased from AXT Inc. The epitaxial processes began with a 500 nm homoepitaxial InP layer. This was followed by the $InAs_xP_{1-x}$ compositionally graded layer. At the end of the graded buffer, a 1 μm constant composition cap layer was grown with same composition as the final layer in the buffer. Cooling from the growth temperature to 350 °C was done under an overpressure of arsine and phosphine to prevent any degradation of the sample surface due to the evaporation of the group V species.

Table 1 provides a summary of the experiments and the parameters of each sample used in the studies. Three sets of experiments were implemented to determine the effects of growth temperature (Temp), strain gradient (SG), and strain initiation sequence (SI) on threading dislocation density, nucleation, and surface roughness. Each experimental set consisted of graded buffers grown with the variation of one design parameter. The only exception was in the growth temperature experimental set.

Table 1: Experimental parameters and results of $InAs_xP_{1-x}$ compositionally graded buffers.

Study	Growth Temperature (°C)	Strain Gradient (%ε/μm)	Grading Method	Initial Misfit (%)	Cap Composition (%As)	V/III	TDD (#/cm²)	RMS Surface Roughness 5x5 μm (nm)	RMS Surface Roughness 25x25 μm (nm)
SG[i]	650	0.33	Linear	0.0	44	160	$1.63 \cdot 10^6$	0.3	4.81
SG	650	0.41	Linear	0.0	39	160	$2.95 \cdot 10^6$	1.0	4.26
SG	650	0.53	Linear	0.0	37	160	$3.29 \cdot 10^6$	2.4	4.84
SG	650	1.37	Linear	0.0	38	160	$5.90 \cdot 10^6$	1.7	5.22
SG	650	--	Linear	0.0	39	160	$7.34 \cdot 10^8$	35.4	36.7
Temp. SI[ii]	650	0.55	Step	0.0	16	160	$3.33 \cdot 10^6$	1.4	3.8
Temp.	675	0.48	Step	0.0	14	320	$1.30 \cdot 10^6$	0.5	4.3
Temp.	700	0.48	Step	0.0	14	320	$7.20 \cdot 10^5$	0.6	3.8
SI	650	0.51	Step	0.16	15	160	$1.27 \cdot 10^5$	0.6	3.2
SI	650	0.55	Step	0.34	16	160	$1.01 \cdot 10^5$	0.3	1.7
SI	650	0.55	Step	0.53	16	160	$1.88 \cdot 10^6$	0.4	1.9

[i]SG: Strain Gradient; [ii]SI: Strain Initiation

It was found that at higher temperatures a higher V/III ratio was needed to compensate for the increased phosphorus vapor pressure. For temperatures greater than 650 °C a V/III ratio of 320 was used and all growths at 650 °C used a ratio of 160. Growth rates for all temperatures were between 0.35 and 0.54 nm/s. Growth temperatures ranged from 650 °C to 725 °C in 25 °C increments and the graded buffers were step graded to 15 %As. For the strain gradient experiments, the composition was linearly graded from 0 %As to 40 %As while the thickness of the graded buffer was adjusted to vary the strain gradient between 0.33 %strain/μm to 1.37 %strain/μm. In the strain initiation experiments, the misfit of the initial layer was varied between 0.16 % (5 %As) and 0.51 % (15 %As). The thickness of this initial layer was such that all structures had the same final thickness. After the initiation layer, the structures were step graded to 15 %As. All structures in the strain gradient and strain initiation experimental sets were grown at 650 °C.

3.2. Results

3.2.1. Morphology of InAsP compositionally graded buffers

Figure 7 and Figure 8 show typical XTEM images of linear and step graded buffers respectively. XTEM imaging used either the <110> pole condition (not pictured) or the bright field <220> two-beam condition. The former is the proper alignment for thickness measurements, while the latter gives improved contrast to the dislocations in the structure. XTEM micrographs were used to confirm the layer thickness of the cap and entire graded layer. The average strain gradient was calculated once the cap composition was measured by HRXRD. Nomarski and AFM micrographs were collected for all films but Figure 9 shows the micrographs of a representative $InAs_xP_{1-x}$ compositionally graded buffer. The characteristic cross-hatch morphology of the graded buffer layer was observed.

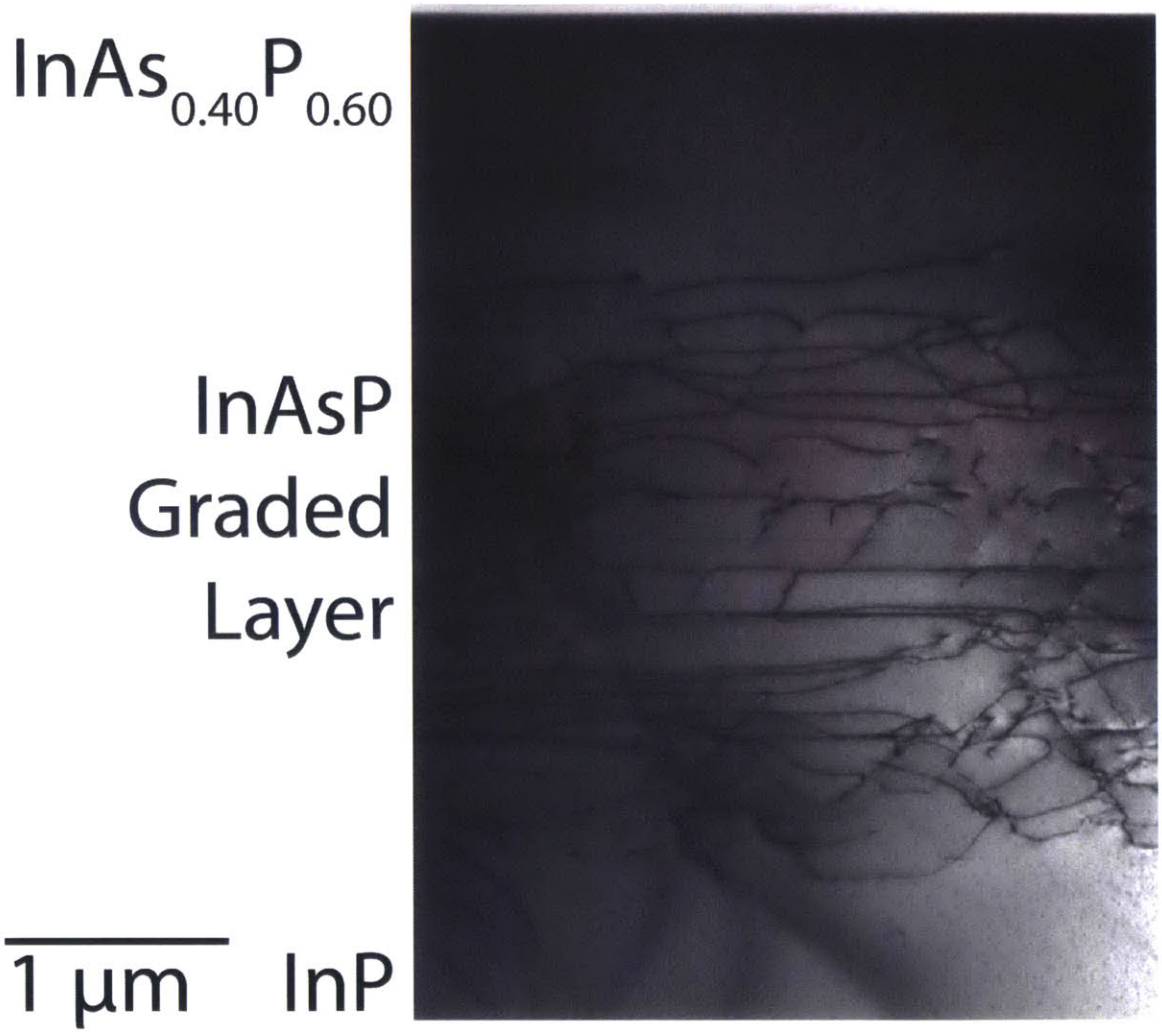


Figure 7: Typical cross section TEM micrograph of a linearly graded $InAs_xP_{1-x}$ buffer imaged with the 220 two-beam diffraction condition. The thin dark lines running nearly horizontal are misfit dislocations. No threading dislocations are observed in the cap layer. The image was edited with non-linear brightness and contrast layers in addition to sharpening effects to enhance the visibility of the dislocations.

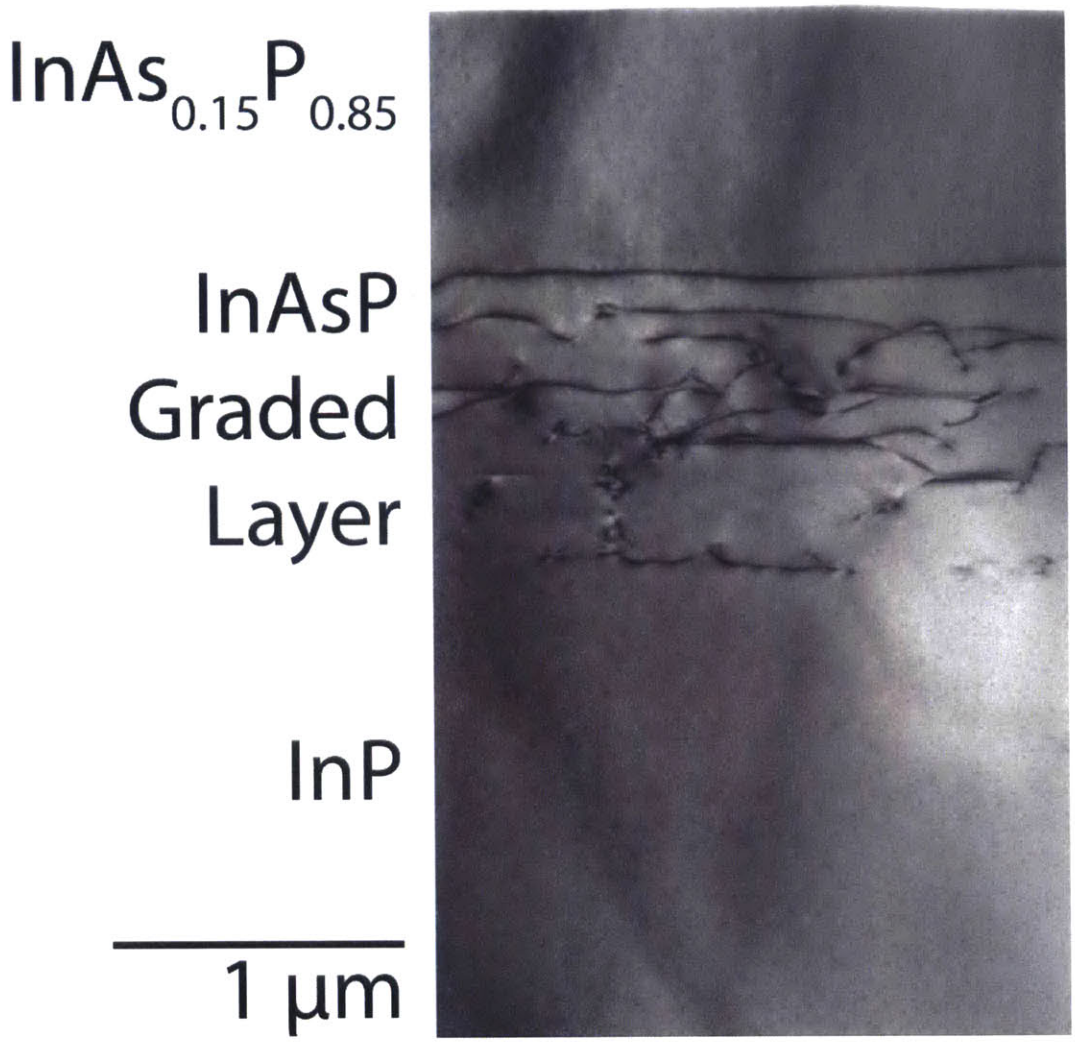
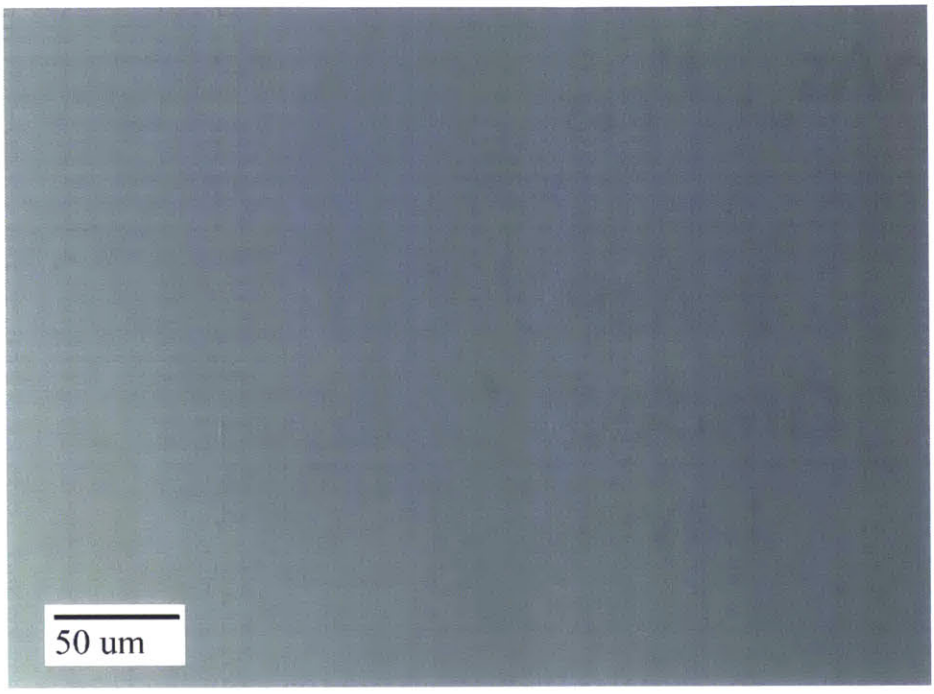


Figure 8: Typical cross section TEM micrograph of a step graded $InAs_xP_{1-x}$ buffer imaged with the bright-field 220 two-beam diffraction condition. The thin dark lines running nearly horizontal are misfit dislocations.



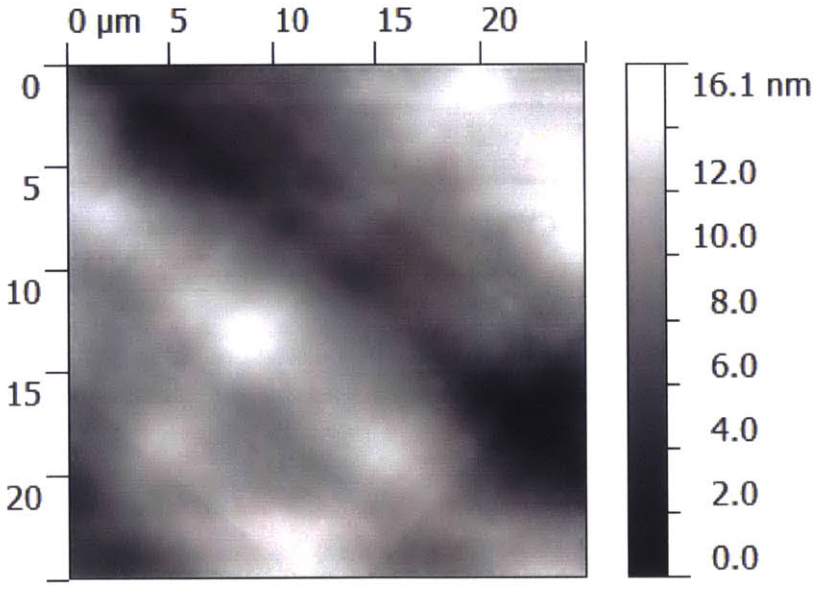


Figure 9: Nomarski (top) and AFM (bottom) micrographs of a representative $InAs_xP_{1-x}$ compositionally graded buffer. Cross-hatch morphology was observed in both micrographs.

HRXRD RSMs of linearly graded buffers revealed distinctive features of $InAs_xP_{1-x}$ buffers. Figure 10 shows a typical RSM for these structures. The map shows that tilt initially develops in the graded buffer but is abruptly halted when the composition reaches 15-20 %As. Tilt is often observed in graded buffers and results from an imbalanced population of the type of Burgers vectors possessed by the misfit dislocations [13]. Since the nature of the tilt changed it implies a dislocation nucleation event occurred which changed the balance of the dislocation population.

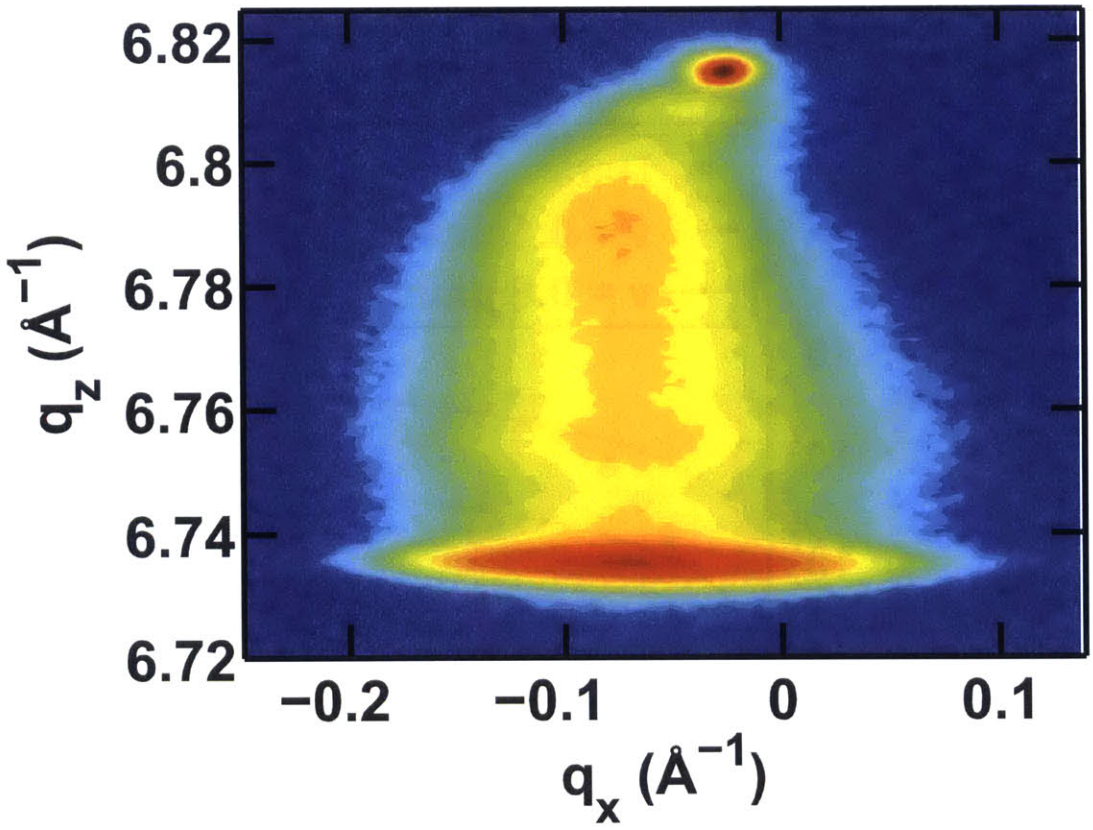


Figure 10: HRXRD RSM of the symmetric 004 reciprocal lattice point of a typical, linearly graded, $InAs_xP_{1-x}$ buffer. The small peak at the top of the figure is the InP substrate and the broader peak at the bottom of the figure is the $InAs_{0.36}P_{0.64}$ cap. The intensity between these peaks was diffracted by the graded buffer layer. In the initial layers of the graded buffer tilt develops in the negative q_x direction but abruptly stops developing when the composition is between 15-20 %As. The color scale is logarithmic.

3.2.2. Effect of strain gradient

By measuring the threading dislocation density as a function of the strain gradient the average glide velocity could be estimated. Plotting Equation 1 with glide velocities of 0.1 - 0.8 μm/s shows an appropriate range of values (Figure 11). A sample which intentionally lacked a graded buffer was used for a comparison. All the samples were grown at 650 °C to a final composition of approximately $InAs_{0.4}P_{0.6}$ confirmed by HRXRD. The thickness of the graded buffers were measured with XTEM. The thickness and composition allowed for the strain gradient to be calculated.

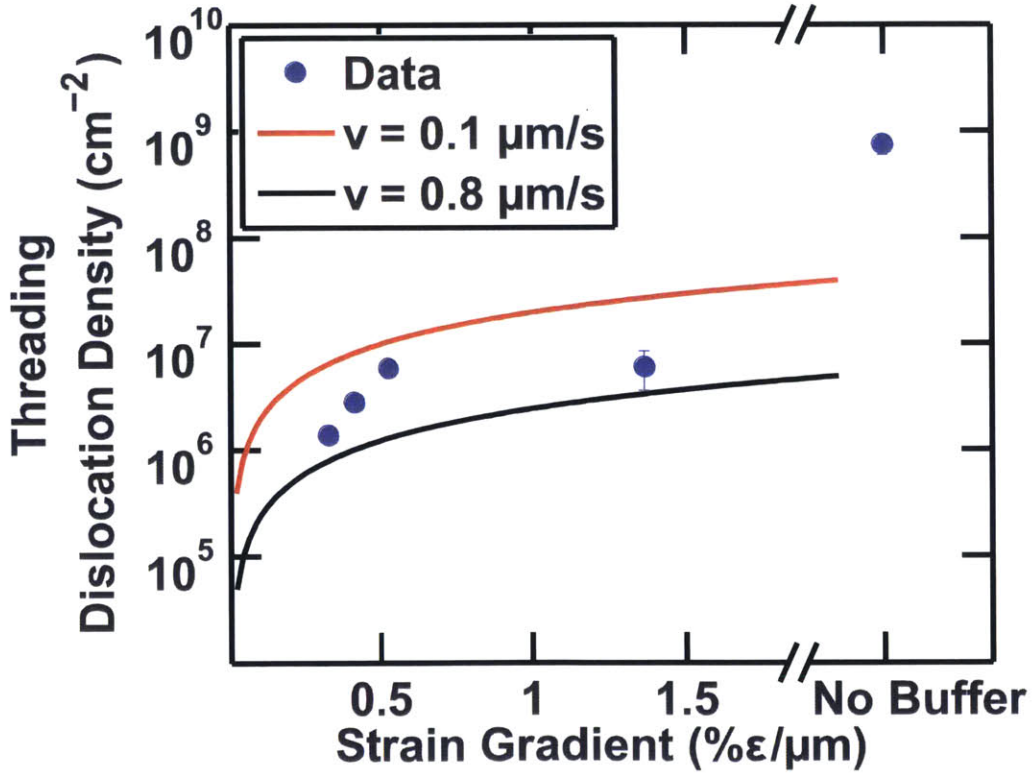


Figure 11: Experimental data and theoretical fit of graded buffers with different strain gradients. The error bars are 95% confidence intervals and fall inside the markers for most of the data points. Equation 1 is plotted with two glide velocities, as noted in the legend. The sample labeled "No Buffer" intentionally lacked any graded buffer and was used as a point of comparison.

3.2.3. Effect of temperature

The threading dislocation density and surface roughness were measured for samples grown at temperatures between 650 °C and 700 °C. The structure grown at 725 °C had a rough surface (Figure 12) and appeared to have been grown with V/III ratio which was too low. Since the MOCVD used in these experiments was not able to increase the flow of the group V species further, it was decided to eliminate this temperature from the experimental set. The purpose of these experiments was to determine how dislocation nucleation and glide were affected by the growth temperature. As the temperature was increased from 650 °C the threading dislocation density decreased toward a minimum at 700 °C (Figure 13). Equation 2 was fit to the data to determine the activation energy for dislocation glide. This energy was found to be 1.3 eV. The surfaces of all samples was slightly roughened due to the formation of cross-hatch morphology or dislocation pile-ups (Figure 14).

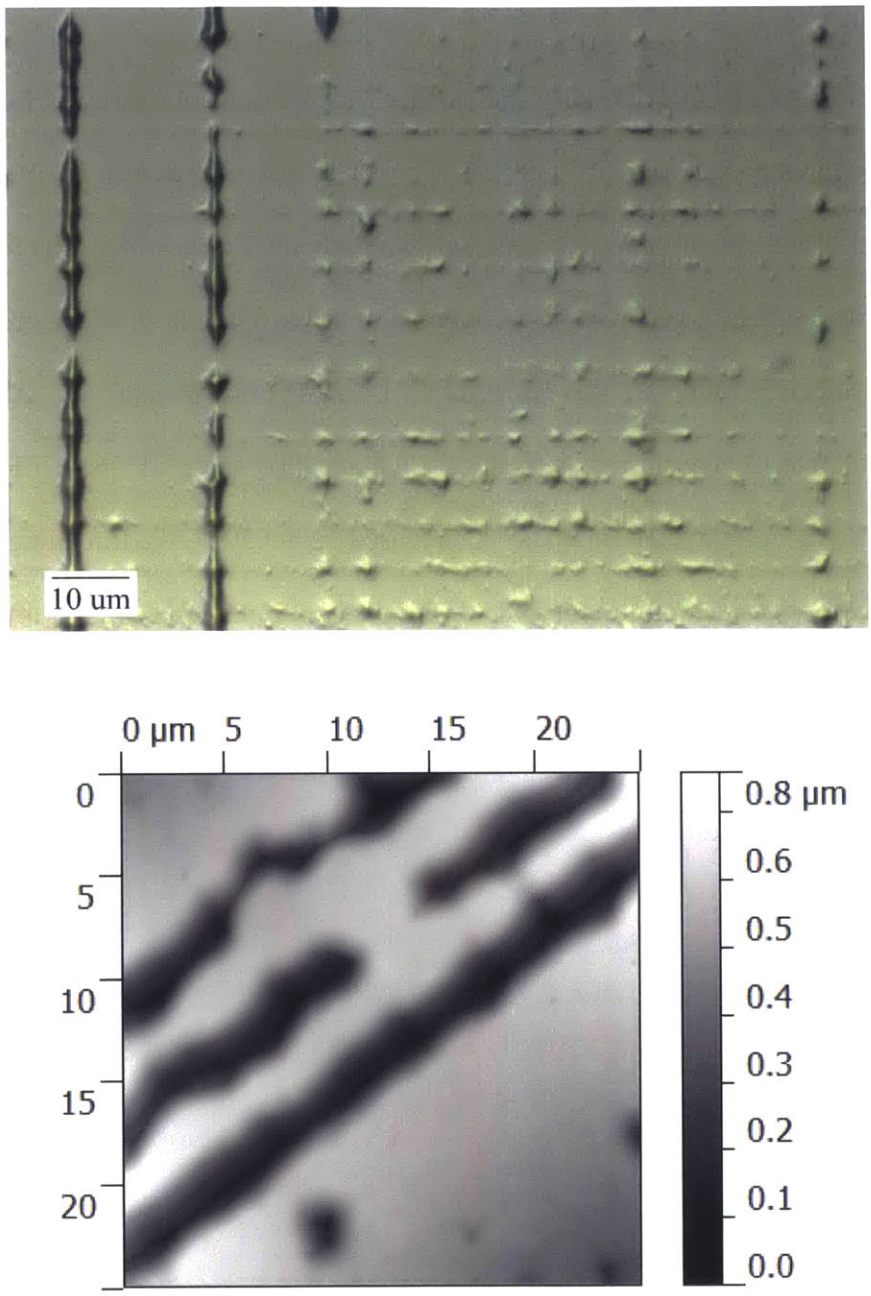


Figure 12: Nomarski (top) and AFM (bottom) micrographs of the structure grown at 725 °C. Deep fissures are observed across the surface of the film and are indicative of a low V/III ratio. Since the V/III ratio could not be increased, it was decided to eliminate this structure from the experimental set.

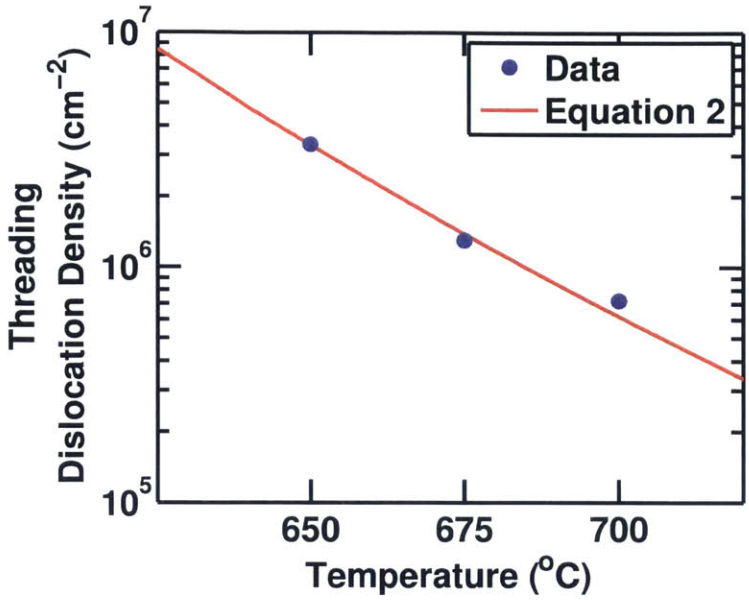


Figure 13: The threading dislocation density as a function of the growth temperature was measured by PVTEM. Increasing the temperature from 650 °C to 700 °C decreased the threading dislocation density by about one order of magnitude. The V/III ratio was 160 at 650 °C and 320 for temperatures of 675 °C and above. The 95% confidence intervals fall within the markers for the data. Equation 2 is fit to the data with E_a = 1.3 eV which is slightly lower than the values reported for InP and InAs by Yonenaga *et al.* [73].

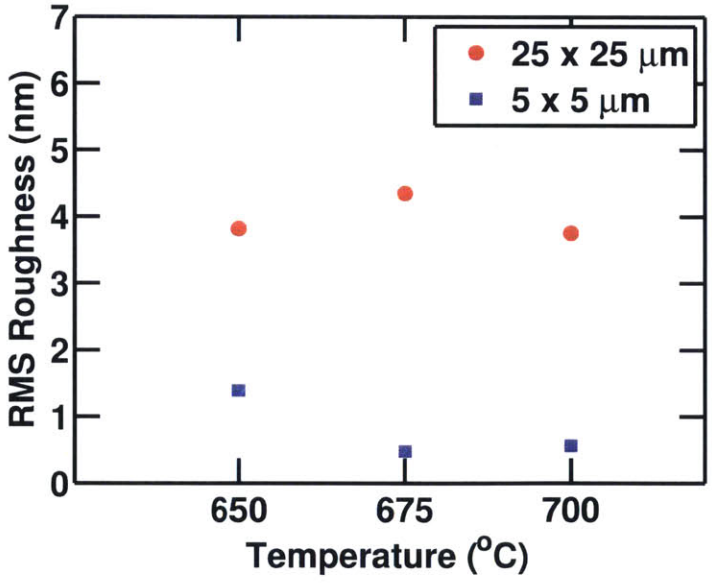


Figure 14: AFM measurements of the root mean square surface roughness for structures with different growth temperatures. The V/III ratio was 160 at 650 °C and 320 for temperatures of 675 °C and above.

3.2.4. Effect of initial misfit

Figure 15 shows the threading dislocation density of the strain initiation experimental set. The dislocation density decreased by more than an order of magnitude when a strain initiation layer of either 5 or 10 %As was used (0.16 and 0.34 % misfit, respectively). When the initial misfit was increased, to 15 %As (0.53 % misfit), the dislocation density increased to an amount similar to the graded buffer which did not have abruptly initiated strain. The surface roughness (Figure 16) did not follow the same trend, however the minimum surface roughness was still observed when the initial misfit was 0.53 %. The roughness for all structures which had abrupt strain initiation was lower than for the structure which had gradual strain initiation. Although the differences in surface roughness were not large, the trend implied that the mechanism of surface roughening was reduced by the abrupt strain initiation.

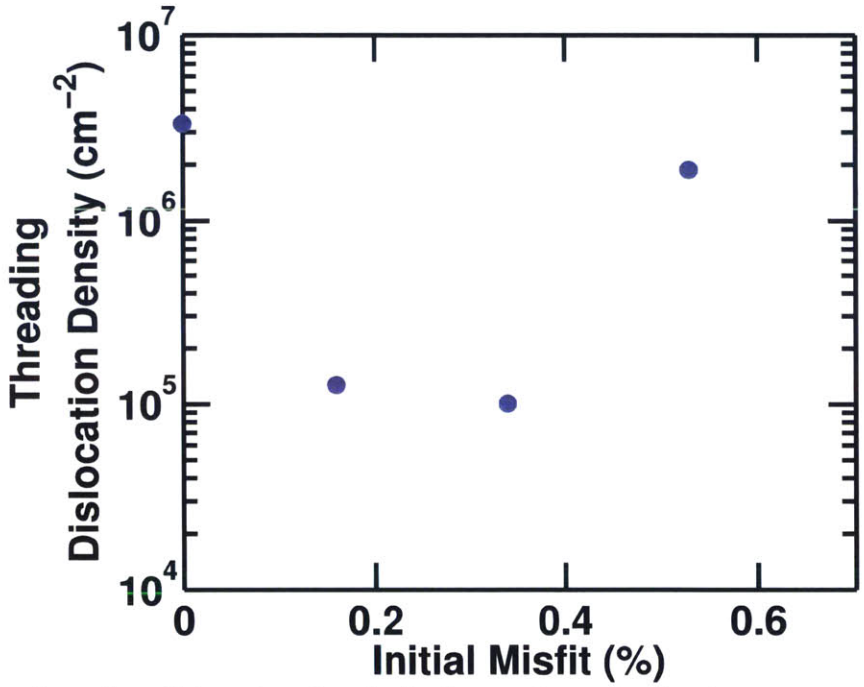


Figure 15: The threading dislocation density in the cap layer for the three structures which had abruptly initiated strain and for one structure which was step graded from 0 %As (plotted as having 0 % initial misfit). The 95% confidence intervals fall within the markers for the data.

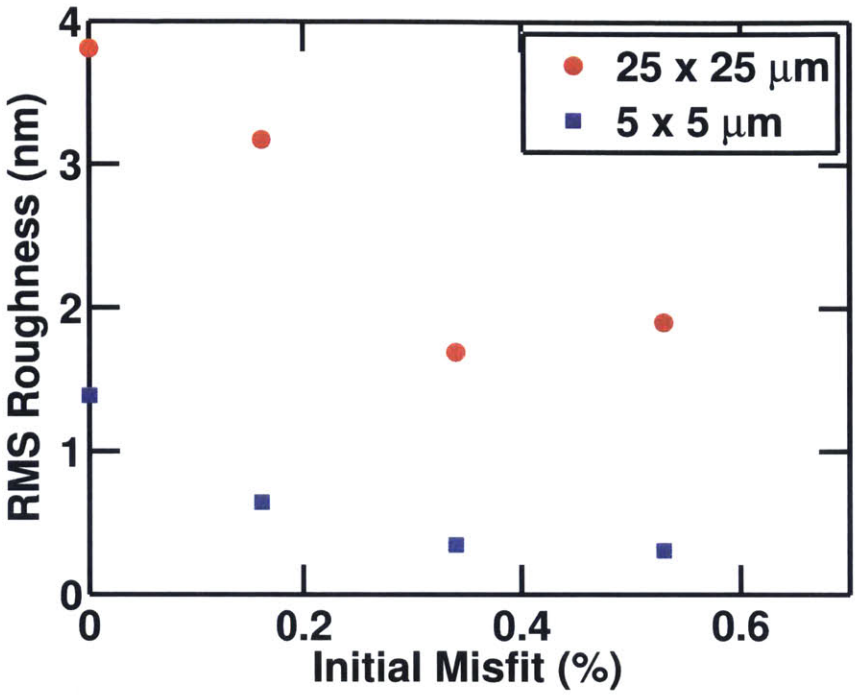


Figure 16: AFM measurements of the root mean square surface roughness for various initial misfits. For the 0% initial misfit sample, the composition was step graded from the InP lattice constant without an abrupt strain layer. The legend indicates the dimensions of the measured region.

HRXRD of the strain initiation experimental set indicated a difference in the dislocation nucleation and relaxation process of the abruptly initiated graded buffers. Figure 17 shows the RSMs of the four structures included in the strain initiation experimental set and the absolute value of the tilt of the cap layer which was measured from the RSMs. Together, these plots show that the tilt decreased as the initial misfit increased. The reduction in tilt suggested that the population of Burgers vectors which were created during the dislocation process were becoming more evenly distributed between the 8 possible glissile orientations allowed in a compressively strained film. Additionally, Figure 18 shows that the average relaxation in the cap layers increased with the initial misfit. This implied that there was less impediment to the glide of the threading dislocations during the relaxation of these structures.

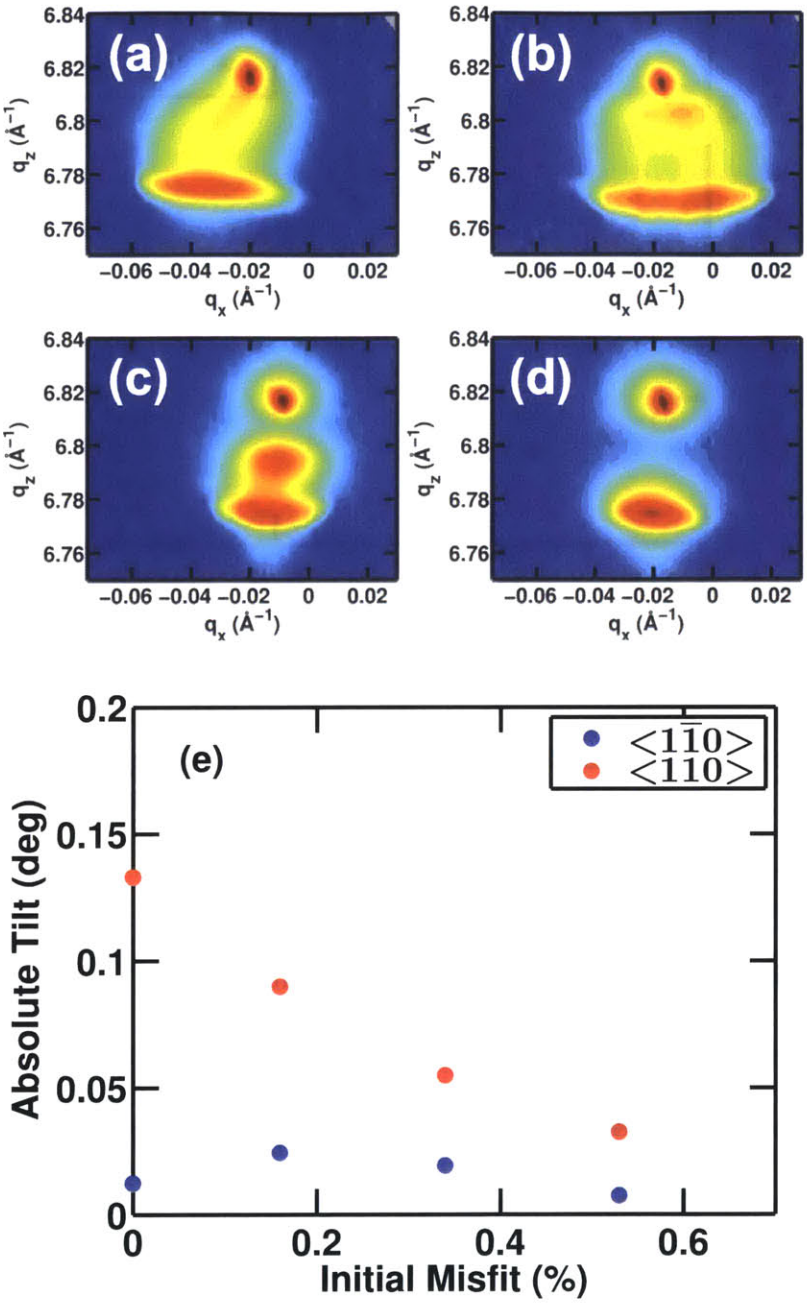

(a)
(b)
(c)
(d)
(e)
6.84
6.82
6.8
6.78
6.76
q_z (Å^{-1})
−0.06 −0.04 −0.02 0 0.02
q_x (Å^{-1})
0.2
0.15
0.1
0.05
0
Absolute Tilt (deg)
0 0.2 0.4 0.6
Initial Misfit (%)
<1$\bar{1}$0>
<110>

Figure 17: (a) RSM with a (110) diffraction plane of a step graded $InAs_xP_{1-x}$ buffer. (b-d) RSMs with a (110) diffraction plane of step graded buffers with abrupt strain initiation. The additional peak observed between the cap layer and substrate layer in (b) and (c) can be used to calculate the lattice constant and composition of the initiation layer. The structure measured in (d) was intentionally initiated at the same composition as the cap, so the initiation and cap layers are contained in the same peak. (e) The absolute value of the tilt of the cap layer for the 4 structures measured in (a-d). The tilt values for (a) are plotted as having 0 % initial misfit. The crystallographic directions indicated in the legend refer to the diffraction plane normal used during the collection of the RSMs. Tilt was recorded as defined by [71].

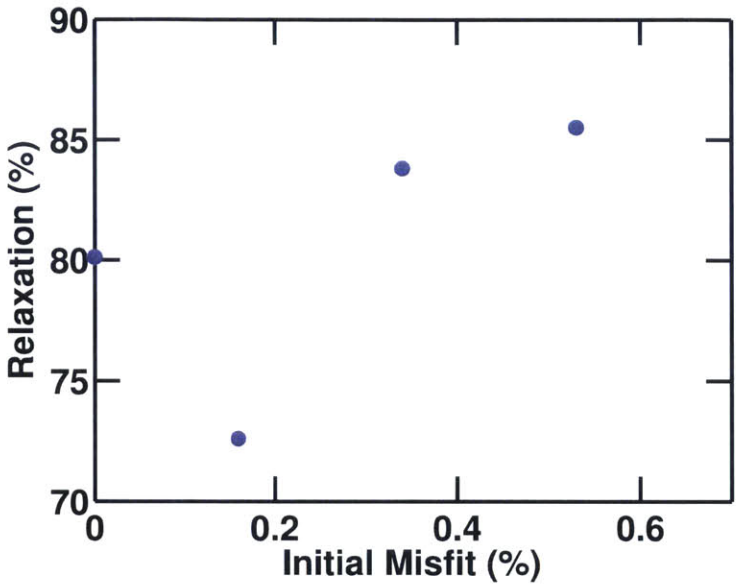


Figure 18: The average relaxation as a function of the initial misfit in the graded buffer. HRXRD measured the relaxation in two perpendicular ⟨100⟩ directions and the average relaxation was calculated with Equation 8. For the 0% initial misfit sample, the composition was step graded from the InP lattice constant without an abrupt strain layer.

3.3. Discussion

Fitting Equation 2 to the experimental data in Figure 13 allowed us to determine the activation energy of 1.3 eV for glide in the $InAs_xP_{1-x}$ material system. This value is slightly lower than the activation energies reported by Yonenaga for α and β dislocations in InP and InAs [73]. Since the values for v_o or the stress factors are not individually known, but are constant given a constant strain rate, only the product can be fit. This stress adjusted velocity factor should be of order $10^5 - 10^6$ cm/s as shown by Fitzgerald *et al.* [55] but was determined to be of order 10 cm/s. This reduction in glide velocity is a result of reduced effective stress caused by an impediment to dislocation motion [55]. The most probable cause of the reduced glide velocities are dislocations pile-ups (Figure 19) which would also explain the increased surface roughness (Figure 14) observed in these structures.

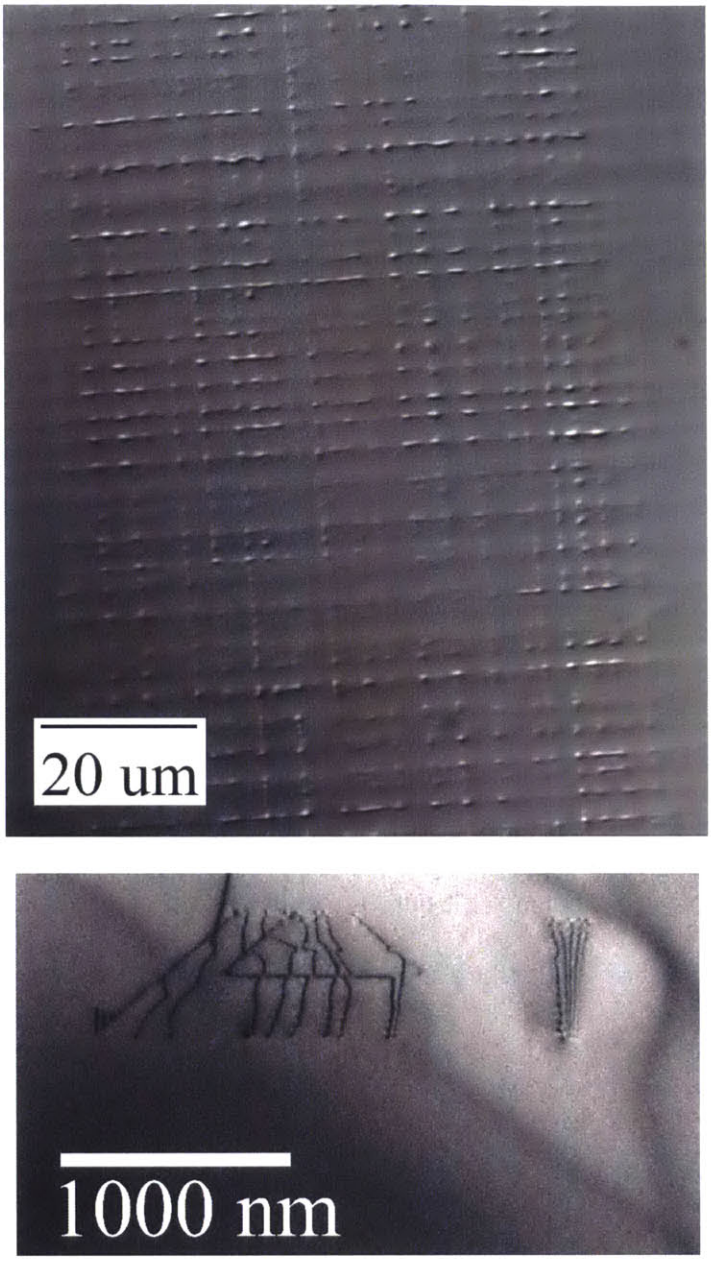


Figure 19: Nomarski (top) and PVTEM (bottom) micrographs of dislocation pile-ups. The ridged lines observed in the Nomarski micrograph are created by underlying bunches of dislocations pictured in the PVTEM micrograph. The strain fields surrounding the pile-ups cause local changes in the growth rate which creates the observed surface roughness.

Equation 1 can explain the results in Figure 11 and again suggests that dislocation glide is being restricted. A fit of the data is not reasonable, since the dependence of the effective stress on the strain gradient is unknown. Instead, a range of glide velocities can be plotted to bound the estimate of the dislocation glide velocity, v. The range of appropriate glide velocities is 0.1 – 0.8 μm/s. This range was less than the glide velocities for $GaAs_wSb_{1-w}$ reported by Yang *et al* [2], and InP or InAs reported by Yonenaga *et al* [74], [75]. These lower glide velocities indicate that the dislocation motion was being impeded, and was again prescribed to the presence of dislocation pile-ups. Since the formation of pile-ups depends on the dislocation nucleation process, we considered the nucleation process in greater detail.

From the HRXRD RSMs (Figure 10) of the linearly graded buffer, there appeared to be two stages of dislocation nucleation. Initially, the graded buffer developed tilt which indicated that the Burgers vectors were not equally distributed between the eight possible glissile orientations. The structure continued to tilt until the composition was between 15 and 20 %As. At this point tilt stopped developing which suggested a sudden nucleation event had occurred to balance the population of Burgers vectors among the possible orientations. Since the orientation of the existing Burgers vectors could not have been redistributed nor eliminated, the total number of dislocations in the structure must have increased by a large amount to make the original imbalance of orientations insignificant. A model for the dislocation nucleation process was created to explain the results of the HRXRD analysis and reduced dislocation glide velocities. In the model there are two types of sites, one with low activation energy and density (#/area) of nucleation sites and the second has a higher activation energy and density (Figure 20). Before continuing with a discussion of the results, a brief explanation of this hypothesis is provided.

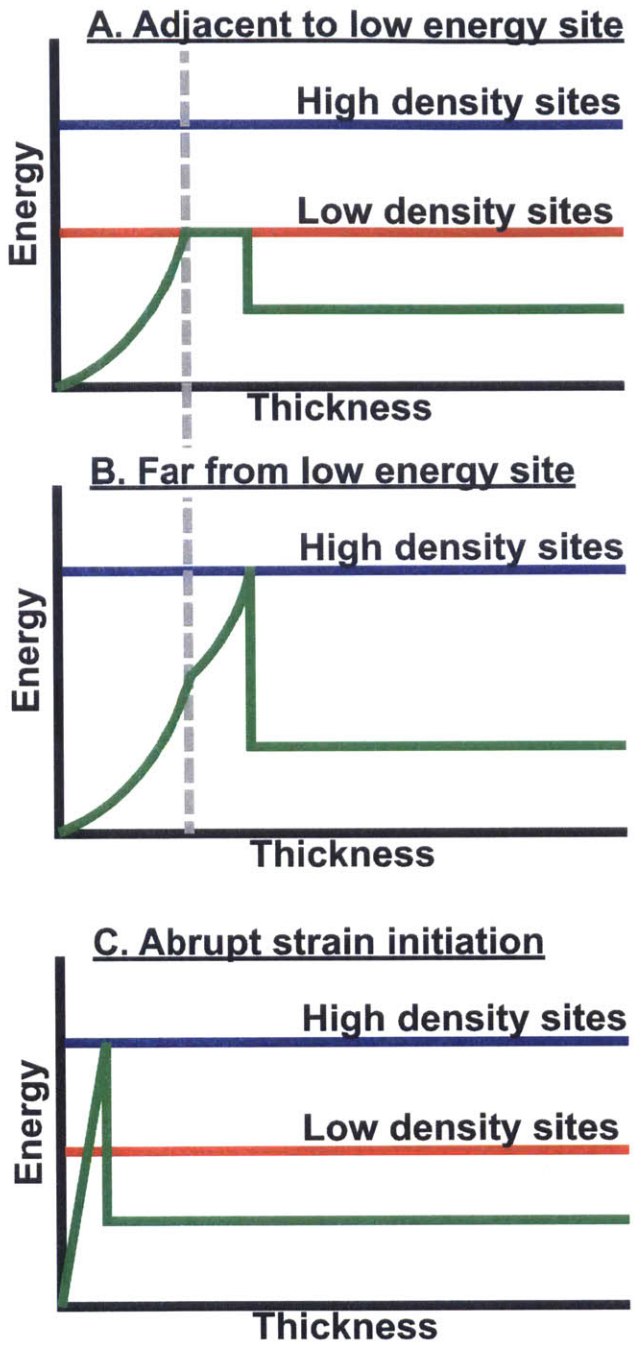


Figure 20: Schematic diagram showing the strain and activation energies as a function of thickness for three proposed situations during the growth and relaxation of $InAs_xP_{1-x}$ graded buffers. Red and blue lines indicate the relative activation energies of the two nucleation sites discussed in the text. The green curve represents the strain energy of the film during growth. Parts (a) and (b) occur simultaneously during growth when strain is gradually introduced in the graded buffer. Part (c) occurs only during abrupt strain initiation. The key feature of the abrupt initiation sequence is the activation of both low and high energy activation sites allowing for a more uniform dislocation population.

3.3.1. Model of dislocation nucleation and relaxation

Since a majority of the film area may lack the lower activation energy sites, the model can be explained as consisting of three phases of relaxation of $InAs_xP_{1-x}$ graded buffers: strain initiation, primary nucleation, and secondary nucleation. During the strain initiation phase (shown left of the grey, dashed line in Figure 20a-b) the strain energy in the film is below the activation energy for nucleation so the strain energy continues to increase as a function of both the thickness and increasing misfit. Once the strain energy reaches the lower activation energy (the red line in Figure 20) the primary nucleation phase begins but only at a few sites throughout the film area. Dislocations which are nucleated from regions similar to Figure 20a will then glide away from the low density nucleation sites towards the regions similar to Figure 20b, which cannot yet nucleate dislocations. These later regions continue to experience an increase in the strain energy but at a lower rate. This phase is pictured as just to the right of the grey, dashed line in Figure 20 and continues until the sharp drop of the strain energy. The final phase of secondary nucleation begins when the strain energy in regions with only high activation energy sites are able to begin nucleation. At this point the entire film can relax at the same rate and the steady-state implied by Equation 2 is established.

The consequences of this three phase nucleation process can explain the lower glide velocities, tilt, surface roughness, and RSMs observed in the linearly graded buffers. Since nucleation from the low energy sites is likely to be from particles or wafer edges, the dislocations are likely to have the same Burgers vector and be aligned along a few ⟨110⟩ directions [76]–[78] which could lead to tilt of the epi-layers, surface roughness, and lower glide velocities from dislocation pile-ups [21].

If nucleation from the sites with a higher density could be promoted over the low density sites, then it is possible that a more spatially uniform distribution of dislocations would be created (Figure 20c). This reduces the probability for dislocation interactions and ultimately reduces the threading dislocation density. The strategy to nucleate a more uniform population of dislocations, that we investigated here, has been employed previously by Vineis *et al.* but has not been discussed in the literature [79]. Erdtmann *et al.* have shown how an initially greater density of dislocations can allow for faster strain gradients and lower threading dislocation densities in the final film[80].

To promote nucleation from the higher activation energy sites, We increased the rate at which strain energy accumulates in the initial phase. In these experiments we grew a constant composition layer directly on the substrate. The goal was to rapidly raise the strain energy above the higher activation energy and site density level. While such a high strain energy would allow for nucleation from both the low and high density sites, it may still favor the high density sites. Since dislocations nucleated at the low density sites would be highly localized, they would require some amount of time to glide and relax the film. Therefore, regions far from the low energy sites would be able to nucleate dislocations from the high energy sites earlier. Since this would lower the strain energy in a majority of the film area, nucleation would only be active for a short time. Once dislocations are present in the film, any amount of additional strain can be relaxed by glide of the dislocations. The dislocations nucleated at the higher energy level are likely to be created at surface steps which means that they are unlikely to have the same Burgers vectors or glide planes [81]. This should substantially reduce the formation of dislocation pile-ups and epi-layer tilt. Ideally, the population of dislocations nucleated would be controlled to a number just sufficient to relax the film given a strain gradient and growth rate (Equation 2).

By initiating layers with increased misfit, the final threading dislocation density was reduced. Figure 15 shows that having an initial misfit of either 0.16 or 0.34 % decreased the dislocation density by about an order of magnitude compared to the other structures in the same set. Additionally, structures which had abrupt strain initiation had decreased surface roughness (Figure 16), decreased tilt (Figure 17), and increased relaxation of the cap layer (Figure 18) compared to the structure which had gradually initiated strain. These results suggest that there is no favored orientation of Burgers vectors and dislocations pile-ups are not created and therefore do not interrupt the glide of threading dislocations. Additionally, we conclude that nucleation of dislocations in the $InAs_xP_{1-x}$ abruptly initiated graded buffers follows a process similar to Figure 20c as opposed to the processes of Figure 20a-b.

The relaxation and dislocation nucleation processes in $InAs_xP_{1-x}$ compositionally graded buffers have been investigated. The results show that gradually initiated strain in the graded buffer layers leads to the development of tilt and eventually a large dislocation nucleation event. Reduced dislocation densities, tilt, and surface roughness as well increased relaxation can be achieved by initiating the graded buffer layer with a strained layer as high as 0.34 %. The initial strain in this layer promotes the nucleation of dislocations throughout the epi-layer and prevents the formation of dislocation pile-ups. Additionally, favorable results were obtained at higher growth temperatures. These results show that the $InAs_xP_{1-x}$ material system provides a low defect density platform for the development of minority carrier devices.

4. Thermal cycle annealing of germanium films on offcut silicon substrates

A combination of a few growth methods are used to form a planar, smooth, and low defect density germanium film on silicon substrates. The growth of germanium is initiated at low temperature in order to maintain a planar surface [26], [27]. This planar layer can have TDD values as high as 10^{11} #/cm^{-2}, but subsequent processing steps can reduce the TDD to 10^{7} #/cm^{2} [27]. After initiating at low temperatures, the temperature is raised. The growth of germanium at higher temperatures allows for faster growths rates [62] and increases the dislocation glide velocity [82] which allows for more relaxation and TDD reduction in the germanium layer. Temperature cycling promotes dislocation glide and increases the probability for dislocation-dislocation reactions which can result in annihilation or coalescence of dislocations. Eventually, the rate of reactions diminishes due to the decreased density of threading dislocations and further reduction of the TDD is limited for continued annealing. One of the goals of this thesis was to determine the most efficient annealing sequence to reduce the TDD to a level which would be suitable for development of majority carrier devices.

4.1. Experimental Procedure

We tested the effects of the number of thermal cycles, the period of annealing time at the high temperature, and the temperature ramp rate on the TDD and surface roughness of the germanium films. We sought to determine which of these parameters was most efficient at reducing the TDD and if there was no effect, then our goal was to determine the minimum annealing time which allowed for TDD < 10^{8} #/cm^{2} and surface roughness less than 10 nm RMS. Both of these metrics have been shown to be suitable for high performance of majority carrier devices [51], [83].

Silicon substrates, p-type (001) with a 6° offcut towards the nearest <111>, were purchased from Okmetic. Silicon substrates were always used as a full 150 mm wafer. The wafers were cleaned for 10 minutes in a freshly mixed piranha solution and thoroughly rinsed in de-ionized (DI) water. Immediately following the DI water rinse the Si wafer was dipped in a diluted hydrofluoric acid solution for 1 minute, resulting in a hydrogen terminated surface. The wafer was then immediately loaded into the MOCVD reactor. The precursor for germanium growth was germane (GeH_4) and the ambient was H_2. The previously reported methods for the growth of germanium on silicon substrates by MOCVD were followed and are summarized here [23], [69]. The growth of germanium on silicon was initiated at 400 °C with a 40 sccm GeH_4 flow. The temperature was raised to 600 °C while maintaining a small flow of 10 sccm GeH_4 during the temperature change. The remainder of the growth was performed at 600 °C with a flow of 190 sccm GeH_4. The total thickness of the germanium layer was 1 μm. The structure was then cyclically annealed in H_2 between 650 °C and 825 °C. The rate of temperature increase and the annealing time at 825 °C were experimental parameters. In order to decrease the temperature, the heating element was abruptly changed to 650 °C and the rate of temperature decrease was determined by the thermal mass of the reactor. The system was allowed 480 s to come to a steady state. A schematic plot of the thermal cycle annealing temperature profile is shown in Figure 21. In our experiments we varied the number of cycles (2, 3, or 8), the rate of temperature increase (0.97 or 1.94 °C/s), and annealing time (0, 120, 480, or 600 s) at 825 °C as shown in Table 2.

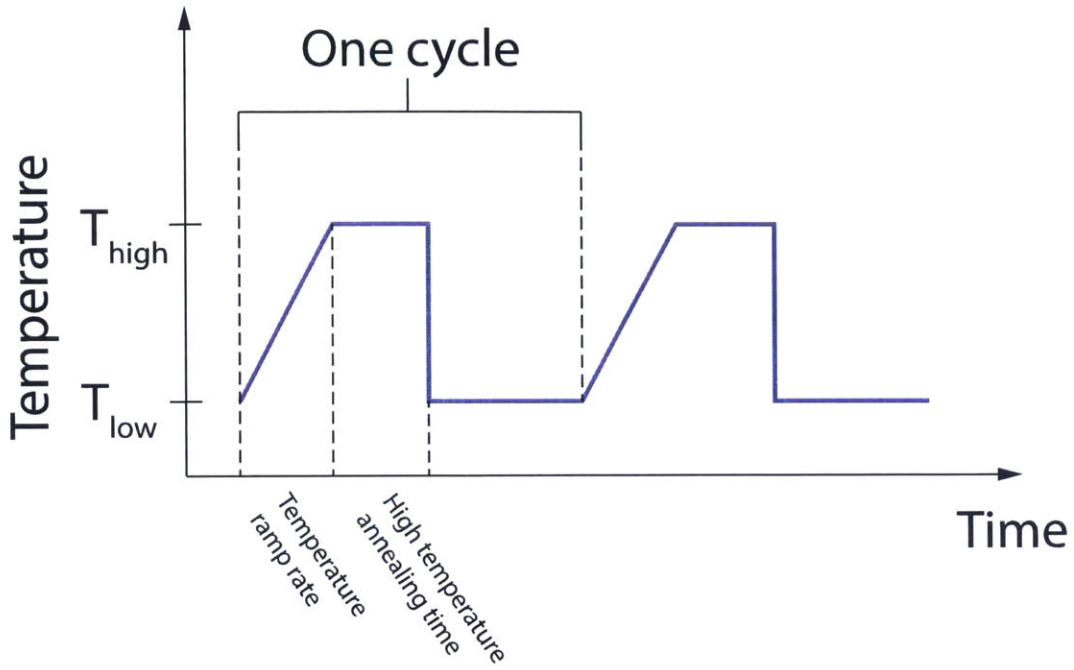


Figure 21: Schematic plot of the temperature profile in the thermal cycle annealing process. The temperature profile shown is the set-point temperature and the actual temperature will be dictated by the laws of heat diffusion. The temperature ramp rate refers to the rate of temperature change between the low and high temperature and has the units °C/s. The high temperature annealing time refers to the period of time the set-point is held constant at the high temperature.

Table 2: Experimental parameters and results of annealed germanium films

Sample Label	Cycles	Annealing Time at 825 °C (s)	Temp. Ramp Rate (°C/s)	Total Annealing Time (s)	EPD (10^7 #/cm^2)	RMS Roughness (nm) 5×5 µm	25×25 µm
A	8	480	1.94	6720	1.17 ± 0.14	1.1, 3.6	6.6, 7.8
B	8	480	1.94	6720	0.75 ± 0.04	1.2, 1.7	7.3, 6.9
C	8	600	0.97	10080	1.07 ± 0.23	1.5, 2.2	8.4, 5.7
D	8	120	0.97	6240	1.03 ± 0.12	2.6, 3.7	8.0, 7.9
E	2	120	0.97	1560	1.96 ± 0.14	1.4, 6.6	7.4, 10.7
F	8	120	1.94	5520	1.55 ± 0.34	1.5, 2.8	6.1, 4.5
G	8	0	0.97	1620	2.67 ± 0.27	1.8, 0.9	3.8, 4.8
H	3	120	0.97	2340	2.12 ± 0.19	3.1, 5.5	5.0, 5.1
I	3	120	1.94	2070	2.68 ± 0.20	5.5, 11.4	6.6, 9.2
J	0	0	0	0	52.5 ± 5.65	3.8, 4.6	7.8, 8.1

4.2. Results

Figure 22 shows an XTEM image of a germanium layer on a silicon substrate after thermal cycle annealing. The defects observed at the Ge/Si interface are predominately misfit dislocations. A few defects away from the interface were observed and were mostly confined to the low temperature initiation layer. The thickness of the germanium film is nominally 1 μm. Figure 23 shows Nomarski and AFM images of the TCA germanium surface. Shallow depressions are observed across the wafers surface. HRXRD measurements found that all of the films were 104 % relaxed, which is the relaxation expected for the growth of germanium on silicon at a temperature of 400 °C [71]. The morphology of the germanium films shown in Figure 22 and Figure 23 was representative of the structures reported in Table 2.

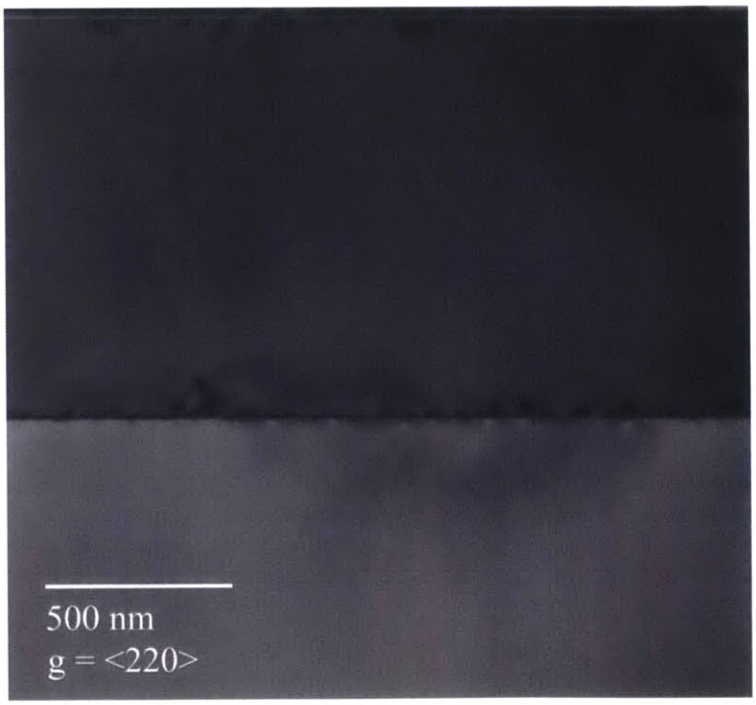


Figure 22: XTEM image of a germanium layer on a silicon substrate. The image was taken in a two-beam condition with a diffraction vector of <220>. Defects were observed at the Ge/Si interface, but few of these defects were found away from the interface.

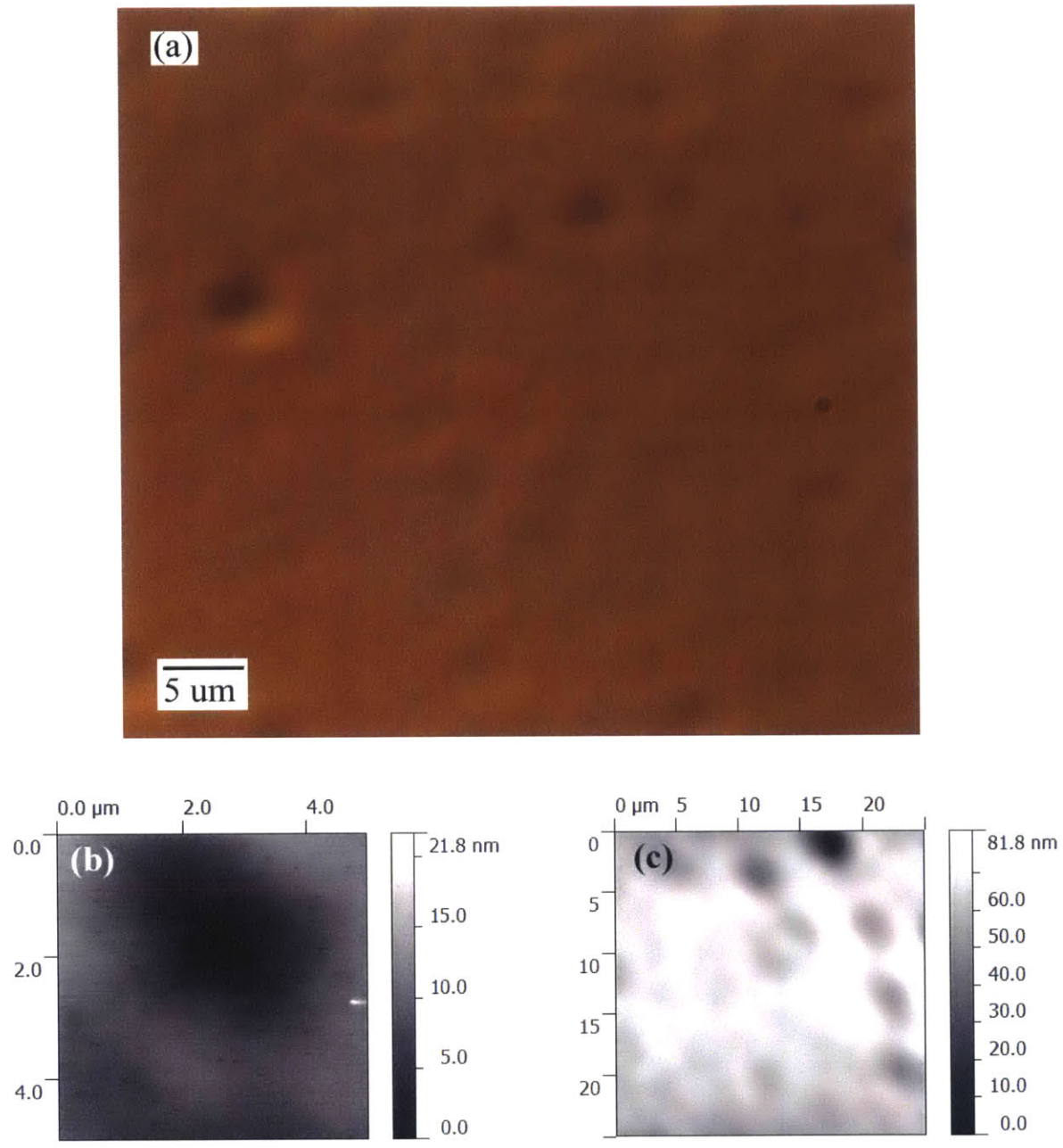


Figure 23: (a) Nomarski image of the TCA germanium surface. (b) 5x5 µm and (c) 25x25 µm AFM images of the TCA germanium surface. Shallow depressions are observed on the surface.

Figure 24 shows the etch pit density (EPD) measurements for each of the annealing treatments shown in Table 2. The pits were etched by exposure to a solution of 300 mg iodine dissolved in 50 mL hydrofluoric acid, 100 mL nitric acid, and 110 mL acetic acid for 2 seconds. The correlation between the EPD and TDD values has been shown to be unity [22] which indicates that each etch pit is produced by a single threading dislocation. The density was calculated by counting the total number of pits in an area of 1.4×10^4 μm^2. In Figure 24a, the EPD decreased by a factor of 10 when the number of annealing cycles was increased from zero to two, but relatively small decreases in the EPD values were observed for additional annealing cycles.

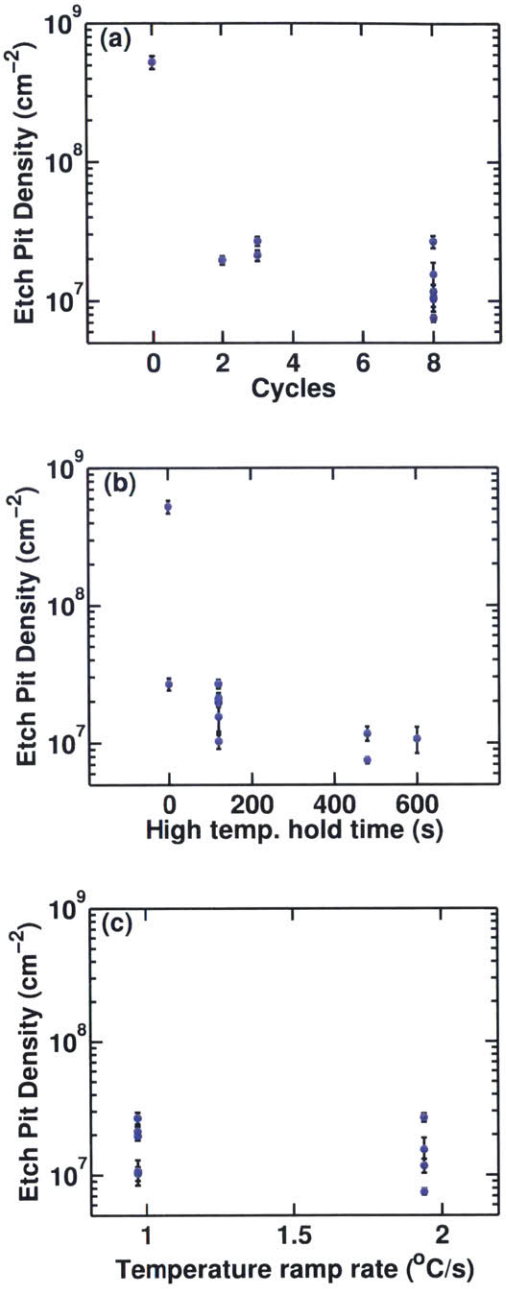


Figure 24: Etch pit density measurements of all of the annealing treatments shown in Table 2. Error bars are the 95% confidence intervals. The measurements are plotted as a function of (a) number of cycles, (b) period of annealing time at 825 °C, and (c) the rate of temperature increase from 650 °C to 825 °C. The germanium film which had no annealing treatment is plotted in (a) and (b) at zero cycles and hold time. The same film is not represented in (c) because no meaningful assignment of the rate of temperature change could be assigned.

The RMS roughness for each of the annealing treatments was measured by AFM (Figure 25). Each film was measured in two randomly selected regions with scan ranges of 5×5 μm and 25×25 μm. AFM images of the germanium surface of sample D is shown in Figure 23. Shallow depressions across the surface of the films were observed. These depressions were observed in all films and their density and depth was independent of the annealing treatment. In the plots of Figure 25, four data points are shown for each germanium film, one point for each region and scan size was plotted.

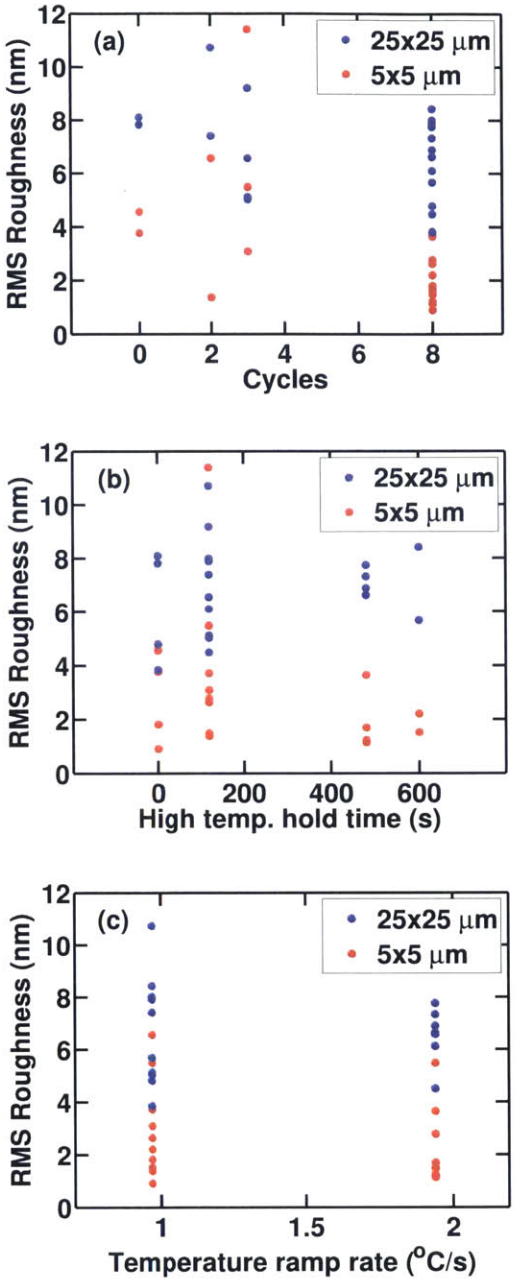


Figure 25: RMS surface roughness measurements by AFM of all of the annealing treatments shown in Table 2. Two randomly selected locations on the wafers were selected for each scan size (scan size indicated by legend). All of the measurements are reported individually. The measurements are plotted as a function of (a) number of cycles, (b) period of annealing time at 825 °C, and (c) the rate of temperature increase from 650 °C to 825 °C.

In order to determine what annealing parameters were the most significant in creating changes in the EPD or surface roughness measurements, a three-way ANOVA test was run on the data reported in Figure 24 and Figure 25. The p-values for the tests are reported in Table 3. Typically, a p-value less than 0.05 is required in order to reject the null hypothesis (i.e. the varied parameter had no effect). Using this metric, none of the parameters in the tested ranges were found to have a significant effect (quantified by changes from the mean) on the EPD or surface roughness.

Table 3: p-values for a three-way ANOVA test of the EPD and roughness measurements

EPD	p-value
Number of cycles	0.062
High temp. annealing time	0.054
Ramp Rate	0.124
RMS Roughness	
Number of cycles	0.2781
High temp. annealing time	0.4457
Ramp rate	0.4477

Figure 26 shows the EPD and surface roughness measurements plotted against the total annealing time. While the number of cycles, high-temperature annealing time, and temperature ramp rate are all independent parameters, the total annealing time is not independent of the others and therefore cannot be included in the analysis presented in Table 3. Figure 26a shows a decrease in the EPD value when the annealing time increases from zero seconds, but for longer total annealing times but the absolute change is small compared to the range of EPD values for the growth of germanium on silicon ($10^6 - 10^9$ #/cm^2). No change in the surface roughness is observed for changes in the total annealing time (Figure 26b). The null effect on surface roughness agrees with the results of Yamamoto *et al.* [84] who found no difference between un-annealed and annealed germanium films on silicon.

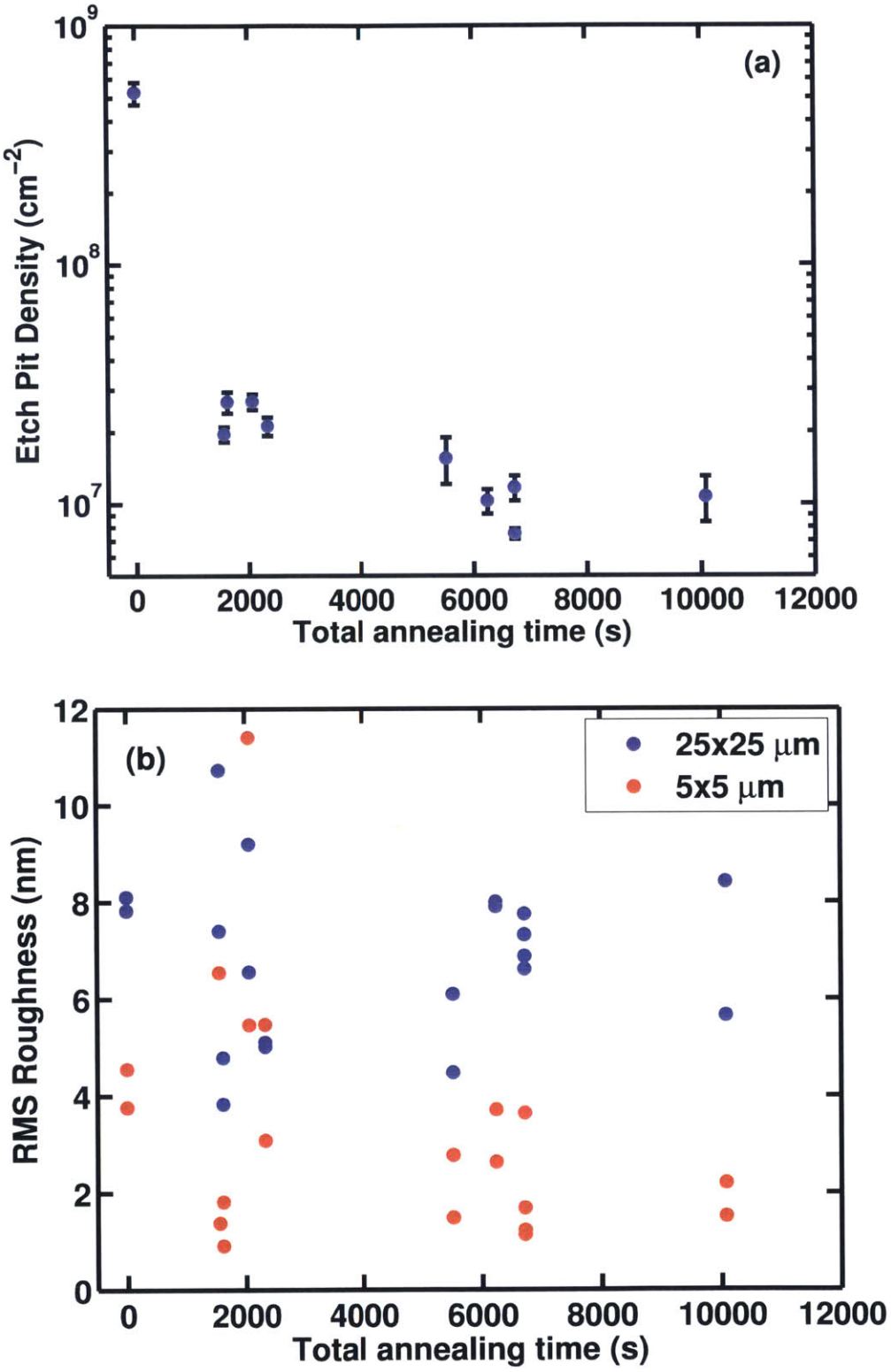


Figure 26: (a) EPD and (b) RMS surface roughness for all annealing treatments plotted as a function of the total annealing time. The data represented in the plots is the same as the data shown in Figure 24 and Figure 25.

4.3. Discussion

The results of the ANOVA test indicate that we cannot conclude that any of the experimental parameters have an effect on the EPD or RMS surface roughness of the thermal cycle annealed Ge/Si samples. However, if we were to use a more relaxed condition for statistical significance (e.g. $p < 0.1$), then we could conclude that increases in either the number of cycles or the high-temperature annealing time could reduce the EPD. Yamaguchi *et al.* have demonstrated the benefit of increased number of thermal cycles [66] but have shown diminishing reductions in the TDD values as the number of cycles is increased. The diminishing rate is a result of the reduced TDD which results in fewer opportunities for dislocation-dislocation interactions. We found that a majority of the EPD reduction occurs for the first one to two cycles (compare sample J to sample E in Table 2) and subsequent annealing cycles reduced the EPD by a relatively small fraction (considering the logarithmic nature of EPD values). For majority carrier devices it is only necessary to use one or two annealing cycles to reduce the EPD to a suitable level.

From Figure 24, the length of annealing period at high temperatures should also be considered as a potentially significant factor in reducing the EPD values. Although a decrease in the EPD was observed for longer high-temperature annealing periods (Figure 24b), it is unlikely that very long annealing times are justified. Since the dislocation glide velocity is determined by the stress in the film created by the thermal strain, the glide velocity will diminish as the films are annealed at the high-temperature. Additionally, the samples which had long annealing periods also experienced the most number of cycles (Table 2, samples A-C) and it is therefore not possible to attribute the EPD reduction to one of these parameters. This aspect of the data reinforces the need for the statistical approach used here. A more detailed study may be able to determine if either of the parameters was significant.

Since none of the experimental parameters had a significant effect on the EPD or RMS roughness, the relationship between these quantities and the total annealing time were investigated (Figure 26). A trend between increasing total annealing time and decreasing EPD was observed. As before, the longest annealing times were for samples which experienced the highest number of cycles and had the longest high-temperature annealing periods. So while it is not possible to determine how the total annealing time affects the EPD, it is still possible to conclude that even brief annealing treatments are capable of reducing the defect density to a level that is suitable for majority carrier devices.

We have shown that the EPD and surface roughness of thermal cycle annealed germanium on silicon substrates were nearly independent of the number of thermal cycles, the annealing time at high temperature, and the rate of temperature increase from 650 °C to 825 °C. We found that only the number of annealing cycles or the high-temperature annealing time could potentially cause significant reductions in the EPD values. However, the reduction in the EPD values is likely to be negligible compared to the absolute EPD values. We conclude that a high number of annealing cycles or long high-temperature annealing times are unnecessary for achieving TDD values low enough for majority carrier devices. Instead we propose that 1 μm thick germanium films experiencing two thermal cycles between 650 °C and 825 °C with annealing times of 120 seconds at 825 °C is sufficient for the development of majority carrier devices on Ge/Si virtual substrates. This abbreviated method is able to achieve the same film morphologies while reducing the processing times by a factor of 6.5. The Ge/Si virtual substrates produced by this method have been shown to be a suitable platform for majority carrier devices.

5. Development of InAlAs compositionally graded buffers Ge/Si virtual substrates

Attempts to integrate $In_yGa_{1-y}As$ HEMTs (or more generally - quantum well devices) on Ge or Si substrates have been reported [35]–[40]. For the integration with Si substrates, a method of accommodating the lattice mismatch between Ge or GaAs must be employed to prevent the formation of a high density of threading dislocations in the virtual substrates. One method which has been proposed is the growth of Ge directly on Si using a low temperature initiation followed by high temperature growth and thermal cycling annealing [23], [69]. This allows for much thinner layers to be deposited in order to reach the germanium lattice constant but has a greater defect density (1 μm epitaxy for 10^7 #/cm^2) than traditional Si_wGe_{1-w} graded buffers (10 μm epitaxy for 10^6 #/cm^2). However, the lower defect density of the Si_wGe_{1-w} graded buffers does not provide any advantage in the performance of majority carrier devices, such as $In_yGa_{1-y}As$ QW devices. Currently, the method of direct growth of germanium on silicon is being developed in order to incorporate Si CMOS devices with a variety of III-V devices [85]. The goal of this integration process is not only to create $In_yGa_{1-y}As$ QW devices on silicon substrates, but also to develop a platform which is compatible with traditional CMOS platforms. Figure 27 shows the fully integrated layer structure. This thesis develops a method for the MOCVD growth of the III-V devices layers on a Ge/Si virtual substrate.

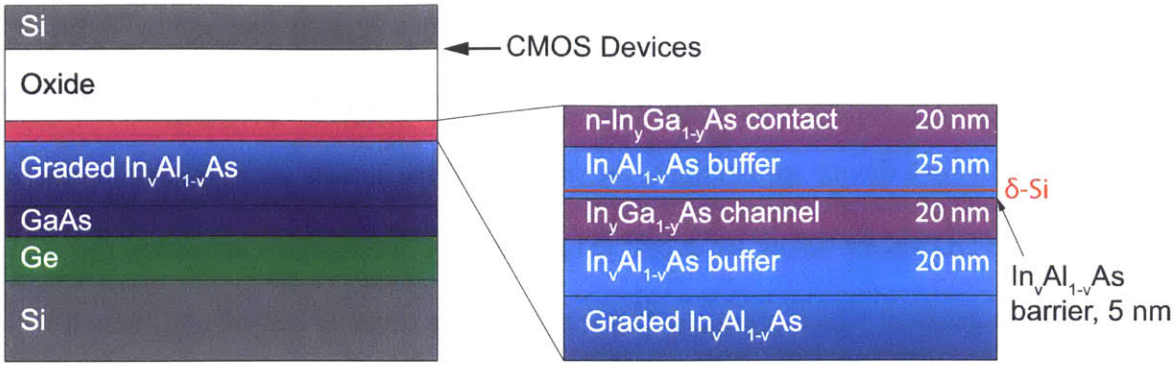


Figure 27: Schematic of the integration structure for CMOS and III-V devices. The top most silicon layer contains the CMOS devices which were processed on an SOI wafer prior to the layer transfer. This thesis developed a method for the fabrication of the layers shown below the oxide.

5.1. Experimental Procedure

The Ge/Si virtual substrate presents some design challenges in the $In_vAl_{1-v}As$ compositionally graded layer which need to be satisfied for the development of $In_yGa_{1-y}As$ QW devices on Si substrates. There is a large difference in the coefficient of thermal expansion between group IV and III-V materials [71]. To prevent the accumulation of large stresses upon cooling from growth temperatures to room temperature, when relaxation by glide is kinetically suppressed, the total thickness of the epitaxial layers should be minimized [71]. From previous studies, it is estimated that the total thickness of the epi-layers should be less than 5 μm in order to avoid crack formation upon cooling from the growth temperature [86].

Typically, thick compositionally graded buffers are used to reduce the strain gradients and therefore the threading dislocation densities (TDD), but such a strategy may not be viable or strictly necessary. The lowest TDD achievable in Ge/Si virtual substrates is on the order of 10^7 cm^{-2}. For the intended device applications, the mobility of the $In_yGa_{1-y}As$ QW will not be diminished for TDD values below 10^8 #/cm^2 [51]. It is only necessary to determine the minimum strain gradient which produces TDDs of the same order of magnitude, since it will not be possible to reduce the defect density below the level in the Ge/Si virtual substrate. The goal of our study was to determine the strain gradient of $In_vAl_{1-v}As$ compositionally graded buffers which would produce suitable morphologies for $In_yGa_{1-y}As$ QW devices on Ge/Si virtual substrates. Once a suitable $In_vAl_{1-v}As$ buffer was developed, we grew an $In_{0.3}Ga_{0.7}As$ QW device on graded $In_vAl_{1-v}As$/Ge/Si.

We grew $In_vAl_{1-v}As$ compositionally graded buffers on GaAs substrates offcut 6° towards the nearest <111>A direction or Ge/Si virtual substrates with an offcut towards a <111> direction. The offcut orientation of the GaAs was used for consistency between the two substrate materials since the Ge/Si substrates had to be offcut in order to prevent the formation of anti-phase domains [70]. The growth of the Ge/Si virtual substrates followed the method described in Chapter 4. The epi-ready GaAs substrates were purchased from AXT Inc. and did not require any cleaning or treatment prior to epitaxial growth. Growth on GaAs substrates used either a full 50 mm wafer or half of a 50 mm wafer. Growth on the Ge/Si virtual substrates always used a full 150mm wafer.

It was found that the initiation of GaAs on Ge surfaces required a high AsH_3 partial pressure. To achieve high AsH_3 partial pressures, the reactor pressure was increased from 100 Torr (the normal pressure used for growth) to 250 Torr and we estimate that the AsH_3 was increased from 1 mTorr to 2.5 mTorr. The MOCVD reactor could not achieve the high partial pressure by increasing the AsH_3 flow only. Regardless of the substrate, the same initiation procedure was used. The initiation process started with a 300 second anneal at 650 °C with an AsH_3 partial pressure of 1 mTorr. The reactor pressure was increased to 250 Torr and the AsH_3 partial pressure increased to 2.5 mTorr. A small flow of 10 sccm TMGa was introduced to the reactor which allowed for the GaAs to be initiated with a high V/III ratio. The initial layer was 100 nm thick. The flow of TMGa was stopped and the reactor pressure was reduced to 100 Torr which decreased the AsH_3 partial pressure to 1 mTorr. A higher flow of 50 sccm TMGa was introduced to the reactor and an additional 100 nm of GaAs was deposited. The flow of TMGa was stopped again and the temperature was increased to 725 °C while maintaining the AsH_3 flow. The growth temperature of 725 °C for the graded $In_vAl_{1-v}As$ layers was chosen to suppress phase separation of the $In_vAl_{1-v}As$ and to allow for greater glide velocities of the threading dislocations in the buffer. Another 100 nm layer of GaAs was deposited followed by a 200 – 500 nm thick AlAs layer. The composition of the epitaxial layer was then linearly graded between AlAs and the target $In_vAl_{1-v}As$ composition. At the final composition, a 1 μm constant composition cap layer was grown. Cooling from the growth temperature to 350 °C was done under an over pressure of AsH_3.

The growth of the $In_yGa_{1-y}As$ QW devices layers was done at either 725 °C or 650 °C. If the layers were grown at 650 °C the temperature was reduced from 725 °C while maintaining an AsH_3 overpressure. The QW layers consisted of a 20 nm $In_{0.3}Al_{0.7}As$ buffer, a 20 nm $In_{0.31}Ga_{0.69}As$ QW channel, a 5 nm $In_{0.3}Al_{0.7}As$ barrier, a disilane delta doping layer, a 25 nm $In_{0.3}Al_{0.7}As$ buffer, and finally a 20 nm n-$In_{0.31}Ga_{0.69}As$ contact layer as shown in Figure 27. The delta doping layer was deposited by stopping the group III flow and annealing the surface with AsH_3 for 10 seconds. The silicon dopants were deposited using a diluted disilane precursor flow under an AsH_3 overpressure and with no group III flow. There was a 10 second AsH_3 anneal after depositing the doping layer and before continuing with the growth of the $In_vAl_{1-v}As$ barrier and $In_yGa_{1-y}As$ contact layer.

5.2. Results

XRD measurements of the three films grown on GaAs (not shown) determined the final composition of the $In_vAl_{1-v}As$ cap layer was between 36 and 41 %In and the relaxation of the cap layer was greater than 88 % for all of the structures. Figure 28 shows the symmetric and asymmetric reciprocal space maps of a representative $In_vAl_{1-v}As$ compositionally graded buffer on a Ge/Si virtual substrate. Between the Si substrate peak and the Ge film peak, no diffracted intensity is observed. Between the GaAs and $In_vAl_{1-v}As$ film peaks, the characteristic shape of a compositionally graded buffer is observed in the diffracted peak intensity. The symmetric scan shows that the $In_vAl_{1-v}As$ compositionally graded buffers experience epitaxial tilt during the growth process. This tilt is oriented opposite to the offcut of the substrate. This effect of epitaxial tilt to compensate for the substrate offcut is commonly observed in lattice mismatched films grown on offcut substrates. The relaxation of the $In_vAl_{1-v}As$ cap layers grown on Ge/Si virtual was 98 % or greater for all films.

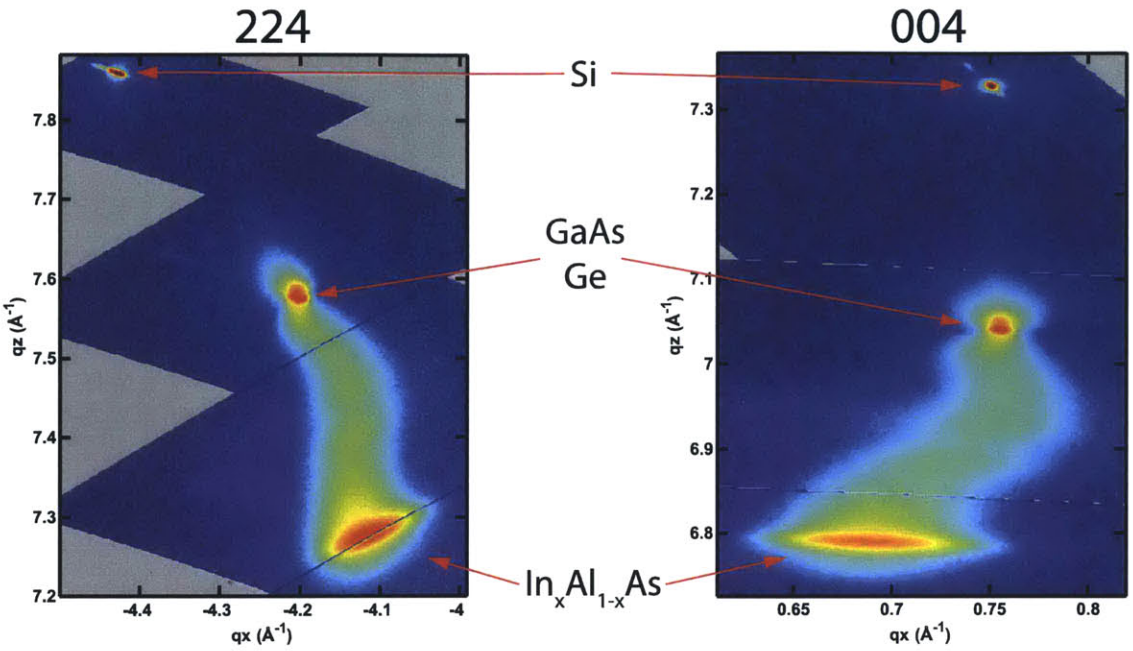


Figure 28: HRXRD reciprocal space maps of an $In_vAl_{1-v}As$ compositionally graded buffer on a Ge/Si virtual substrate. The reciprocal lattice points are labelled above each image. The 224 scan is shown to the left of the 004 scan to preserve the orientation of the q_x axis. The area of reciprocal space at each RLP was too large to be captured in a single scan. Therefore, multiple successive scans were stitched together with the *PeakSelector.mat* script (Appendix 7.2.) which creates the line artifacts observed in the images. The peaks are marked with the layer which produced the diffracted intensity. The GaAs and Ge peak nearly overlap since they have very similar lattice constants, however the Ge peak can be observed at slightly lower values of q_z due the slightly larger lattice constant of that layer. Epitaxial tilt of the $In_vAl_{1-v}As$ peak was observed as a shift in the q_x position of the film peak away from the q_x position of the substrate in the (004) scan.

XTEM (Figure 29a-b) images revealed high quality metamorphic growth with relaxation confined to the compositional graded layers. Figure 29c-d show higher magnification images of the $In_yGa_{1-y}As$ QW layers for the structure grown entirely at 725 °C and the structure which had a temperature change from 650 °C to 725 °C.

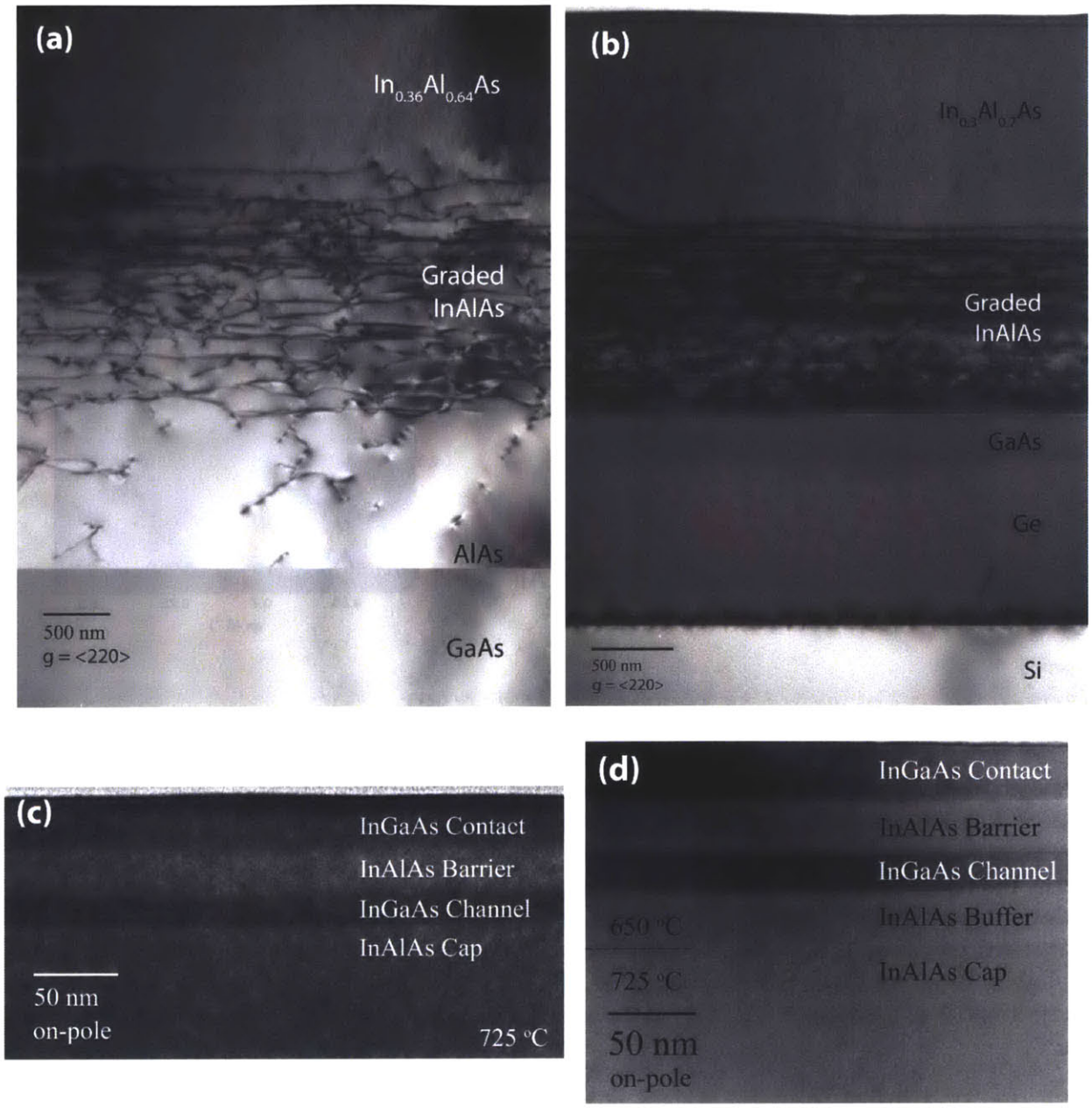


Figure 29: XTEM images of the InAlAs compositionally graded buffer on GaAs with final composition of $In_{0.4}Al_{0.6}As$ (a) and the same graded buffer reproduced on the Ge/Si virtual substrates with final composition of $In_{0.3}Al_{0.7}As$ (b). An InGaAs QW device was grown on top of the structure grown on the Ge/Si virtual substrate. Two higher magnification images of the QW layers grown at 725 °C (c) or 650 °C (d). The dashed line in (d) indicates the location in the growth structure where the temperature was changed.

Figure 30 shows the TDD as a function of the strain gradient in the $In_vAl_{1-v}As$ buffer. Generally as the strain gradient increases the TDD also increase since more dislocations are needed to accommodate the faster strain rate. However, for large strain gradients there will be a critical strain for which the strain energy is sufficient to nucleate a high density of dislocations. Relaxation of the graded layer will then proceed by nucleation instead of glide. A strain gradient as high as 2.1 %ε/μm allowed for TDD values as low 10^7 cm^{-2} which was suitable for use on Ge/Si without increasing the final defect density. Strain gradients of 3.7 %ε/μm were found to have greater TDD consistent with relaxation by nucleation. This implies that the critical transition between relaxation by glide to relaxation by nucleation occurs between strain gradients of 2.1 %ε/μm and 3.7 %ε/μm for $In_vAl_{1-v}As$ compositionally graded buffers. The thickness of the graded layer in the structures with the lowest two TDD and strain gradient values are 1.76 μm and 1.31 μm respectively and were thin enough to allow for the growth of $In_yGa_{1-y}As$ QW devices on Si without the formation of cracks.

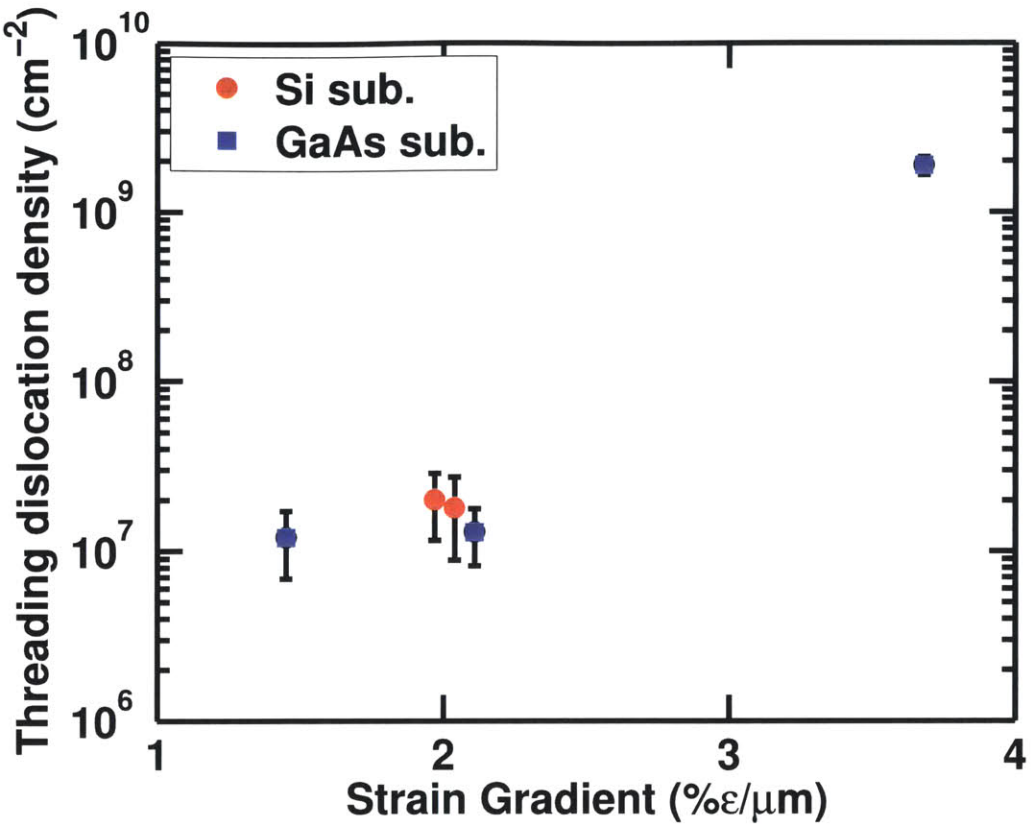


Figure 30: The TDD as measured in PVTEM as a function of the strain gradient. For the lowest two strain gradients on GaAs substrates, the TDD is nearly equivalent. When the $In_vAl_{1-v}As$ graded layers are reproduced on Ge/Si virtual substrates the TDD increases only slightly. The error bars indicate the 95% confidence interval. The error bars for the structure with the highest TDD fall within the marker.

The strain gradient in the graded buffer layers also has an effect on the surface roughness through the formation of a "cross-hatch" morphology. Greater strain gradients generally led to increased surface roughness due to the reduced distance between the surface and misfit dislocation array in the graded layer [9]. Figure 31 shows the resulting surface roughness for the three graded buffers grown on GaAs substrates as well as for the graded buffer and $In_yGa_{1-y}As$ QW structures grown on Si substrates. We found that the surface roughness was less than 10 nm RMS for strain gradients up to 2.1 %ε/μm grown on GaAs substrates. The surface roughness increased for the same graded buffers grown on silicon substrates, up to 20.2 nm RMS for the structure with $In_yGa_{1-y}As$ QWs grown at 725 °C. If the surface roughness becomes too large, the mobility in the $In_yGa_{1-y}As$ QW could be diminished due to increased scattering. For the $In_vAl_{1-v}As$ graded buffer and $In_yGa_{1-y}As$ QW devices grown on Ge/Si virtual substrates, strain gradients of approximately 2.0 %ε/μm or less were targeted to maintain a sufficiently smooth surfaces.

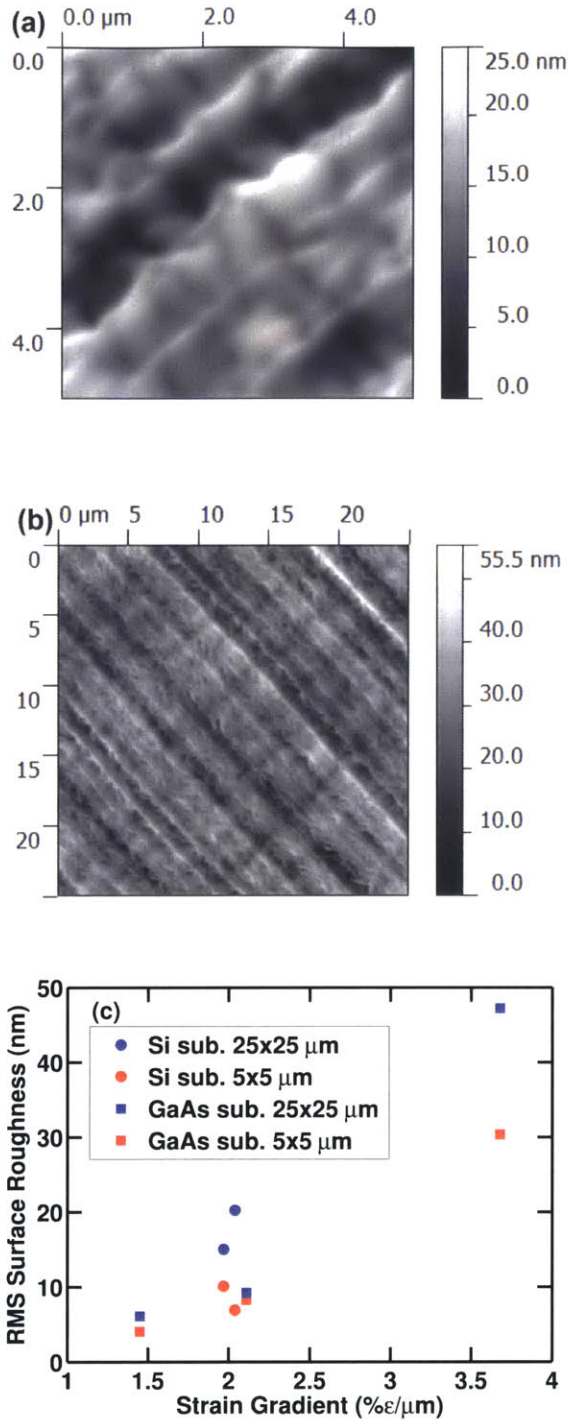


Figure 31: (a-b) AFM height images of graded buffers grown on GaAs substrates with final composition of $In_{0.4}Al_{0.6}As$. Two scan ranges of 5x5 µm and 25x25 µm are shown respectively. The structure shown here corresponds to the lowest strain gradient used in this study (1.44 %ε/µm). (c) The RMS roughness of the $In_vAl_{1-v}As$ graded buffers on GaAs and Si substrates as a function of the strain gradient in the graded layer. The substrate material and size of the scan ranges used for each measurement are indicated in the legend.

5.3. Discussion

Initial attempts to grow $In_{0.52}Ga_{0.48}As$ QW layers on silicon substrates were prevented by severe phase separation in the $In_vAl_{1-v}As$ grade buffer. We found that phase separation in graded $In_vAl_{1-v}As$ layers on Ge/Si virtual substrates would prevent the glide of dislocations if the indium composition was increased beyond $In_{0.3}Al_{0.7}As$. Figure 32 shows the XTEM image from one of these attempts. The dashed line (which corresponds to a layer with composition of approximately 25 %In to 30 %In) indicates the boundary between relaxation by dislocation glide and relaxation by dislocation nucleation. Below the line, misfit dislocations were observed which indicated relaxation by glide but above the line there were no misfit dislocations observed. The defects above the line were primarily threading dislocations and were most likely created by many nucleation events.

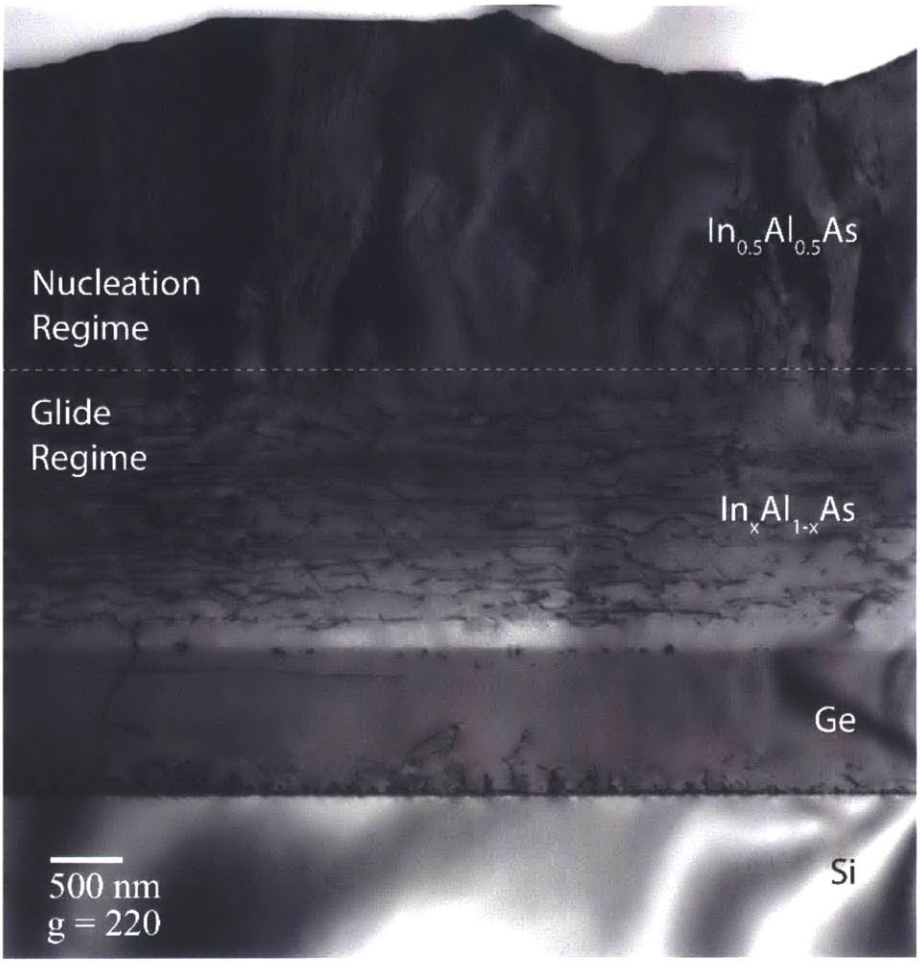


Figure 32: XTEM image of an $In_vAl_{1-v}As$ graded buffer on Ge/Si virtual substrate. The strain gradient was 2 %ε/μm and the final composition was $In_{0.5}Al_{0.5}As$. The dashed line indicates the boundary between relaxation by glide and relaxation by nucleation. Correlation with XRD and *in-situ* reflectivity indicate that this boundary is between 25 %In and 30 %In. Below the dashed line misfits are observed which indicates that relaxation was progressing by glide of the threading dislocations. Above the dashed line, only threading dislocations are observed which is consistent with nucleation. The strong, vertically oriented bands of contrast were due to either phase separation or residual strain in the layer.

Since the phase separation was only observed for films grown on Ge/Si substrates, it is thought that the increased surface roughness of the virtual substrate may have assisted in the phase separation at the surface of the growing film as reported by Kurihara *et al.* [87]. A roughened surface would decrease the barrier to phase separation by allowing the more mobile indium atoms to incorporate into the lattice at the bottom of valleys during the deposition. This lead to indium rich regions near the bottom of the valleys and aluminum rich regions at the ridges. The phase separation and surface roughness would then prevent the glide of the threading dislocations [21] leading to further increases in the surface roughness [9] which created a positive feedback for increased phase separation and reduction in dislocation glide. Eventually the strain energy was sufficient to nucleate new dislocations to relax the film and leads to the breakdown of the epitaxial process observed in Figure 32.

We targeted compositions of $In_{0.31}Ga_{0.69}As/In_{0.3}Al_{0.7}As$ in order to avoid the issues of phase separation. We speculate that greater indium compositions could be achieved by growing at lower temperatures to reduce the surface mobility of indium adatoms, by using lower strain gradients in the $In_vAl_{1-v}As$ graded layer in order to reduce the roughness from the cross-hatch morphology, or by developing methods to reduce the surface roughness of the Ge/Si virtual substrate.

XTEM images of the graded buffer layers with a final composition of $In_{0.3}Al_{0.7}As$ (Figure 29a-b) found relaxation continued throughout the compositionally graded layer. The constant composition $In_vAl_{1-v}As$ cap layer above the graded layer shows slight contrast fluctuations in both images which are consistent with minor phase separation. Although phase separation is present in these lower %In structures, the effect does not appear to have caused significant increases in the surface roughness or to have impeded the dislocation glide in the graded layer. The higher magnification images of the $In_yGa_{1-y}As$ QW layers (Figure 29c-d) show that interface between the $In_yGa_{1-y}As$ channel and the $In_vAl_{1-v}As$ barrier appears to be more abrupt for growth at lower temperatures. While the abruptness of this interface is difficult to quantify, the images shown in Figure 29 were representative of all the regions we observed.

The surface roughness, TDD, electron mobility, and sheet carrier concentration were measured for the $In_yGa_{1-y}As$ QW devices. For structures grown entirely at 725 °C, the TDD was $1.81\pm0.92\times10^7$ #/cm^2 and the surface roughness was 20.2 nm RMS (25×25 μm). For structures with the QW layers grown at 650 °C the TDD was $2.02\pm0.86\times10^7$ #/cm^2 and the surface roughness was 15.0 nm RMS (25×25 μm). Van der Pauw - Hall measurements found the electron mobility and sheet concentration to be 3.28×10^{12} cm^{-2} and 2801 cm^2/Vs respectively for structures grown at 725 °C. The same measurements for the structures with the QW layers grown at 650 °C were 1.16×10^{12} cm^{-2} and 6398 cm^2/Vs respectively. To analyze these results we considered the effect of the growth temperature and compared the mobility of these QWs to similar devices on silicon substrates.

We attribute the increased mobility of the structure grown at 650 °C to the more abrupt interface between the top of the $In_yGa_{1-y}As$ channel and the bottom of the $In_vAl_{1-v}As$ barrier. A more abrupt interface reduces the scattering of the electrons in the two dimensional electron gas which developed adjacent to this interface. The delta doping procedure was not changed for the growth at the different temperatures and may need to be modified in order to achieve greater carrier concentrations. We speculate that the incorporation of the silicon atoms into the lattice was reduced at 650 °C and that a larger dose in the delta doping layer would allow for increased carrier concentration in the QW.

For $In_{0.3}Ga_{0.7}As$ QWs, the electron mobility has been reported to be as large as about 8000 cm^2/Vs for QWs grown on graded buffers on (001) GaAs substrates [7], [88]. So further improvement of the mobility is possible at this composition. It is possible that the greater surface roughness of the devices reported here could be decreasing the channel mobility, however, surface roughness as large as 10 nm RMS have previously been shown to have no effect on the channel mobility in $In_yGa_{1-y}As$ QW devices [83]. The highest mobility for any $In_{0.53}Ga_{0.47}As$ QW on silicon was a $In_{0.53}Ga_{0.47}As$ QWs grown on GeOI/Si substrates and had a mobility of 10850 cm^2/Vs [39]. The highest mobility previously reported for an $In_{0.53}Ga_{0.47}As$ QW using a continuous growth process starting on a silicon substrate was 6710 cm^2/Vs [89]. Both of these devices measured $In_yGa_{1-y}As$ channels with higher indium content than the devices investigated in this thesis. Therefore, the methods reported here for the growth of $In_{0.3}G_{0.7}As$ QWs starting with a silicon substrate compare favorably with QW of similar composition having only small reductions in the electron mobility. Additionally our methods may offer improvements for higher indium composition channels if the phase separation of the $In_vAl_{1-v}As$ buffer can be eliminated.

A method for the integration of $In_yGa_{1-y}As$ QW devices on silicon substrates has been demonstrated. This method used the direct growth of Ge onto Si substrates followed by the growth of compositionally graded $In_vAl_{1-v}As$ layers to the final $In_yGa_{1-y}As$ composition. The TDD in the final layers was sufficiently low that the electron mobility was not adversely affected. It was found that higher mobility could be achieved if the growth temperature of the QW layers was reduced to 650 °C. This method allows for the growth of $In_yGa_{1-y}As$ device structures on silicon substrates in a single process run and does not require any additional pre- or post-growth processing.

6. Conclusion

6.1. Summary of results

6.1.1. InAsP compositionally graded buffers

We studied the dislocation dynamics and nucleation mechanisms to describe the relaxation process of $InAs_xP_{1-x}$ compositionally graded buffers. We found that gradual introduction of strain allows for nucleation from a few low energy sites. The dislocations created at these sites are only able to relieve strain in a fraction of the film which leads to dislocation pile-ups, asymmetric relaxation, and increased surface roughness. A method of abrupt strain initiation which allowed for more spatially uniform nucleation was shown to reduce TDD, epitaxial tilt, and surface roughness.

By varying the strain gradient in the $InAs_xP_{1-x}$ compositionally graded layers with gradual strain initiation we found that dislocation glide was being impeded. Dislocation glide is strongly dependent on the temperature, so to determine if the glide was being kinetically suppressed due to a low growth temperature we grew a series of graded buffers at successively higher temperatures. Again we found dislocation glide was being impeded but the activation of glide was not being suppressed. The lower glide velocity led to a higher TDD in the $InAs_xP_{1-x}$ films so it was desired to find a way to increase the glide velocity by removing the impediment.

In both experimental sets (strain gradient and growth temperature) of films, dislocation piles-ups were observed. Pile-ups can lead to greater surface roughness, and both of these features can reduce the dislocation glide velocity in the graded buffer layers. Since the formation of pile-ups is a result of many nucleation events from an individual site, we created a study to investigate our two energy level model of dislocation nucleation mechanisms in the $InAs_xP_{1-x}$ compositionally graded layers.

A two energy level model was developed to explain how a few low energy sites could result in dislocation pile-ups, reduced glide velocities, asymmetric relaxation, and increased TDD. The model states that there exists a low energy, low areal density type of nucleation site, most likely associated with the edge of the wafer or particles on the surface. There also exists a higher energy, higher areal density type of site most likely associated with step bunches which are uniformly distributed across the wafer surface. It is thought that the step bunches are typical nucleation sites for dislocations in other compositionally graded buffer material systems that do not form dislocation pile-ups. Promotion of nucleation from the higher energy sites allows for a more spatially uniform distribution of dislocations which prevents the formation of dislocations pile-ups.

To determine if nucleation from the higher energy sites could improve the morphology of the $InAs_xP_{1-x}$ graded buffers we grew a series of samples with abrupt strain initiation at the $InAs_xP_{1-x}$/InP interface. By abruptly initiating strain in the structure the strain energy was quickly raised above the highest energy level. This allowed both types of nucleation sites to become active. We found that by introducing a moderate amount of strain abruptly at the $InAs_xP_{1-x}$/InP interface the TDD could be reduce by an order of magnitude. Reductions in the surface roughness and epitaxial tilt were also observed. We concluded that a more spatially uniform distribution of dislocations was nucleated and resulted in improved morphology of the $InAs_xP_{1-x}$ films.

6.1.2. Thermal cycle annealing of Ge/Si virtual substrates

We investigated methods of thermal cycle annealing of germanium films grown directly on silicon substrates to determine which annealing parameters were most efficient at reducing the TDD in the germanium layer. We determined that only brief annealing treatments were required to reduce the TDD to a level which was sufficient for majority carrier devices. Additional annealing of the films in any way did not result in a significant decrease beyond the initial reduction. We proposed an annealing treatment with minimal processing time of Ge/Si virtual substrates for majority carrier devices.

We varied the number of thermal cycles, the period of annealing time at the high temperature (the hold time), and the rate of temperature increase from the low to high temperature (the ramp rate). A statistical analysis of the EPD and surface roughness measurement results determined that none of the parameters had a significant effect. We noted that a slightly less restrictive assessment of statistical relevance would change the conclusion to state that both the number of annealing cycles and the hold time were significant in reducing the TDD. The surface roughness of the films was never found to be affected by the annealing treatment. However, we concluded that even the briefest annealing strategy resulted in a suitable TDD.

We conclude that two temperature cycles between 650 °C and 825 °C with 120 second pauses at 825 °C of a 1 μm germanium film were sufficient to reduce the TDD to less than or equal to 2×10^7 #/cm^2. This level of TDD is well below the limit of 10^8 #/cm^2 required for high performance majority carrier devices. The total annealing time for this abbreviated annealing treatment is reduced by at least a factor of 6.5 compared to the previously reported methods.

6.1.3. InGaAs QWs and InAlAs compositionally graded buffers

We developed $In_yGa_{1-y}As$ QW devices on an $In_vAl_{1-v}As$/Ge/Si platform. The $In_vAl_{1-v}As$ compositionally graded buffers were grown as thin as possible in order to minimize the total epitaxial thickness. We wanted to minimize the epitaxial thickness to avoid the formation of cracks in the wafer developing large stresses during cooling from the growth temperature. Additionally, since the Ge/Si virtual substrates would always have a TDD as large as 10^7 #/cm^2 it was not necessary to use graded buffers which had lower TDD values. Once a suitable graded buffer was developed, we grew $In_yGa_{1-y}As$ QW devices to demonstrate high electron mobility.

To determine the thinnest viable $In_vAl_{1-v}As$ graded buffer, we measured the TDD and surface roughness of three buffers grown on offcut GaAs substrates with different strain gradients. We found that strain gradients as high as 2.1 %ε/μm had a TDD of 1.3×10^7 #/cm^2 and an RMS surface roughness of 9.2 nm which was suitable for $In_yGa_{1-y}As$ devices. The graded buffers also had signs of slight phase separation but it did not appear to significantly affect the morphology. However, when the same $In_vAl_{1-v}As$ graded buffers were grown on the Ge/Si virtual substrates, the phase separation prevented relaxation and dislocation glide.

$In_vAl_{1-v}As$ graded buffers grown on Ge/Si virtual substrates had greater phase separation. When an $In_vAl_{1-v}As$ graded buffer with final composition of $In_{0.5}Al_{05}As$ was grown on a Ge/Si virtual substrate, the film appeared to phase separate beginning at approximately 30 %In. The phase separation was severe enough to limit dislocation glide which resulted in a very rough surface and high TDD. We speculated that the increased surface roughness of the Ge/Si virtual substrate compared to the GaAs substrates increased the tendency for phase separation. Therefore we decided to limit the final composition to $In_{0.3}Al_{0.7}As$ to avoid the problems created by the phase separation.

Films with suitable morphology were attained by limiting the composition of the $In_vAl_{1-v}As$ graded buffers to 30 %In on Ge/Si virtual substrates. These graded buffers had TDD values of 1.8×10^7 #/cm^2 and surface roughness of 20.2 nm. $In_{0.31}Ga_{0.69}As$ QW devices grown on these graded buffers had an electron mobility of 6398 cm^2/Vs when grown at 650 °C. The mobility is less than reported for similar compositions of $In_yGa_{1-y}As$, but is an improvement on previously reported devices grown on silicon substrates.

6.2. Recommendations for future work

The results from the research on $InAs_xP_{1-x}$ graded buffers suggests experiments in both the $InAs_xP_{1-x}$ system and other graded buffer material systems. Within the $InAs_xP_{1-x}$ material systems, new insights into the relaxation process may be gained by increasing the final composition of the graded buffer beyond the 15 %As used in our study. It is possible that in graded buffers that the mobile dislocations could be 'used up' by either gliding to the wafer edge or becoming trapped in a dislocation pile-up. This would suggest that another abrupt change in the misfit strain would be needed. The result of those experiments could also address whether linearly graded or step graded buffers offer any relative advantages. The theory of graded buffer relaxation implies that linearly graded buffers should be better since the misfit strain is spread throughout the layer instead of at discrete interfaces, but our results indicate that this may not always be advantageous due to the nature of dislocation nucleation. The experiments conducted on $InAs_xP_{1-x}$ should also be extended to other materials systems. Our results rely on the presence of the two energy level system of nucleation sites. Extension of these experiments to other graded buffer material systems could determine if both types of nucleation sites are present.

In our experiments with germanium films grown on silicon, we did not change the annealing temperatures. However, since both the thermal stress and the glide velocity are temperature dependent, it is possible that increasing the high annealing temperature could allow for faster reductions in the TDD. Likewise, experiments which change the low annealing temperature could be insightful. Due to the very strong temperature dependence of dislocation motion, it is possible that the dislocations are essentially immobile at the low temperature. Increase this temperature would allow for greater mobility of the dislocations throughout the annealing process but would decrease the thermal stresses developed during the cycling. This suggests that there is an ideal temperature difference that is a function of the low and high temperatures. Exploration of these relationships is recommended. Lastly, we attempted to use different temperature ramp rates, but were limited by the fragility of the graphite heater in our MOCVD reactor. Post-growth annealing of the germanium films in a rapid thermal annealing (RTA) system would not be limited in the same way and could reach very high temperature ramp rates. Faster temperature ramps may allow entangled dislocations to break free due to the very fast increase in thermal stress. At lower temperature ramp rates, dislocations adjacent to the entangled dislocations are able to glide and relieve the stress around the entangled dislocation, preventing their motion and diminishing their probability to participate in dislocation-dislocation reactions. A final note of caution, it has been shown that annealing of the germanium films should be done with an H_2 ambient to maintain smooth surfaces, but most RTA systems use an N_2 ambient atmosphere. Accounting for the differences in surface roughness or using a specialty RTA system would be required.

The $In_vAl_{1-v}As$ graded buffers that we developed experience phase separation which limited the compositions of $In_yGa_{1-y}As$ QW devices that we could develop. Future experiments should attempt to eliminate the phase separation by either increasing the growth temperature or reducing the strain gradient. It is suspected that the phase separation is caused by indium migration towards the valleys of the roughened surface. By growing at higher temperatures, the mobility of the aluminum atoms will increase and may prevent the segregation of the indium in the valleys. A lower strain gradient will reduce the surface roughness created by the cross hatch morphology. Either of these, or a combination, may be able to eliminate the phase separation and allow for the development of materials with greater indium compositions.

7. Appendix

7.1. XRD_analysis.mat

```
% This script allows the user to select peaks from 004 and 224 scans.  The
% script then corrects for any substrate misorientation (intentional or
% experimental).  Finally the script calculates the layer tilt of each
% film peak selected.

% This script calls the PeakSelector.m function.  That function returns a 3
% column matrix.  The 1st and 2nd columns are the qx and qz values, respectively,
% of the substrates and peaks.  The 3rd column will have values of
% 0 or 1, with 1 indicating that it is the substrate peak.  If no values in
% the 3rd column are 1, this script will allow the user to choose which row
% contains the substrate coordinates.

% Allow the user to select peaks with the PeakSelector function.  Change
% xrd_path to point to the root directory with data sets, the FitPeaks
% function uses uigetfile to allow for direct selection of the .dat files
clear allpeaks004 allpeaks224 In Jn Kn allpeaks004_cor allpeak224_cor ...
    del_qx del_qz film004_cor film224_cor film004_rot film224_rot ...
    filmpeaks004 filmpeaks224 gammma sub004_cor sub224_cor sub004_rot ...
    sub224_rot subpeak004 subpeak224 theta_mis tilt layer_tilt allpeaks angles uz

disp('Open the .dat file for the 004 RSM');
parts_004 = input('How many parts in the 004 RSM?');
[allpeaks004,path] = PeakSelector(xrd_path, parts_004);

if sum(allpeaks004(:,3)) ~= 1
    fprintf('\n')
    allpeaks004(:,3) = 0;
    disp(allpeaks004);
    sub004_row = input('No 004 substrate peak indicated, please enter the row of the peak in the
displayed matrix. Remeber that the rows are not necessarily in the order in which you selected
the peaks.');
    allpeaks004(sub004_row,3) = 1;
end

disp('Open the .dat file for the 224 RSM');
parts_224 = input('How many parts in the 224 RSM?');
[allpeaks224,~] = PeakSelector(path, parts_224);
```

```
if sum(allpeaks224(:,3)) ~= 1
    fprintf('\n')
    allpeaks224(:,3) = 0;
    disp(allpeaks224)
    sub224_row = input('No 224 substrate peak indicated, please enter the row of the peak in the
displayed matrix. Remeber that the rows are not necessarily in the order in which you selected
the peaks.');
    allpeaks224(sub224_row,3) = 1;
end

%Sort the peaks into Substrate and Film peaks

subpeak004 = zeros(1,2);
subpeak224 = zeros(1,2);

clear filmpeaks

%004 sorting
Kn = 1;
for In = 1:length(allpeaks004(:,1))
    if allpeaks004(In,3) == 1
        subpeak004(In,:) = allpeaks004(In,1:2);
    else
        filmpeaks004(Kn,:) = allpeaks004(In,1:2);
        Kn = Kn + 1;
    end
end

%224 sorting
Kn = 1;
for In = 1:length(allpeaks224(:,1))
    if allpeaks224(In,3) == 1
        subpeak224(In,:) = allpeaks224(In,1:2);
    else
        filmpeaks224(Kn,:) = allpeaks224(In,1:2);
        Kn = Kn + 1;
    end
end

% Find the substrate mis-orientation
theta_mis = atan(subpeak004(1,1)/subpeak004(1,2));

% Construct matrix to correct all peaks for the substrate mis-orientation
sub_mis = [[cos(theta_mis), -sin(theta_mis)];[sin(theta_mis), cos(theta_mis)]];

% Correct the peak positions for the substrate mis-orientation.  Then
% calculate the tilt for each film peak.  Finally, correct the film peak
% position for the tilt
sub004_rot = sub_mis*subpeak004';
sub224_rot = sub_mis*subpeak224';
sub004_cor = sub004_rot';
sub224_cor = sub224_rot';
```

```
for Jn = 1:length(filmpeaks004(:,1))
    film004_rot(Jn,:) = sub_mis*filmpeaks004(Jn,:)';
    film224_rot(Jn,:) = sub_mis*filmpeaks224(Jn,:)';
    del_qx = film004_rot(Jn,1) - sub004_cor(1,1);
    del_qz = film004_rot(Jn,2) - sub004_cor(1,2);

    gamma = atan(del_qx/film004_rot(Jn,2));
    tilt = [[cos(gamma), -sin(gamma)];[sin(gamma),cos(gamma)]];
    film004_cor(Jn,1:2) = tilt*film004_rot(Jn,:)';
    film224_cor(Jn,1:2) = tilt*film224_rot(Jn,:)';
    layer_tilt(Jn) = gamma;
end

angles = [theta_mis;layer_tilt'];
allpeaks004_cor = [sub004_cor;film004_cor];
allpeaks224_cor = [sub224_cor;film224_cor];
allpeaks = [allpeaks004_cor,allpeaks224_cor,angles];

%num2clips is a 3rd party function which places the passed array into the
%clipboard for easier pasting into excel
num2clip(allpeaks)
```

7.2. PeakSelector.mat

```
function [peaklocs_sorted,path] = PeakSelector(fpath,part_num)
% FitPeaks plots RSM data from Leptos in (qx,qz) coordinates and fits peaks.
% Click to the northwest and southeast of a peak to fit it.  Hit enter when
% finished.

% get filename and import data.  file must be in current directory.
old_path = pwd;
cd(fpath);

for n = 1:part_num
    [name, path] = uigetfile('*.dat');
    cd(path);
    rsm{n} = importdata([path,name],' ');
end

for n = 1:part_num
    % find number of qz and qx iterations
    x_size(n)=length(find(rsm{n}==rsm{n}(1,1)));
    y_size(n)=length(find(rsm{n}==rsm{n}(1,2)));

    % construct matrix of intensities (Z) for easy plotting

    for i = 1:y_size(n)
        for j = 1:x_size(n)
            Z{n}(i,j)=rsm{n}((i-1)*x_size(n)+j,3);

            % define vectors of qx and qz values
            X{n} = rsm{n}(1:x_size(n),2);
            Y{n} = rsm{n}(1:x_size(n):size(rsm{n},1),1);

            % Determine the step size of both x and y indices.
            Xstep{n} = (X{n}(end)-X{n}(1))/(length(X{n})-1);
            Ystep{n} = (Y{n}(end)-Y{n}(1))/(length(Y{n})-1);
        end
    end
end
```

```
for n = 1:part_num
    figure(1)
    [~,h] = contourf(X{n},Y{n},log(Z{n}+1),30);
    hold on;

    set(h,'EdgeColor','none');
    set(gcf, 'Color', 'w');
    xmin(n) = min(rsm{n}(:,2));
    xmax(n) = max(rsm{n}(:,2));

    ymin(n) = min(rsm{n}(:,1));
    ymax(n) = max(rsm{n}(:,1));
end


abs_xmin = min(xmin);
abs_xmax = max(xmax);
abs_ymin = min(ymin);
abs_ymax = max(ymax);
axis([abs_xmin, abs_xmax, abs_ymin, abs_ymax]);
xlabel('qx (Å^-^1)')
ylabel('qz (Å^-^1)')
title(name,'Interpreter','none')

disp('Click to the northwest and southeast of the peak that you want to fit. Be sure to hold
SHIFT while selecting the substrate peak. Hit enter when you are done.')

hold on
i = 1;
run_while = 1;
while run_while == 1
    % User clicks on top-left and bottom-right of rectangle containing peak
    % position.

    [peakX,peakY,button] = ginput(2);

    if length(peakX)~=2;
        break
    end

    peakArea(:,1) = peakX;
    peakArea(:,2) = peakY;

    % Plot user-specified box in red.
    plot([peakArea(1,1) peakArea(1,1)],[peakArea(2,2) peakArea(1,2)],'r-',...
        [peakArea(1,1) peakArea(2,1)],[peakArea(1,2) peakArea(1,2)],'r-',...
        [peakArea(2,1) peakArea(2,1)],[peakArea(1,2) peakArea(2,2)],'r-',...
        [peakArea(1,1) peakArea(2,1)],[peakArea(2,2) peakArea(2,2)],'r-');
```

```
    % This next part assumes that the part files go from the largest qz
    % values to the smallest qz values.  If your part files go in the
    % oposite direction, then they should be opened in reverse order.
    for corn = 1:2
        n = 1;
        part_found = 0;
        while part_found == 0

            if n > part_num
                part_n(corn) = input(['Exceeded maximum part number search. Please indicate part
number for corner ',num2str(corn),'?']);
                break;
            end

            findx = abs(X{n}-peakX(corn));
            findy = abs(Y{n}-peakY(corn));
            ix = min(findx)==findx;
            iy = min(findy)==findy;

            Counts = Z{n}(iy,ix);

            if isnan(Counts)
                n = n + 1;
            else
                part_n(corn) = n;
                part_found = 1;
            end
        end
    end

    % Let part A be the part with greater max qz and part B be the part
    % with the lesser max qz.  Note that part B is plotted on top of part A

    % Find the width and height of the user selected region based on the
    % step size of part B.
    iXwidth = abs(peakX(1)-peakX(2))/Xstep{part_n(2)};
    iYwidth = abs(peakY(1)-peakY(2))/Ystep{part_n(2)};

    % Find edges of part A
    p_n = part_n(1);
    corn1x = abs(X{p_n}-peakX(1));
    corn1y = abs(Y{p_n}-peakY(1));
    ixA_w = find(min(corn1x)==corn1x);
    izA_n = find(min(corn1y)==corn1y);
    ixA_e = ixA_w + iXwidth;
    izA_s = izA_n - iYwidth;

    if ixA_e > length(Z{p_n}(1,:))
        ixA_e = length(Z{p_n}(1,:));
    end
```

```
    if izA_s < 1
        izA_s = 1;
    end

    % Find edges of part B
    p_n = part_n(2);
    corn2x = abs(X{p_n}-peakX(2));
    corn2y = abs(Y{p_n}-peakY(2));
    ixB_e = find(min(corn2x)==corn2x);
    izB_s = find(min(corn2y)==corn2y);
    ixB_w = ixB_e - iXwidth;
    izB_n = izB_s + iYwidth;

    if ixB_w < 1
        ixB_w = 1;
    end

    if izB_n > length(Z{p_n}(:,1))
        izB_n = length(Z{p_n}(:,1));
    end


    % cull out rectangle and pass to peak fit function. This section again
    % assumes that the part files go from largest qz to smallest qz.
    if part_n(1) == part_n(2) % If the corners are in the same part number, then cull out the
rectangle from that region only.
        p_n = part_n(1);
        subset = Z{p_n}(izB_s:izA_n,ixA_w:ixB_e);
        Xsub = X{p_n}(ixA_w:ixB_e);
        Ysub = Y{p_n}(izB_s:izA_n);

        % A problem can arise (especially in 224 maps) where the shape of
        % the RSMs cause significant overlap in the qz direction.  When
        % both part numbers are equal, it is possible that they are one too
        % large due to the large overlap.  In this case, the subset would
        % consist of entirely NaNs.  If this is the case, we want to set
        % p_n to be part_n(1) - 1 and then reevaluate the subset and the
        % Xsub and Ysub values
```

```
        if isequaln(subset, NaN(size(subset))) % Evaluates to TRUE if all elements of subset are
NaN
            p_n = part_n(1) - 1;
            corn1x = abs(X{p_n}-peakX(1));
            corn1y = abs(Y{p_n}-peakY(1));
            ixA_w = find(min(corn1x)==corn1x);
            izA_n = find(min(corn1y)==corn1y);

            corn2x = abs(X{p_n}-peakX(2));
            corn2y = abs(Y{p_n}-peakY(2));
            ixB_e = find(min(corn2x)==corn2x);
            izB_s = find(min(corn2y)==corn2y);

            subset = Z{p_n}(izB_s:izA_n,ixA_w:ixB_e);
            Xsub = X{p_n}(ixA_w:ixB_e);
            Ysub = Y{p_n}(izB_s:izA_n);
        end

    else

        % Stich the 2 parts together: begin (1st) by taking the rows of part B from the
        % southern edge of the selected region up to the row where parts B
        % and A begin sharing values of Y (approx.).  2nd, in the
        % overlapping rows of A and B, use the value of B unless B is NaN.
        % If A and B are NaN, then let the stiched value be NaN. 3rd, take
        % the rows of part A starting at the point where A and B stop
        % sharing Y values (approx.) up to the northern edge of A.

        % Begin by extracting the subsets of A and B that fall within the
        % user selected region.
         temp_subA = Z{part_n(1)}(izA_s:izA_n,ixA_w:ixA_e); %The subset of part A that is within
the user selected region
         temp_YsubA = Y{part_n(1)}(izA_s:izA_n);
         temp_XsubA = X{part_n(1)}(ixA_w:ixA_e);


         temp_subB = Z{part_n(2)}(izB_s:izB_n,ixB_w:ixB_e); %The subset of part B that is within
the user selected region
         temp_YsubB = Y{part_n(2)}(izB_s:izB_n);
         temp_XsubB = X{part_n(2)}(ixB_w:ixB_e);

        clear subset;
         %Initialize with size of A plus B
         subset(size(temp_subA,1)+size(temp_subB,1),...
             size(temp_subA,2)+size(temp_subB,2)) = 0;

         %Add A to the upper left
         subset(1:size(temp_subA,1),1:size(temp_subA,2)) = temp_subA;

         %Add B to the lower right
         subset(size(temp_subA,1)+1:end,size(temp_subA,2)+1:end) = temp_subB;
```

```
    %Horizontally concatenat the X and Y vectors
    Xsub = [temp_XsubA;temp_XsubB];
    Ysub = [temp_YsubA;temp_YsubB];


end


Threshold = 0.5*max(max(subset));
subset_thresh = max(subset,Threshold)-Threshold;

% Center of Mass for all points in subset

mass_tot_all = sum(sum(subset_thresh));
[iind, jind] = ndgrid(1:size(subset_thresh,1),1:size(subset_thresh,2));
i_com_all = sum(subset_thresh(:).*Xsub(jind(:)))/mass_tot_all;
j_com_all = sum(subset_thresh(:).*Ysub(iind(:)))/mass_tot_all;


% This code plots the selected rectangle by itself, showing more detail
% incase the actual peak location is hard to see in the full RSM.
figure(2)
[~,h2] = contourf(Xsub,Ysub,log(subset_thresh+1),30);


set(h2,'EdgeColor','none');
xlabel('Arb. Units')
ylim([min(Ysub),max(Ysub)]);
figure(2)
hold on
plot(i_com_all,j_com_all,'go')
hold off

goodpeak = questdlg('Continue with this peak?');
if strcmp(goodpeak,'No')
    disp('Please select the peak manually on the zoomed in plot (Figure 2).')
    figure(2)
    [~,h2] = contourf(Xsub,Ysub,log(subset+1),30);
    set(h2,'EdgeColor','none');
    hold on
    plot(i_com_all,j_com_all,'go')
    hold off
    [i_com_all,j_com_all] = ginput(1);
end
```

```
    figure(1)
    % save coordinates of fitted peak into matrix
    peaklocs(i,1) = i_com_all;
    peaklocs(i,2) = j_com_all;
    if button(1) ~= 1
        peaklocs(i,3) = 1;
    else
        peaklocs(i,3) = 0;
    end

    % plot fitted peak location as green circle
    plot(i_com_all,j_com_all,'go');
    i = i+1;
end

hold off


reverse = sortrows(peaklocs,2);
peaklocs_sorted = reverse(end:-1:1,:);

cd(old_path);
```

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