Design of a Hardware Solar Emulator for an Experimental Microgrid

by

Colm Joseph O'Rourke

Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

Microgrids are regions where local generation and loads are clustered together. Students from the LEES group at MIT are currently developing an experimental microgrid. This will enable various studies in the area of microgrid dynamics. The setup consists of a variety of modules that emulate both conventional and renewable sources. In this thesis, we focus on the design of one of these modules: the solar PV emulator.

The complete design of a solar PV emulator will be described. Firstly, AC and DC models of a solar cell are introduced. These models specify design constraints for the power electronic circuitry. They also indicate a desired performance for the feedback control system. The controller design is discussed and the effect of load type on the closed-loop dynamics are considered. This is especially interesting for the grid-connected case.

The design methodology culminates in the construction of an experimental prototype of the hardware solar PV emulator. The modular design approach is outlined as are its benefits to the overall construction of the microgrid. A Generic Controller board that can be used for all future power electronic modules in the microgrid is also designed and fabricated. The results of simulations and experiments are discussed and it is shown that it is possible for a buck converter to emulate the steady state dynamics associated with solar PV panels.

Thesis Supervisor: James L. Kirtley Jr
Title: Professor of Electrical Engineering

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I would like to sincerely thank everyone who gave of their time, knowledge and experience to aid the process of completing this thesis. In particular I wish to offer a huge thanks to Professor James L. Kirtley Jr - for his support, expertise and dedication to this work. During the course of this project he generously gave his time, resources and knowledge resulting in a great deal of learning on the author's part.

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To all the guys in Professor Kirtley's group. I have really enjoyed working and learning from you. Also, the Friday visits to the Muddy Charles have been great at keeping me sane in the most stressful of times.

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Prior to beginning this course I believed coming to MIT would be the end of fun. Thanks to my wonderful housemates and friends for making MIT an enjoyable expe-

rience.

As a musician I am delighted to say I have finally joined a band. Thanks to Gus and Pavel for all the fun we have had writing songs and playing gigs. Hopefully we can finish that album soon.

To my wonderful girlfriend Julie. Thanks for being such a cool person to hang around with. Your care has always been really appreciated (not to mention your Irish soda bread). You are the best!

Finally, I wish to thank my family for their support and inspiration. I am lucky to have such an amazing family community and I look forward to seeing you all again.

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Chapter 1

Introduction

Microgrids are regions where generation and loads are clustered together. A manufacturing plant with its own combined cycle generation system, or a housing estate powered by local renewables are two examples of microgrids. Recently, the term has become quite popular in literature. However the concept of a microgrid is very old indeed. The early electricity systems developed by Edison and Tesla were essentially microgrids [10, 6]. These systems were smaller and more sensitive to changes in load. After Tesla and Westinghouse won the "war of the currents", the AC electricity grid continued to expand [9]. The US system now comprises of a large interconnection of AC transmission and distribution systems. The trend over the last century or more has been the expansion and interconnection of electricity grid systems [10]. This is true for North America as well as countries in Europe. Considering these long term trends, one might ask why are we concerned with microgrids?

There has been a considerable rise in the level of Distributed Generation (DG) in recent years [5, 1]. Although there has been a tendency for electricity grids to become more integrated, at the same time many areas are installing local generation via solar photovoltaic (PV) panels and small wind turbines [4]. Additionally, in the future it is possible that loads can be configured to have centralized control from utilities [2]. Thus, a better overall picture of the changing electric grid would be a larger and

more integrated electricity grid that has a greater generation capacity on the medium voltage (MV) and low voltage (LV) distribution network [7].

1.1 Thesis Overview

The goal of this thesis is to design a buck converter that is used for emulating the behavior of an actual photovoltaic (PV) array. This PV emulator is to be implemented as a source to a three-phase microgrid. At present, students at the LEES laboratory at MIT are building a microgrid experimental setup. This setup is indoors and does not include a real PV array. Therefore, a solar emulator has been proposed as a substitute for an actual PV array. Although this thesis focuses purely on the design of the buck converter, we shall discuss the wider system in order to explain the purpose of the buck converter more clearly. Figure 1-1 shows the setup for a real array.

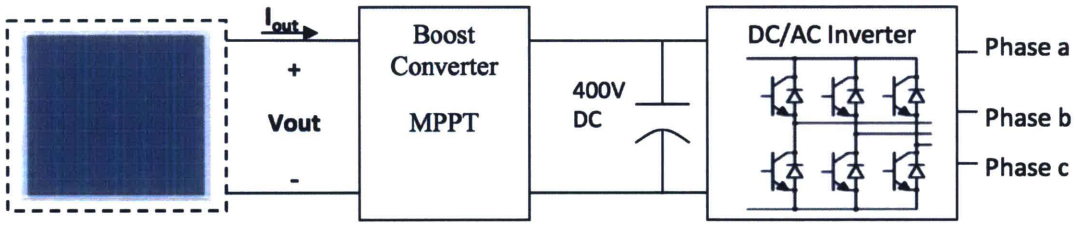


Figure 1-1: Solar PV with MPPT integrated into a Microgrid

We explain the operation of figure 1-1 from right to left. The inverter outputs three-phase voltage at 60Hz. It also includes a control loop that maintains the desired DC link voltage. The boost converter implements the Maximum Power Point Tracking algorithm (MPPT). It perturbs the PV panel output current I_{OUT} and then calculates P_{OUT}. Using this information it can find the I_{OUT} corresponding to I_{MPP}, the maximum power point current. At this operation point V_{OUT} will equal V_{MPP}.

By replacing the PV array in figure 1-1 with a voltage source in series with a buck converter we obtain the circuit in figure 1-2. This figure illustrates a hardware system

that emulates the behavior of an actual PV array. The goal of this project is to design the buck converter shown in 1-2. The operation of this circuit is very similar to the previous example with a real PV system. The buck converter measures I_{OUT} which is its output current. It then finds the corresponding V_{REF} on a photovoltaic I-V curve which can be simply stored in a lookup table. It then implements a duty cycle that makes V_{OUT} equal to V_{REF}. The control loop is constructed such that only the boost converter needs to implement the MPPT algorithm for both I_{MPP} and V_{MPP} to be achieved. Once the boost converter sets I_{OUT} equal to I_{MPP}, the buck converter will automatically find the corresponding voltage which will be maximum power point voltage.

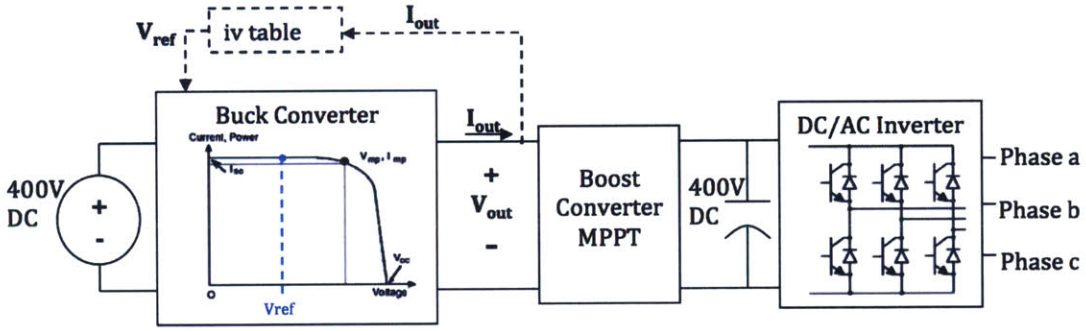


Figure 1-2: PV Emulator with MPPT integrated to Microgrid. Buck converter simulates PV characteristics

1.2 Solar Cell Models

1.2.1 DC Model of a Solar Cell

The DC model is more popular than the AC circuit and is typically seen in literature. A model of a single diode solar cell model is shown in figure 1-3. This model determines the I-V curve of a typical PV panel, as a panel is usually a series combination of several cells. The DC model suggests steady state specifications (see table 2.1) for the operation of a solar PV emulator.

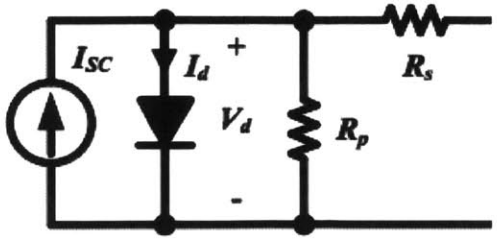


Figure 1-3: DC solar cell model

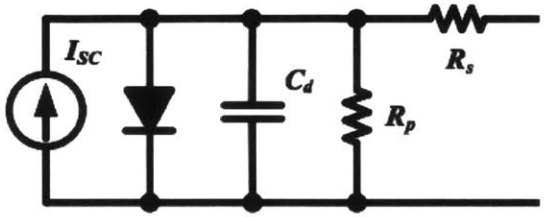


Figure 1-4: AC solar cell model [3]

1.2.2 AC Model of a Solar Cell

As transient dynamics are also of interest when designing a PV emulator, we must use a different model. A suitable model is presented by Chang in [3]. This includes a nonlinear capacitance that represents the effects of both junction and diffusion capacitance. This capacitance is included in figure 1-4. An expression for this capacitance [8] is written in equation 1.1.

$$C_d = \frac{\tau_F}{V_T} \cdot I_0 \cdot exp\left(\frac{V_T}{\eta \cdot V_d}\right) = C_0 + \frac{\tau_F}{V_T} \cdot I_d \tag{1.1}$$

The most pertinent aspect of equation 1.1 is that the capacitance is a function of both the operating voltage of the cell and the temperature. It is discussed in [8] and [3] that although the diffusion capacitance dominates near the Maximum Power Point (MPP), a single cell has a typical value of 5 μF.

1.2.3 Characterising the time constant of a solar PV panel

Using 5 μF for C_d we can estimate a response time for an individual solar cell. We apply this to a real solar PV panel using data from table 1.1 for the JKM250P-60 250 W panel. The cell of figure 1-4 shall now represent a single cell of this panel. We determine $V_{MPP_{CELL}}$ and $I_{MPP_{CELL}}$ in equations 1.2 and 1.3 in order to find the MPP for a cell.

Table 1.1: Paramaters for JKM250P-60 250 W panel

Parameter	Value
V_{MPP}	29.8 V
I_{MPP}	7.89 A
N_S	60
R_S	4 mΩ

$$V_{MPP_{CELL}} = \frac{V_{MPP}}{N_S} = 0.496V \tag{1.2}$$

$$I_{MPP_{CELL}} = I_{MPP} \tag{1.3}$$

A single cell of this panel is connected to a resistive load $R_{MPP_{CELL}}$ of 62.9 mΩ such that it is operating at its MPP. Neglecting the shunt resistor we approximate the equivalent resistance in equation 1.4. The time constant τ_{CELL} of the solar cell can be estimated as it becomes an R-C circuit.

$$R_{eq} = R_{MPP_{CELL}} + R_S = 64.9m\Omega \tag{1.4}$$

$$\tau_{CELL} = R_{eq}C_d = 0.335\mu s \tag{1.5}$$

Furthermore we can approximate the time constant of the PV panel of table 1.1. This panel has 60 cells in series which means the total resistance increases by a factor of N_S. However, the capacitance decreases by the same factor giving the same time constant for the panel as the cell.

$$\tau_{PANEL} = (N_S R_S + R_{MPP}) \frac{C_d}{N_S} = (N_S R_S + N_S R_{MPP_{CELL}}) \frac{C_d}{N_S} = \tau_{CELL} \tag{1.6}$$

This time constant presents a very difficult design problem for the solar PV emulator. It is quite challenging to meet the steady state requirements set by the DC model while also ensuring the response time is sufficiently fast.

It is quite apparent from this analysis that the effective capacitance of a solar panel would be completely dominated by the input capacitance of the power electronic circuitry connected to it. As this is the case for the microgrid experimental setup, it is not necessary for the solar PV emulator to have an extremely fast response time. For this reason preference is given to meeting the steady state requirements, while keeping in mind the dynamic characteristics.

Chapter 2

Converter Design

The power converter design is the most significant aspect of designing the solar PV emulator. This section describes the process of designing the input and output filters. Methods of electrical isolation and MOSFET drives are discussed. The modular design approach is outlined and the Generic Controller for microgrid power electronics modules is designed and fabricated. Finally, the section describes the layout of the printed circuit board.

Before we commence the converter design discussion, we will first define the required specifications of the buck converter, as shown in table 2.1. The origin of these parameters comes from simplifications made in the desired I-V curve, as well as application requirements. One of the main experiments for which this solar emulator will be utilised is comparing different ratios of inverter-based sources to synchronous sources such as the diesel generator emulator. Such an experiment requires the solar PV emulator to be of similar or greater power rating than the diesel generator module. This is why an MPP of 3.5 kW was chosen to be the maximum power rating of the solar PV emulator. This represents the MPP for a solar array comprising of panels conected in series and parallel. For example the JKM250P-60 250 W panel has an open circuit voltage V_{OC} of 30 V and a short circuit current I_{SC} of 9 A during Stan-

Table 2.1: Buck converter specifications

Quantity	Symbol	Value
Input voltage	V_{IN}	400 V
Input voltage transient limit	v_{INtran}	550 V for up to 1ms
Output power range	p_{OUT}	0–3.5 kW
Output current range	i_{OUT}	2-11 A
Output voltage (static requirement)	v_{OUT}	$V_{REF} \pm 3\%$
Allowed output voltage ripple (p-p)	Δv_{OUT}	1 V
Maximum output current ripple (p-p)	Δi_{OUT}	4 A
Allowed input current ripple (p-p)	Δi_{IN}	175 mA
Efficiency at maximum power point	η_{MPP}	>88%
Gain of input filter at resonant frequency	Q	3 dB
Power rating	P_{MAX}	3.5 kW
Switching frequency	f_{SW}	70 kHz

dard Test Conditions (STC).[1] Using these values as a reference we can determine the number of such panels required in series and parallel.

$$Number_{SERIES} = \frac{V_{OCdesired}}{V_{OC}} = \frac{400V}{30V} \approx 14 \tag{2.1}$$

$$Number_{PARALLEL} = \frac{I_{SCdesired}}{I_{SC}} = \frac{11A}{9A} \approx 2 \tag{2.2}$$

Using these values and operating points as a guide, we can determine a simplified I-V curve for which we want our converter to emulate. Figure 2-1 illustrates the maximum power conditions that we used to determine the specifications in table 2.1.

It is important to consider what aspects of this curve we wish to emulate most accurately. For a real solar PV panel its operation usually begins at the open circuit voltage, as its terminals are open. Then the MPPT algorithm perturbs the current drawn until the panel operates near its maximum power point. This sequence of

[1]Standard Test Conditions: $1kW/m^2$ irradiance, 25°C cell temperature and Air Mass 1.5 spectral distribution

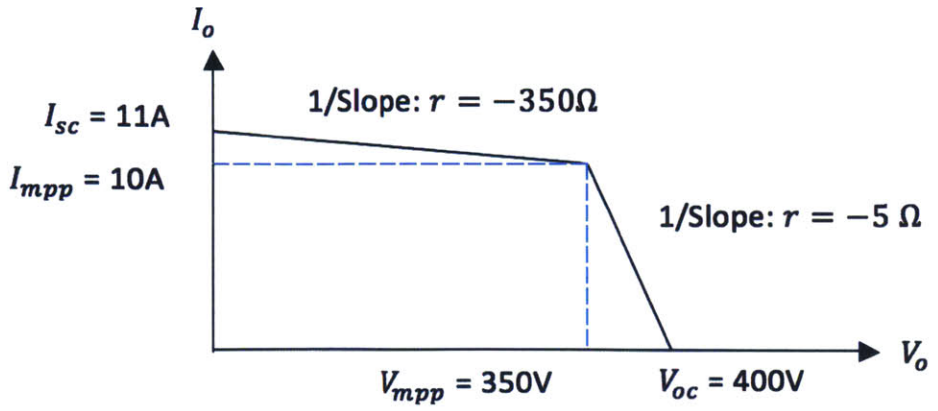


Figure 2-1: Simplified I-V curve

conditions presents an interesting range of operation for our buck converter. Firstly, we may not be able to operate near its open circuit voltage without the converter entering discontinuous conduction mode. Secondly, although the MPP can be used as the worst case for our design, it is not the point where the output current and voltage ripple will be most severe. This actually occurs at a lower voltage than the maximum power point.

In addition to emulating the steady state I-V curves of a solar PV panel, the buck converter must also have comparable dynamic characteristics. This translates to having a faster response time. To achieve such a response time it is important that we design using the smallest output filter components required. This is why a high switching frequency is desirable. However, because we have chosen a hard-switched topology we are limited to an f_{SW} in the kHz range, so that the switching losses are maintained within a safe level.

Figure 2-2 illustrates the complete circuit. The next sections will determine values for each of the components in order to meet the specifications tabulated in table 2.1

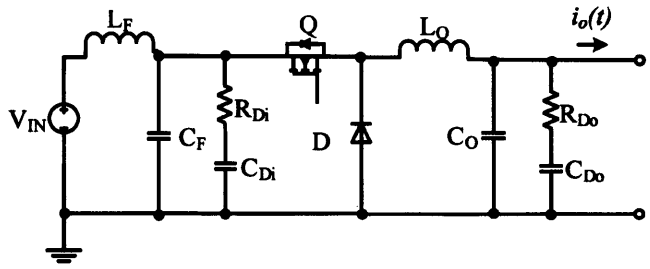
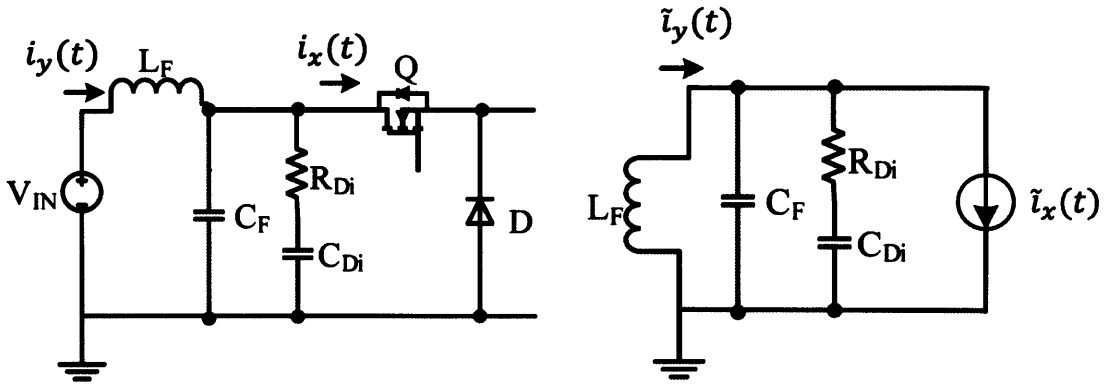


Figure 2-2: Complete Circuit



(a) Input Filter of Buck Converter

(b) AC Model of Input Filter

Figure 2-3: Input Filter Circuit and AC Model

2.1 Buck Converter Input Filter

The input filter was designed to mitigate both conducted and radiated electromagnetic interference (EMI). It has little effect on the important dynamics of the buck converter as we are using a fixed input voltage. An L-C filter is used, where the values of the components are given by L_F and C_F. In addition, a damping leg is used to mitigate the magnitude peak at the resonant frequency.

In order to select appropriate values of the input filter, we first apply the relevant constraints from table 2.1. The input filter specifications are a Δi_{IN} of 175mA and a gain of 3 dB at the resonant frequency. A schematic of the input section of a buck converter and its corresponding AC circuit model are given in figure 2-3.

We can replace the downstream circuit with a current source whose value equals the

current $i_x(t)$ flowing into the MOSFET. The DC input voltage has no AC component and thus it acts as a short circuit from the point of view of the AC circuit model. As the circuit shown in figure 2-3b contains purely AC signals, we may analyze it using impedance circuit analysis. Replacing each passive component with its equivalent impedance and using the current divider rule we can obtain a transfer function that relates the current $\widetilde{i}_x(t)$ and $\widetilde{i}_y(t)$.

$$H_{IN_1}(s) = \frac{\widetilde{i}_y(t)}{\widetilde{i}_x(t)} = \frac{1}{s^2 L_F C_F + s\left(\frac{L_F}{R_{Di}}\right) + 1} = \frac{1}{s^2\left(\frac{1}{\omega_0^2}\right) + s\left(\frac{1}{Q\omega_0}\right) + 1} \tag{2.3}$$

$$H_{IN_2}(s) = \frac{\widetilde{i}_y(t)}{\widetilde{i}_x(t)} = \frac{sR_{Di}C_{Di} + 1}{s^3 R_{Di}C_{Di}L_F C_F + s^2(L_F C_F + L_F C_{Di}) + sR_{Di}C_{Di} + 1} \tag{2.4}$$

The function $H_{IN_1}(s)$ represents the transfer function obtained without a damping leg. $H_{IN_2}(s)$ is the resulting transfer function when damping is included. The damping resistor R_{Di} provides a means for power to dissipate during resonance. To reduce the power dissipation due to the DC component of the voltage, we add a damping capacitor C_{Di}.

We choose C_{Di} to be 3 times larger than C_F. The resonant frequency ω_0 can be written as:

$$\omega_0 = \frac{1}{L_F C_F} \tag{2.5}$$

Evaluating $H_{IN_2}(s)$ at the resonant frequency enables us to write a 4^{th} order equation in terms of the resonant frequency ω_0. The MATLAB script 'solvew0' solves this equation and is included in the appendix. Solving the fourth order equation yields the following component values listed in table 2.2.

Alternatively, we can solve for the component values by first making the assumption that $C_{Di} \gg C_F$. This allows us to neglect this C_{Di} term in the transfer function

Table 2.2: Input filter component values

Component	Value
L_F	79.3 μH
C_F	6.3 μF
R_{Di}	5 Ω
C_{Di}	18.9 μF

$H_{IN_1}(s)$. Further justification for this assumption is illustrated by figure 2-4. This magnitude response comparison shows that ignoring C_{Di} has very little impact, as the bode plots for both cases match quite well. If C_{Di} is eliminated, we can begin determining the component values by first choosing a damping resistor value and then calculate the capacitor and inductor values required to achieve the desired gain of 3 dB at the resonant frequency.

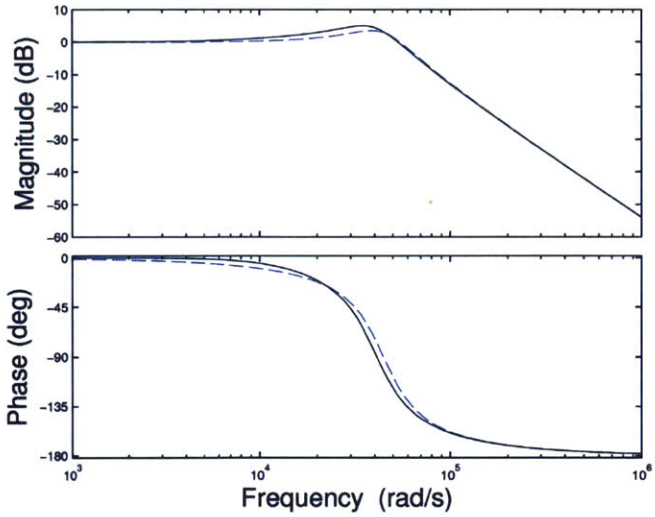


Figure 2-4: Input Filter Bode Plot without C_{Di} (blue) and with C_{Di} (black)

2.2 Buck Converter Output Filter

The output filter determines the main dynamics of the plant system. It is the most pertinent section of the buck converter circuit design from the perspective of capturing

the fast response time of a real solar PV panel. We must also be conscious of the controller's requirements of both the buck converter and the MPPT circuit, in order to specify what Δv_{OUT} and Δi_{OUT} they can tolerate. The MPPT system measures both v_{OUT} and i_{OUT} in order to calculated p_{OUT}. It is quite apparent that if v_{OUT} and i_{OUT} vary substantially then the MPPT controller should apply digital averaging to the sampled values. As typical MPPT algorithms operate at frequencies close to 1 kHz, the MPPT controller has a relatively large averaging window when compared with an f_{SW} of 70 kHz. This indicates that the MPPT controller does not put any constraints on the design of the output filter.

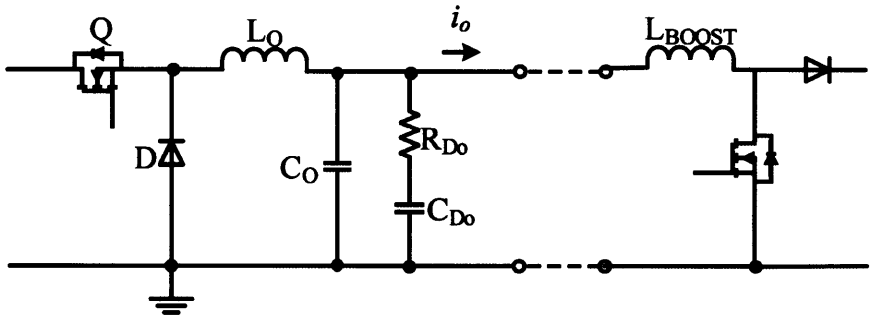


Figure 2-5: Output Filter of Buck Converter connected to the input of the MPPT Boost circuit

The completed design shown in figure 2-5 has the same L-C structure as the input filter. Despite this, the design process is quite different as the specifications required differ. Table 2.1 specifies a Δv_{OUT} of 1 V and a Δi_{OUT} of 4 A. To ensure that the converter operates in continuous conduction mode it is important that we keep the maximum output current ripple Δi_{OUT} below twice the lowest output current, when operating near the open circuit voltage.

2.2.1 Output inductor

The value of the output inductor L_O can be found by analyzing the circuit and obtaining an equation that describes the minimum inductance required to prevent DCM . In periodic steady state (PSS), the output inductor current is a periodic

triangular waveform. This is because the voltage across the inductor is a periodic square wave. Furthermore the output voltage and current are DC quantities in PSS. As the inductor voltage waveform is known we can integrate to find the inductor current. This allows us to determine Δi_{L_O}.

$$i_{L_O}(DT) = \int_0^{DT} (\mathrm{V_{IN}} - \mathrm{V_{OUT}})\,\mathrm{d}t + i_{L_O}(0) \tag{2.6}$$

$$\Delta i_{L_O} = \frac{(V_{IN} - V_{OUT})DT}{L_O} = \frac{V_{IN}D(1-D)}{f_{SW}L_{MIN}} \tag{2.7}$$

$$L_{MIN} \geq \frac{V_{IN}D(1-D)}{f_{SW}\Delta i_{L_O}} \tag{2.8}$$

Equation 2.8 shows that the minimum inductance required depends on the chosen DC operating point. The term $D(1-D)$ is maximised for a duty of $\frac{1}{2}$. Thus, the value of Δi_{L_O} is largest for this duty cycle. However, we are most concerned with the current ripple when the steady state output current is lowest. This is when the duty cycle is 0.975 giving an I_O of 2 A. These operating points on our simplified I-V curve are illustrated in figure 2-6. This plot shows the interesting fact that the maximum inductor current ripple will occur when the duty cycle is 0.5, and that Δi_{L_O} will be much smaller near the point where I_O is smallest. Using our constraint of a Δi_{L_O} of 4 A when I_O is 2A we find that the minimum inductance required is 34.8 μH.

The issue with the previous method is that the resulting inductor current ripple can be very large relative to its averaged value at operating points near a duty cycle of $\frac{1}{2}$. For example if we evaluate equation 2.7 at 50% duty cycle using an inductance of 34.8 μH we get a Δi_{L_O} of 41 A which is unacceptable. We now introduce another constraint called the ripple ratio R_{i_L}. If we specify a maximum ripple ratio of 47.9% (ie. Δi_{L_O} of 5 A) at the 50% duty cycle operating point then we can find a new expression for L_O.

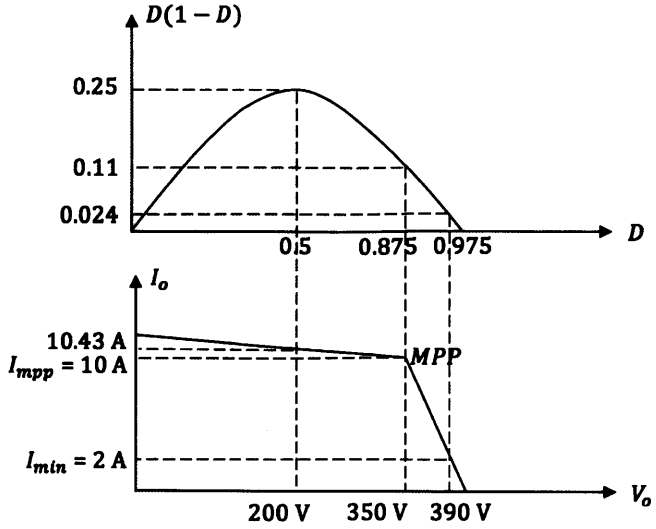


Figure 2-6: Variation of $D(1-D)$ with steady state operating point

$$R_{i_L} = \frac{\Delta i_{L_O}}{\langle i_{L_O}(t) \rangle} \tag{2.9}$$

$$L_{MIN} \geq \left. \frac{V_{IN} D(1-D)}{f_{SW} R_{i_L} I_O} \right|_{D=\frac{1}{2}} = 285.7 \mu H \tag{2.10}$$

This corresponds to a Δi_{L_O} of 5 A at a duty cycle of $\frac{1}{2}$. The current ripple Δi_{L_O} at the minimum output DC current of 2 A is now 0.96 A which is much less than the specified maximum in table 2.1.

2.2.2 Output capacitor

Our goal in this section is to identify the minimum capacitance required to achieve a voltage ripple Δv_{C_O} that is less than our specified maximum value. Recall that we commenced the inductor calculation by analysing the inductor current and voltage waveforms in PSS. Similarly we can use the waveforms of the capacitor current and voltage to construct an equation that calculates the minimum capacitance necessary.

In PSS for a large capacitor we can assume that $\langle i_{C_O}(t)\rangle$ is zero. In other words, the AC component of $i_{L_O}(t)$ flows into the output capacitor alone. This represents a worst case voltage ripple analysis. Integrating $i_{C_O}(t)$ we can determine the minimum capacitance in terms of Δv_{C_O} and Δi_{L_O}.

$$C_{MIN} \geq \frac{\Delta i_{L_O}}{8 f_{SW} \Delta v_{C_O}} \tag{2.11}$$

The ripple ratio for the output capacitor voltage R_{v_C} is chosen to be 1%. This results in a Δv_{C_O} of 2 V. Using this we can write a new expression for the minimum capacitance required.

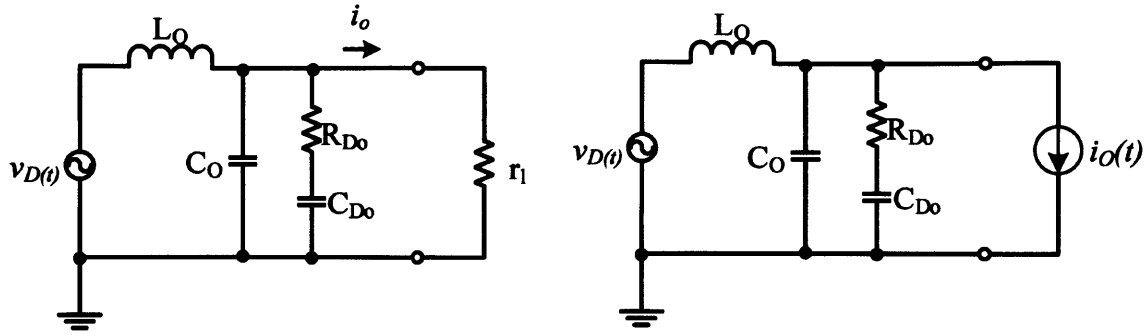
$$R_{v_C} = \frac{\Delta v_{C_O}}{\langle v_{C_O}(t)\rangle} \tag{2.12}$$

$$C_{MIN} \geq \left.\frac{R_{i_L}\langle i_{L_O}(t)\rangle}{8 f_{SW} R_{v_C}\langle v_{C_O}(t)\rangle}\right|_{D=\frac{1}{2}} = 4.46\mu F \tag{2.13}$$

2.2.3 Output damping leg

The significance of the output damping leg directly relates to the load powered by the solar PV emulator. In the case of resistive loads, the load itself provides damping for the output L-C filter and a damping leg is not very useful. On the other hand, if the PV emulator is grid connected via an inverter then this corresponds to a very stiff load that provides little damping. Figure 2-7b illustrates how we model the grid-connected case of little or no damping using a current source. Conceptually, this makes sense as the input to the MPPT boost converter is an inductor. Alternatively, we can choose to model the MPPT boost circuit as a negative incremental resistance as shown in 2-7a. The reasoning behind this stems from the negative slope of the operating region on the I-V curve which the MPPT algorithm forces. An r_l of -1 Ω was determined by estimating the slope of the JKM250P-60 250 W panel near its

maximum power point.



(a) MPPT boost circuit modeled with negative incremental resistance r_l

(b) Boost circuit modeled with current source

Figure 2-7: Output Filter Circuit with Boost converter models

During resonance we must ensure that the effective small signal resistance r_{eff} connected to the output of the buck converter filter is positive. Choosing a damping resistor R_{Do} of 0.5 Ω provides an r_{eff} of 1 Ω .

$$r_{eff} = \frac{r_l R_{Do}}{r_l + R_{Do}} \tag{2.14}$$

2.2.4 Output Filter Summary

The output filter component values are summarized in table 2.3. The DC blocking capacitor C_{Do} is included and was chosen to be 3 times larger than C_O.

Table 2.3: Output filter component values

Component	Value
L_O	285.7 μH
C_O	4.46 μF
R_{Do}	0.5 Ω
C_{Do}	13.4 μF

2.3 Inductor Design

The inductor is typically one of the heaviest components in a switching converter. It also is a major contributor to the overall efficiency and performance of the circuit. This section outlines how the buck converter input and output inductors were designed.

2.3.1 Design methodology

The inductance of an element is defined by the relationship between flux linkage and voltage. Using this definition we can determine the peak value of the magnetic flux density B_{pk}.

$$d\lambda = Ldv \tag{2.15}$$

$$L = \frac{\lambda_{pk}}{i_{L_{pk}}} = \frac{N\Phi_{pk}}{i_{L_{pk}}} \tag{2.16}$$

$$B_{pk} = \frac{Li_{L_{pk}}}{NA_C} \tag{2.17}$$

The maximum B_{pk} was chosen to be 0.3 T. The PM50 core by EPCOS was chosen as this was found to be the smallest inductor whose B_{pk} did not exceed our 0.3 T limit. This has an A_L value of 250 nH. The required number of turns are calculated based on this A_L.

$$N = \sqrt{\frac{L(nH)}{A_L}} \tag{2.18}$$

The minimum required wire gauge can be found based on the maximum allowable

current density J_{pk} which was chosen to be 500 A/cm^2. Thicker wires have lower resistance, however the cross-sectional area occupied by the turns inside the core window must be less than the window area. Both L_F and L_O were assembled and their values are listed in table 2.4.

Table 2.4: Measured inductance values

Component	N	Desired L	Measured L
L_F	18	79.3 μH	87.6 μH
L_O	34	285.7 μH	289 μH

2.4 Gate Driver

The solar PV emulator contains a single high-side MOSFET. Turning on and off MOSFET devices is essentially about charging and discharging capacitors. The MOSFET has two input capacitances C_{GD} and C_{GS}, which are charged by the gate driver such that V_{GS} exceeds its threshold. Large currents are required to achieve this, thus we are not able to drive a MOSFET directly from a microcontroller and require a gate driver. One common way of driving high-side MOSFETs is using a bootstrap gate driver. These gate drivers can use a ground-referenced power supply. Alternatively, a regular low-side gate driver can be used as long as the supply powering the gate driver has its ground connected to the source of the MOSFET. The latter was the chosen option in this case.

The NC7SZ125 digital buffer was selected to provide isolation from the PWM pin of the DSP to the gate driver IC. Although the optocoupler gate driver already provides isolation, the digital buffer provides the 15 mA required by the LED inside the driver. The buffer has an active low enable pin, which we tie to ground. This ensures the output Y is in a known voltage state. This output connects to the anode of the optocoupler gate driver LED. A resistor R_{LED} is inserted to limit the current provided by the digital buffer.

$$R_{LED} = \frac{v_{BUFFER}}{i_{LED}} \tag{2.19}$$

The optocoupler gate driver input LED requires a current of 15 mA from the 3.3 V digital buffer, giving a desired R_{LED} of 220 Ω.

There are three main criteria when choosing a high-side gate driver: required gate current, speed and common mode voltage rejection. The FOD3180 is a 2 A MOSFET gate driver optocoupler. It can switch up to 250 kHz, which exceeds the 70 kHz operation of the solar emulator. The source terminal of the MOSFET jumps from 0 V to V_{IN} every switching period in a buck converter. The gate voltage must exceed this level in order for the MOSFET to turn on. This is why the FOD3180 has a 15 kV common mode voltage rejection. Decoupling and filter capacitors are required between the 15 V supply pin and the VEE pin which connects to the source of the MOSFET. These provide the reactive power associated with switching the MOSFET on and off.

A resistor should be inserted between the gate driver and the MOSFET to limit the current flowing during turn-on. This is necessary for both the protection of the 2 A optocoupler and the gate itself. The 15 V gate driver has an output resistance of 1.5 Ω and the gate resistance of the IPW60R045CP is 1.3 Ω . Using a desired gate current of 2 A we can approximate the necessary resistance.

$$R_{G_{LIM}} = \frac{15V}{2A} - 1.5\Omega - 1.3\Omega = 4.7\Omega \tag{2.20}$$

High-side MOSFETs often require gate to source voltage clamping protection. Gate to source transients are similar to drain to source transients, in that they are both caused by abruptly changing current in parasitic inductances. A simple and effective solution to mitigate this is to insert a Transient Voltage Suppression (TVS) diode. These diodes are specifically designed to prevent voltage transients, just as Zener

diodes are used for voltage regulation.

The reverse standoff voltage V_{RS} is the main parameter used in selecting TVS diodes. The chosen diode should have a V_{RS} that is greater than the expected gate voltage during turn on. The second criterion for selecting a TVS diode is its clamping voltage V_C. This should be less than the maximum gate to source voltage of the MOSFET. The DF2S6.8UFS TVS diode has a 19 V reverse standoff voltage, which is compatible with the 15 V gate driver. In addition its 22 V clamping voltage ensures that the gate to source voltage of the IPW60R045CP MOSFET does not exceed its 30 V rating.

2.5 PCB layout

It is logical for one to expect that the layout of a power electronic circuit should be represented by its schematic. This is a dangerous mistake that many engineers make when building their first power converters. Each trace we layout has its own resistance, capacitance and inductance. Therefore, the simplified diagrams used to explain power converters in textbooks that have zero impedance connections between elements are clearly not a complete representation of a physical circuit.

2.5.1 Critical Nodes and Loops

When designing the PCB layout of a power converter, we first consider what the most critical nodes and loops are. The critical node in the buck converter is the point where the source of the MOSFET meets the cathode of the freewheeling diode. The voltage at this point jumps from the input voltage to ground every switching period. Parasitic inductance between the switch and the diode can become significant if the devices are far apart. This can cause voltage spikes as current in the parasitic inductor changes sharply. This is why we ensure that these devices are as close as possible.

There are two very important loops in the buck converter circuit that must be kept as small as possible. The first is the gate-driver and MOSFET circuit. Having the gate driver far from the MOSFET means that we are adding parasitic inductance, capacitance and resistance between the driver and the MOSFET. This has two possible adverse effects: slow turn-on and/or gate-to-source voltage ringing.

The gate-driver provides a step-like pulse in voltage. The parasitic filter may round this pulse, causing the MOSFET to turn on slower. Secondly, if the gate-to-source voltage pulse contains frequencies close to the resonant frequency of the parasitic L-C combination, then the voltage will begin to ring. This may cause the MOSFET to switch unpredictably. To prevent these effects traces are kept short to reduce inductance and wide in order to reduce resistance. Now when placing a gate resistor the designer can have control over how fast they wish the device to turn on.

The second loop of high importance is the one containing C_F, Q and D. If this circuit is not sufficiently compact, then voltage spikes will appear at the source of the MOSFET due to parasitic inductance. To mitigate these effects C_F is placed as close as possible to the MOSFET. The type of capacitor used is also important. Although film capacitors have a very low ESR, they naturally have more inductance than ceramic capacitors due to the way they are physically constructed from wound foil. Therefore, it is wise to use a ceramic capacitor for C_F. Otherwise, if C_F is a film capacitor we may add an additional small ceramic capacitor and place this close to the drain of the MOSFET.

2.6 Modular Design

2.6.1 Generic Controller Circuit

The microgrid setup includes several printed circuit boards that share common features such as memory, microcontrollers and UART to USB communication. A Generic

Controller board was designed to supply these auxiliary elements.[2] Figure 2-8 illustrates the main functions of the Generic Controller. The physical circuit is included in figure 2-9.

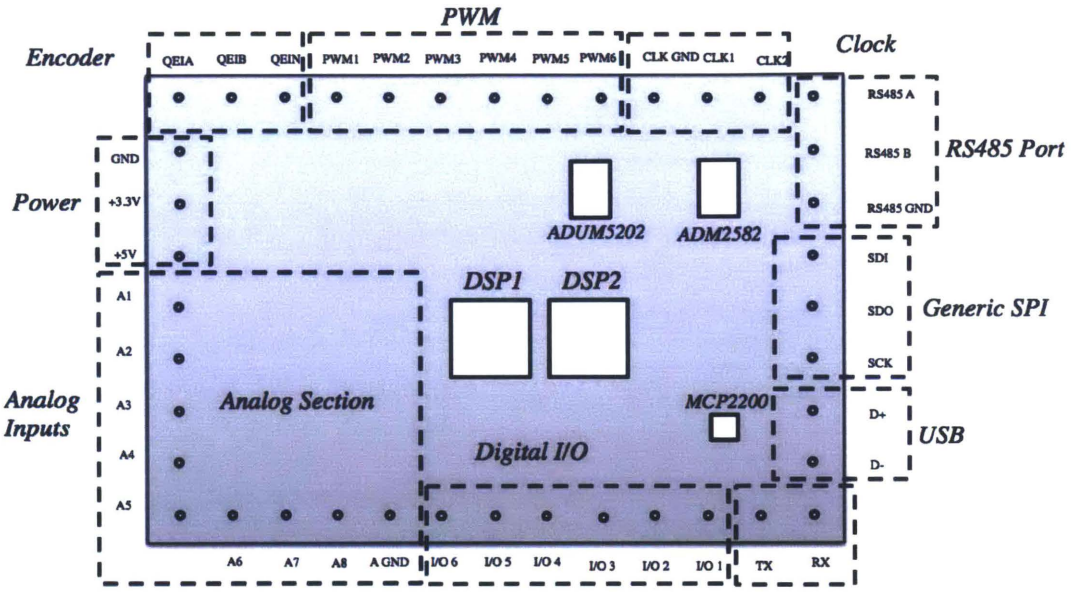


Figure 2-8: Generic Controller Board Schematic

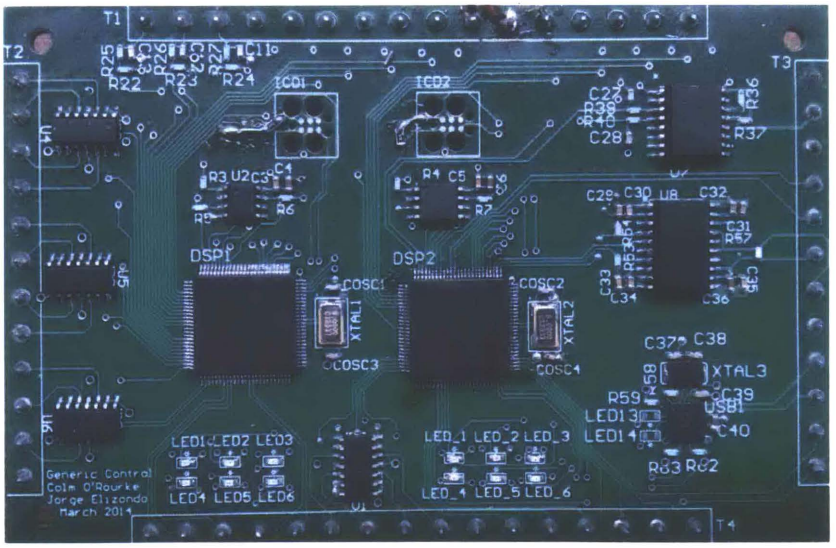


Figure 2-9: Generic Controller Board

[2]The Generic Controller functionality was specified following a collaboration of the author and Jorge Elizondo Martinez. The circuitry and PCB layout were designed by the author.

2.6.2 Experimental Prototype

The insights gained from the analysis of the converter design culminates in the construction of an experimental prototype. This prototype includes the power electronic circuitry, as well as the various auxiliary circuits. The Generic Controller described in section 2.6.1 implements the digital control and is seen in figure 2-10. Voltage and current sensor circuits were designed and analog signal conditioning was included to ensure the signals were within the voltage range of the ADC. The schematics and PCB layout are included in the Appendix. A discussion of the experimental results is included in section 4.2.

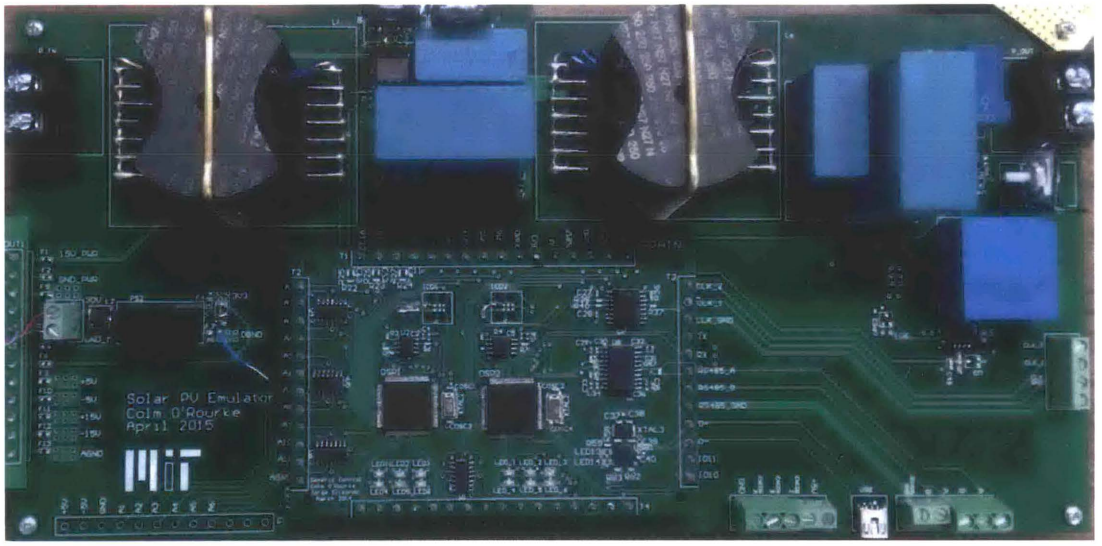


Figure 2-10: Constructed Prototype

Chapter 3

Controller Design

In this section we develop the feedback controller that enables the buck converter to emulate a PV panel. The state space models of the solar PV emulator are introduced. We use these models to determine transfer functions of the plant. This facilitates in the design of the feedback controller.

The solar PV emulator will be mainly used in two experimental scenarios: grid-connected via an MPPT circuit with an inverter and connected directly to a resistive load. These situations have very different load characteristics as discussed in section 2.2.3. Resistive loads are much less problematic from a control perspective as the load can provide significant damping. On the contrary if the PV emulator is used as a module in the microgrid, it will certainly have less damping. This is why a current source is used to model the downstream circuit. It provides a worst case damping scenario. Practically, the MPPT algorithm works by making the MPPT circuit appear like a resistive load whose load line intersects the MPP. Thus the damping conditions on the solar PV emulator in grid-connected mode are probably not as severe as with a current source load.

Voltage control can be implemented for the grid-connected buck converter as shown in figure 3-1. The converter measures the current drawn by the MPPT circuit. It

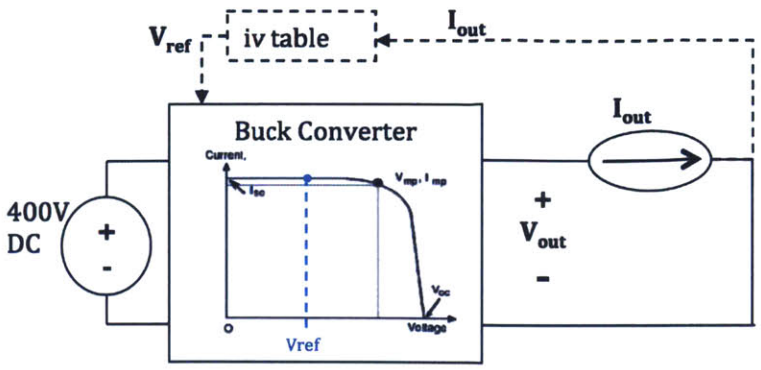


Figure 3-1: Buck converter with MPPT controller operation

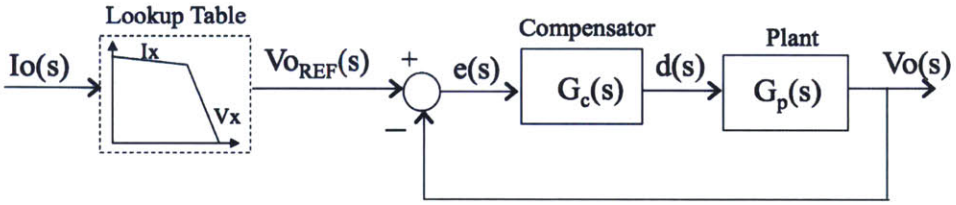
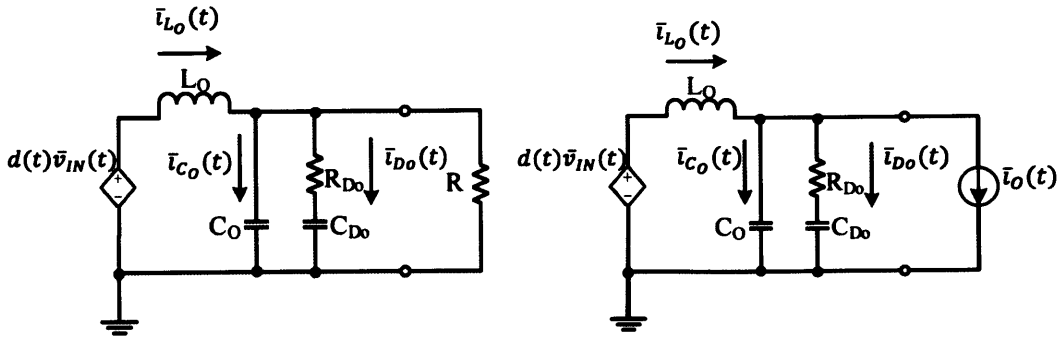


Figure 3-2: Voltage control block diagram

employs a lookup table that outputs a voltage reference for a measured current. This output voltage reference is compared with the actual measured output voltage. The voltage control operation of figure 3-1 is represented in block diagram form in figure 3-2. This shows how the error signal generated by the difference between the measured and reference voltage is used to generate a duty cycle.

We begin our controller design by evaluating the second and third order models for both resistive and current source loads. Following this the compensator is designed. Finally, we end with a discussion of implementing the controller in discrete time and compare this with continuous control.



(a) Resistive load (b) Current source load

Figure 3-3: Averaged Circuit Model of Buck Converter

3.1 State Space Models

Prior to developing a state space model, we define the characteristics of interest. Averaged circuit models are very useful for capturing the important dynamics of switching converters. They exhibit the underlying trends in waveforms by removing the component of the signal at the switching frequency. This is accomplished by applying the moving average of equation 3.1 to the current and voltage waveforms.

$$\overline{x}(t) = \int_{-\frac{T}{2}}^{\frac{T}{2}} \mathrm{x}(\tau)\,\mathrm{d}\tau \tag{3.1}$$

Using this definition we develop the averaged circuit models as depicted by figures 3-3a and 3-3b. These replace the circuitry to the left of the output filter with a dependent voltage source. This is justified, as the plant dynamics between the output voltage and the duty cycle are not affected by the input filter. However, as discussed earlier in this section, the output load affects the dynamics significantly. Hence we include models for the resistive load in figure 3-3a and the current source load in figure 3-3b.

3.1.1 Second Order State Space Model

The second order state space model refers to neglecting the damping leg in figures 3-3a and 3-3b. To find the state space models we simply apply the KCL and KVL equations. The equations for the resistive load case will be used as a demonstration. The same approach is taken to find the state space models for the current source case.

$$d(t)\overline{v_{IN}(t)} = \overline{v_{L_O}(t)} + \overline{v_{C_O}(t)} \tag{3.2}$$

$$\overline{i_{L_O}(t)} = \overline{i_{C_O}(t)} + \overline{i_O(t)} = C_O \frac{d}{dt}\overline{v_{C_O}(t)} + \frac{\overline{v_{C_O}(t)}}{R} \tag{3.3}$$

$$\frac{d}{dt}\overline{i_{L_O}(t)} = \frac{-1}{L}\overline{v_{C_O}(t)} + \frac{d(t)}{L}\overline{v_{IN}(t)} \tag{3.4}$$

$$\frac{d}{dt}\overline{v_{C_O}(t)} = \frac{1}{C_O}\overline{i_{L_O}(t)} - \frac{1}{RC_O}\overline{v_{C_O}(t)} \tag{3.5}$$

For a constant input voltage the above equations are already linear. Otherwise, we would develop a linearized set of state space equations by restricting the operation of the circuit to AC perturbations about a quiescent point. The second order state space model for a resistive load is given by equations 3.6 and 3.7.

$$\frac{d}{dt}\widetilde{i_{L_O}}(t) = \frac{-1}{L}\widetilde{v_{C_O}}(t) + \frac{d(t)}{L}V_{IN} \tag{3.6}$$

$$\frac{d}{dt}\widetilde{v_{C_O}}(t) = \frac{1}{C_O}\widetilde{i_{L_O}}(t) - \frac{1}{RC_O}\widetilde{v_{C_O}}(t) \tag{3.7}$$

The same approach is followed to determine the second order state space model for the buck converter connected to a current source load. This model is delineated by equations 3.8 and 3.9. It was observed that this state space model had damping problems which made the controller design difficult. Therefore, it is necessary to analyse the third order model with the damping leg included.

$$\frac{d}{dt}\widetilde{i_{L_O}}(t) = \frac{-1}{L}\widetilde{v_{C_O}}(t) + \frac{d(t)}{L}V_{IN} \tag{3.8}$$

$$\frac{d}{dt}\widetilde{v_{C_O}}(t) = \frac{1}{C_O}\widetilde{i_{L_O}}(t) - \frac{1}{C_O}\widetilde{i_O}(t) \tag{3.9}$$

3.1.2 Third Order State Space Model

To determine the state space model of figures 3-3a and 3-3b we simply apply the same approach as for the second order case. As the compensator is designed based on a current source load we shall focus on the state space model of figure 3-3b. The model for this linear averaged circuit is given by equations 3.10, 3.11 and 3.12.

$$\frac{d}{dt}\widetilde{i_{L_O}}(t) = \frac{-1}{L}\widetilde{v_{C_O}}(t) + \frac{d(t)}{L}V_{IN} \tag{3.10}$$

$$\frac{d}{dt}\widetilde{v_{C_O}}(t) = \frac{1}{C_O}\widetilde{i_{L_O}}(t) - \frac{1}{C_O}\widetilde{i_O}(t) - \frac{1}{R_{Do}C_O}\widetilde{v_{C_O}}(t) + \frac{1}{R_{Do}C_O}\widetilde{v_{C_{D_o}}}(t) \tag{3.11}$$

$$\frac{d}{dt}\widetilde{v_{C_{D_o}}}(t) = \frac{1}{R_{Do}C_{Do}}\widetilde{v_{C_O}}(t) - \frac{1}{R_{Do}C_{Do}}\widetilde{v_{C_{D_o}}}(t) \tag{3.12}$$

3.1.3 Compensator Design

Using the state space model of section 3.1.2 we can derive the transfer function of the plant that relates the duty cycle to the output voltage of the buck converter.

$$G_P(s) = \frac{\widetilde{v}_O(t)}{\widetilde{d}(t)} \tag{3.13}$$

$$G_C(s) = k_P + \frac{1}{s}k_I \tag{3.14}$$

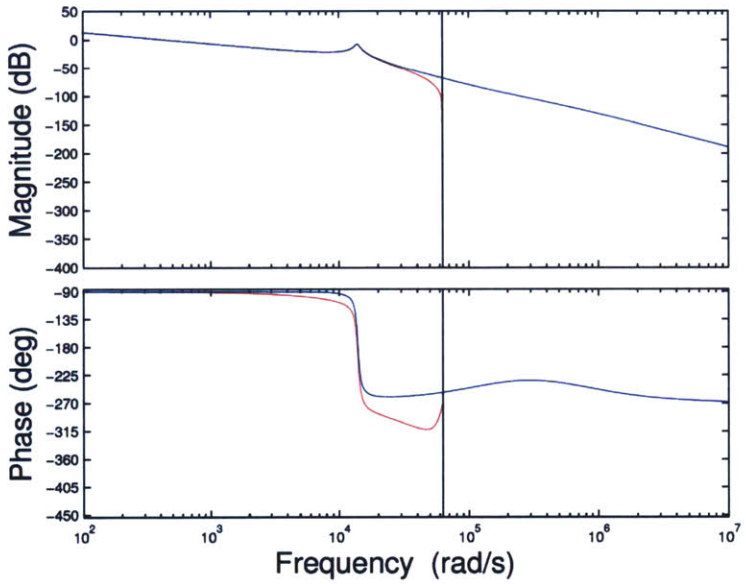


Figure 3-4: Bode Plot of Open-Loop transfer function in CT (blue) DT (red)

The gains k_P and k_I were selected to give a fast response, while keeping the system stable during disturbances. Figure 3-4 provides a comparison between the continuous and discrete time systems. This verifies that a digital controller can perform acceptably and its additional delay is not problematic. The figure illustrates that the chosen gains provide a positive gain margin of 6.7 dB and a positive phase margin of 90°, for both the continuous and discrete systems. This ensures that the error is not amplified if we input a signal at the frequency where the phase is negative 180°.

Chapter 4

Results

4.1 Simulation Results

The third order state space model and compensator are implemented in a closed-loop voltage control configuration. Section 2.2.3 established the need to analyse both resistive loads and a current source load. The response to these loads is shown in figures 4-1 and 4-2 respectively.

Figure 4-1 indicates that the closed-loop response time for a change in resistance is approximately 5 ms. This does not match the 0.335 μs response time of a real solar panel given in section 1.2.2. However, it was concluded in that section that the dynamics of a solar panel would be completely dominated by the power electronics connected to its output. Thus, it is not necessary to achieve such a rapid response and 5 ms is quite acceptable. The output current of the buck converter given by $i_{OUT}(t)$ in figure 4-1 is very steady with an $\Delta i_{OUT}(t)$ of 0.25 A during the step transition.

Figure 4-2 shows how the closed loop system responds to a step change in current, for the case where the circuitry downstream from the buck converter is represented as a current source. The output current step from 5 A to 11.5 A is applied and the corresponding steady state of $v_{OUT}(t)$ lies on the I-V curve of figure 2-6. The plots

illustrate the same 5 ms response time as figure 4-1. The peak-to-peak ripple of the output inductor current of the buck converter indicated by $i_{L_{OUT}}(t)$ is initially 1 A and settles to a value of 4.5 A after the transition. This agrees with figure 2-6 which illustrates how the $D(1-D)$ term of $\Delta i_{L_{OUT}}(t)$ is higher when we operate closer to the 50% range.

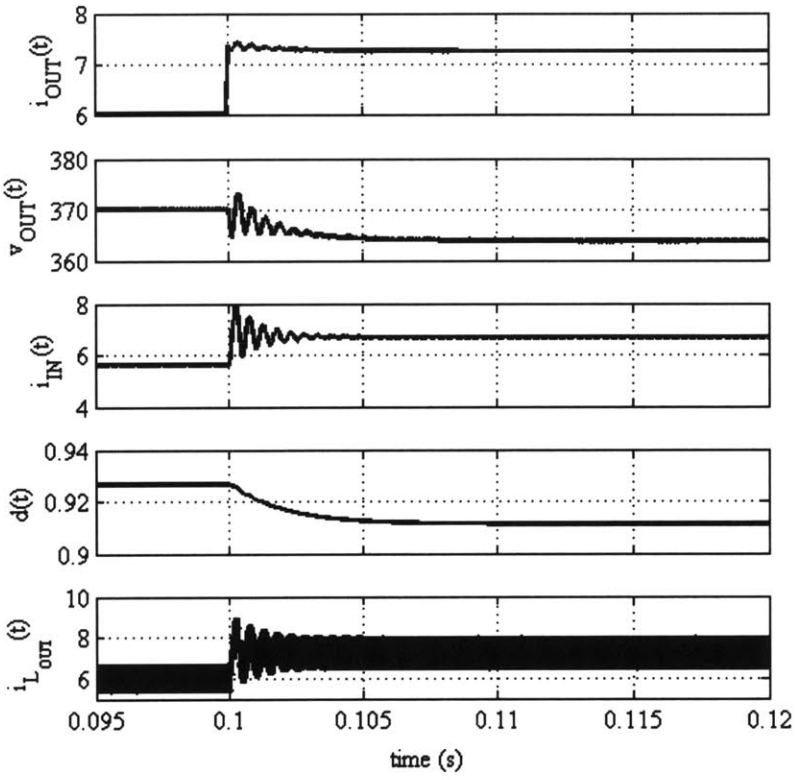


Figure 4-1: Step in output resistance from 19.1 Ω to 50 Ω

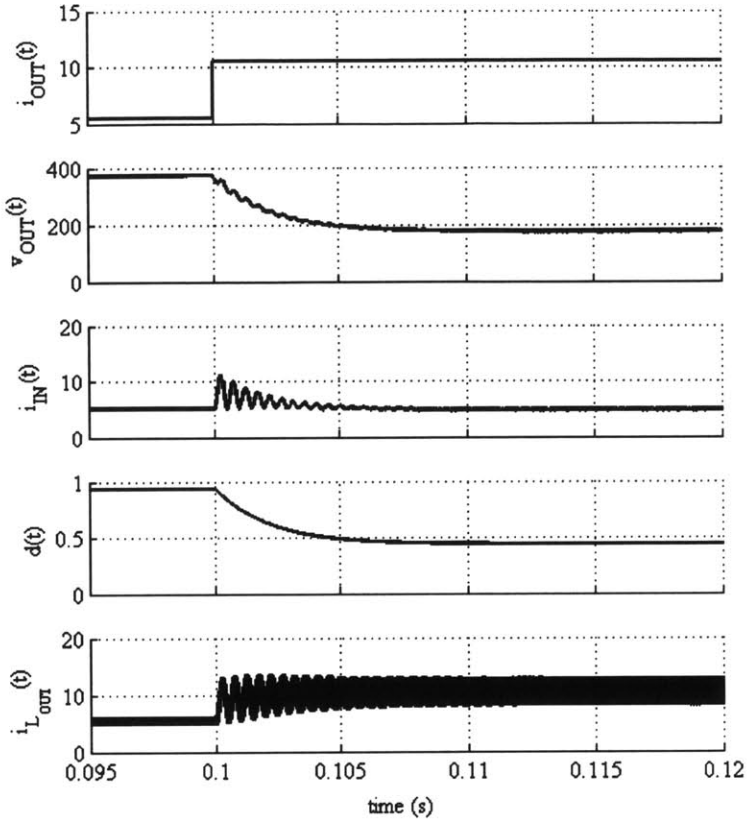


Figure 4-2: Step in output current from 5 A to 11.5 A

4.2 Experimental Results

The experimental setup shown in figure 2-10 was used to conduct open-loop tests. The setup was configured such that the user could input the duty cycle via a potentiometer. The microcontroller was also programmed to apply a step change in the duty cycle. This facilitated measurements of the plant dynamics. The results for a step change in the duty cycle are included in table 4.1. Figure 4-3 shows the waveforms of $v_{OUT}(t)$ and $v_{GS}(t)$. The voltage ripple is quite small and the gate driver is functioning correctly.

Table 4.1: Test Results for duty step from 20% to 80%

Component	Value
V_{IN}	100 V
Rise Time	200 μs
V_{OUT} Overshoot	43.8%
$V_{OUT_{pk}}$	115 V

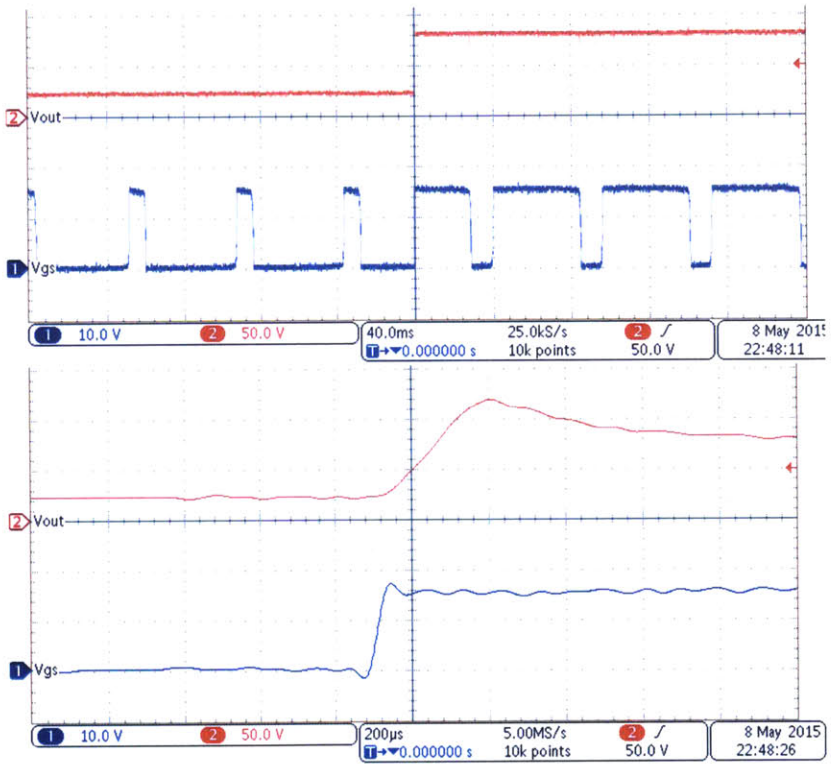


Figure 4-3: $v_{OUT}(t)$ (red) and $v_{GS}(t)$ (blue) for step in duty cycle

4.3 Future Work

The main application of the solar PV emulator is for an experimental microgrid. Some interesting research results may arise from the interaction between the microgrid and the solar emulator. It would be very interesting to explore the effect of varying solar irradiation on the operation of the microgrid. To do this an MPPT circuit that interfaces the solar PV emulator with the inverter will need to be designed and

constructed.

Regarding the solar PV emulator itself, the next stages involves programming various I-V curves. Applying interpolation could provide a means with which to emulate the dynamic characteristics. A comprehensive user interface should be designed using LabVIEW. An ideal GUI would allow the user to specify parameters from the datasheet of a solar PV panel. These quantities could be used to generate I-V curves which are then implemented in the solar emulator. This may present an interesting control challenge if the compensator needs to take account of the I-V operating range by adapting its gains.

Appendix A

MATLAB Code

A.1 Buck Converter and Controller Design

```
%% Buck Converter and Controller Design
% Colm O'Rourke
% July 16th 2014
clc;
close all;
clear all;
%% Figure Specs

bode_title_font=10;
bode_xlabel_font=14;
bode_ylabel_font=14;
fig=1;

%% Defining default Bode Plot Properties
opts=bodeoptions; % Creates plot options handle with default settings
opts.Title.FontSize=16;
opts.XLabel.FontSize=16;
opts.YLabel.FontSize=16;
```

```
opts.XLabel.FontWeight='normal';
opts.YLabel.FontWeight='normal';
opts.FreqUnits='rad/s'; %opts.FreqUnits='Hz';
opts.Grid = 'off'; % Use the form "bode(sys,'k',opts),grid;" to ...
    turn the grid on for a particular graph.

% Set Background of all figures to white.
% Alternatively insert "set(gcf, 'Color', 'w');" after any plot ...
    to make it
% have a white background.
get(0,'Factory')
set(0,'defaultfigurecolor',[1 1 1])
%% Specifications & Paraameters%%

T_simulation = 3e-7; % Tsim=2e-7 is fine for fsw=70kHz; ...
    %Tsim=1e-6 is fine for fsw=20kHz; ie. Tsw/Tsim=50
Tamax = 50; % max ambient temperature

% Duty and switching frequency
D = 0.5;
fsw =   70000;
w_sw     =  2*pi*fsw;

% Diode Specs
vf = 1.6;
Tjmax_D = 150;
Rjc_D = 0.7;

% MOSFET specs
Rdson = 0.045;
trise = 20E-9;
tfall = 10E-9;
Tjmax_Q = 150;
Rjc_Q = 0.29;

% Thermal Pad
```

```
52 Rcs = 0.35;
53
54 % Current Source Load
55 Im = 2; % Im=73/7 = 10.4...
56 impp = 0; % set to zero for DC current
57 w_boost = 0;
58
59 % Resistive Load. Specifying operating point
60 % Rload = 175/38;      % Vm=50;  Im=76/7 = 10.85..
61 % Rload = 1400/73;     % Vm=200; Im=73/7 = 10.4...
62 % Rload = 35;          % Vm=350; Im=10;
63 % Rload = 370/6;       % Vm=370; Im=6;
64 % Rload = 195;         % Vm=390; Im=2;
65
66 % Voltages
67 Vin_min =   400; Vin_max =  400; Vin_maxtr = 550;
68 Vo_max  =   400; Vo_min  =  0;   Vo_mpp   = 350;
69
70 % Currents
71 Io_max  =   11;  Io_min  =  2;   Io_mpp   = 10;
72 Iopp_max = 4; % To Prevent DCM, maximum ripple allowed:IL_pp = ...
       2*Io_min=4A
73
74 % Power
75 Po_min  =   0;   % Check that this can be achieved
76 Po_max  =   3500;
77
78 % Input Filter
79 Rdi = 5; % Damping Resistor
80 Q_db =  3; % 3dB gain at resonance
81 Q = 10^(Q_db/20); % Converting from dB
82 iypp = 150E-3; %input current ripple
83 ni = 3; % Ratio of DC blocking cap to input LPF cap
84
85 % Output Filter: See NOTES 11th & 16th July 2014
```

```
86 RR_ilo_half_duty = 35/73; %RR = 35/73 ----> ilpp≤5A % RR = 28/73 ...
       ----> ilpp≤4A
87 ilo_avg_half_duty = 73/7;
88 RR_vo_half_duty = 1/100; % ie ?% ripple ratio
89 Rdo = 0.5; % Must be less than magnitude of resistance of curve ...
       about MPP
90 no = 3; % Ratio of DC blocking cap to output LPF cap
91
92 %% Calculations %%
93
94 %% Output Filter & Damper: Design and RMS values
95 % Solve for Lo,Co,Rdo,Cdo and their maximum RMS currents
96
97 % Lo & Co
98 % Minimum Inductance for DCM = (Vin_max*D*(1-D))/(fsw*IL_pp)
99 % Note that for Im=2A, D=0.975. ie. D*(1-D) = .024...
100 % This gives Lomin_DCM = 122uH
101 % output cap voltage depends on the inductor ripple current.
102
103 % ilopp & vopp vary with duty cycle(position on solar emulator ...
       i-v curve)
104 % most ripple occurs for D=0.5, as D(1-D) is maximised
105 ilopp_half_duty = RR_ilo_half_duty*ilo_avg_half_duty;
106 vopp_half_duty = RR_vo_half_duty*(Vin_max*0.5);
107
108 Lo_min = ((Vin_max*0.25))/(fsw*ilopp_half_duty);
109 Co_min = ilopp_half_duty/(8*fsw*vopp_half_duty);
110
111 Lo = Lo_min;
112 Co = Co_min;
113
114 % Resonant Frequency
115 wo = 1/sqrt(Lo*Co);
116 fo = wo/(2*pi);
117
118 % Output Damper
```

```
119 Cdo =    no*Co;
120
121 % Bode Plot of output filter: output voltage over input voltage
122 Hout1 = tf(1,[(Lo*Co) (Lo/Rdo) 1]);
123 Hout2 = tf([Rdo*Cdo 1],[Co*Lo*Cdo*Rdo (Co*Lo+Cdo*Lo) (Cdo*Rdo) 1]);
124
125 figure;
126 bode(Hout1,'b',opts);
127 title('Output Filter Bode Plot without Cdo ')
128 set(gcf, 'Position', [100 100 470 370]);
129 export_fig(sprintf('plot%d', fig), '-fig1', '-pdf', '-eps', ...
        '-nocrop'); fig=fig+1;
130
131
132 figure;
133 bode(Hout2,'k',opts);
134 title('Output Filter Bode Plot with Cdo')
135 set(gcf, 'Position', [100 100 470 370]);
136 export_fig(sprintf('plot%d', fig), '-fig1', '-pdf', '-eps', ...
        '-nocrop'); fig=fig+1;
137
138
139 figure;
140 bode(Hout1,'b--',Hout2,'k',opts)
141 title('Output Filter Bode Plot without Cdo (blue) and with Cdo ...
        (black)')
142 set(gcf, 'Position', [100 100 470 370]);
143 export_fig(sprintf('plot%d', fig), '-fig1', '-pdf', '-eps', ...
        '-nocrop'); fig=fig+1;
144
145
146 % Worst Case RMS Calculations
147 % RMS current for Lo
148 iLpp_max   = Vin_maxtr/(4*Lo*fsw);
149 iLpk       =(iLpp_max/2)+Io_max;
150 ILrms_max = sqrt((((iLpp_max/2)/sqrt(3))^2)+((Io_max)^2));
```

```
151
152 % RMS current for Co (we can base this on AC current)
153 iL_AC_pk  = iLpp_max/2;
154 iL_AC_RMS = iL_AC_pk/sqrt(2);
155
156 iCo_AC_RMS = (iL_AC_pk*(sqrt(((Co^2)+((w_sw*Rdo*Co*Cdo)^2))/(((Co ...
       + Cdo)^2)+((w_sw*Rdo*Co*Cdo)^2)))))/(sqrt(2));
157
158 % RMS current for the Damping Resistor and Capacitor
159 iCDo_AC_RMS = sqrt((iL_AC_RMS^2)-(iCo_AC_RMS^2));
160
161 % RMS current for MOSFET
162 IQrms_max = ...
       Io_max*sqrt(0.5)*sqrt(1+((1/3)*(((iLpp_max/2)/Io_max)^2)));
163
164 % RMS current for Diode
165 IDrms_max = ILrms_max; % IDrms_max = sqrt((ILrms^2) - ...
       (IQrms_min^2))..IQrms_min=0
166
167 %% Thermal Model
168 %    [Pq, Pd] = thermal_model(vf, Rdson, trise, tfall, IDrms_max, ...
       IQrms_max, Vo_max, Io_max, fsw);
169
170 [Pq, Pd, Rsa] = thermal_model(vf, Rdson, trise, tfall, IDrms_max, ...
       IQrms_max, Vo_max, Io_max, fsw, Tjmax_Q, Tjmax_D, Rjc_Q, ...
       Rjc_D, Rcs, Tamax);
171
172 %% Input Filter & Damper: Design and RMS values
173 % Solve for Lf,Cf,Rdi,Cdi and their maximum RMS currents
174
175 % Define iypp/ixpp
176 ixpp = Io_max + (iLpp_max/2);
177 iypp_ixpp = iypp/ixpp;
178
179 % Intput Filter
180 % Solve 4th Order Quadratic to determine w0 and hence Lf,Cf, Cdi
```

```
[w0_exacta, w0_exactb, w0_exactc, w0_exactd] = solve_w0(Q, w_sw, ...
    iypp_ixpp);
w0_exact1 = w0_exactc;
Lf_exact = Rdi/(w0_exact1*Q);
Cf_exact = 1/(Lf_exact*(w0_exact1^2));

% Input Damper
Cdi_exact   =   ni*Cf_exact;
w0_exact2 = 1/((Lf_exact*Cdi_exact)^0.5);

% Bode Plot
Hin1 = tf(1,[(1/(w0_exact1^2)) (1/(w0_exact1*Q)) 1]);
Hin2 = tf([Rdi*Cdi_exact 1],[Cf_exact*Lf_exact*Cdi_exact*Rdi ...
    (Cf_exact*Lf_exact+Cdi_exact*Lf_exact) (Cdi_exact*Rdi) 1]);

figure;
bode(Hin1,'b',opts);
title('Input Filter Bode Plot without Cdi ')
set(gcf, 'Position', [100 100 470 370]);
export_fig(sprintf('plot%d', fig), '-fig1', '-pdf', '-eps', ...
    '-nocrop'); fig=fig+1;


figure;
bode(Hin2,'k',opts);
title('Input Filter Bode Plot with Cdi')
set(gcf, 'Position', [100 100 470 370]);
export_fig(sprintf('plot%d', fig), '-fig1', '-pdf', '-eps', ...
    '-nocrop'); fig=fig+1;

figure;
bode(Hin1,'b--',Hin2,'k',opts)
title('Input Filter Bode Plot without Cdi (blue) and with Cdi ...
    (black)')
set(gcf, 'Position', [100 100 470 370]);
```

```
export_fig(sprintf('plot%d', fig), '-fig1', '-pdf', '-eps', ...
    '-nocrop'); fig=fig+1;


Lf = Lf_exact;
Cf = Cf_exact;
Cdi = Cdi_exact;
% figure(7)
% pzmap(Hin1)
% grid on
% title('Input Filter Pole Zero Plot')
%
% figure(8)
% pzmap(Hin2)
% grid on
% title('Input Filter Pole Zero Plot with Cdi')

% % % figure(9)
% % % pzmap(Hin1,'b--',Hin2,'r')
% % % grid on
% % % title('Input Filter Pole Zero Plot without Cdi (blue) and ...
    with Cdi (red)')

%% Define ESR for various components
RLo_ESR = 1E-3; %ESR of Lo
RCo_ESR = 1E-3; %ESR of Co
RCdo_ESR = 1E-3; %ESR of Cdo
Rd = Rdo + RCdo_ESR; %Total resistance of output damping leg


%% State space average (and small signal) model

% sX = A.X + B.I
% y = C.X + E.I

```

```
244 A = [-(RLo_ESR + RCo_ESR*Rd/(Rd + RCo_ESR))/Lo, -Rd/(Lo*(Rd + ...
        RCo_ESR)), -RCo_ESR/(Lo*(Rd + RCo_ESR))
245      Rd/(Co*(Rd + RCo_ESR)), -1/(Co*(Rd + RCo_ESR)), 1/(Co*(Rd + ...
             RCo_ESR))
246      RCo_ESR/(Cdo*(Rd + RCo_ESR)), 1/(Cdo*(Rd + RCo_ESR)), ...
             -1/(Cdo*(Rd + RCo_ESR))];
247
248 B = [Vin_min/Lo, Rd*RCo_ESR/(Lo*(Rd + RCo_ESR))
249      0,   -Rd/(Co*(Rd + RCo_ESR))
250      0,   -RCo_ESR/(Cdo*(Rd + RCo_ESR))];
251 C = [0 1 0];
252 E = [0 0];
253
254 [num,den] = ss2tf(A,B,C,E,1); %'1' corresponds to first input ...
        (which is 'd'. See equation on notes)
255 Gvco_d = tf(num,den);
256
257 [num,den] = ss2tf(A,B,C,E,2);
258 Gvco_im = tf(num,den);
259
260 % figure(2)
261 % step(Gvco_d);
262 %
263
264 figure;
265 bode(Gvco_d,'k',opts),grid;
266 title('Bode Plot of Gvco__d(s)')
267 set(gcf, 'Position', [100 100 470 370]);
268 export_fig(sprintf('plot%d', fig), '-fig1', '-pdf', '-eps', ...
        '-nocrop'); fig=fig+1;
269
270
271
272 %
273 % figure(4)
274 % pzmap(Gvco_d);
```

```
% grid on
%
% figure(5)
% step(Gvco_im);
%
% figure;
% bode(Gvco_im);
%
% figure(6)
% pzmap(Gvco_im);
% grid on


disp(sprintf('Lf = %d H',Lf_exact));
disp(sprintf('Cf = %d F',Cf_exact));
disp(sprintf('Cdi = %d F',Cdi_exact));
disp(sprintf('Rdi = %d Ohms',Rdi));
Hin1
Hin2

disp(sprintf('Lo = %d H',Lo));
disp(sprintf('Co = %d F',Co));
disp(sprintf('Cdo = %d F',Cdo));
disp(sprintf('Rdo = %d Ohms',Rdo));
Hout1
Hout2

%% Write Excel Table

% headings = {'fsw','Lf','Cf','Rdi','Cdi','Lo',' Co', 'Rdo', ...
    'Cdo', 'Rsa'};
% values=[fsw,Lf,Cf,Rdi,Cdi,Lo, Co, Rdo, Cdo, Rsa];
% xlswrite('design_options', headings, '1') % by defualt starts ...
    from A1
% xlswrite('design_options', values, '1','A2') % array under the ...
    header.
```

```
308
309 % values=[fsw,Lf,Cf,Rdi,Cdi,Lo, Co, Rdo, Cdo, Rsa];
310 % xlswrite('design_options', values, '1','A13') % array under the ...
      header.
311
312 %% Control Shtuff
313 load('controller.mat');
314 open_loop = controller*Gvco_d;
315 closed_loop = (controller*Gvco_d)/(1+controller*Gvco_d);
316
317 figure;
318 bode(open_loop,'k',opts),grid;
319 title('Bode Plot of open loop transfer function')
320 set(gcf, 'Position', [100 100 470 370]);
321 export_fig(sprintf('plot%d', fig), '-fig1', '-pdf', '-eps', ...
      '-nocrop'); fig=fig+1;
322
323
324 figure;
325 step(open_loop);
326 title('Step response of open loop transfer function')
327 set(gcf, 'Position', [100 100 470 370]);
328 export_fig(sprintf('plot%d', fig), '-fig1', '-pdf', '-eps', ...
      '-nocrop'); fig=fig+1;
329
330
331 figure;
332 step(closed_loop);
333 title('Step response of closed loop transfer function')
334 set(gcf, 'Position', [100 100 470 370]);
335 export_fig(sprintf('plot%d', fig), '-fig1', '-pdf', '-eps', ...
      '-nocrop'); fig=fig+1;
336
337 Ts=1/20000; % set ADC sampling frequency to 20kHz
338
339 %convert controller and plant to z-domain
```

```
340 cz = c2d(controller,Ts,'tustin');
341 Gz = c2d(Gvco_d,Ts,'zoh');
342
343 figure;
344 bode(cz*Gz,'r',open_loop,'b',opts);
345 title('Bode Plot of open loop transfer function in CT (blue) DT ...
      (red)')
346 set(gcf, 'Position', [100 100 470 370]);
347 export_fig(sprintf('plot%d', fig), '-fig1', '-pdf', '-eps', ...
      '-nocrop'); fig=fig+1;
```

A.2 Thermal Design

```
1  function [Pq, Pd, Rsa] = thermal_model(vf, Rdson, trise, tfall, ...
       IDrms_max, IQrms_max, Vo_max, Io_max, fsw, Tjmax_Q, Tjmax_D, ...
       Rjc_Q, Rjc_D, Rcs, Tamax)
2
3  % July 31st 2014
4  % Colm O'Rourke
5
6  % Description: function to solve for conduction and switching ...
       losses in
7  % the FET & Diode. Also op/s heat sink requirements
8
9  %% Conduction Losses
10 Pq_cond = (IQrms_max^2)*Rdson;
11 Pd_cond = IDrms_max*vf;
12
13 %% Switching Losses
14 ton = 2*trise;
15 toff = 2*tfall;
16 Pq_sw = 0.5*Vo_max*Io_max*(ton+toff)*fsw;
17 Pd_sw = 0;
```

```
18
19 %% Total FET & Diode Losses
20 Pq = Pq_cond +Pq_sw;
21 Pd = Pd_cond + Pd_sw;
22
23 %% Heat Sink requirements
24
25 Rsa_Q = (Tjmax_Q - Tamax - Pq*(Rjc_Q + Rcs))/(Pq+Pd);
26 Rsa_D = (Tjmax_D - Tamax - Pd*(Rjc_D + Rcs))/(Pq+Pd);
27 Rsa= min(Rsa_Q, Rsa_D);
```

A.3 Input Filter Solver

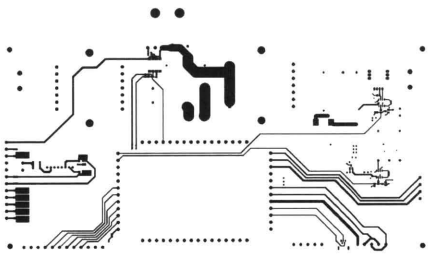
```
1 function [w0_exacta, w0_exactb, w0_exactc, w0_exactd] = ...
      solve_w0(Q, w_sw, iypp_ixpp)
2 % July 1st 2014
3 % Solving 4th order polynomial
4 % Description: function to solve w0
5 a = (iypp_ixpp^2)-1;
6 b = (((iypp_ixpp^2)*(w_sw^2))/(Q^2)) -(2*(iypp_ixpp^2)*(w_sw^2));
7 c = (iypp_ixpp^2)*(w_sw^4);
8 x1 = (-1)*b + ((b^2)-(4*a*c))^0.5; x1 = x1/(2*a);
9 x2 = (-1)*b - ((b^2)-(4*a*c))^0.5; x2 = x2/(2*a);
10 w0_exacta = x1^0.5;
11 w0_exactb = -1*w0_exacta;
12 w0_exactc = x2^0.5;
13 w0_exactd = -1*w0_exactc;
```

Appendix B

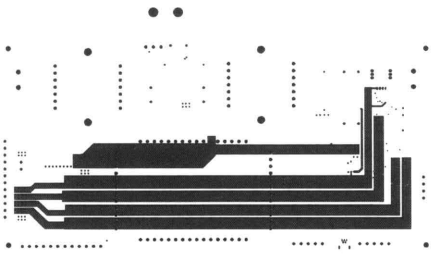
Figures

B.1 Solar Emulator: Buck Converter

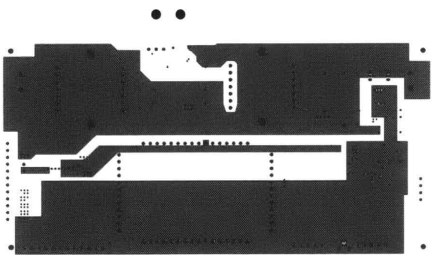
B.1.1 Solar Emulator PCB



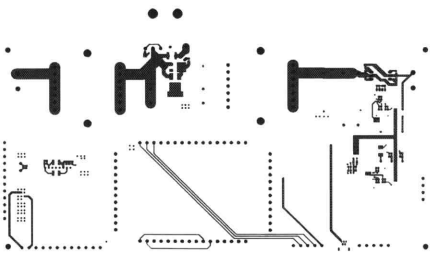
(a) Layer 1: Top Signal Layer



(b) Layer 2: Power Planes

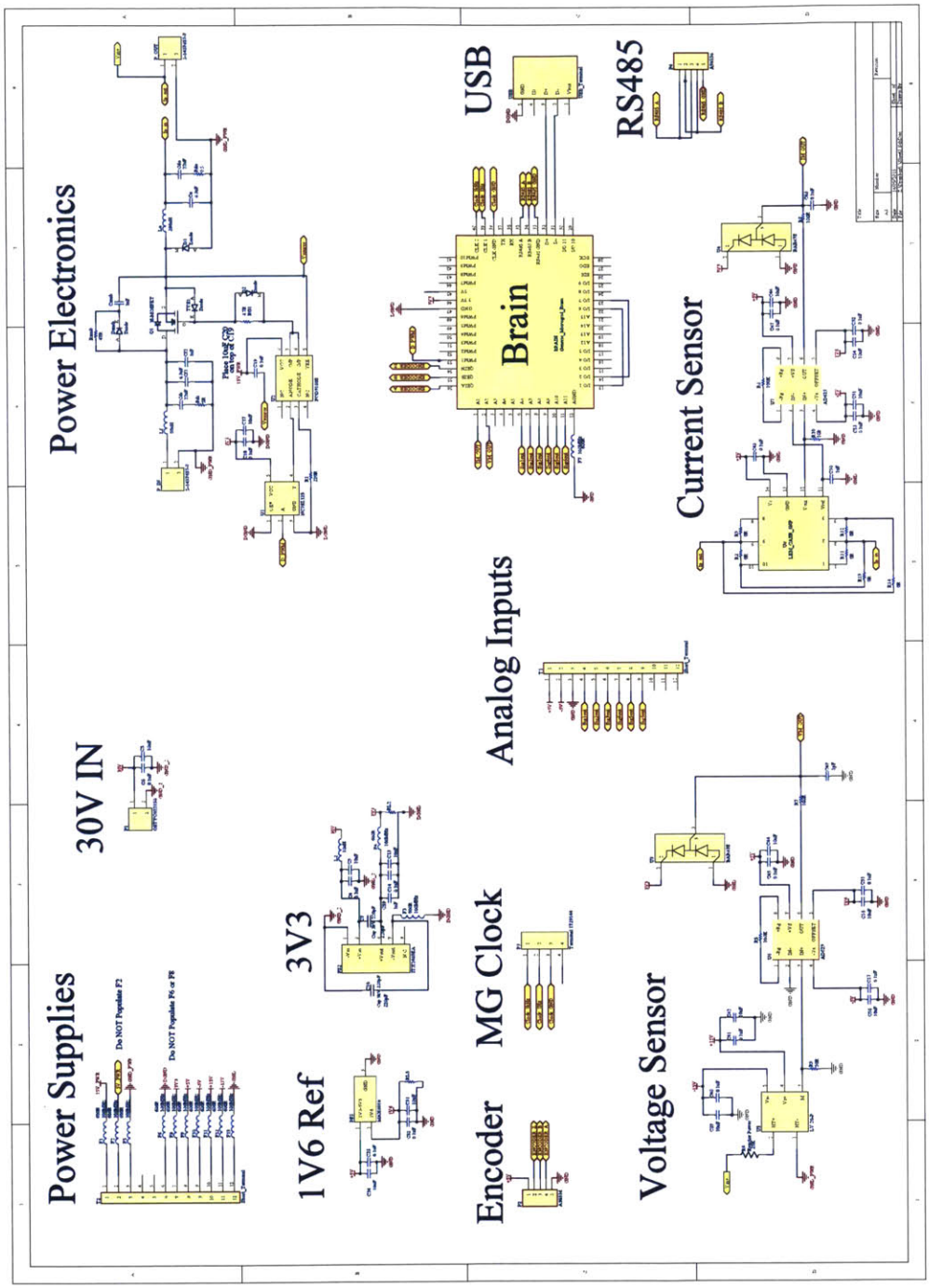


(c) Layer 3: Ground Planes



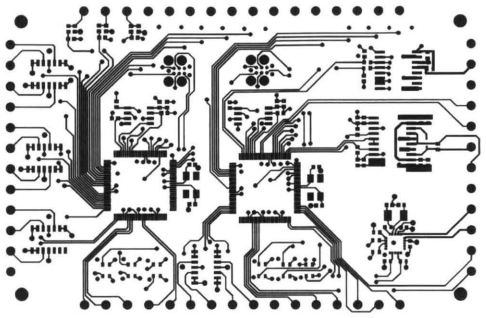
(d) Layer 4: Bottom Signal Layer

B.1.2 Solar Emulator Schematic

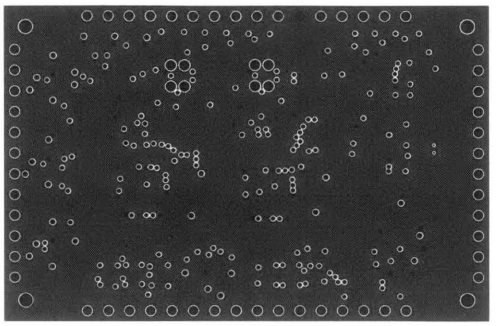


B.2 Generic Controller

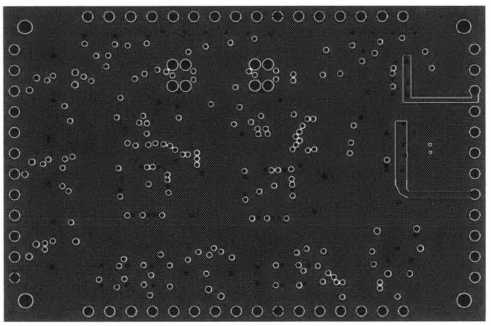
B.2.1 Generic Controller PCB



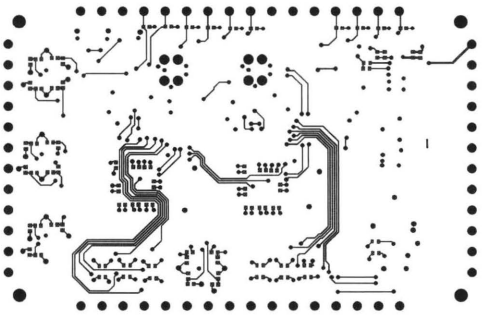
(a) Layer 1: Top Signal Layer



(b) Layer 2: Power Plane

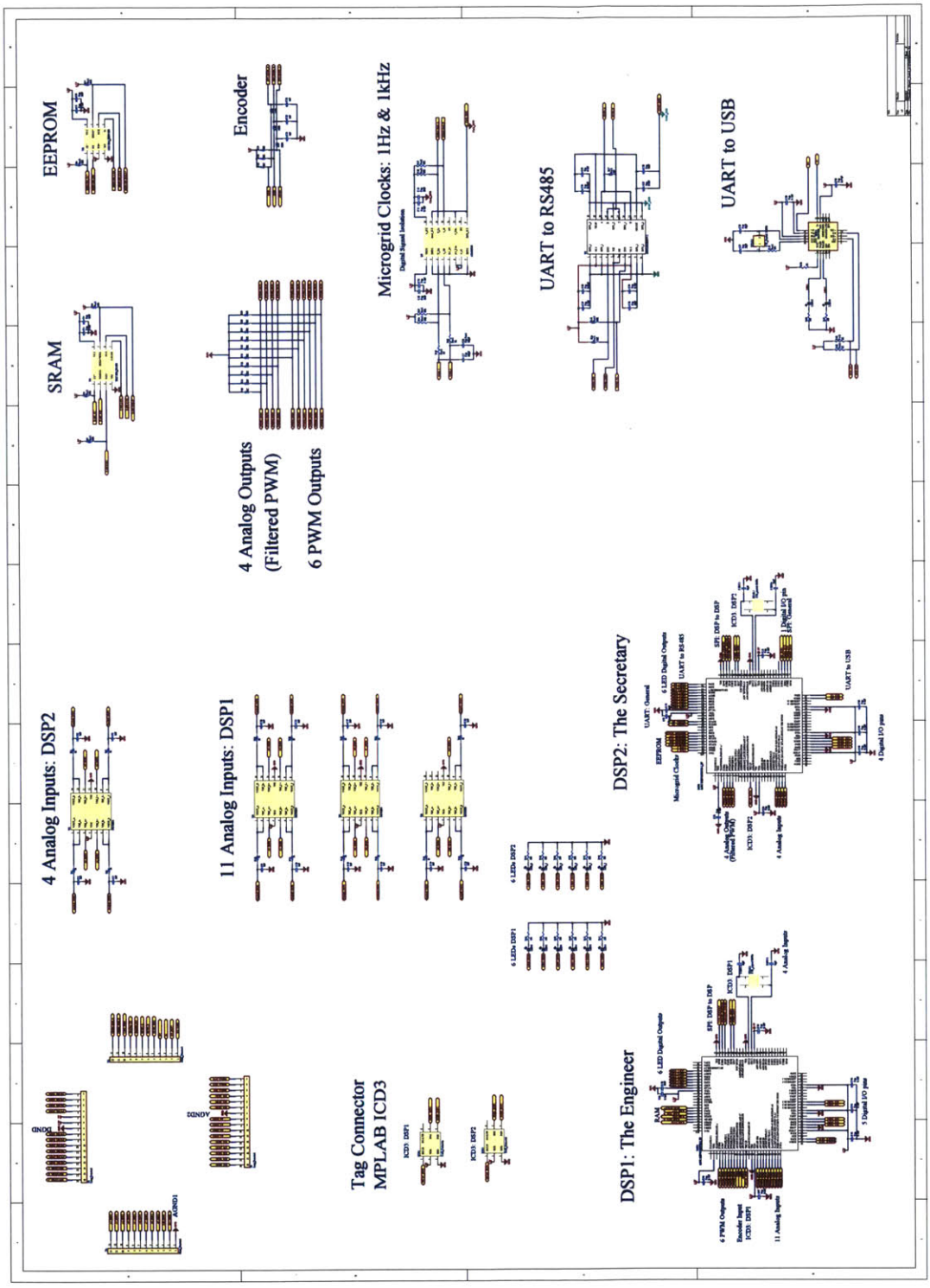


(c) Layer 3: Ground Plane



(d) Layer 4: Bottom Signal Layer

B.2.2 Generic Controller Schematic



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