Fundamental Limits of the Switching Abruptness of Tunneling Transistors

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Abstract

The tunneling field-effect transistor (TFET) is one of the most promising candidates for future low-power electronics because of its potential to achieve a subthreshold swing less than the 60 mV/decade thermal limit at room temperature. It can surpass this limit because the turn-on of tunneling does not sample the Maxwell-Boltzmann distribution of carriers that gives rise to the 60 mV/decade limit in conventional devices. However, theoretical predictions and experimental measurements of TFET device characteristics have differed by a wide margin—experimental subthreshold characteristics have not achieved the switching steepness (i.e., the change in drain current with applied gate voltage) of theoretical simulations. Non-ideal effects, such as non-abrupt band edges, phonon-assisted tunneling, and trap states, are discussed as mechanisms that may degrade theoretical predications.

A strained-Si/strained-Ge bilayer TFET is used as a test-bed device to better understand the discrepancy between simulation and experiment. The bilayer TFET studied in this work eliminates channel doping and uses the strained-Si/strained-Ge heterostructure. Band-to-band tunneling occurs perpendicular to the gate, in-line with the gate electric field. Multiple gates are used so that the impact of the directionality of tunneling on switching abruptness can be studied.

The band alignment of the strained-Si/strained-Ge heterostructure is extracted from a MOS-capacitor structure though an experimental quasistatic CV technique. The extracted effective band gap (related to the tunneling barrier) is shown to be only ~200 meV for the heterostructure, and the valence band offset is shown to be ~100 meV larger than predicted by density-functional theory. New deformation potentials are suggested for the Si-Ge material system based on the experimentally extracted band alignments.

The impact of quantization on the turn-on voltage and gate-leakage current in a thin-body bilayer TFET structure is studied, and large confinement energy is shown to be especially problematic at body thicknesses less than 10 nm. An InAs structure with a body thickness less than 7 nm is shown to require a larger turn-on voltage than either Si or Ge homostructures due to the very light electron mass in InAs that leads to a large confinement energy. The strained-Si/strained-Ge heterostructure is shown to dramatically reduce the turn-on voltage due to its small effective band gap. Quantization is shown to limit the gate efficiency since increasing the body voltage, in order to align the electron and hole eigenstates in energy, increases the electric field across the structure, which in turn increases quantization. Gate leakage current increases exponentially as the body thickness decreases because the body voltage (and hence, the electric field) at turn-on increases with decreasing body thickness and gate leakage is exponentially dependent on the electric field.

Non-ideal two-dimensional effects are investigated as mechanisms that degrade the switching characteristics of perpendicular TFETs (i.e. devices with tunneling perpendicular to the gate). Abrupt termination of a heavily doped semiconductor layer, often present in perpendicular TFET structures, can lead to large in-plane electric fields that give rise to parasitic diagonal tunneling paths, as opposed to the desired perpendicular tunneling paths. While the turn-on of each leakage path may be individually sharp, the sum of all tunneling paths is smeared by the multiple turn-ons and results in a degraded transfer characteristic for the device. The characteristic length, used for determining the length scale of potential fluctuations in short-channel MOSFETs, is suggested as a parameter that can be used to evaluate the likelihood of parasitic tunneling paths in a perpendicular TFET structure.

The fabrication of the 3Gate strained-Si/strained-Ge bilayer TFET is detailed. The process includes epitaxial growth of a highly strained heterostructure, planarization of a bottom gate, wafer bonding of an epitaxial wafer to a handle wafer, etch-back of the epitaxial wafer leaving the thin strained-Si/strained-Ge heterostructure, and standard processing to create devices.

Future work on electrical characterization of the experimental 3Gate bilayer TFET is discussed. Several test configurations are suggested as a way to probe the effects of diagonal tunneling on the abruptness of the switching characteristics.

Thesis Supervisors: Judy L. Hoyt, Professor of Electrical Engineering
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To my family and my love, Christy

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Table 4.1. Semiconductor material properties used in calculations. The effective mass is calculated along $\mathbf{100}$ for the lowest energy (heaviest) eigenstate. Subscripts $\boldsymbol{l}$, $\boldsymbol{t}$, $\boldsymbol{\Gamma}$, and $\boldsymbol{hh}$ denote longitudinal, transverse, gamma-point, and heavy-hole masses, respectively. The relative permittivity is given by $\boldsymbol{\epsilon_r}$. 68

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Chapter 1: Background on Tunneling Transistors

The great pace of the electronics industry can be attributed to the successful scaling of silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) from one technology generation (node) to the next since the 1970s; however, beginning in the early 2000s, additional enhancement techniques beyond feature size reduction were required to push to the next technology node. Some technologies for transistor improvement were strain engineering of the channel [1] and new materials, such as high-κ dielectrics and metal gates [2]. Yet even with these technological boosters, scaling of the oxide thickness and supply voltage have slowed (beginning around 2005) compared to constant-field scaling theory proposed by Dennard [3]. The net result is that power density of microprocessors has dramatically increased in the past decade [4] and in response, switching frequency and die area have stabilized to control total power usage (see Figure 1.1). To enable greater mobility and increased energy efficiency, one of the foremost goals of the nanoelectronics industry is to reduce power while maintaining performance. The aim of tunneling field-effect transistors (TFETs) is to meet these goals.

TFETs have created excitement for their potential to overcome the fundamental limit for turn-on steepness, as discussed later, enabling lower power electronics. In the following sections, the TFET structure is introduced, and motivation for its potential for low power electronics is presented. Next, promises and shortcomings of current TFET results are discussed, followed by an overview of the different types of TFETs currently being pursued in the field of research. The chapter ends with discussion of non-ideal effects in TFETs and the overview of this work.

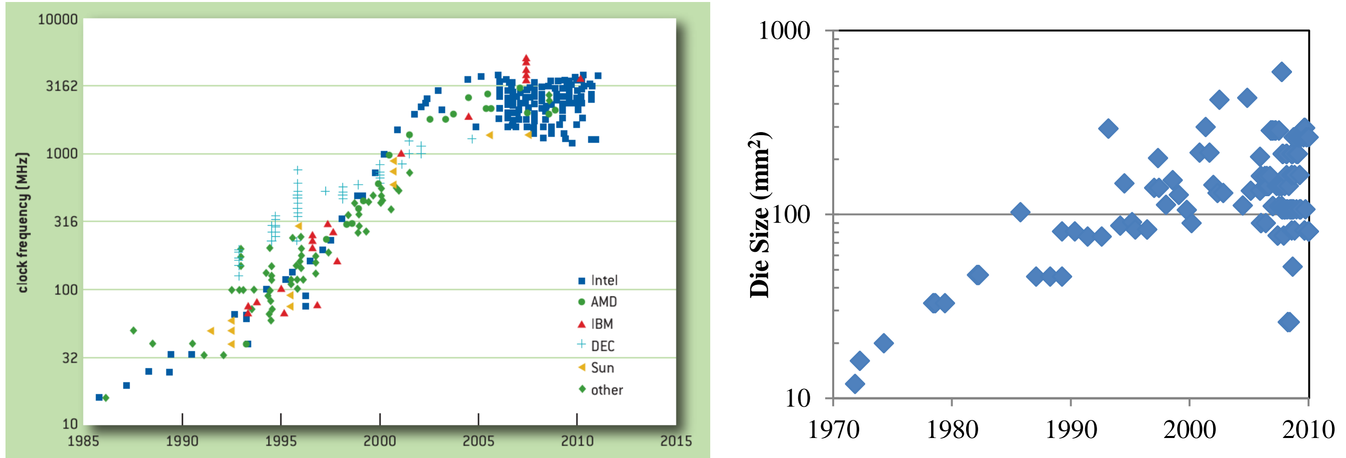

Figure 1.1. (left) Processor clock frequency as a function of time for different manufacturers [5]. (right) Die size of Intel processors as a function of time [5].

1.1 How a TFET Works

At the core of a TFET is a gated *p-i-n* diode. A Si homojunction TFET with a *p*-type source, intrinsic channel, and *n*-type drain is illustrated in Figure 1.2b. The gate modulates the channel potential, which in turn modulates the tunneling barrier between the source and channel. Additionally, the channel potential controls the availability of channel states to which electrons from the source can tunnel into. The TFET seeks to use tunneling as an advantageous effect, where carriers are injected through a barrier instead of thermal excitation over a barrier, as in a traditional MOSFET.

The biasing scheme for an *n*-TFET is similar to that of an *n*-MOSFET. The device would normally be biased such that the source is grounded and a positive potential is applied to the drain $(+V_{ds})$. The off-state occurs when the gate is biased such that the conduction band (CB) of the channel is higher in energy than the valence band (VB) of the source, shown in Figure 1.2d. Ideally, no band-to-band tunneling (BTBT) can occur due to the misalignment of the bands in energy, and I_{off} is small and set by the reverse-bias *pn* junction leakage.

The main advantage of an ideal TFET is that very little current (only the reverse-bias *pn* junction saturation current) flows until the energy bands align such that BTBT of electrons from the source VB to the channel CB can occur. Ideally, tunneling cannot occur before the bands align in energy because there are no states for an electron to tunnel into. The CB of the channel and the

VB of the source will overlap in energy once a sufficiently positive gate bias is applied, which is called the on-state. In this state, electrons in the VB of *p*-type source tunnel through the band gap to an unoccupied state in the CB of the channel. The electrons are then swept into the *n*-type drain by a small positive drain bias. Just as in an *n*-MOSFET, the drain is merely a collector of the electrons that make it from the source into the channel. Once the bands align, a BTBT current begins to flow.

Ideally, the transition from the off- to on-state occurs abruptly once the source VB and channel CB align in energy, yielding favorable transistor characteristics. Non-idealities cause a more gradual increase in drain current with gate voltage at a rate given by the subthreshold swing, discussed in the following sections.

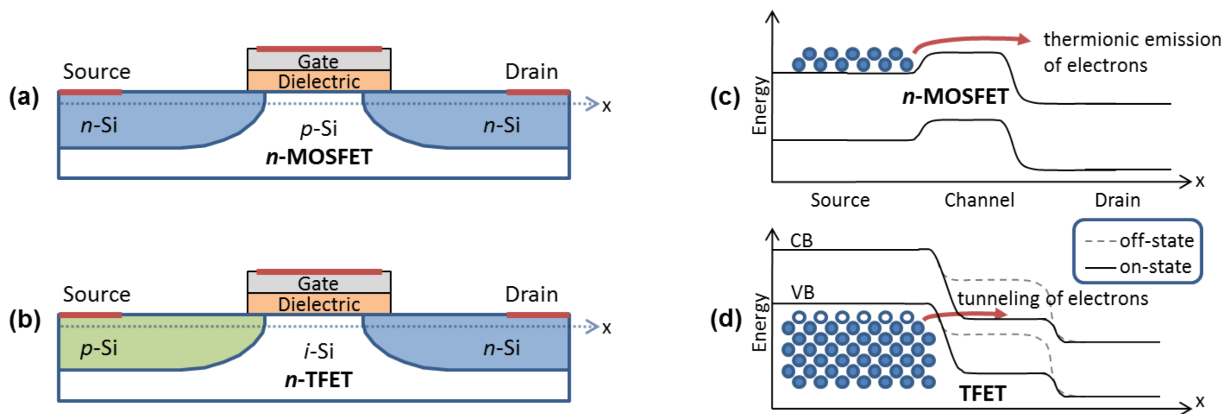

Figure 1.2. (a) *n*-MOSFET structure. (b) *n*-TFET structure. The TFET has non-symmetric source and drain doping. (c) Energy band diagram for the MOSFET. Current is carried by thermionic emission of electrons over a potential barrier. (d) Energy band diagram for the TFET. On-state current is carried by band-to-band tunneling of electrons from the source to the channel. In both devices, the gate voltage modulates the channel potential. In a MOSFET, the channel potential controls the number of carriers from the source that can make it over the channel barrier. In a TFET, the channel potential controls the width of the tunneling barrier and the availability of channel states to which electrons from the source can tunnel into.

1.2 Motivation for TFETs, Improved Power Scaling

Practical limits exist for reducing power consumption of MOSFETs. Total power consumption is given by the sum of switching and leakage power:

$$P_{switch} = \alpha C V_{dd}^2 f$$
$$P_{leakage} = I_{off} V_{dd} + I_G V_{dd} \tag{1.1}$$

α is the switching activity or fraction of clock cycles that device switches, C is the total gate capacitance including parasitics, V_{dd} is the supply voltage, f is the switching frequency, I_{off} is the off-state source-to-drain leakage current, and I_G is the gate leakage current.

The equations above suggest reducing V_{dd} in order to reduce both switching and leakage power, yet they obscure the relationship between I_{off} and V_{dd}. The threshold voltage (V_t) of a MOSFET must be decreased in-step with V_{dd} in order to maintain the on-current density (and therefore maintain performance improvements). Decreasing V_t exponentially increases I_{off} through the equation

$$I_{off}^f = I_{off}^i \exp\left(-\frac{q \cdot \Delta V_t}{nkT}\right) \tag{1.2}$$

where I_{off}^i $\left(I_{off}^f\right)$ is the initial (final) off-state leakage current, q is the elementary charge, ΔV_t is the change in threshold voltage, n is the ideality factor of the subthreshold slope, and kT is the thermal energy. Thus, continual reduction of V_{dd} (and hence V_t) will eventually increase power dissipation since leakage power increases exponentially with decreasing V_t. In fact, leakage power in modern devices is comparable to switching power, so V_t and V_{dd} scaling has dramatically slowed [5] as shown in Figure 1.3. Additionally, increasing I_{off} also decreases the on-/off-current ratio which creates additional complexity for robust circuit design. Given these problems, a new type of switching mechanism is required to allow for continued voltage and power scaling.

Unlike a MOSFET, the off-state current of a TFET is limited by reverse-bias *pn* junction leakage current, and the on-state is governed by BTBT. For such a device, power savings may be achieved by engineering a steep subthreshold swing (explained in the following section), enabling V_{dd} scaling without increased off-current.

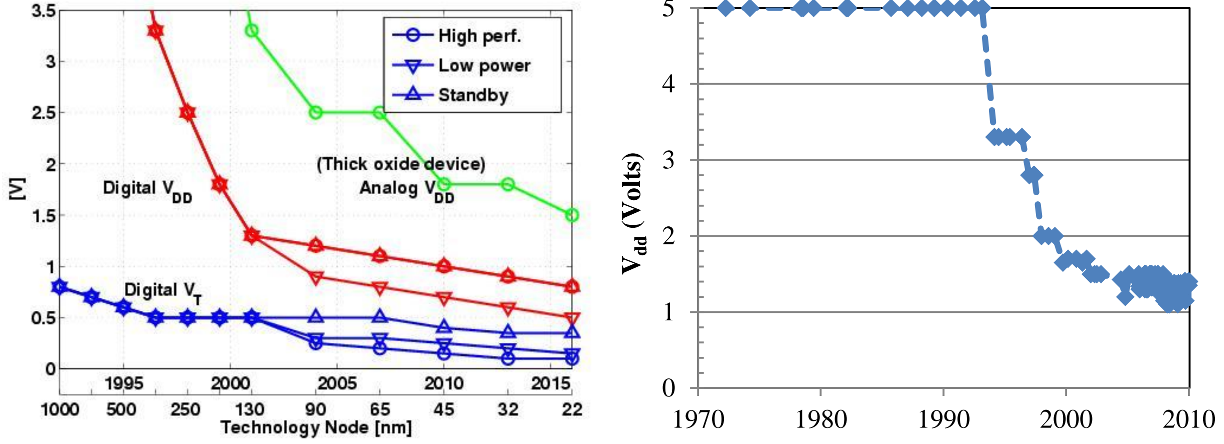

Figure 1.3. (left) Power supply voltage (V_{dd}) and threshold voltage (V_t) scaling as a function of time [6]. (right) V_{dd} scaling of Intel processors from 1970 to 2010 [5].

1.2.1 Subthreshold Swing

The subthreshold swing (SS) of a transistor, given by the change in gate-to-source voltage required to increase the source-to-drain current by ten-fold, is highlighted in the transfer characteristics of Figure 1.4. In the following analysis, it is assumed that the absolute voltage of the transfer characteristics can be shifted by an arbitrary constant through work function engineering of the metal gate. V_{dd} can be thought of as setting a voltage window over which to sample the transfer characteristics. The window can be shifted to the right for high performance devices (higher I_{on}) or to the left for low-power devices (lower I_{off}). Shrinking the window size (i.e. V_{dd}) without any other process enhancements results in decreased I_{on}, increased I_{off}, or both.

A reduced SS would permit a lower V_{dd} without compromising the on- or off-state. Consequently, total power dissipation could be greatly reduced. Yet, a fundamental limit exists for the minimum SS of MOSFETs: $\frac{kT}{q}\ln(10) = 60$ mV/decade at room temperature. This limit arises due to thermionic transport over the energy barrier of the MOSFET channel region. For the case of electrons, the carrier distribution in the source of a MOSFET has a Maxwellian distribution in energy $\left[n(E) \propto \exp\left(-\frac{E-E_f}{kT}\right)\right]$ shown in Figure 1.5. Every additional 60 mV rise of the channel potential blocks an additional range of carriers in the source's thermal tail which reduces leakage current by ten-times.

Conversely, in a TFET, the off-state current is limited by leakage current across a reverse-biased *pn* junction, which has very weak dependence on gate voltage. The device does not turn on until the CB of the channel is overlapped in energy with the VB of the source. Because the off-state current has a weak voltage dependence, and the on-state occurs suddenly once the bands are overlapped, TFETs are not restricted to the 60 mV/decade limit of conventional devices.

TFETs may allow for markedly steeper SS due to their tunneling-based switching, but non-idealities may severely degrade the expected characteristics. Very few experimental devices have achieved a SS below the thermal limit, and those that have are plagued by other problems, especially very low on-state current. In particular, effects such as non-abrupt band-edges, tunneling to trap states, and inefficient gate control of the channel of TFETs must be controlled in order to realize a steep subthreshold swing over several decades of drain current. They are discussed in greater detail in §1.5.

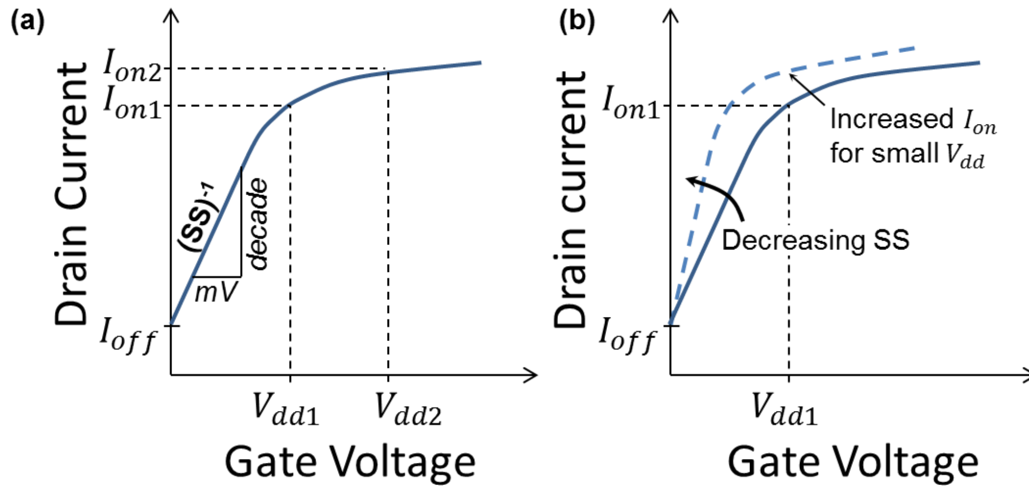

Figure 1.4. (a) Transfer characteristics highlighting the subthreshold swing (SS). Decreasing the supply voltage (V_{dd}) results in a decrease of on-current for a constant off-current (I_{off}). (b) Decreasing the SS allows for increased on-current for small V_{dd}.

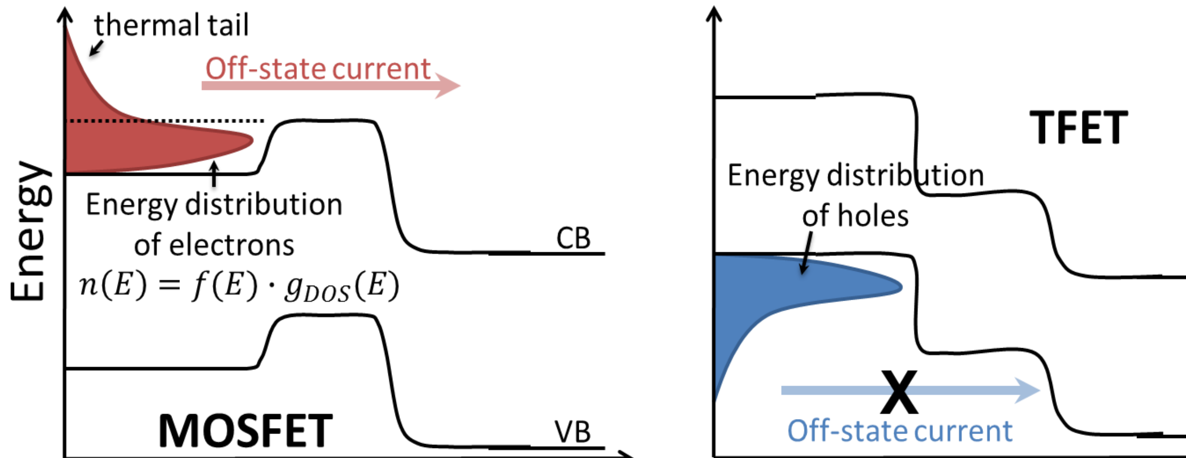

Figure 1.5. (left) Depiction of the thermal tail of electrons in the source of a MOSFET. The tail limits the SS of thermionic devices, such as MOSFETs, to 60 mV/decade at room temperature. (right) Depiction of bands and thermal tail of holes in the source of a TFET. The off-state current is blocked by the reverse-biased *pn* junction.

1.3 Promises and Shortcomings of TFETs

Several TFET properties make them attractive for future CMOS applications. A significant world-wide research effort is underway to demonstrate devices with steep switching over several decades of drain current. Unfortunately, experimental devices have not shown the ideal behavior predicted by simulations, often showing poor SS, poor on-current, or both. The following subsections detail the benefits of ideal TFETs and the shortcomings of experimental TFET results.

1.3.1 Benefits of Proposed TFETs

First, the design of a parallel TFET (shown in Figure 1.2) is very similar to a conventional MOSFET. A parallel TFET has tunneling parallel to the gate and is described in detail in §1.4.1. If such a TFET with superior characteristics (especially one made from group IV elements) was demonstrated, its introduction into high volume processing could likely occur in a relatively short time frame using standard processes. As has been common for the past decade, the 5 to 10 year future roadmap for continued transistor scaling looks bleak, and the introduction of the TFET at that time is appealing from an engineering prospective due to the compatibility and leverage of existing infrastructure.

Second, as transistor channel lengths are scaled to ever smaller dimensions, source-to-drain intra-band tunneling and gate-induced drain leakage (GIDL) become problematic by increasing the off-state leakage current of MOSFETs. For an *n*-MOSFET, source-to-drain intra-band tunneling is the tunneling of source CB electrons through the channel barrier to the CB of the drain, and GIDL is the band-to-band tunneling of VB electrons from the channel to the CB of the drain. Tunneling at small length scales is inevitable. It exists in MOSFETs as a parasitic phenomenon that degrades device performance. The idea to engineer tunneling into a desirable effect for highly scaled devices is alluring. In this way, the undesirable tunneling-induced degradation hampering conventional devices would be utilized for steep switching in future TFETs.

Third, many *simulations* have predicted incredible TFET device performance in a variety of material systems and device geometries and configurations [7]. Often, the simulations show super-steep SS, low off-current, and high on-current. For example, Figure 1.6 shows simulations of a specific bilayer TFET (described in detail in Chapter 2: *Introduction to the Bilayer TFET*) with a nearly perfect SS of ~0 mV/decade at the turn-on voltage [8]. Simulations of a range of TFETs made from different materials and architectures are shown in Figure 1.8. These simulations have encouraged many that great switching performance can be attained if only they can make an ideal device.

Fourth, TFETs have the best predicted performance among other beyond-CMOS devices. A 2013 benchmarking study by Intel's Nikonov and Young shows that the predicted energy-delay product of TFETs significantly outperforms other emerging technologies based on spintronics [9].[*] A plot of the energy-delay product for a 32-bit adder for different beyond CMOS devices is shown in Figure 1.7.

For the combination of the reasons described above, TFETs currently look to be the best, if not only, candidate with potential to beat MOSFETs in low-power digital logic applications at moderate speeds.[†]

[*] To be fair, the energy-delay product figure-of-merit does not capture other advantages of spintronic devices including non-volatility and reconfigurability.

[†] Nano-electro-mechanical relays have also shown promise [10], but doubt remains concerning their scaling ability, switching speed, and longevity.

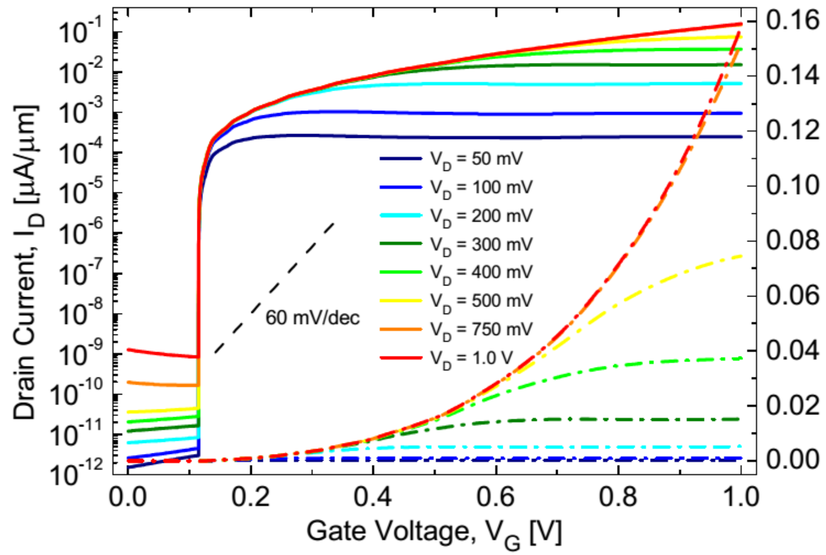

Figure 1.6. Simulated I_D-V_G as a function of V_D in linear (dashed) and logarithmic (solid) scales for a Si bilayer TFET. The simulations show a nearly perfect SS of ~0 mV/decade around V_G = 0.1 V. Reproduced from [8].

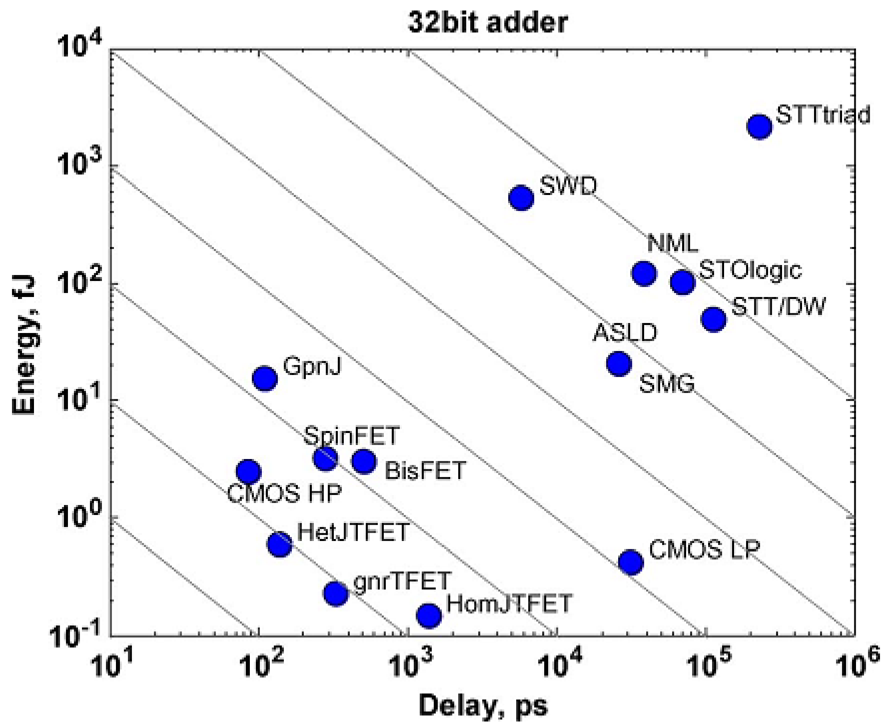

Figure 1.7. Benchmarking of energy versus delay of 32-bit adders made from different beyond-CMOS device architectures. The results show that TFETs have a favorable energy-delay product compared to other emerging architectures. Reproduced from [9]. HetJTFET—heterojunction TFET; HomJTFET—homojunction TFET; gnrTFET—graphene nanoribbon TFET.

1.3.2 Shortcomings of Today's Experimental TFETs

Overall, experimental TFET measurements have not mirrored idealized simulation results. Figure 1.8 and Figure 1.9 show the sharp contrast between simulations and experimental results. Few experimental TFETs have shown SS less than the thermal limit (see Figure 1.9), and those that have only show steep SS for less than four decades of drain current [11]–[15]. This behavior is in contrast to well-designed scaled MOSFETs, which show a 65 mV/decade SS for over five decades of drain current [16].

Additionally, experimental TFETs have only shown steep SS for low current densities less than 10 nA/µm [17]. They have not been able to show both high drive current and steep SS. Compare for example, the steep SS of 40 mV/decade with low on-current of 10 nA/µm in [18] with the high on-current of 700 µA/µm but with horrible SS of 375 mV/decade in [19]. Currently

no published experimental TFET device has shown switching behavior comparable to that of existing MOSFETs despite intensive research over more than a decade.

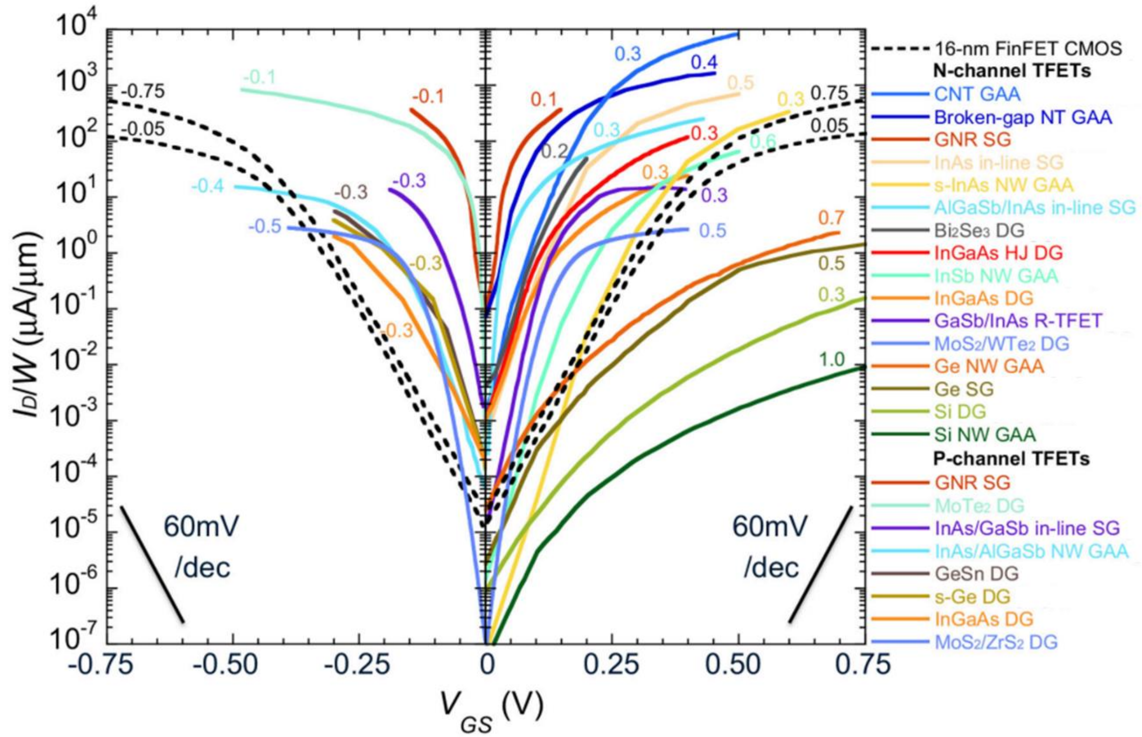

Figure 1.8. Comparison of *simulated* TFET transfer characteristics. The numbers on the curves indicate V_{DS}. The majority of the results predict steep SS and high on-current for a variety of materials and device architectures. Compare with the experimental TFET results in Figure 1.9. Reproduced from [17].

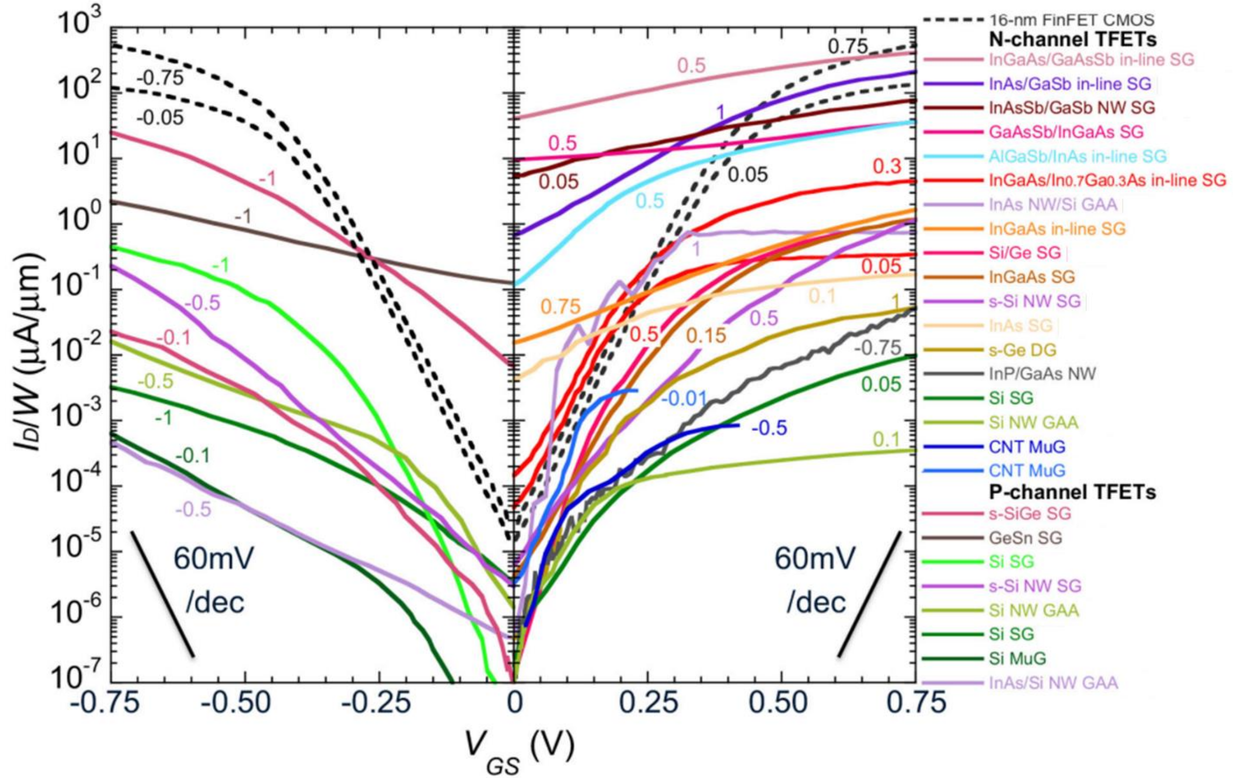

Figure 1.9. Comparison of *experimental* TFET transfer characteristics. The numbers on the curves indicate V_{DS}. Experimental TFET results significantly trail the low-power MOSFET transfer characteristics for 16-nm FinFETs indicated with dashed lines [16]. Reproduced from [17].

1.4 Types of TFETs

TFET structures can be divided into several categories depending on device geometry, material, and doping. This section details the different TFET structure parameters that are currently being investigated by the research community.

1.4.1 Parallel and Perpendicular Structures

TFET structures can be fabricated with either a parallel or perpendicular geometry, shown in Figure 1.10. In a parallel geometry (sometimes called a *point* TFET), tunneling occurs parallel to the gate. In a perpendicular geometry (sometimes called a *line* or *in-line* TFET), tunneling occurs perpendicular to the gate.

Parallel TFETs benefit from their similarity to conventional MOSFET structures. The device structure can be scaled as tunneling current does not significantly depend on the gate length. Many

of the best experimental devices have used a parallel structure with either a lateral or vertical device geometry [11]–[15], but these devices often exhibit low on-current because tunneling occurs only over a small area and there is difficultly achieving a high field between the source and the channel.

Conversely, perpendicular TFETs are difficult to fabricate as they require non-uniform doping in both lateral and vertical dimensions. For well-behaved devices, the tunneling current is proportional to the gate area, which limits their scaling ability. However, the perpendicular structure employs tunneling *in-line* with the gate field, which can enhance tunneling efficiency since tunneling probability is exponentially dependent on the electric field in the tunneling direction. The perpendicular structure can also utilize quantum wells (QW) for the *n*- and *p*-type layers. Theoretical calculations of tunneling conductance considering the impact of density-of-states and momentum conservation suggest that tunneling between the face of two QWs will give a step like turn-on in device conductance, ideal for a steep SS transistor [20]. In contrast, the predicted turn-on for a thin-body parallel TFET (with tunneling from the edge of the source QW to the edge of the channel QW) would have a $E_{ov}^{3/2}$ dependence, where E_{ov} is the overlap energy between the source VB and channel CB [20].

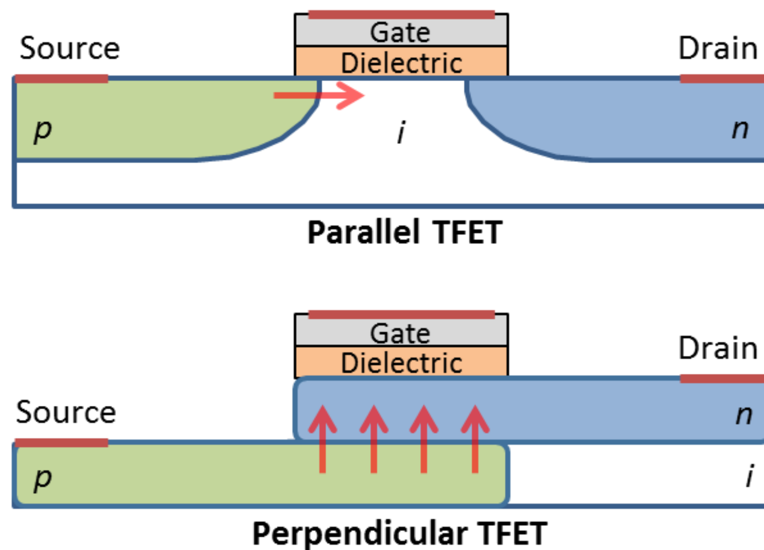

Figure 1.10. Parallel and perpendicular TFET structures. The red arrows indicate the tunneling path. The names reflect tunneling *parallel* or *perpendicular* to the gate..

1.4.2 Homojunction and Heterojunction Structures

Heterojunction TFETs, in which the source and channel are made from different semiconductor materials, have advantages and disadvantages. By using a heterojunction (as compared to a homojunction), the effective tunnel barrier height can be significantly reduced, while potentially maintaining low reverse-bias leakage currents afforded by the larger band gap of the constituent materials. For instance, the 1.12 eV tunneling barrier of homojunction Si (equal to its band gap) can be reduced to ~0.2 eV by using the strained-Si/strained-Ge heterojunction [21]. However, in a heterojunction TFET, the tunneling occurs across the heterojunction boundary. Any imperfections or trap states at the heterojunction interface will lead to leakage currents and degraded switching performance. In this way, heterojunction TFETs differ from heterojunction HEMTs, in which transport is mainly confined to a single semiconductor layer that is cladded by other wider band-gap semiconductors.

1.4.3 Undoped and Doped Channel Regions

Band tails caused by heavy doping of the tunneling region of TFET devices have recently been proposed as a mechanism that may limit the switching steepness of tunneling devices [20]. The bilayer TFET structure that utilizes an undoped channel has been proposed, which makes use of gate-induced electrostatic doping to create an *n*-layer and *p*-layer at the top and bottom of the structure between which tunneling occurs. However, in such an architecture, the gates that create the oppositely doped layers compete for electrostatic control of the channel reducing gate efficiency. Likewise, heavy doping can also reduce gate efficiency as the gate is less able to effectively change the surface potential of the channel.

1.5 Non-ideal Effects in TFETs

As detailed in §1.3, TFET simulations and experimental results have been in strong disagreement [7]. To reconcile simulation and experiment, different physical effects need to be better understood so that they can be properly modeled in a simulation environment and eventually mitigated in the experimental structures. In the subsections below, the impact of several non-ideal effects are described.

1.5.1 Non-abrupt Band Edges

Abrupt band edges are often assumed when modeling TFET device characteristics. Abrupt band edges assume a sharp drop-off in the density-of-states, such that zero states exist below the band edge, or equivalently in the band gap of the material. This assumption gives nearly zero off-current until the gate is biased such that the CB of the channel aligns in energy with the VB of the source shown in Figure 1.2d.

An exponential decay of the density-of-states of the CB and VB, called an Urbach tail after [22], has been long been observed in a large variety of materials, including crystalline Si [23], [24]. The Urbach tail results from disorder in the crystal system [25]. One explanation of the tail is spatial and temporal band gap fluctuations due to phonons in the crystalline system that smear the band edge [26]. As a result, Urbach tails seem unavoidable unless the phononic modes of the system can be engineered.

The Urbach tails limit the intrinsic band edge abruptness and suggest a more gradual turn-on than as expected with abrupt band edges. In Si, the band-edge density-of-states, as measured by the optical absorption coefficient, decays exponentially at the rate of 27 meV/decade [20]. Whereas a MOSFET is limited by the Maxwell-Boltzmann tail of carriers in the source, the off-current in a TFET is limited by the Urbach tail of states within the channel.

Doping also introduces donor states below the CB and acceptor states above the VB edge [27]. Carriers may tunnel into these dopant states and then be emitted into the bands thus allowing tunneling current before the ideal band-edge of the channel and source align in energy.

Furthermore, finite temperatures thermally broaden the energy distribution of carriers resulting in a more gradual turn-on characteristic. Lastly, other non-idealities, such as lattice defects and surface thickness variations also lead to broadening of the band-edges. These effects increase the SS of the device.

1.5.2 Phonon- and Photon-assisted Tunneling

Phonon-assisted tunneling smears the switching characteristics of TFETs (i.e. increases the SS). When the device is biased in the off-state (CB of the channel is higher in energy than the VB of the source), phonons may provide the required energy for tunneling to occur. Multiple phonons

can act simultaneously such that the total phonon energy provided to a carrier is greater than the optical phonon energy.

Alternatively, the situation can be viewed in terms of generation and recombination‡—both the electron and hole wavefunctions extend into the band gap such that spatial overlap of the wavefunctions occurs (see Figure 2.1c). Phonons or photons may provide energy for excitation of a VB electron into the CB, increasing the off-state current of the device. Just as there is thermal generation of electrons from the VB to CB, thermal generation (or equivalently, photon-assisted tunneling) of electrons from the VB eigenstate to the CB eigenstate should also occur, and it should increase exponentially as the energy separation between the eigenstates decreases.

1.5.3 Trap States

Traps states come in a variety of forms and can have two profound impacts on the behavior of TFETs. Interface traps may exist at the semiconductor/dielectric surface, and bulk traps may exist in the semiconductor body.

Firstly, traps can introduce a state to which electrons can tunnel. When biased into a nominally-off state where the bands are not aligned, the traps could allow a significant tunneling leakage path that limits the observation of steep switching behavior. The trap states could be created by threading dislocations inherent in the material or created during heterostructure growth. A small number of these dislocations along the tunneling path could severely limit the ability to turn off the device. This impact of traps is similar to the effect of non-abrupt band edges discussed in §1.5.1.

Secondly, traps can degrade gate efficiency. Efficient control of band-to-band tunneling in a TFET requires efficient control of the channel potential. Though the gate efficiency depends on the semiconductor doping as well as the bias regime, one of the most important parameters is the gate dielectric. Interface trap states at the dielectric/semiconductor surface degrade gate control as these states have to be *charged-up* by the gate potential, such that a larger fraction of the gate voltage is dropped across the oxide instead of the semiconductor resulting in loss of efficiency [29].

‡ Generation and recombination in the depletion region of an ideal *pn* junction is often neglected in analytical expressions for the diode current, and the predicted reverse-bias saturation current for diodes is quite small [28]. Experimentally, a much larger reverse-bias saturation current is often seen due to generation and recombination phenomena within the depletion region of the junction. The generation and recombination mechanisms may be due to optical, SRH through trap states, and Auger processes [28].

The gate efficiency, given by the ratio of the change in the surface potential ϕ_s with respect to the change in gate voltage V_G, can be expressed as [30]

$$\frac{d\phi_s}{dV_G} = \frac{C_{ox}}{C_{ox} + C_{semi} + C_{it}} \tag{1.3}$$

and

$$C_{it} \equiv \frac{dQ_{it}}{d\phi_s} = q^2 D_{it}{}^{\S} \tag{1.4}$$

where C_{ox} is the oxide capacitance, C_{semi} is the total semiconductor capacitance, and C_{it}, Q_{it}, and D_{it} are the capacitance, charge, and density of interface traps. The gate efficiency represents the fraction of applied gate voltage that appears across the semiconductor body, and it varies between 0 to 1.[**]

Equation (1.3) shows that in order to maximize gate efficiency, C_{ox} must be much larger than C_{semi} and C_{it}. Practical limits exist to the maximum value of C_{ox} before the oxide thickness is so thin that gate leakage becomes problematic. Therefore, to minimize the impact of traps on gate efficiency, the number of traps must be reduced such that $C_{it} \ll C_{ox}$.

High-quality, scaled gate dielectrics are very important in attaining a steep SS. As an example, a transistor with 75% gate efficiency would require an intrinsic SS of 45 mV/decade in order to have a measureable (extrinsic) SS of 60 mV/decade. Poor gate efficiency in TFET devices can wash away any intrinsic benefits of the tunneling-based switching. Inefficient gate control has continued to be a major challenge in fabricating III-V heterostructure TFETs with a small SS as dielectric quality on these materials is often inferior to Si (e.g., [32] shows a large D_{it} affecting InGaAs/GaAsSb TFET characteristics).

1.5.4 Quantization

Commercial TCAD device simulators including Sentaurus Device, Dessis, Medici, and Silvaco Atlas are classical single-band effective-mass simulators. The modeling of band-to-band tunneling

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[§] D_{it} is typically expressed as the # of traps/(eV·cm^2). One of the q's of the q^2 term cancels with the *e* of eV to give capacitance in Coulombs/(V·cm^2) or equivalently, Farads/cm^2 [29].

[**] Negative capacitance field-effect transistors seek to achieve values of $d\phi_s/dV_G$ greater than 1 through the use of ferroelectric gate insulators [31].

in these simulators was added using a WKB formulism (e.g., see [33]). The method employed does not take into account eigenstate quantization which restricts the allowable k-values in the quantization direction from a continuum to a discrete set dependent on the degree of confinement. In Sentaurus Device, the tunneling methodology reduces to two fitting parameters: A, a scalar pre-exponential constant; and B, a constant of an exponential function. Changing these constants can significantly change the shape of the simulated curve, and the impact of these constants is discussed in more detail in Chapter 5: *Electrostatic Design of Perpendicular TFETs*.

1.6 Overview of This Work

Much work has been performed on a wide array of different TFET designs ranging in materials and device geometry. With nearly all designs, a huge discrepancy exists between theoretical simulations and experimental results as discussed in §1.3. Two reasons may explain the vast inconsistency: relevant physics in these devices are not properly modeled and/or the input (i.e. material) parameters in the simulations are inaccurate. This thesis seeks to make progress in resolving the discrepancy between theory and experiment through the study of a bilayer TFET.

The bilayer TFET is used as an investigational test-bed to study tunneling. In Chapter 2: *Introduction to the Bilayer TFET*, the details of the bilayer structure are explained. Its main features include perpendicular tunneling induced by oppositely-biased top and bottom gates across an undoped channel composed of a strained-Si/strained-Ge heterostructure. The device also features multiple top gates so that the direction of tunneling and electrostatics across the device can be modulated.

Chapter 3: *Band Alignment of the Strained-Si/strained-Ge Heterostructure* details the extraction of valence band offset and effective band gap of the Si/Ge heterostructure under various biaxial strain created by pseudomorphic growth on virtual, relaxed SiGe substrates with varying Ge fraction. The effective band gap, a crucial parameter in modeling the tunneling current, is shown to be only ~200 meV and relatively independent of substrate Ge fraction. The extracted valence band offset of the strained-Si/strained-Ge heterostructure is shown to be ~100 meV larger than previous values predicted by density-functional theory. Deformations potentials for the Si and Ge material system are suggested from the extracted band alignments.

Chapter 4: *Impact of Quantization on Body Voltage at Eigenstate Alignment in Bilayer TFETs* presents a detailed analysis that shows how confinement energy of the electron and hole

wavefunctions is affected by body thickness and electric field across perpendicular TFETs, which includes the bilayer structure. In the case of thin-body devices, InAs (with a small band gap and small effective mass) can require more potential across the body to overlap the bands than Si (with a large band gap and heavy mass). The strained-Si/strained-Ge heterostructure is shown to dramatically reduce the body voltage required to align the electron and hole eigenstates in energy.

Chapter 5: *Electrostatic Design of Perpendicular TFETs* discusses design considerations for perpendicular TFETs. The 2D nature of these devices creates parasitic diagonal tunneling paths that can turn on before the desired perpendicular tunneling. The net effect is that the overall turn-on of a perpendicular TFET can be significantly degraded compared to an idealized 1D structure that only considers pure perpendicular tunneling.

Chapter 6: *Fabrication of the 3Gate Strained-Si/strained-Ge Bilayer TFET* discuss the process steps to create the 3Gate TFET structure. The structure provides many benefits for studying tunneling, but the fabrication is challenging due to the highly-strained Si/Ge heterostructure, bottom gate planarization, wafer bonding and etch-back, and two top-side gate stacks.

Chapter 7: *Suggestions for Future Work* provides electrical test configurations under which to measure the 3Gate strained-Si/strained-Ge bilayer TFET once fabrication of the device is complete. The test configurations suggest a way to provide experimental evidence of the impact of diagonal tunneling on the subthreshold characteristics of perpendicular TFETs.

Chapter 2: Introduction to the Bilayer TFET

The electron-hole bilayer TFET was first published by Lattanzio et al. [8] in 2011. The main attractions to the bilayer TFET are the ability to dynamically control electrostatic doping in the device through application of a gate voltage and its freedom from dopant-induced states in the band gap of the semiconductor. The bilayer TFET is studied as a research device to better understand the physics of tunneling.

A bilayer TFET consists of a *p*-source, *n*-drain, and intrinsic channel bounded by offset top and bottom gates shown in Figure 2.1. The gates are offset such that, when biased, a hole-rich layer is created along the bottom gate connecting to the *p*-source and an electron-rich layer is created along the top gate connecting to the *n*-drain. The device employs perpendicular band-to-band tunneling (see §1.4.1)—induced by the oppositely-biased gates—from the bottom to top of the intrinsic channel.

While the scalability of such a device is unclear, the structure provides an excellent test-bed for studying band-to-band tunneling. The sections that follow detail specific aspects of the strained-Si/strained-Ge bilayer TFET investigated in this work.

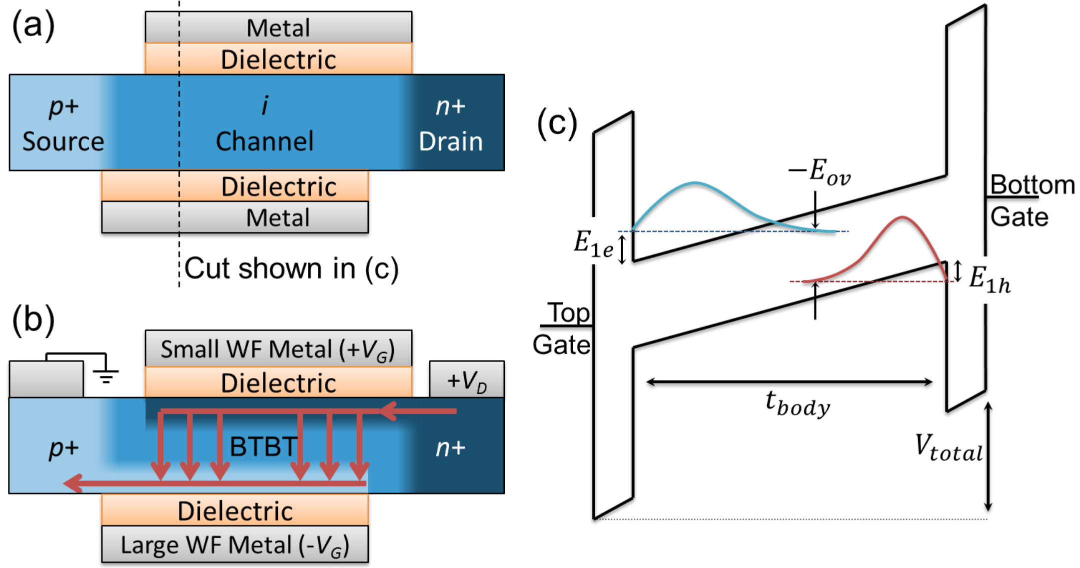

Figure 2.1. (a) Structure of the homojunction bilayer TFET. (b) Structure with applied bias. The current path is indicated by the red arrows. (c) Energy band diagram of the channel of (a). The electron and hole distribution is quantized and shown in blue and red, respectively. $-E_{ov}$ indicates the overlap energy between the electron and hole wavefunctions (negative values indicate an underlap).

2.1 Strained-Si/strained-Ge Heterostructure

The bilayer structure can employ either a homojunction or heterojunction, shown in Figure 2.1 and Figure 2.2 respectively. By using a heterojunction, the tunneling barrier and voltage required to align the electron and hole eigenstates in energy can be significantly reduced, increasing the tunneling probability and decreasing the gate voltage required to turn on the device. The bilayer structure at the focus of this work uses a strained-Si/strained-Ge heterostructure.

The tunneling barrier height can be reduced from 1.12 eV to ~200 meV by using the strained-Si/strained-Ge heterostructure as opposed to homojunction Si (see §3.5). The small effective band gap, $E_{G,eff}$, of the heterostructure significantly increases the tunneling probability. The transmission coefficient $\mathcal{T}$ of an electron striking a tunneling junction with a constant field is proportional to

$$\mathcal{T} \propto \exp\left(-\frac{\pi m^{*1/2} E_{G,eff}^{3/2}}{2\sqrt{2}\hbar F}\right) \tag{2.1}$$

where m^* is the effective mass of the carrier, $\hbar$ is the reduced Planck constant, and F is the electric field [34]. By reducing $E_{G,eff}$, a smaller electric field (and correspondingly a smaller gate voltage) can be used to achieve the same transmission probability. $E_{G,eff}$ in the strained-Si/strained-Ge heterostructure is therefore a critical parameter, and its experimental extraction is detailed in Chapter 3: *Band Alignment of the Strained-Si/strained-Ge Heterostructure*.

The strained-Si/strained-Ge heterostructure also has the key advantage that it can be grown such that the top and bottom interfaces of the gate dielectrics are both to Si, which is one of the best passivated surfaces of all electronic materials [35], [36]. High quality gate oxides can be formed on Si with excellent uniformity and low interface trap densities as demonstrated by past research of the MIT group [37]–[40]. This is especially important in a MOS device (such as a TFET or MOSFET) where surface trap states reduce gate efficiency [29]. A discussion of the impact of interface trap states on gate efficiency is presented in §1.5.3.

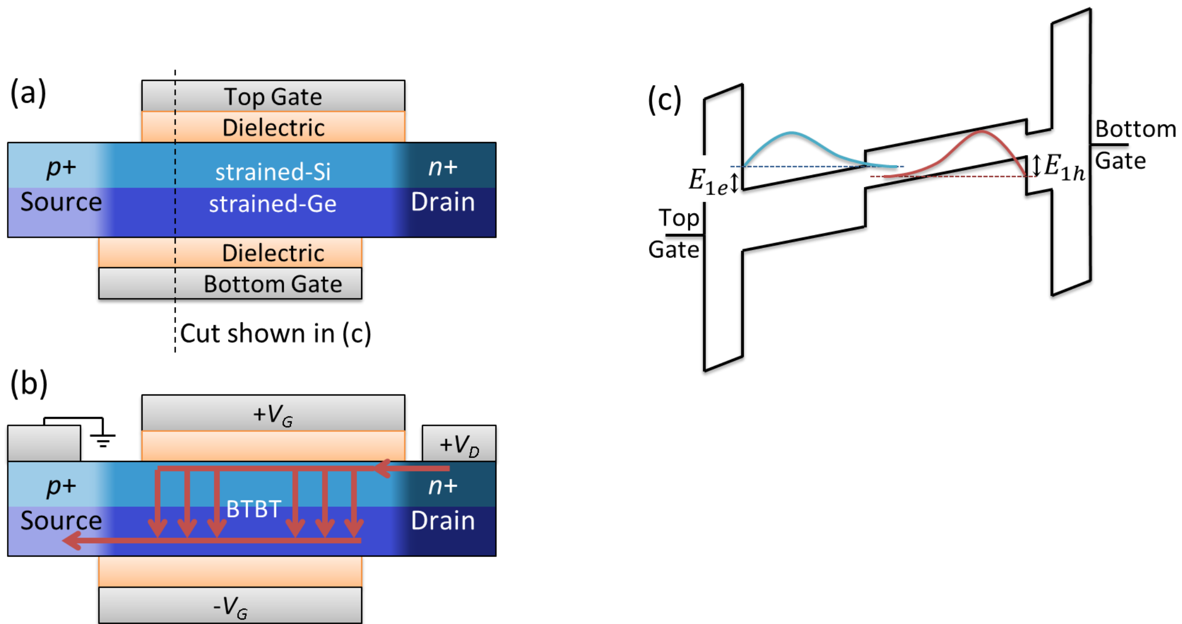

Figure 2.2. (a) Strained-Si/strained-Ge heterojunction bilayer TFET. (b) Structure with applied bias. The current path is indicated by the red arrows. (c) Energy band diagram of the channel of (a). The electron and hole distribution are quantized and shown in blue and red, respectively. The heterojunction significantly reduces the tunneling barrier and the voltage required to align the electron and hole eigenstates in energy.

2.2 Perpendicular Tunneling

The bilayer TFET makes use of tunneling perpendicular to the gate (see §1.4.1), in-line with the gate electric field, which can enhance tunneling efficiency. As shown in Eq. (2.1), tunneling probability is exponentially dependent on the electric field in the tunneling direction. The strained-Si/strained-Ge bilayer structure creates a quantum well for electrons in the Si layer and a quantum well for holes in the Ge layer shown in Figure 2.2. Theoretical calculations by Agarwal [20] suggest that tunneling between the face of two QWs (as opposed to the edge) will give a step-like turn-on in device conductance, ideal for a steep SS transistor.

2.3 Electrostatic Doping

Tunneling in the bilayer TFET takes place across an intrinsic channel with no intentional doping. Non-idealities due to dopant atoms therefore can be minimized such that the fundamental limitations of intrinsic band-edge broadening and phonon-assisted tunneling and their impact on the best attainable SS can be studied. The electrostatic doping also gives the flexibility that the carrier concentration of the semiconductor layer can be changed through application of a gate bias. The impact of heavy doping on non-abrupt band edges is discussed previously in §1.5.1.

2.4 Multiple Gates for Electrostatic Control

The 3Gate bilayer TFET investigated in this work uses three independent gates so that electrostatics across the device can be tuned such that the tunneling path can be controlled and analyzed. A diagram of the device is shown in Figure 2.3.

The bottom gate is used induce a high hole concentration along the bottom of the device. In normal operating conditions, the bottom gate is held at a constant bias. The high hole concentration pins the surface potential on the bottom of the device such that the bias of top gate 1 does not affect the surface potential at the bottom of the semiconductor layer. This maximizes the effect of top gate 1 in changing the potential across the body of the device, V_{body}. Conversely, if the surface potential at the bottom of the semiconductor is not pinned, then a fraction of the voltage of top gate 1 is dropped across the bottom oxide, which is not useful in overlapping the semiconductor bands such that BTBT occurs.

Top gate 1 is used to create a well in the CB over which tunneling occurs. This well is completely contained within the length of the bottom gate. The electrostatics should be uniform

along the length of the electron well created by top gate 1 and along the bottom of the semiconductor body. The turn-on of BTBT in this region should not be limited by electrostatic effects (such as diagonal tunneling) because the electrostatics are uniform. Other mechanisms, such as trap states *could* influence the turn-on of BTBT allowing the isolation of electrostatic effects from other parasitic effects.

Top gate 2 is used to induce an electron channel so that electrons tunneling into the well under top gate 1 can travel to the drain to be collected. Top gate 2 can be thought of as the gate of a MOSFET in series with a TFET controlled by top gate 1 and the bottom gate. Top gate 2 would not be used in a sacled version of the bilayer TFET. It is used in the experimental test bed structure as a knob to control the band bending of the Si layer near the right edge of the bottom gate independently from the band bending used to create a tunneling well under top gate 1. In a device with single top gate, the bands of the Si layer can dip to the right of the bottom gate providing a parasitic diagonal tunneling path that could limit the sharpness of the turn-on. The effect of parasitic diagonal tunneling is detailed in Chapter 5: *Electrostatic Design of Perpendicular TFETs*.

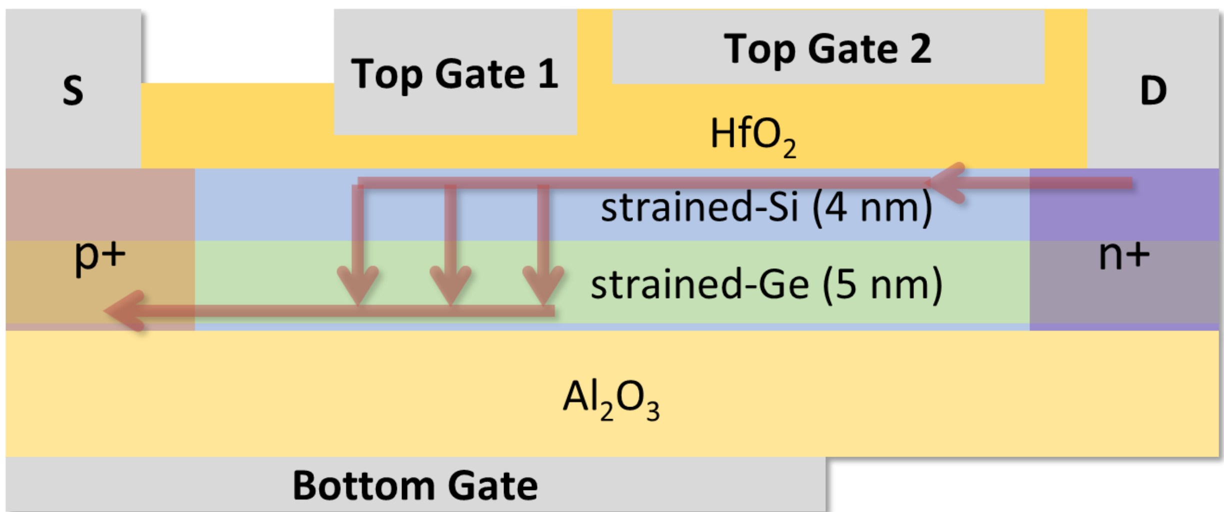

Figure 2.3. A simplified device structure of the 3Gate strained-Si/strained-Ge bilayer TFET. Key features of the structure are three independent gates to control the direction of the tunneling path, a doping-free intrinsic channel, and small $E_{G,eff}$ heterostructure for improved tunneling probability. The red arrows indicate the ideal current path in the device.

Chapter 3: Band Alignment of the Strained-Si/strained-Ge Heterostructure

The bilayer TFET investigated in this work utilizes a strained-Si/strained-Ge heterostructure. Tunneling is exponentially dependent on $E_{G,eff}$, which is related to the heterojunction energy band alignment (see §2.1). Understanding the energy band alignment is crucial for predicting the tunneling current in a TFET. To this end, the energy band alignment of the strained-Si/strained-Ge heterostructure was thoroughly investigated as detailed below. In the work that follows, a strained-Si/strained-Ge MOS capacitor is used to extract the energy band alignment of the heterostructure because its simpler 1D electrostatics provide fewer uncertainties compared to a three-terminal transistor structure. The MOS capacitor contains the same heterojunction used in the bilayer TFET although the thickness of the Si and Ge layers vary between the MOS-capacitor and TFET devices.

3.1 Calculation of Energy Band Alignments

The electronic band structure of tetrahedral semiconductors can be referred to a common energy scale from which the band offsets in the heterostructures can be derived, including those involving alloys of these materials [41]–[45]. In the case of Si and Ge, earlier *ab initio* calculations indicated that in this common energy scale the "natural" valence band offset between Si and Ge is about 500-600 meV, with the Ge valence band higher in energy [45], [46]. Starting from these values, the band lineups at specific heterojunctions can be predicted by performing appropriate strain corrections, which can be conveniently done by expressing the strain tensor as the sum of a hydrostatic contribution and a traceless shear component. Two widely used prescriptions are the expression obtained by People and Bean [47], based on the Van de Walle and Martin 1985 paper [48]:

$$\Delta E_v \text{ for strained Si/strained Ge on } \langle 100\rangle\ Si_{1-xs}Ge_{xs} = 740 - 530x_s \text{ meV} \quad (3.1)$$

where x_s is the Ge fraction of the relaxed substrate and ΔE_v is the valence band offset between strained-Si (s-Si) and strained-Ge (s-Ge) in meV, and the expression recommended by Rieger and Vogl [49]:

$$\Delta E_{v,av} \text{ for strained } Si_{1-x}Ge_x \text{ on } \langle 100 \rangle\, Si_{1-xs}Ge_{xs} = (470 - 60x_s)(x - x_s) \text{ meV} \qquad (3.2)$$

where $\Delta E_{v,av}$ is the offset between the average valence band energy of s-$Si_{1-x}Ge_x$ on a relaxed $Si_{1-xs}Ge_{xs}$ virtual substrate. The average energy of the top three valence bands ($E_{v,av}$) is unaffected by the shear component of the strain or by the spin-orbit interaction. The predictions from Eqs. (3.1) and (3.2) are quite similar. For the s-Ge/unstrained-Si interface, for example, Eq. (3.2) leads to ΔE_v = 700 meV once the valence band splitting is taken into account, which is close to the value ΔE_v = 740 meV from Eq. (3.1).

Despite their widespread use, the validity of Eqs. (3.1) and (3.2) for the prediction of the band lineups of Si/Ge heterostructures is not firmly established. This is remarkable in view of the intense scrutiny on this material system for over 40 years; however, the Si/Ge heterostructure is particularly difficult from the standpoint of band offset theory not just because of the large lattice mismatch, but also due to the fact that the conduction band minima in Si and Ge are located at different indirect valleys in the Brillouin zone. The calculation of the effect of strain on such states requires the use of several deformation potentials, which are not well known for both materials because most experimental probes provide values associated with the conduction band minimum. A known (but not widely acknowledged) discrepancy between theory and experiment is the band alignment at s-$Si_{1-x}Ge_x$/unstrained-Si interfaces. Using Eq. (3.1), (3.2), or similar expressions, combined with experimental band gaps and reasonable choices for the strain deformation potentials, it can be shown that the band alignment is type I for s-$Si_{1-x}Ge_x$/unstrained-Si (valence band maximum and conduction band minimum both in the s-$Si_{1-x}Ge_x$ layer), for $x < 0.7$ (Refs. [46], [50]), whereas experimental results for s-$Si_{0.70}Ge_{0.30}$/unstrained-Si clearly show that the alignment is type II (valence band maximum in s-$Si_{0.70}Ge_{0.30}$ and conduction band minimum in unstrained Si) [51], [52]. Rieger and Vogl [49] *do* predict a type-II alignment for s-$Si_{0.70}Ge_{0.30}$/unstrained-Si, but they use theoretical hydrostatic deformation potentials for the Δ-minimum indirect band gap that differ from experimental values. Their theoretical deformation potential for Si is much larger and for Ge is of opposite sign compared to experimental values [53].

Interest in quantitatively understanding the type-II staggered band alignment of tensile strained-Si on compressively strained-Ge grown on relaxed SiGe (shown in Figure 3.1a) has been recently revived due to the relevance of this system in tunneling applications for which the current depends exponentially on the effective band gap between the Si conduction band and the Ge

valence band [54]. In addition, the s-Si/s-Ge heterointerface is present in high-mobility strained-Ge *p*-MOSFETs, which are under study for future CMOS technology (e.g. Refs. [55]–[62]). The valence band offset determines the threshold voltage and gate-to-channel capacitance of such devices.

In view of the remaining discrepancies and the renewed interest in Si/Ge heterojunctions, new measurements of the valence band offsets in this system have been performed using a quasistatic CV technique that is an extension of the method first described by Voinigescu et al. [63]. It is found that the valence band offsets at the Si/Ge interface are much larger than predicted by Eqs. (3.1) and (3.2). Combining these results with a judicious choice of deformation potential constants, this work shows that the newly determined band offsets can explain the long-standing puzzles in the heterostructure band alignment of the Si-Ge system.

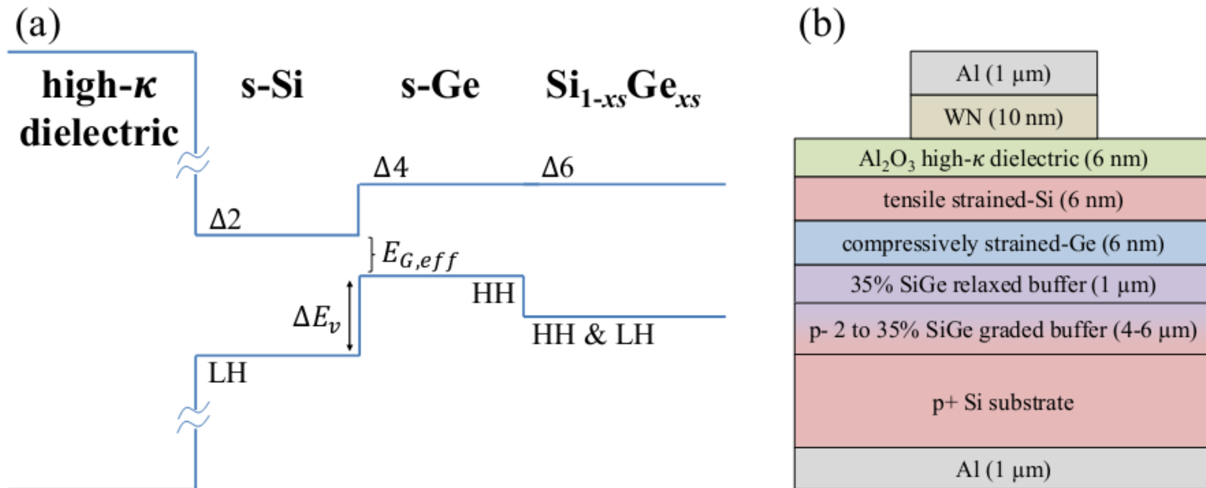

Figure 3.1. (a) Schematic of the energy band diagram illustrating the type-II band alignment between tensile strained-Si and compressively strained-Ge. The heavy-hole (HH) band is the topmost s-Ge valence band, and the Δ2 band is the bottommost s-Si conduction band. (b) MOS-capacitor structure with a 35% SiGe relaxed buffer fabricated for valence-band offset extraction.

3.2 Fabrication of Heterostructure MOS Capacitors

The MOS-capacitor structure for s-Si/s-Ge on a relaxed 35% SiGe substrate is shown in Figure 3.1b. First, the initial SiGe layer (i.e. graded buffer layer) was epitaxially grown at 900 ˚C on a

(100)-oriented *p*+ Si substrate using an Applied Materials Epi Centura low-pressure chemical vapor deposition (LPCVD) system. The layer was *in situ* doped with boron at approximately 5×10^{16} cm^{-3}. In order to create a high quality SiGe virtual substrate, the Ge alloy percentage of the initial SiGe layer was linearly graded from 2% to 35% over 4 μm of SiGe growth. Next, a 1-μm thick undoped relaxed 35% SiGe layer was grown on top of the graded buffer layer to form a relaxed virtual substrate. Subsequently, approximately 6 nm of undoped compressively strained-Ge followed by 6 nm of undoped tensile strained-Si was grown on the surface of the SiGe virtual substrate. Similar growth procedures were also used to create s-Si/s-Ge heterostructures on 42% and 52% SiGe virtual substrates.

The epitaxial wafers underwent a modified RCA clean immediately before high-κ dielectric deposition in an atomic layer deposition (ALD) system. A modified RCA clean was used to remove contaminants while limiting removal of the thin s-Si layer, and it consisted of four key steps: 1) H_2SO_4:H_2O_2 (3:1) piranha clean, 2) dilute-HF dip, 3) HCl:H_2O_2:H_2O (1:1:5) clean, and 4) dilute-HF dip. The last HF dip removes any native SiO_2 that forms during the chemical cleaning. MOS capacitors were created by heating the sample to 250 ˚C in the ALD chamber and initially flowing 20% ozone *in situ* for 5 minutes. This was followed by the deposition of 6 nm of Al_2O_3 dielectric using trimethylaluminium (TMA) and water as precursors. These steps were followed by atomic layer deposition of 10 nm of tungsten nitride (WN). Sputtered aluminum was used to create contacts at the top and bottom surfaces of the samples. The devices were patterned using typical photolithographic techniques to create MOS capacitors of various sizes. A final forming gas anneal was performed at 450 ˚C for 30 minutes, which dramatically lowers the density of interface traps at the Si/dielectric interface.

The Ge molar fraction in the relaxed buffer layer was measured by secondary ion mass spectrometry (SIMS) and micro-Raman spectroscopy using 514-nm excitation. The measured Ge content derived from each technique is listed in Table 3.1. Whereas SIMS measures the chemical concentration of Ge, Raman spectroscopy measures the shift in the vibrational frequencies of the atomic bonds of the crystal. Due to anharmonic and mass substitution effects, these frequencies are dependent on the strain-state and Ge fraction of the SiGe alloy. The shift ($\Delta\omega$) of the Si-Si Raman peak of the SiGe alloy relative to the bulk Si Raman frequency is related to the Ge fraction by [64]–[66]

$$xs = -0.015 \cdot \Delta\omega \tag{3.3}$$

This expression assumes that the SiGe layer is fully relaxed. Therefore, the excellent agreement between SIMS data and Raman-extracted Ge fraction indicates that the SiGe is nearly completely relaxed, as expected based upon the growth conditions. It should be noted that the Si and Ge layers are too thin for accurate measurements of strain using 514-nm excitation.

Ni Chleirigh performed an experimental analysis on the valence band offset of the related s-Si/s-$Si_{1-x}Ge_x$ on relaxed $Si_{1-xs}Ge_{xs}$ heterostructure system [67]; however, her work only covered s-$Si_{1-x}Ge_x$ layers with up to 70% Ge. This research expands that work by providing extraction of the band alignments for s-Si/s-Ge heterostructures on relaxed SiGe substrates of different Ge fractions, i.e. with different levels of biaxial strain in the heterostructure. Also, in contrast with the previous work, the present work employs a full-band quantum mechanical simulator for the CV simulations.

Table 3.1. Extracted and theoretical values for s-Si/s-Ge heterojunctions on different relaxed SiGe substrates. The experimental values were extracted by fitting quantum mechanical simulations to experimental QSCV measurements. The theoretical values were calculated using an average valence band offset of $\Delta E_{v,av}$ = 800 meV between s-Si and s-Ge and deformation potentials from Table 3.2. The calculation of the theoretical values is described in §3.7 *Unified Theoretical Description of the Si-Ge System*, which uses the methodology of [44].

Name	Measured Ge fraction of SiGe layer		Band alignments between s-Si/s-Ge layers					s-Si cap thickness (Å)
			ΔE_v (meV)		$E_{G.eff}$ (meV)		$E_{G,Si}$ (meV)	
	SIMS	Raman	Exp.	Theory (this work)	Exp.	Theory (this work)	Exp.	Exp.
"35% SiGe"	35.5%	34.1%	770 ± 25	783	190 ± 50	137	960 ± 50	49 ± 2
"42% SiGe"	42.6%	41.3%	760 ± 25	755	185 ± 50	122	950 ± 50	45 ± 2
"52% SiGe"	52.7%	52.2%	670 ± 25	715	190 ± 50	101	870 ± 50	43 ± 2

3.3 Physics of the CV Extraction Technique

A quasistatic CV obtained from one of the samples is shown in Figure 3.2. The band alignment extraction procedure originally developed by Kroemer et al. [68] for Schottky and *pn* junction devices was expanded by Voinigescu et al. [63] to low-frequency CV measurements on high quality metal-oxide-semiconductor (MOS) structures. Voinigescu found that the low-frequency CV curve of a Si/SiGe heterostructure MOS capacitor produces a distinctive plateau region (see region II of Figure 3.2), which can be used to extract the valence band offset of the heterostructure. The valence band offset extraction requires the material with a lower valence band energy (in this case Si) to be at the surface of the heterostructure, thus producing a well for holes separated from the oxide/semiconductor surface.

The CV curve of the s-Si/s-Ge heterostructure MOS capacitor has four distinct regions illustrated in Figure 3.2 and Figure 3.3: (I) hole accumulation in the Si and Ge layers, (II) hole accumulation in the Ge layer, (III) depletion of holes, and (IV) electron inversion in the Si layer. The maximum capacitance of regions I and IV allow fitting of the dielectric thickness to an equivalent [SiO_2] oxide thickness (EOT), while region II, called the plateau region, allows for determination of the s-Si thickness and valence band offset at the s-Si/s-Ge interface. The narrow width of region III is indicative of the small effective band gap ($E_{G,eff} = E_{c,Si} - E_{v,Ge}$) of the s-Si/s-Ge heterostructure.

In a p-type s-Si/s-Ge heterostructure MOS capacitor, represented in Figure 3.2 and Figure 3.3, as the gate voltage is swept from positive to negative, holes are first accumulated in the buried s-Ge quantum well (region II), and then eventually at the s-Si/dielectric interface as a more negative gate bias is applied (region I). The plateau width of region II is directly related to the valence band offset. As the valence band offset increases, increased negative gate voltage is required to bend the Si valence bands toward the Fermi level in order to accumulate the Si layer with holes, and this causes an increase in the plateau width (region II) of the CV curve. The plateau width of the simulated CV data is fit to the experimental data by varying the s-Si/s-Ge valence band offset of the simulation.

The capacitance of the plateau region (region II) is given by the series combination of the oxide- and Si-layer capacitances because the unpopulated Si layer acts as a dielectric. During the transition from region II to region I, as the gate bias is swept to more negative voltages, holes begin

to populate the Si layer as the Si valence bands bend toward the Fermi level. The Si layer no longer acts as a dielectric, and the capacitance increases towards the oxide capacitance due to the decrease of the effective dielectric thickness.

Region III of the CV curve provides information on the effective band gap, $E_{G,eff}$, at the s-Si/s-Ge heterojunction, given by

$$E_{G,eff} = E_{c,Si} - E_{v,Ge} \tag{3.4a}$$

$$= E_{G,Si} - \Delta E_v \tag{3.4b}$$

where $E_{c,Si}$ is the conduction band energy of s-Si, $E_{v,Ge}$ is the valence band energy of s-Ge, $E_{G,Si}$ is the band gap of s-Si, and ΔE_v is the valence band offset at the s-Si/s-Ge heterojunction. For a given s-Si band gap, an increase in ΔE_v gives a decrease in $E_{G,eff}$ by the same amount.

Due to the small effective band gap of the heterostructure, electrons begin to collect in the Si conduction band before holes are fully depleted from the structure. Thus, the width of region III is very narrow, and the capacitance of region III does not decrease to the low values typically measured in Si homostructure MOS capacitors in depletion. $E_{G,eff}$ is directly related to the width and capacitance of region III, and $E_{G,Si}$ (the sum of ΔE_v and $E_{G,eff}$) is directly related to the total width of regions II and III. The band alignment of s-Si/s-Ge can be extracted by varying ΔE_v and $E_{G,eff}$ of the simulation until a good fit is found between simulated and experimental CV. Since ΔE_v and $E_{G,eff}$ affect different regions of the CV curve, their values can be extracted independently.

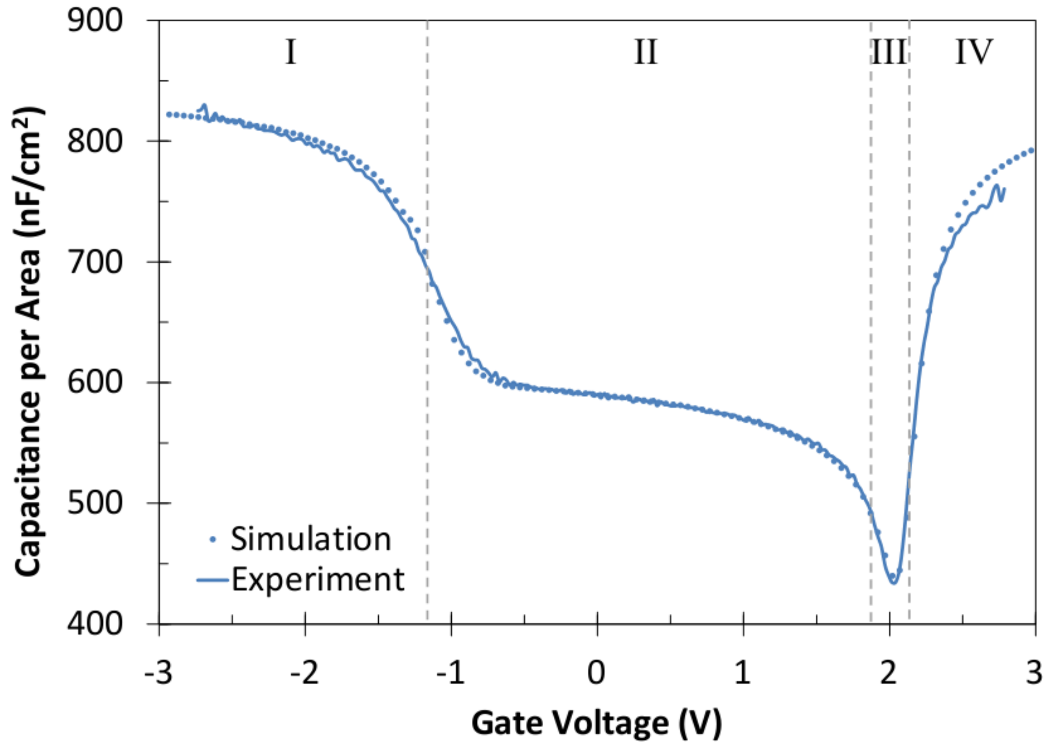

Figure 3.2. Experimental and simulated QSCV curves for s-Si/s-Ge on a relaxed 35% SiGe substrate. The following parameters were used to produce the simulated CV curve: EOT = 38 Å, 49 Å s-Si cap thickness, ΔE_v = 770 meV, and $E_{G,eff}$ = 190 meV. The CV analysis does not provide significant sensitivity to other parameters. Voltage regions of distinct carrier distributions are identified by Roman numerals, described in the text, and shown schematically in Figure 3.3.

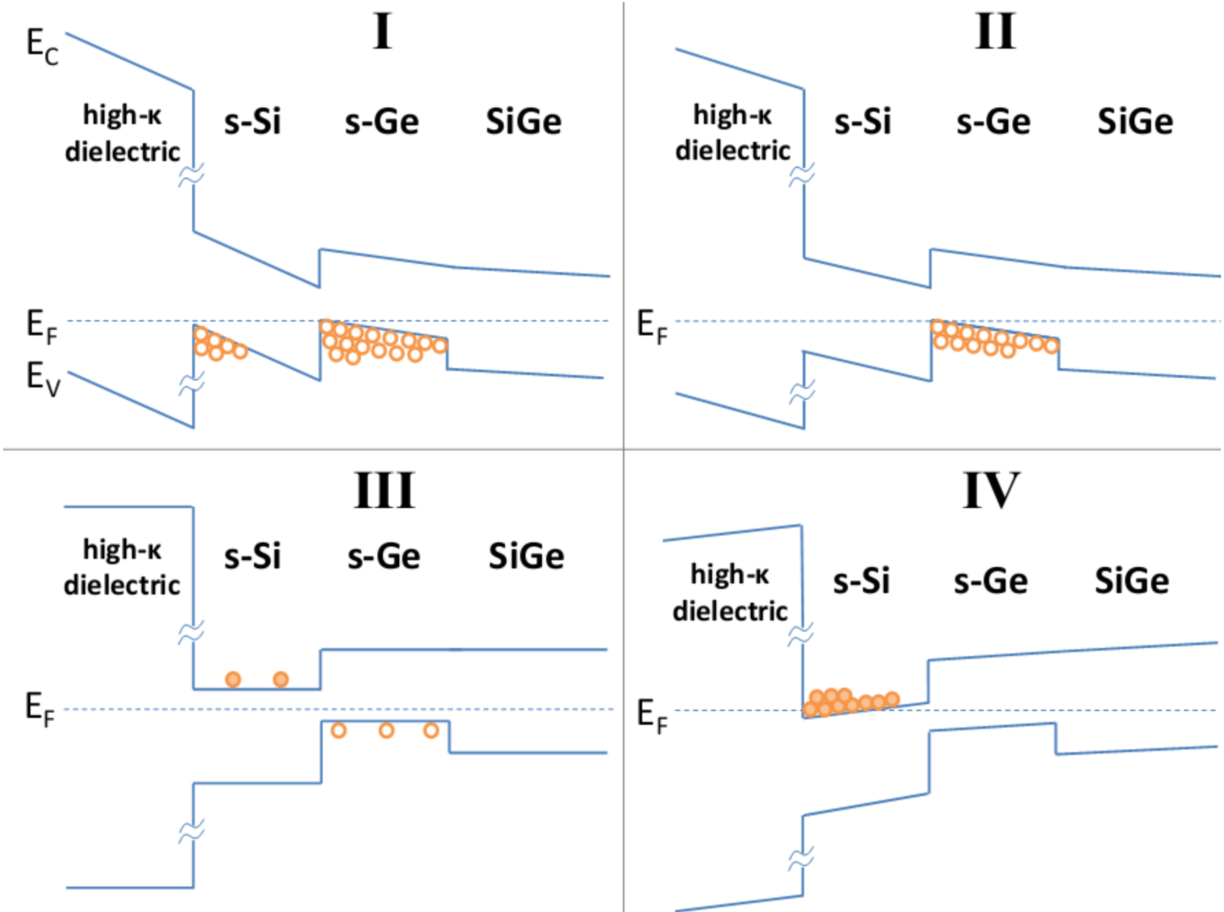

Figure 3.3. Depiction of the heterostructure band diagrams and carrier populations (not drawn to scale) under the different regimes labeled in Figure 3.2.

3.4 Measurement and Experimental Details

The CV curves were measured using a quasistatic method. For this technique, an Agilent 4156C Parameter Analyzer was used to apply a DC bias across the device. The parameter analyzer steps the voltage and integrates the current to determine the change in charge, ΔQ, that occurred over the voltage step, ΔV. The equipment also applies some basic algorithms to mitigate the effect of integrating oxide leakage current. A detailed description of the technique is given in [69]. The quasistatic capacitance-voltage (QSCV) technique has the advantage that it emulates the quasistatic simulation method and is able to probe the inversion regime of the CV curve. The inversion regime is difficult to measure with conventional low-frequency CV techniques due to

the long carrier lifetimes attributed to the high quality of the epitaxial materials and $1/f$ noise that becomes substantial at frequencies less than 1 kHz.

The measurements shown in this thesis were made using the QSCV technique on unpackaged samples in a dark, electromagnetically shielded probe station at room temperature. Voltage steps of 24 mV were used, with 500 ms of quasistatic integration time and 100 ms of leakage current integration time.* Devices were screened to ensure low DC gate leakage and high quality dielectrics. The DC leakage current through the dielectric of the MOS capacitors was measured to be less than 1 nA/cm^2 in the gate voltage range from -2 to 2.75 V. There was good agreement between low-frequency and quasistatic CV measurements for AC frequencies less than 500 Hz. CV measurements at frequencies higher than 500 Hz showed a decrease in the inversion capacitance due to long carrier lifetimes in the high quality material. The observed hysteresis between positive- and negative-directed voltage sweeps was less than 20 mV, indicating a high quality dielectric.

A requirement for obtaining clean QSCV data reflecting only the semiconductor band structure is that the dielectric/semiconductor interface be of high quality. In the MIT laboratory, significant work has been conducted on the deposition of high quality Al_2O_3 on unstrained Si and strained-Si/strained-Ge heterostructures with minimal density of interface traps (D_{it}) and mobile oxide charge that causes hysteresis [37]–[40]. In the present work, the D_{it} of a Si control wafer with the same Al_2O_3 procedure as used for the heterostructure wafers was measured to be 10^{11} cm^{-2}eV^{-1} at mid-gap by using the conductance method [29], [70]. Simulations incorporating D_{it} (not shown in this work) suggest that at values determined from the Si control wafer there is minimal impact on the valence band extraction method. Though the D_{it} of the Si control wafer may be considered a lower bound for the expected D_{it} of the heterostructure wafers, other features of the measured CV curves of the heterostructure devices also suggest a low D_{it}. After accounting for series resistance, a capacitance offset, which would suggest the presence of D_{it}, does not appear between the high and low-frequency CV curves when transitioning from accumulation to depletion. Furthermore, a large D_{it} would stretch-out the CV curve yielding a larger value for the valence band offset *and* for the s-Si band gap. However, the extracted s-Si band gap, shown in

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* The 4156 uses the charge measured during the leakage current integration time to remove the effects of gate leakage on the calculated quasistatic capacitance.

Figure 3.7a, is slightly lower than expected based on previous experiments and theory, which signifies a small D_{it} that has minimal impact on the extraction technique. Moreover, the slope of the experimental CV curve at the point where holes begin to accumulate in the s-Si layer (transitioning from region II to region I in Figure 3.2) would also be stretched-out by a large D_{it}. But the simulation without D_{it} matches the experimental data as shown in Figure 3.2, which is consistent with a small D_{it}.

Though a large hole barrier (i.e. the valence band offset) exists between the s-Si and s-Ge (shown in region I of Figure 3.3) limiting the rate at which holes can populate the s-Si layer, the slow voltage sweep rate of the quasistatic measurement method allows enough time for the carriers to respond so that quasi-equilibrium can be reached between each voltage step. Ultimately, the path that the holes take (whether through thermionic emission or tunneling through the large valence band barrier) to populate either of the quantum wells does not impact the QSCV measurement. What *is* important is that the carriers reach quasi-equilibrium between each voltage step so that the change in charge in each quantum well is representative of the quasi-equilibrium simulations.

3.5 Results and Simulations

The simulated QSCV capacitance is calculated by taking the numerical derivative of the change of integrated charge density in the semiconductor layers divided by the voltage step ($C = dQ/dV$). An advanced simulation tool that accounts for quantum mechanical effects and band splitting due to strain is necessary to properly model the charge density at different voltages. Whereas Ni Chleirigh [71] used a single-band simulator with a density gradient model for quantum corrections and a modified valence band density-of-states N_v to account for strain, this work uses *nextnano3* [72], [73], a full-band quantum mechanical simulator. *nextnano3* is used to model multiple valence bands with a 6×6 $k \cdot p$ method that captures the non-parabolic valence band structure with strain. Additionally, the Schrödinger-Poisson equation is self-consistently solved to determine the charge density that is then used to calculate the capacitance.

A comparison of the measured and simulated CV data is shown in Figure 3.2 for s-Si/s-Ge on a relaxed 35% SiGe substrate. The extracted valence band offset and effective band gap for the sample are ΔE_v = 770 ± 25 meV and $E_{G,eff}$ = 190 ± 50 meV, respectively. The quoted uncertainty reflects the range of these parameter values that yields a qualitatively good fit between simulation

and experimental data. The extracted EOT and s-Si cap thicknesses are 38 ± 2 Å and 49 ± 2 Å respectively, in agreement with the expected values based on the device fabrication.

In this work the standard definition of valence band offset is used: the energy difference between the valence band maxima at both sides of a heterojunction between two semi-infinite materials. In the case of a Si/Ge heterostructure strained to SiGe, this definition corresponds to the difference between the top of the s-Ge heavy hole valence band and the s-Si light hole valence band, as shown in Figure 3.4. The simulation includes the effects of quantization, but the valence band offset is quoted as the difference in the band-edges. While the figure uses the terms *heavy hole* and *light hole* to identify the split valence bands, it should be noted that even at $k = 0$, the strain Hamiltonian mixes the characteristics of the bands [74].

In general, good agreement is obtained between experimental and simulated CV curves, with high sensitivity to the following parameters: equivalent [SiO_2] oxide thickness of the dielectric (EOT), Si thickness, valence band offset, and effective band gap. Other parameters, such as the doping concentration, have a weaker impact on the simulation results. Additionally, the EOT, Si thickness, and valence band offset can be extracted independently from fitting different regions of the CV curve. The maximum capacitance determines the EOT. As shown in Figure 3.5, the Si thickness affects the plateau capacitance, which is the series combination of the oxide and Si capacitances. The Si layer acts as a dielectric in the plateau region of the CV curve because of the low carrier density in Si. Increasing the Si thickness effectively increases the dielectric thickness and results in a lower capacitance in the plateau region of the CV curve, and the high sensitivity to small changes in the s-Si thickness enables low uncertainty (± 2 Å) in its extraction. As discussed earlier, the s-Si/s-Ge valence band offset modifies the plateau width, as shown in Figure 3.6. The effective band gap, $E_{G,eff}$, is not as easily extracted because changes in the effective band gap and doping in the SiGe both produce similar effects on the simulation CV curve in region III, and these parameters are not easily decoupled. For this reason, the uncertainty of the extracted effective band gap is larger than the quoted uncertainty of the valence band offset.

The sensitivity of the extraction method to changes in ΔE_v is illustrated in Figure 3.6 for s-Si/s-Ge on a 35% SiGe substrate. For these structures, a small change in the valence band offset produces about a four times larger change in the width of the plateau region (e.g. a 50 meV increase

in ΔE_v produces a ~200 mV enlargement of the plateau width). The extracted values for the valence band offset, effective band gap, and silicon band gap are shown in Table 3.1.

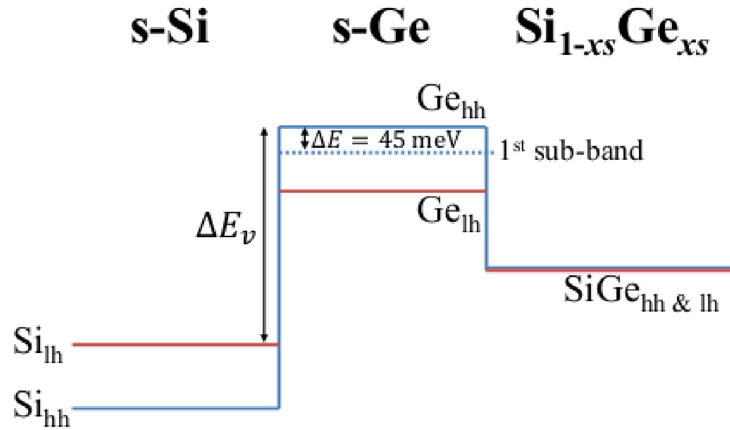

Figure 3.4. Valence band diagram of the s-Si/s-Ge/relaxed SiGe heterostructure. The valence bands in s-Si and s-Ge split due to tensile and compressive strain, respectively. The valence band offset quoted in this work is the difference between the top valence band of s-Ge and s-Si. The simulation models quantization effects, but only the band-edge difference is quoted in order to provide information about the band lineup that is independent of the quantum well thickness.

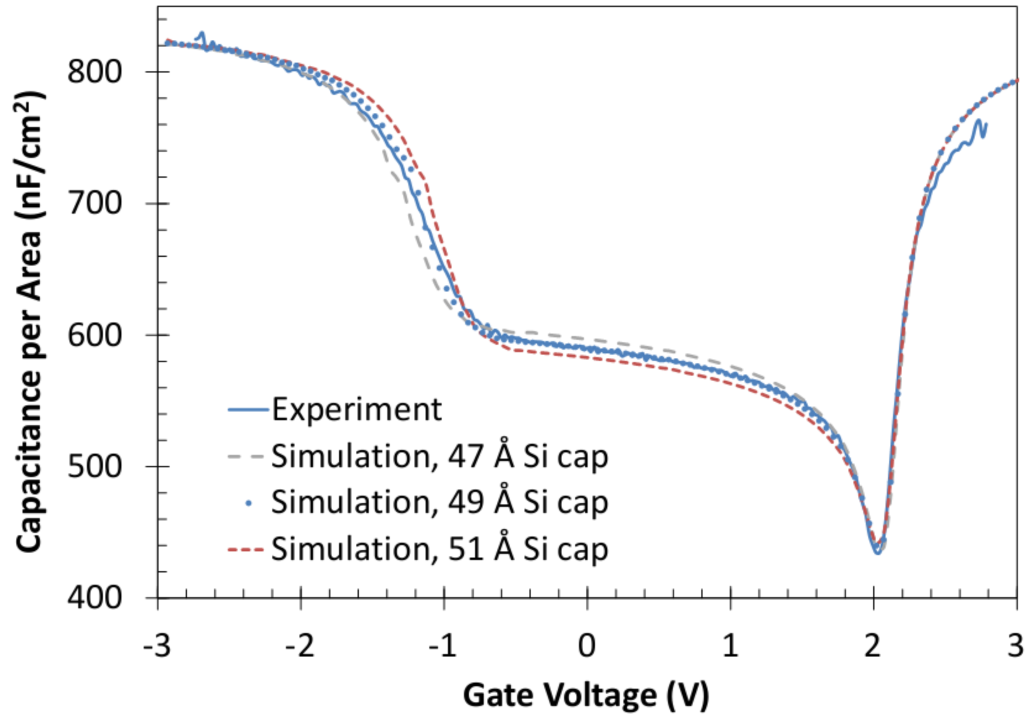

Figure 3.5. Simulated QSCV for different s-Si cap thicknesses. The simulated CV displays a high sensitivity to small changes in the s-Si cap thickness which allows the physical thickness to be extracted with low uncertainty (± 2 Å).

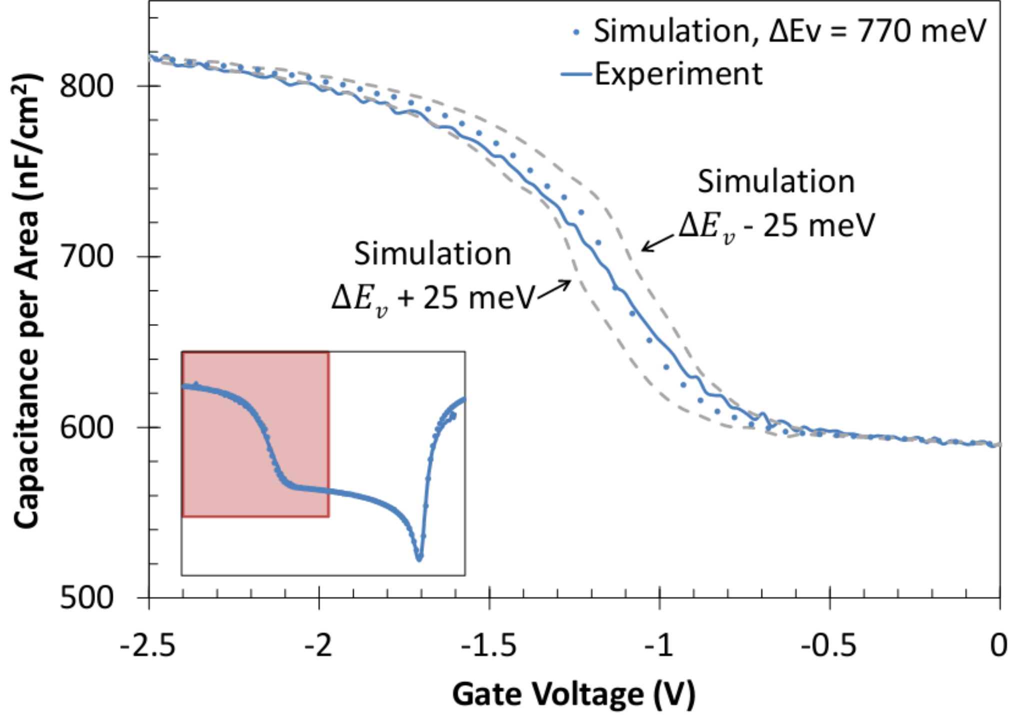

Figure 3.6. Measured and simulated CV curves illustrating the high sensitivity of the simulation to ΔE_v. A 25 meV change in ΔE_v produces about a 90 mV change in the plateau width. A change in ΔE_v only impacts the portion of the CV curve shown here.

3.6 Discussion

Figure 3.7a compares the theoretical values of the s-Si band gap from [47] with values extracted in this work as a function of substrate Ge fraction (xs). Also plotted are Welser's experimental data [64] extracted using a MOS CV technique for s-Si grown directly on relaxed SiGe. The data show that the band gap of s-Si decreases as biaxial strain in the silicon is increased (i.e., increasing Ge mole fraction of the substrate, xs), and the values are in reasonable agreement with People and Bean's calculated values. However, Figure 3.7b shows that the extracted valence band offset between s-Si/s-Ge is about 100 meV greater than the theoretical values represented by Eq. (3.1).

Since ΔE_v is roughly 100 meV larger than reported calculated values, $E_{G,eff}$ is found to be significantly smaller than previously expected: $E_{G,eff}$ ~ 190 meV versus 300-400 meV based on Eqs. (3.1) and (3.2).

Interestingly, $E_{G,eff}$ remains relatively constant as a function of the substrate Ge fraction, xs, as shown in Table 3.1. As xs increases, biaxial tensile strain in the s-Si increases and biaxial compressive strain in the s-Ge decreases. Increasing strain in s-Si causes the silicon valence and conduction bands to move towards one another, whereas decreasing strain in s-Ge causes the germanium valence and conduction bands to move apart. The net result is that both the s-Si conduction band and s-Ge valence band move lower in energy with increasing xs so that $E_{G,eff}$ remains relatively constant. The same effect causes ΔE_v to decrease with increasing xs. The movement of the bands with strain is shown schematically in Figure 3.8.

The valence band offset extracted in this work is compared to previous experimental work on the s-Si/s-$Si_{1-x}Ge_x$ heterojunction grown on relaxed $Si_{1-xs}Ge_{xs}$ in Figure 3.9. The value extracted in this work for s-Si/s-Ge on ~40% SiGe substrate is in good agreement with the extrapolated value from Ni Chleirigh's data.

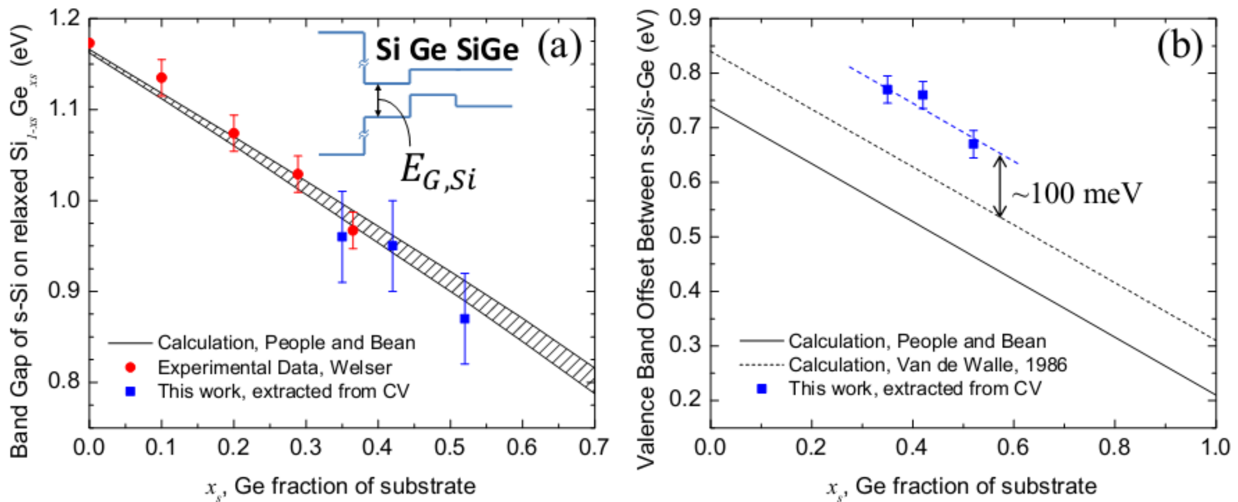

Figure 3.7. (a) Calculations by People and Bean [47] of the band gap of s-Si for different Ge fractions of the relaxed $Si_{1-x}Ge_x$ substrate compared to values extracted from CV analysis in this work. The experimental data from Welser [64] is also included for comparison. (b) Valence band offset, ΔE_v, as a function of Ge fraction in the substrate. People and Bean [47] calculate a linear relation from the 1985 theoretical work by Van de Walle and Martin [48]. The dotted line is a linear relationship derived from updated calculations in Van de Walle and Martin's 1986 paper [46]. The valence band offsets extracted in this work are about 100 meV larger than the linear relationship derived from the theoretical values of [46].

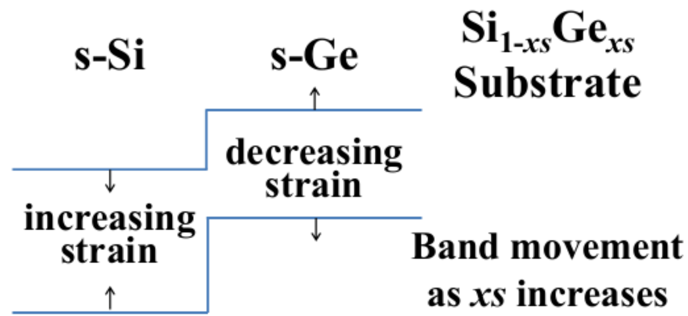

Figure 3.8. Illustration of changes in the band-edge energy with increased Ge fraction in the substrate (xs).

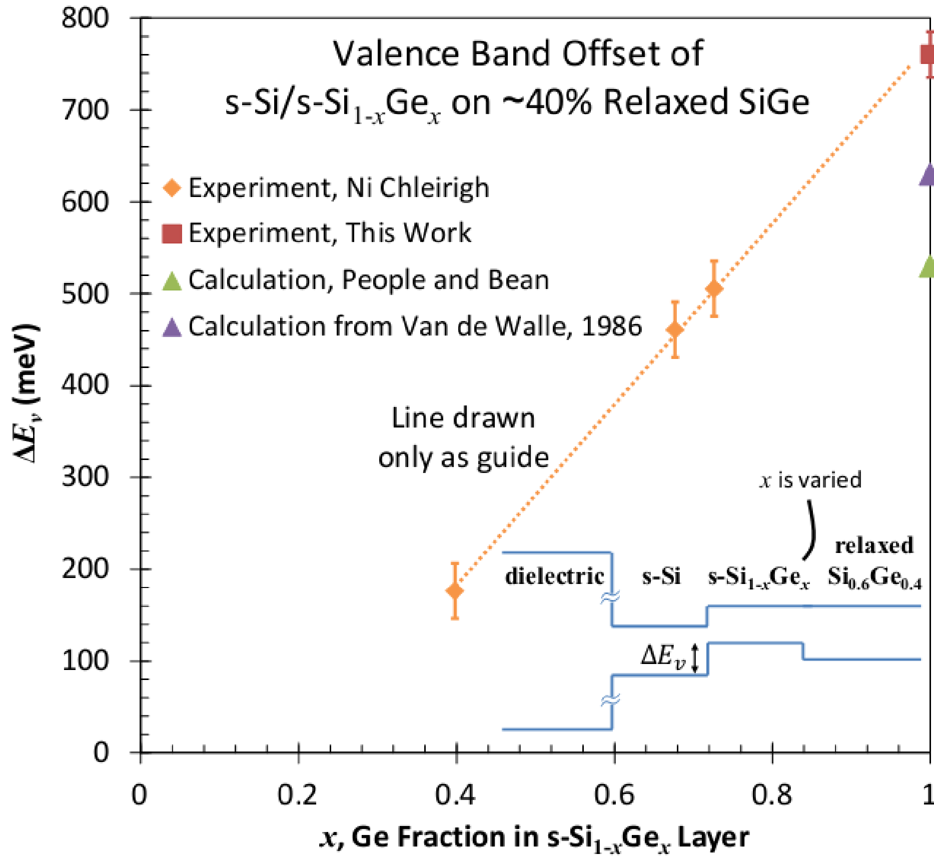

Figure 3.9. Valence band offset for s-Si/s-Si$_{1-x}$Ge$_x$ grown on a relaxed SiGe substrate with ~40% Ge, as a function of Ge fraction in the s-Si$_{1-x}$Ge$_x$ layer. The inset shows a depiction of the heterostructure band diagram highlighting the valence band offset. Ni Chleirigh [71] extracted the valence band offset using a CV technique similar to this work. Both calculations shown in the plot are linear relations derived from theory by Van de Walle and Martin. People and Bean [47] calculate a linear relation from Van de Walle and Martin's 1985 paper [48], while the purple data point is calculated using updated values from Van de Walle and Martin's 1986 paper [46].

3.7 Unified Theoretical Description of the Si-Ge System

The calculation of band lineups based on common reference levels is described in detail by Van de Walle [44]. The starting point is the average energy $E_{v,av}$ of the top three valence bands of each bulk, unstrained semiconductor. For elemental and binary compounds, these averages can be predicted theoretically on a common energy scale. The corresponding energies for alloys are interpolated following Ref. [75]. The average energy $E_{v,av}$ is a convenient reference because it is unaffected by either the shear component of the strain or the spin-orbit interaction. When a strained

heterojunction is formed, only the hydrostatic component of the strain affects the $E_{v,av}$ energies. The corresponding shifts can be calculated using the absolute valence band deformation potentials, a_v, for each material. The shear strain and the spin-orbit interaction split the electronic bands in ways that can be computed using standard deformation potential theory. For the case of unstrained Si/Ge, $\Delta E_{v,av}$ between Si and Ge was calculated to be between 500 and 700 meV [45], [46]. Using the deformation potentials in Table 3.2, which are justified in Appendix A: *Deformation Potentials for Si and Ge*, the value of $\Delta E_{v,av}$ was adjusted to reproduce the 40-meV type-II band offset of $Si_{0.70}Ge_{0.30}$/Si, as observed by Thewalt et al [51], [52]. An exact fit is obtained using $\Delta E_{v,av}$ = 800 meV. Using this value without any other adjustments the band offsets and effective band gaps in the three samples of this work are then calculated using standard deformation potential theory. These are shown as the theoretical entries in Table 3.1.

Representative band lineups calculated with standard deformation potential theory are shown in Figure 3.10. Remarkable agreement of the theoretical predictions with the experimental data is found, particularly when one takes into account the assumption of linear elasticity and deformation potential theory in the presence of very large biaxial strains of up to 2% in Si and -2.7% in Ge. The extracted and theoretical valence band offsets are well within experimental error for two samples and marginally outside experimental error for the sample with the largest strain in the Si layer, whereas the effective band gaps are just below the lower end of the experimental error bar. These effective band gaps, as mentioned above, are more difficult to extract from the data, and their theoretical values are also more sensitive to the exact values of the deformation potentials. Had the sample shown in Figure 3.10 been computed using $\Delta E_{v,av}$ = 600 meV, a value considered until now to be consistent with experiment, the result would have been ΔE_v = 550 meV and $E_{G,eff}$ = 320 meV, in strong disagreement with this work's experimental results. It is also worth noting that the calculations reproduce the weaker dependence of the effective band gap on the substrate composition.

This work's results imply a band offset ΔE_v = 910 meV for the s-Ge/Si interface, much larger than expected from Eq. (3.1). It is instructive to compare this work's results with core-level spectroscopy measurements of the band offsets. In these experiments, the band-edges are measured relative to core levels. The band offsets follow immediately from the data if the core levels are independent of the volume (i.e. if their absolute hydrostatic deformation potential is zero). This

however, is not necessarily the case. Schwartz and coworkers [76] find ΔE_v = 740 ± 130 meV for s-Ge on Si, in agreement with Eq. (3.1), using theoretical Si 2p and Ge 3d deformation potentials which are not known independently, so that the accuracy of their result is difficult to assess. Morar et al. [77] introduced a very elegant transmission electron energy loss method which yields $\Delta E_{v,av}$ between Ge and Si directly from measurements of the Si 2p conduction band absorption edge in relaxed $Si_{1-x}Ge_x$ alloys. They find $\Delta E_{v,av}$ = 690 meV. However, in their estimate of the possible corrections to the assumption of a constant Si 2p level, they compute a volume deformation potential of 2 eV for the 2p level. More detailed calculations by Franceschetti et al. [78], give -0.1 eV for the same deformation potential. If Morar's results are computed using the Franceschetti deformation potential, it is found that their measurements imply $\Delta E_{v,av}$ = 770 meV, in much better agreement with this work's results. Moreover, the most recent *ab initio* calculations of band offsets [79] yield $\Delta E_{v,av}$ = 750 meV for the Si-Ge system, which is also closer to this work's results than previous *ab initio* predictions.

Table 3.2. Selected deformation potentials for Si and Ge. The notation is as in [44], and the values are explained in Appendix A: *Deformation Potentials for Si and Ge*. For alloys, the deformation potentials are linearly interpolated.

	Valence band absolute deformation potential, a_v	Valence band shear deformation potential, b	Hydrostatic deformation potential, $\left(\Xi_d + \frac{1}{3}\Xi_u - a_v\right)^{\Delta}$
Si	2.24 eV	-1.73 eV	1.47 eV
Ge	2.10 eV	-1.88 eV	1.80 eV

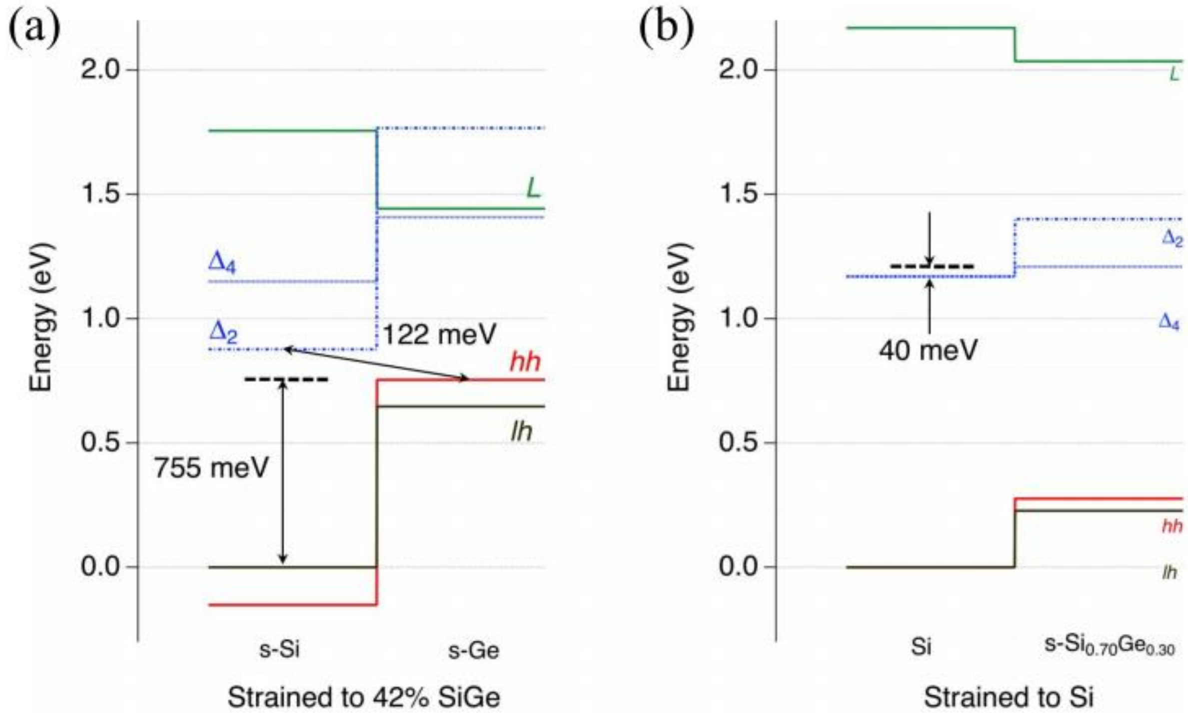

Figure 3.10. Calculated band lineups of the (a) s-Si/s-Ge heterostructure pseudomorphic to 42% SiGe, and (b) s-$Si_{0.70}Ge_{0.30}$/Si heterostructure pseudomorphic to Si using standard deformation potential theory. The calculations assume that the average valence band offset between Si and Ge is $\Delta E_{v,av}$ = 800 meV.

3.8 Summary

The valence band offsets for s-Si/s-Ge heterojunctions pseudomorphic to various relaxed SiGe substrates were extracted by fitting full-band quantum mechanical simulations to experimental MOS-capacitor QSCV measurements. Good agreement was found between simulated and measured CV curves with high sensitivity to the valence band offset of the s-Si/s-Ge heterostructure. Values of ΔE_v = 770, 760, and 670 meV were obtained for 35, 42, and 52% Ge fraction in the SiGe substrates, respectively. The effective band gap was found to be about 190 meV, irrespective of the substrate Ge fraction.

The large valence band offsets measured here, as well as type-II measurements from Thewalt et al. can be simultaneously explained by assuming an average valence band offset, $\Delta E_{v,av}$ = 800 meV between Si and Ge. This value is much larger than usually assumed in simulations of the of the Si-Ge system.

Chapter 4: Impact of Quantization on Body Voltage at Eigenstate Alignment in Bilayer TFETs

The bilayer TFET consists of a thin semiconductor layer bounded by oppositely biased top and bottom gates. For the specific structure described in this work, the top gate is biased positively to attract electrons and the bottom gate is biased negatively to attract holes as shown in Figure 4.1b. Ideally, band-to-band tunneling cannot occur until sufficient bias is applied across the structure such that the electron eigenstate aligns in energy with the hole eigenstate (see Figure 4.1c).

For reasonable tunneling current in the on-state, the distance between the electron wavefunction and hole wavefunction cannot be too large, and so the body thickness of the semiconductor layer should be kept reasonable thin, on the order of 10 nm. However, at these thicknesses, quantization energy increases the gate voltage required to turn on the device, which may limit the power-scaling benefits of the TFET structure.

Lattanzio et al. simulated the bilayer structure for both Si and Ge homostructures and reported impressive results [8], [80]; however, these papers did not elaborate on the impact of quantization. This work provides an in-depth analysis of vertical quantization in the channel of electron-hole bilayer TFETs and suggests fundamental limits to the scalability of the semiconductor body thickness. The evaluation is performed for Si, Ge, and InAs homostructures and the strained-Si/strained-Ge heterostructure. The results highlight the trade-offs between tunneling distance, quantization energy, gate efficiency, and gate leakage current.

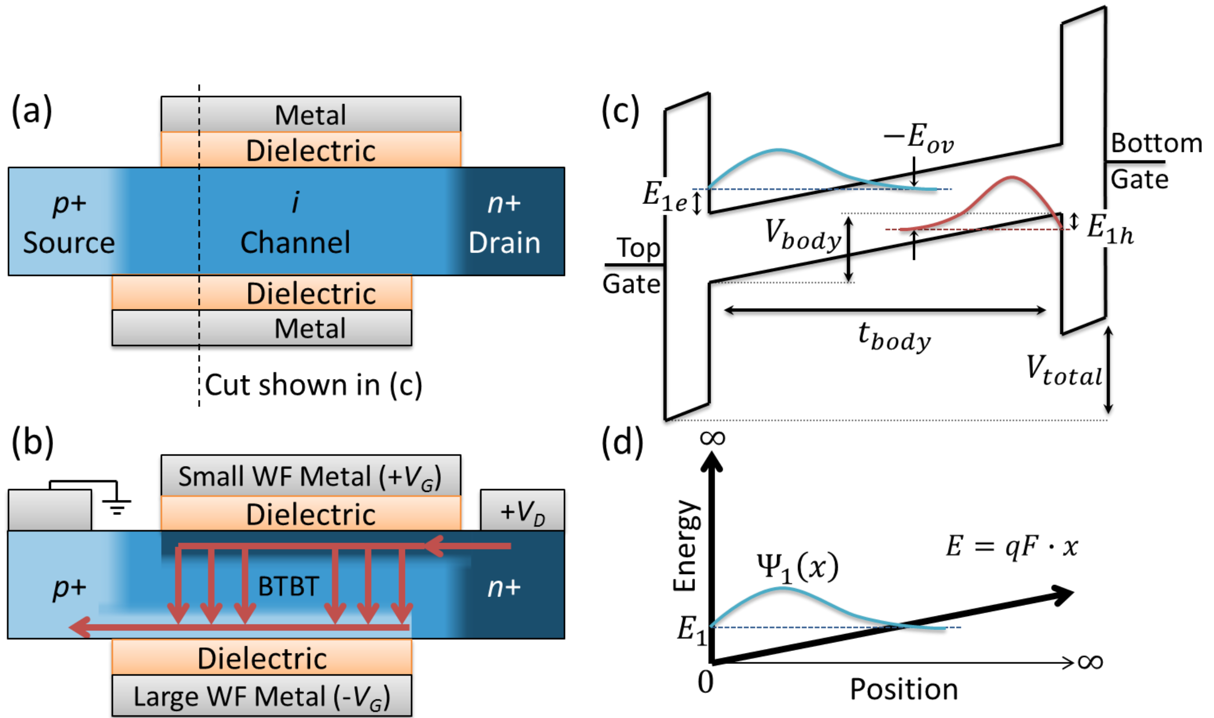

Figure 4.1. (a) Electron-hole bilayer TFET. (b) Structure with applied bias and current flow indicated by arrows. BTBT occurs between electron- and hole-rich layers induced by oppositely-biased top and bottom gates. (c) Vertical band diagram of (a) before eigenstate alignment. Ideal BTBT first occurs when the first electron eigenstate (blue) overlaps in energy with the first hole eigenstate (red). (d) Ideal infinite triangular potential barrier, similar to (c), in which the eigenstates are calculated analytically.

4.1 Bilayer Biasing Scheme

The electron-hole bilayer TFET studied in this work consists of a *p+* source, *n+* drain, and nominally undoped channel bound by offset top and bottom gates with equal dielectric thickness shown in Figure 4.1a. The gates are oppositely biased to create a 2D electron (hole) gas along the top (bottom) gate extending to the *n+* drain (*p+* source). The device turns on when sufficient potential is applied between the gates to enable perpendicular band-to-band tunneling (BTBT) across the channel [81], as shown in Figure 4.1b. To facilitate small *applied* gate voltages, it was suggested [8] that all or part of the voltage be absorbed by the work function difference of the two gate materials; however, common metals only span ~1 eV in work function energy, and voltage differences far beyond this would require new circuit architectures accommodating uneven gate

and drain biases. It is therefore important to assess the range of required voltages, and the impact of this voltage range on device operation.

In this work, the body voltage at the onset of conduction of a bilayer TFET is investigated. The onset of conduction is expected to occur when the first electron and hole eigenstates align in energy. The body voltage is analytically determined in order to deduce the total voltage, the gate efficiency, and the expected gate leakage at the onset of eigenstate alignment at V_{ds} = 0 V.

4.2 Quantization Theory

Figure 4.1c shows a vertical band diagram of the channel with oppositely-biased top and bottom gates. Assuming an ideal triangular potential (shown in Figure 4.1d) for holes and electrons, the quantization energy of the *n*th level is

$$E_n \approx \left(\frac{3\pi}{2}\left(n-\frac{1}{4}\right)\right)^{2/3}\left(\frac{q^2F^2\hbar^2}{2m^*}\right)^{1/3} \; * \tag{4.1}$$

where q is the elementary charge, F is the electric field in the semiconductor, $\hbar$ is the reduced Planck constant, m^* is the effective mass of either holes or electrons in the direction of quantization, and $n = 1, 2, 3, \ldots$ [82]. Equation (4.1) is used to calculate the required potential across the semiconductor, V_{body}, and the entire structure, V_{total}, (shown in Figure 4.1c) at eigenstate alignment in §4.3.

Equation (4.1) assumes an infinite barrier at zero and a triangular potential that goes as $qF \cdot x$ from x = 0 to ∞, as shown in Figure 4.1d. The potential profile of Figure 4.1c can be better approximated by a quantum well with infinite barriers in an electric field (i.e. one that does not extend from x = 0 to ∞). The eigenfunctions for such a potential profile can be written as a combination of Airy functions. The exact eigenenergies for a quantum well in an electric field can be found by solving [84]

$$A_i\left(-\frac{E}{\hbar\omega_c}\right)B_i\left(a_c-\frac{E}{\hbar\omega_c}\right)-B_i\left(-\frac{E}{\hbar\omega_c}\right)A_i\left(a_c-\frac{E}{\hbar\omega_c}\right)=0 \tag{4.2}$$

---

* The eigenfunction solutions to the Schrödinger equation for the triangular potential problem are two linearly independent Airy functions provided in Eq. (4.3). The expression for the energy levels is inexact because the zeros of the Airy functions (i.e. $\{x|A_i(x) = 0\}$), used to find the eigenenergy, cannot be expressed analytically [82], [83].

where $A_i(x)$ and $B_i(x)$ are the two linearly independent solutions to the differential equation $y'' - xy = 0$ and are given by

$$A_i(x) = \frac{1}{\pi}\int_0^\infty \cos\left(\frac{u^3}{3} + xu\right) du \tag{4.3a}$$

$$B_i(x) = \frac{1}{\pi}\int_0^\infty \left[\sin\left(\frac{u^3}{3} + xu\right) + \exp\left(-\frac{u^3}{3} + xu\right)\right] du \tag{4.3b}$$

and

$$a_c = \pi\sqrt{\frac{\hbar\omega_c}{E_0}}; \quad \omega_c = \frac{(qF)^{2/3}}{(2m^*\hbar)^{1/3}}; \quad E_0 = \frac{\hbar^2\pi^2}{2m^*L^2} \tag{4.4}$$

A_i and B_i are the Airy functions of the first and second kind, E_0 is the ground state energy for the quantum well (QW) with zero field, and L is the length of the QW.

Equation (4.1) is an excellent approximation of the solution of Eq. (4.2) when the condition

$$qV_{body} \gg E_o \tag{4.5}$$

is satisfied. In words, this occurs when the potential drop across the QW ($qV_{body} = qF \cdot L$) is much greater than the ground state quantization energy of the QW (E_0). Equation (4.5) is met when the ground state energy is minimized, which occurs in QWs with a heavy carrier mass or wide width. Under this condition, confinement due to the triangular electric field is much more significant than confinement due to the infinite walls of the QW.†

In the strained-Si/strained-Ge bilayer heterostructure, electrons and holes are confined to the Si and Ge layers, respectively (see Figure 4.2). The ground state energy of electrons in a 5-nm Si QW is only 0.016 eV due to the heavy longitudinal mass of electrons in the [100] direction. The ground state energy of holes in a 5-nm Ge QW is only 0.046 eV. Since the values of E_0 for both electrons and holes are so small, the condition of Eq. (4.5) is satisfied for most body voltages. Thus, it is reasonable to approximate the QWs of the strained-Si/strained-Ge bilayer

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† In the case where the potential drop across the QW is much greater than the ground state energy, the variational method [85] and the perturbative approach [86] to calculating the eigenenergies in a QW under bias are invalid and give significant errors from the exact solution.

heterostructure as a triangular potential that goes as from zero to infinity using Eq. (4.1), where E_{1e} and E_{1h} are calculated using m_l for Si and m_{hh} for Ge, respectively.

To verify the use of Eq. (4.1) in modeling the strained-Si/strained-Ge heterostructure, the minimum possible value of V_{body} at eigenstate alignment is determined, and it is verified that Eq. (4.5) is still satisfied. The body voltage (V_{body}) must be at least as large as the effective band gap ($E_{G,eff}$) at eigenstate alignment. For this case, where $qV_{body} = E_{G,eff} = 0.2$ eV, the condition of Eq. (4.5) is satisfied, and the use of Eq. (4.1) is justified for body voltages at eigenstate alignment.

Equations (4.1) and (4.2) both assume a constant vertical electric field throughout the semiconductor body, yet any charge distribution in the body will create a non-uniform field. Indeed, appreciable charge distributions do accumulate near the top and bottom gates at eigenstate alignment, i.e. at the expected sharp onset of conduction, which causes a larger electric field near the semiconductor surface than by simply assuming $F = V_{body}/t_{body}$. The analytical approximation to numerical simulations of the actual structure is compared in §4.3, and it is found that the analytical solution adequately and succinctly captures the physics of the problem and provides insight into the parameters that affect quantization.

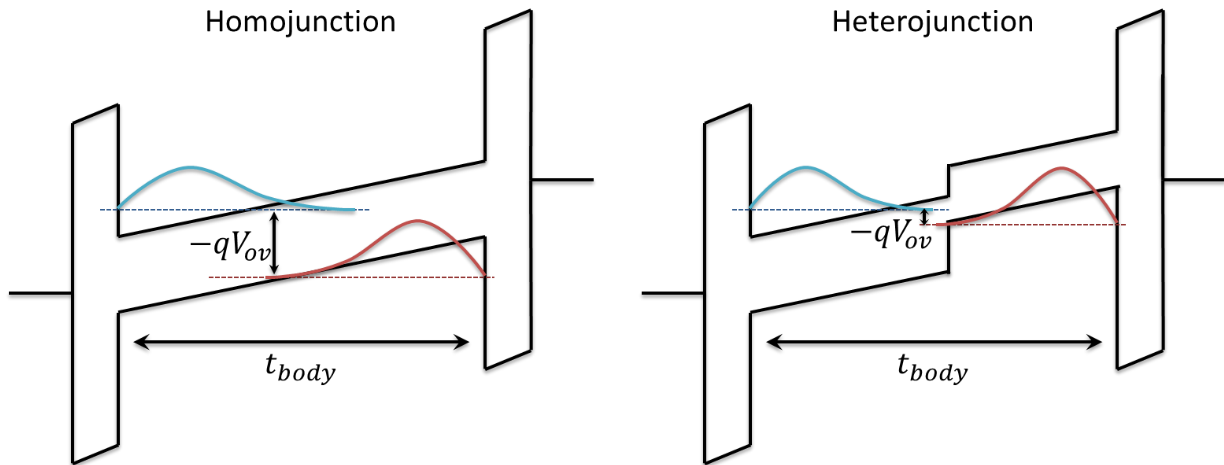

Figure 4.2. Depiction of the electron and hole eigenstates in a homojunction and heterojunction structure. qV_{ov} is the energy overlap of the electron and hole eigenstates, and a negative value indicates that the eigenstates are not yet overlapped.

4.3 Body Voltage at Eigenstate Alignment

Using Eq. (4.1), the energy overlap (E_{ov}) is determined between the first electron and hole eigenstates as a function of the vertical potential difference across the semiconductor body, and it is given by

$$E_{ov} = qV_{body} - (E_G + E_{1e} + E_{1h}) \tag{4.6a}$$

$$= qV_{body} - E_G - \left(\left(\frac{9\pi}{8}\right)^{2/3}\left(\frac{\hbar^2}{2}\right)^{1/3}\left(\frac{qV_{body}}{t_{body}}\right)^{2/3}\left[\left(\frac{1}{m_e^*}\right)^{1/3} + \left(\frac{1}{m_h^*}\right)^{1/3}\right]\right) \tag{4.6b}$$

E_G is the bulk semiconductor band gap, E_{1e} and E_{1h} are the quantization energy for the first electron and hole eigenstates, t_{body} is the semiconductor thickness, and m_e^* and m_h^* are electron and hole effective masses along the quantization direction—assumed to be [100] in this work. The first electron and hole eigenstates are aligned in energy when $E_{ov} = 0$, which is called *eigenstate alignment*.

For the strained-Si/strained-Ge heterostructure, Eq. (4.6) is slightly modified to

$$E_{ov} = qV_{body} - \left(E_{G,eff} + E_{1e,Si} + E_{1h,Ge}\right) \tag{4.7a}$$

$$= qV_{body} - E_{G,eff} - \left(\left(\frac{9\pi}{8}\right)^{2/3}\left(\frac{\hbar^2}{2}\right)^{1/3}\left(\frac{qV_{body}}{t_{body}}\right)^{2/3}\left[\left(\frac{1}{m_{e,Si}^*}\right)^{1/3} + \left(\frac{1}{m_{h,Ge}^*}\right)^{1/3}\right]\right) \tag{4.7b}$$

Equation (4.6) or (4.7) is solved at eigenstate alignment ($E_{ov} = 0$) to find V_{body} as a function of t_{body} for Si, Ge, InAs, and the strained-Si/strained-Ge heterostructure, and the result is shown in Figure 4.3. A runaway condition occurs at small t_{body} when the confinement energy becomes exceedingly large.

The Schrödinger-Poisson equations are self-consistently solved with *nextnano3* [73] using the effective mass quantization method for the structure shown in Figure 4.1c. The numerical results for the InAs body with infinite and finite dielectric energy barriers is plotted in Figure 4.3. The HfO_2 dielectric parameters from [87] were used in the numerical simulation of the finite barrier, except that the conduction and valence band barriers for HfO_2/InAs were set to 2.36 and 3.11 eV, respectively, due to the electron affinity difference of InAs and Si. As expected, the analytical infinite triangular potential solution of Eq. (4.6) compares very well with the numerical solution for infinite barriers, but the finite barrier solution yields a smaller V_{body} at eigenstate alignment

due to wavefunction penetration into the dielectric resulting in less quantization. Though a finite barrier reduces the voltage required for eigenstate alignment, wavefunction penetration into the dielectric results in increased gate leakage current.

Of the chosen materials, InAs exhibits the widest variation between finite and infinite barrier solutions due to its small conduction band mass. Quantization of electrons in the Γ-band of InAs increases rapidly for body thickness less than 10 nm. This may lead to electron population of the L- and X-bands at eigenstate alignment. Nonparabolicity of the InAs Γ-conduction-band will increase the quantization mass [88], but doubling m_e^* only reduces the quantization energy by 20% due to the $-1/3$ power-law dependence on mass. Therefore, the non-parabolicity is not expected to substantially affect this work's conclusions.

Table 4.1. Semiconductor material properties used in calculations. The effective mass is calculated along $[100]$ for the lowest energy (heaviest) eigenstate. Subscripts l, t, Γ, and hh denote longitudinal, transverse, gamma-point, and heavy-hole masses, respectively. The relative permittivity is given by ϵ_r.

	Si	Ge	InAs	strained-Si/strained-Ge
E_G (eV)	1.12	0.66	0.35	0.20
m_e^* (m_o)	$m_l = 0.92$	$\frac{3m_l m_t}{m_t + 2m_l} = 0.12$	$m_\Gamma = 0.026$	$m_{l,Si}$
m_h^* (m_o)	$m_{hh} = 0.49$	$m_{hh} = 0.33$	$m_{hh} = 0.41$	$m_{hh,Ge}$
ϵ_r	11.7	16.2	15.15	--

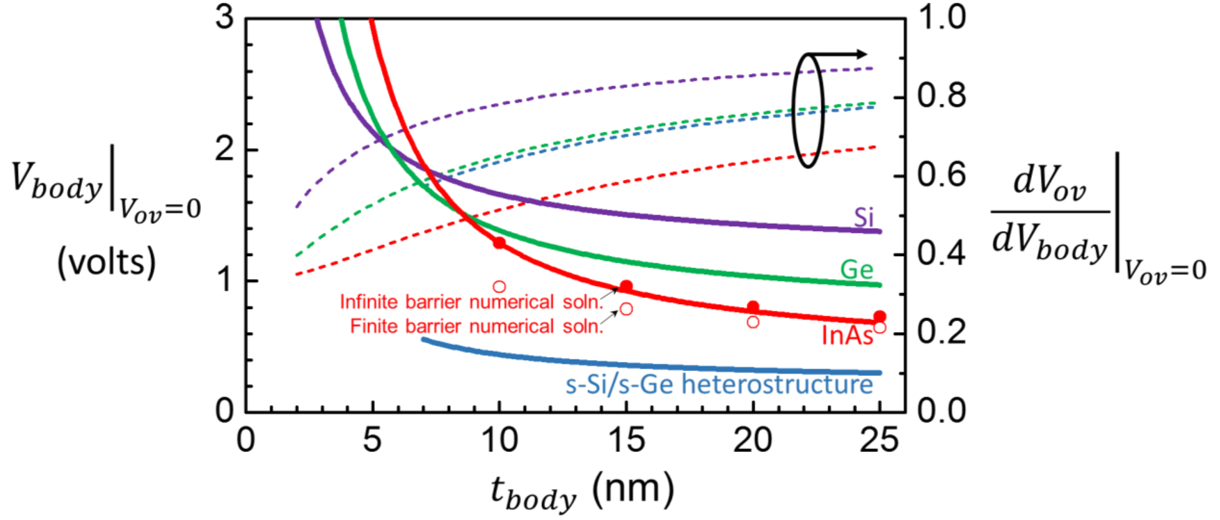

Figure 4.3. Body voltage V_{body} (solid lines) and body-voltage efficiency dV_{ov}/dV_{body} (dashed lines) at eigenstate alignment ($V_{ov} = 0$) as a function of body thickness calculated analytically for an infinite triangular well using Eqs. (4.6)-(4.8). Symbols represent numerical calculations of V_{body} at eigenstate alignment for an InAs structure shown in Figure 4.1c. At small body thicknesses, V_{body} surges because of the rapidly growing quantization energy. qV_{ov} is the energy overlap between electron and hole eigenstates, depicted in Figure 4.2. The material parameters used in the calculation are provided in Table 4.1.

4.4 Gate Efficiency at Eigenstate Alignment

The incremental body-voltage efficiency (dV_{ov}/dV_{body}) is calculated from the derivative of Eq. (4.6b) or (4.7b) and is given by

$$\frac{dV_{ov}}{dV_{body}} = 1 - \left(\left(\frac{9\pi}{8t_{body}}\right)^{2/3}\left(\frac{\hbar^2}{2}\right)^{1/3}\left[\left(\frac{1}{m_e^*}\right)^{1/3} + \left(\frac{1}{m_h^*}\right)^{1/3}\right]\right)\cdot\frac{2}{3}\left(qV_{body}\right)^{-1/3} \tag{4.8}$$

where $qV_{ov} = E_{ov}$. The incremental body-voltage efficiency is plotted in Figure 4.3 at eigenstate alignment ($V_{ov} = 0$) for different body thicknesses of Si, Ge, InAs, and the strained-Si/strained-Ge heterostructure.

Of particular interest is that for a given t_{body}, m_e^*, and m_h^*, a larger V_{body} yields better body-voltage efficiency due to the $V_{body}^{-1/3}$ dependence of Eq. (4.8). To understand this dependence, it is helpful to recall the $F^{2/3}$ dependence of the confinement energy of an infinite triangular potential from Eq. (4.1). The rise of the triangular confinement energy (dE_n/dF) is sharpest for small

electric fields. Since the body voltage is proportional to the electric field, it is expected that the sharpest rise in the confinement energy for electron and hole eigenstates (dE_n/dV_{body}) would occur for small body voltages.

By applying a body voltage, the electron and hole eigenstates are brought closer together in energy, but any increase in confinement (due to the electric field created by the body voltage) separates the eigenstates. Because of this effect, the right-hand axis of Figure 4.3 shows that the incremental body-voltage efficiency for the strained-Si/strained-Ge heterostructure is lower than both Si and Ge at any given body thickness because V_{body} at eigenstate alignment is significantly reduced in the heterostructure. A reduced V_{body} is helpful for reducing the gate voltage required to turn on a bilayer TFET, but the reduced body-voltage efficiency will limit the SS of the device, negating some of the benefits and making a steep switching characteristic harder to realize.

Quantization limits the efficiency to less than 1. *Increasing the body voltage, in order to increase eigenstate overlap, increases the electric field, which in turn increases quantization.* The corresponding incremental gate-voltage efficiency is calculated as the product of dV_{ov}/dV_{body} and dV_{body}/dV_{total}, which represents the fraction of the total gate-to-gate incremental voltage (dV_{total}) that appears across the semiconductor body. The voltage across the gate dielectrics can be calculated from the electric field at the semiconductor surface ($\epsilon_{ox}F_{ox} = \epsilon_{semi}F_{semi}$).

Reduced gate efficiency is especially troubling for materials with small effective mass. For a 20-nm InAs body with a 1-nm effective oxide thickness (EOT), the total gate-to-gate voltage efficiency at eigenstate alignment is given by $\frac{dV_{ov}}{dV_{total}} = \frac{dV_{ov}}{dV_{body}} \cdot \frac{dV_{body}}{dV_{total}} = 0.63 \cdot 0.72 = 0.45$.[‡] The total gate efficiency declines to 0.29 when the body thickness is decreased to 10 nm. Therefore, in order to realize a gate-voltage SS ($dV_{total}/dlog(I)$) of less than 60 mV/decade in a 10-nm InAs structure, the internal SS ($dV_{ov}/dlog(I)$) must be lower than 18 mV/decade due to the poor gate efficiency.

4.5 Gate Leakage

Large electric fields exist in the gate dielectric at eigenstate alignment, which can cause significant gate tunneling current that will increase off-state current and inhibit the small SS seen at low

[‡] Relative permittivity values used in the calculation are provided in Table 4.1.

currents in simulations [8], [80]. Increasing the body thickness decreases the electric field, but at the expense of the on-current, since tunneling probability depends exponentially on tunneling distance.

The experimental data for scaled HfO_2/SiO_2 compound dielectrics on Si is used to estimate the gate leakage [87]. Results are shown for Si (Figure 4.4a) and InAs (Figure 4.4b) vs. body thickness and EOT at eigenstate alignment. The dielectric field of the experimental nFETs of [87] is calculated, and the field is mapped to the corresponding body thickness of the bilayer TFET structure at eigenstate alignment. The gate leakage current at eigenstate alignment as a function of t_{body} for EOT values between 0.61 and 0.97 nm is then interpolated from the experimental J_{gate} $vs.$ V_{gate} plots. The gate leakage analysis is performed for InAs (Figure 4.4b) using the same experimental data as for Si, assuming that the compound HfO_2/SiO_2 dielectric on Si represents the best-expected performance for dielectrics on other material systems. Remarkably, the gate leakage contours of Figure 4.4a and Figure 4.4b are quite similar. Though the net voltage required for eigenstate alignment is lower for InAs compared to Si for large body thicknesses, the 30% larger permittivity of InAs causes a higher electric field in the dielectric, and these effects compensate each other.

Figure 4.4 represents the design tradeoff between gate leakage, total voltage, and body thickness. Increasing the dielectric thickness exponentially decreases gate leakage but increases V_{total} for a given V_{body} which reduces gate efficiency. Based on this analysis, it is believed that an InAs electron-hole bilayer TFET with a body thickness of ~15 nm and an EOT of ~0.9 nm may represent a reasonable balance between off- and on-state performance: smaller body thickness and EOT result in objectionably high leakage current; larger body thickness would greatly reduce tunneling probability and therefore on-state current; and thicker EOT requires larger total voltages.

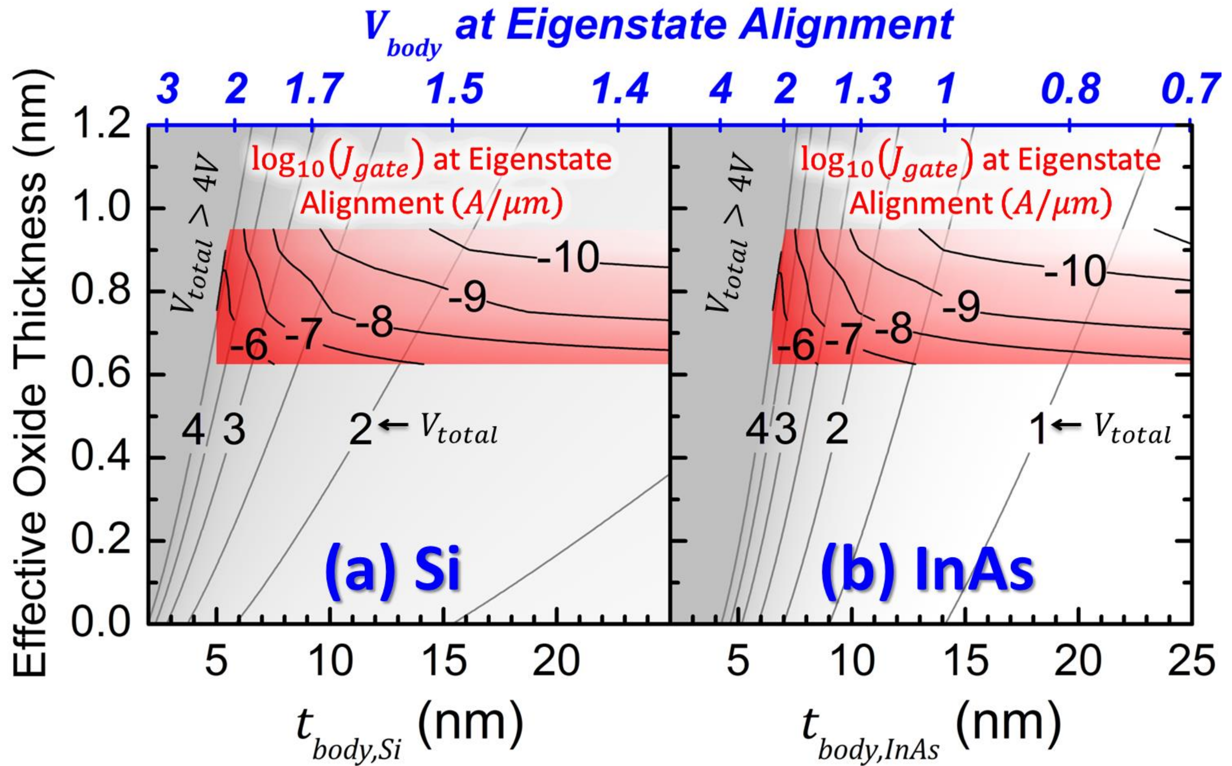

Figure 4.4. Gate leakage current (inset black contours with red shading) and V_{total} (gray contours) at eigenstate alignment as a function of effective oxide thickness and body thickness for (a) Si and (b) InAs. The leakage current is derived from high-κ on Si experimental data [87], and the top axis (V_{body}) is derived from Figure 4.3. The gate leakage (in $A/\mu m$ of width) is calculated for a 50-nm gate length but can be scaled linearly with gate length. Decreasing t_{body} increases V_{body} (due to quantization) and thus increases the electric field and gate leakage current. While InAs generally requires less voltage for eigenstate alignment compared to Si, the 30% larger relative permittivity of InAs causes a higher dielectric field resulting in similar gate leakage current contours.

4.6 Summary

The adverse effect of increasing quantization energy with decreasing body thickness on the gate efficiency of proposed electron-hole bilayer TFETs has been shown. The gate leakage tunneling current is also shown to increase dramatically with decreased body thickness at small EOT, limiting the minimum body thickness that can be used for such devices in the quest for increased source-drain current. The SS of experimental devices is expected to be significantly degraded compared to reported ideal simulations due to gate leakage caused by large electric fields at

eigenstate alignment. Additionally, the strained-Si/strained-Ge heterostructure is shown to significantly reduce the body voltage required for eigenstate alignment.

Chapter 5: Electrostatic Design of Perpendicular TFETs

Often, perpendicular TFETs are conceptualized as 1D devices where the switching physics occurs along a vertical cross-section of the channel. This methodology was used in Chapter 4: *Impact of Quantization on Body Voltage at Eigenstate Alignment in Bilayer TFETs* to study the voltage required for eigenstate alignment for devices made from different materials and different body thicknesses. The 1D approach is powerful for deriving analytical expressions and exploring trends; however, perpendicular TFETs are inherently two-dimensional devices. The 1D methodology neglects effects occurring near the edges of the tunneling region where electrostatics vary in two-dimensions. These 2D effects can have significant consequences to the subthreshold behavior of perpendicular TFETs. This chapter examines the impact of transistor geometry on 2D electrostatics.

5.1 Perpendicular TFET Designs

Un-optimized electrostatic design of TFET structures can contribute to significant degradation of the subthreshold swing seen in experimental devices (see §1.2.1 more discussion on the subthreshold swing). The swing degradation is often not captured in device simulations due to poor calibration of the band-to-band tunneling (BTBT) tunneling parameters, which exponentially affect the tunneling rates.* Furthermore, theoretical analysis of tunneling (such as the author's works [89], [90]) often neglects two-dimensional effects such as the parasitic tunneling path at the focus of this chapter.

Figure 5.1 shows two related perpendicular TFET designs: the air-bridge and pillar structures. Advantages of these perpendicular structures include 1) tunneling aligned with the gate electric field for enhanced gate modulation, 2) a two-dimensional tunneling area for increased current-drive, and 3) elimination of direct source-to-drain leakage paths, which excludes designs in which the p layer extends all the way to the drain. Perpendicular TFETs have been fabricated using the

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* The BTBT rate is often modeled as $R_{net} = AF^P exp(-B/F)$, where R_{net} is the net recombination rate, F is the electric field, and A, B, and P are model parameters. As B is increased, tunneling at low fields decreases sharply due to the exponential dependence, and the majority of tunneling occurs only at high fields. Simulations may show that only purely perpendicular BTBT (and not parasitic diagonal tunneling) occurs in a device structure with specific tunneling parameters, but this may not represent the actual tunneling physics in a physical device.

direct-gap p+InP/n+InGaAs [91], p+AlGaSb/n-InAs [92], p+GaSb/n-InAs [93], and p+GaAsSb/n-InGaAs [32] material systems, but the results of this current analysis are general and can be applied to most perpendicular p-n homo- or heterostructures. The on-state of such structures is achieved when sufficient gate bias is applied such that the conduction band (CB) of the n layer lies below the valence band (VB) of the p layer so that electrons tunnel from the p layer VB to the n layer CB.

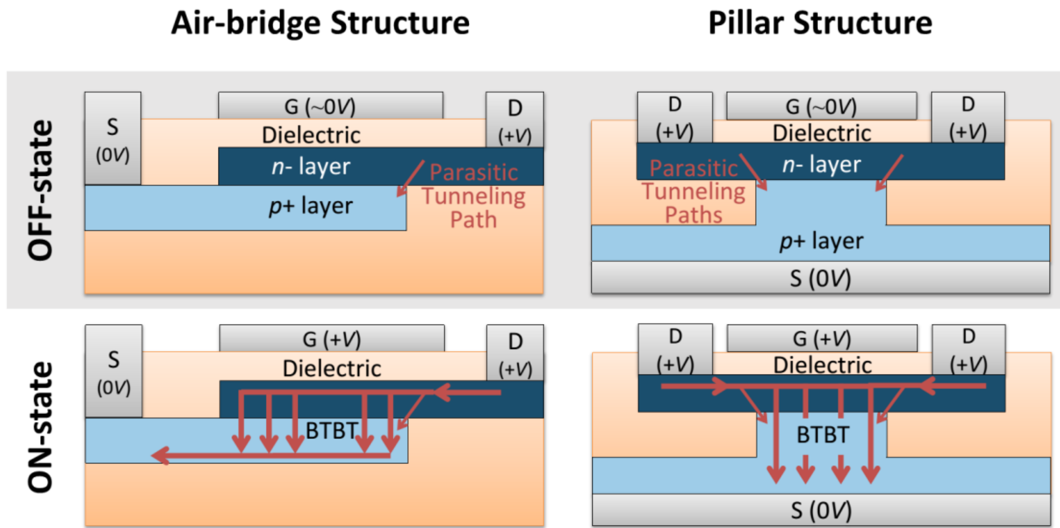

Figure 5.1. Diagram of the air-bridge and pillar structures in the OFF- and ON-states. The red arrows indicate BTBT currents. Both structures suffer from diagonal parasitic tunneling that limits OFF-state current and degrades the switching abruptness.

5.2 Non-uniform Electrostatics in Perpendicular Structures

Non-perpendicular tunneling paths exist in the off-state (Figure 5.1), which degrade the switching characteristics. The p+ layer depletes the thin n- material directly above it; however, where the p+ layer is absent, the n- material is not depleted, which results in a lower CB energy. Electrons from the p+ VB initially tunnel diagonally at the device edges to the lower CB before tunneling vertically at larger gate bias (Figure 5.2). The diagonal parasitic tunneling paths have a longer tunneling distance and lower electric field compared to pure perpendicular tunneling which result in smaller currents (Figure 5.3). Once sufficient gate bias is applied, perpendicular tunneling dominates due to the larger tunneling area, smaller tunneling distance, and larger electric field.

Figure 5.3 depicts the impact of the parasitic tunneling paths on the overall transfer characteristics. While the turn-on of each leakage path is individually sharp, the sum of all the paths results in a degraded transfer characteristic. In order to realize abrupt switching, the parasitic paths—caused by the large *horizontal* electric field created by the abrupt termination of the *p*+ layer—must be eliminated. Direct source-to-drain leakage will result if the *p*+ layer extends to the drain. If one could control the lateral doping profile, such that the *p*+ layer gradually became intrinsic towards the drain-end, these parasitic paths could be avoided, but processing and material limitations restrict this in practice.

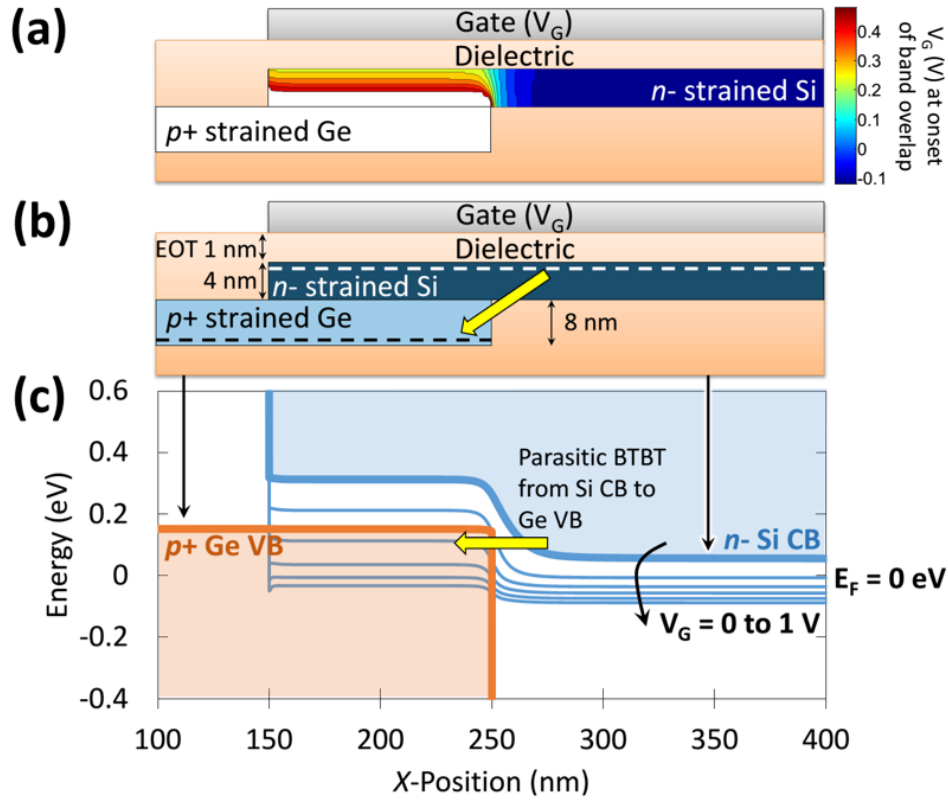

Figure 5.2. The horizontal axes of (a)-(c) are aligned and all plots assume zero source and drain bias. (a) Gate voltage (V_G) at which the *n*- strained-Si CB first overlaps in energy with the *p*+ strained-Ge VB as a function of position in the device. Overlap of the CB directly above the *p* layer requires an additional 0.3 V of V_G compared to the un-depleted *n* region to right of the *p* layer. The simulation was computed neglecting quantization. (b) Diagram of the air-bridge structure in the off-state for the strained *p*+Ge/*n*-Si material system. Vertical dimensions of the simulated structure are provided. (c) Simulated energy band diagram as a function of horizontal position in the device [73]. The VB is plotted for the bottom of the 5×10^{19} cm^{-3} *p*+ Ge layer while the CB is plotted for the top of the 1×10^{18} cm^{-3} *n*- Si layer as indicated by dashed lines shown in (b). Increasing gate voltage (V_G) lowers the Si CB energy, but does not affect the VB at the bottom of the Ge layer due to its heavy doping and distance from the gate. The rise in the CB energy for $x < 250$ nm is caused by depletion of the *n*- Si due to the *p*+ layer. The yellow arrows indicate the diagonal parasitic tunneling path that limits the off-state current and switching abruptness.

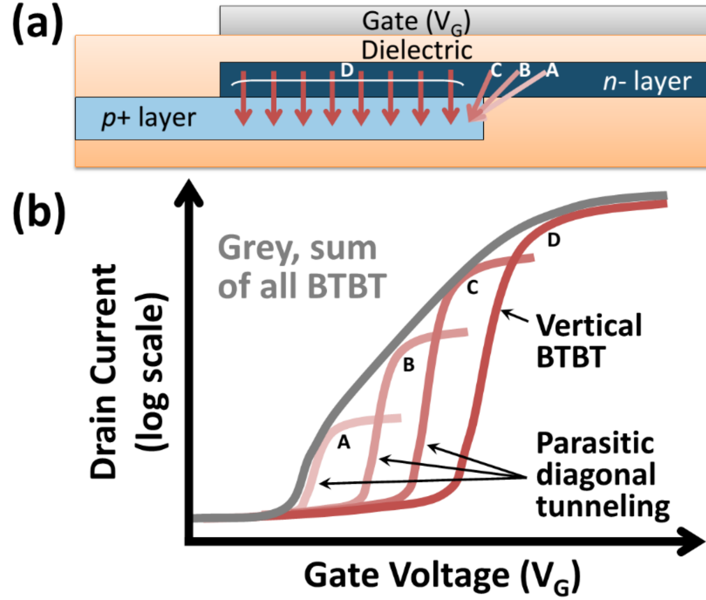

Figure 5.3. Diagram of the air-bridge structure with dark red arrows (labeled D) indicating the desired perpendicular BTBT path and light red arrows (labeled A-C) indicating parasitic tunneling paths. (b) Sketch of drain current versus gate voltage for a hypothesized device. The colored curves represent the contribution of each of the tunneling paths depicted in (a). Each individual tunneling path generates a steep swing, but the summation of all the tunneling paths (gray curve) results in a very gradual turn-on. Parasitic tunneling paths must be eliminated in order to realize a steep turn-on.

5.3 Analytical Framework for Modeling Electrostatics in Perpendicular TFETs

In this section, the analytical expressions for the potential as a function of position in short-channel MOSFETs are reviewed. It is then shown how the analytical expressions for MOSFETs can be mapped to perpendicular TFETs, so that the electrostatics can be better understood.

5.3.1 Characteristic Length λ in Short-Channel MOSFETs

For a bulk semiconductor device, the characteristic length λ over which potential fluctuations occur is given by [28]

$$\lambda_{bulk} = \sqrt{\frac{\epsilon_{semi}}{\epsilon_{ox}} t_{d,semi} t_{ox}} \tag{5.1}$$

where ϵ_{semi} and ϵ_{ox} are the electric permittivities of the semiconductor and oxide, $t_{d,semi}$ is the semiconductor depletion region thickness under the specific bias conditions, and t_{ox} is the oxide thickness. For a fully-depleted silicon-on-insulator (FDSOI) MOSFET (shown in Figure 5.5), the total depletion thickness is limited to the physical semiconductor body thickness t_{semi}, and the characteristic length can be rewritten as [94], [95]

$$\lambda_{FDSOI} = \sqrt{\frac{\epsilon_{semi}}{\epsilon_{ox}} t_{semi} t_{ox}} \tag{5.2}$$

For the short-channel FDSOI MOSFET described in [95], the potential across the channel can be written as

$$\phi(x) = \frac{\phi_s\left(e^{(L_{eff}-x)/\lambda} - e^{-(L_{eff}-x)/\lambda}\right) + \phi_d\left(e^{x/\lambda} - e^{-x/\lambda}\right)}{e^{L_{eff}/\lambda} - e^{-L_{eff}/\lambda}} \tag{5.3}$$

where x is the lateral position along the channel from the source to the drain, L_{eff} is the effective channel length, and ϕ_s and ϕ_d are the potentials at the source- and drain-ends of the channel referenced with respect to the channel potential of a long-channel device.[†] The potential of a long-channel device is defined as the zero reference potential, i.e. $\phi = 0$. Using this reference scheme, the potentials at the source- and drain-end of the channel are expressed as

$$\phi_s \equiv \phi(0) = V_{bi} - \Phi_{gs} + \frac{qN_A}{\epsilon_{semi}}\lambda^2 \tag{5.4a}$$

$$\phi_d \equiv \phi(L_{eff}) = V_{bi} - \Phi_{gs} + \frac{qN_A}{\epsilon_{semi}}\lambda^2 + V_{ds} \tag{5.4b}$$

Equation (5.3) is plotted for $\phi_s = \phi_d = 1$ in Figure 5.6. The plot shows that λ determines the exponential decay from the potential at the source- or drain-end to the long-channel potential ($\phi = 0$). The potential decays roughly as $e^{-x/\lambda}$, and at a distance of the λ from the source, the potential has dropped by a factor of $1/e$. Over 95% of the total potential drop occurs over a distance of 3λ from the source-edge of the channel.

[†] A long-channel device is one in which the source and drain potentials have little influence on the potential at the center of the channel, i.e. the potential at the center of the channel is determined solely by the gate and channel doping.

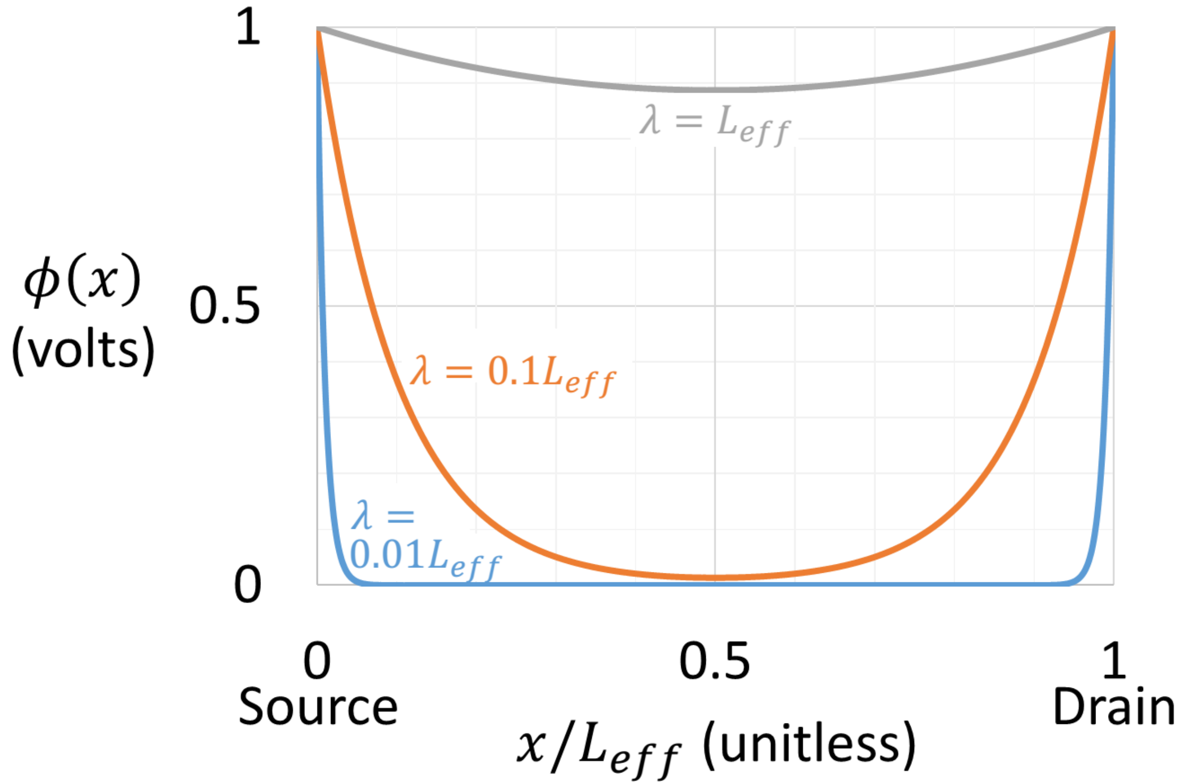

Figure 5.4. Channel potential $\phi(x)$ of a FDSOI MOSFET as a function of the normalized channel position (x/L_{eff}), calculated from Eq. (5.3) using $\phi_s = \phi_d = 1$V and $\phi \equiv 0$ for a long-channel device. The characteristic length λ is varied from 0.01 to 1× the effective channel length L_{eff}. The plot shows that λ determines the exponential decay length of the potential from the source and drain.

5.3.2 Characteristic Length λ in TFETs

The basic structure of a perpendicular TFET and a FDSOI MOSFET are shown in Figure 5.5. The middle illustration shows a conceptualized device where the $p+$ layer of the TFET is replaced with a *virtual* contact in intimate contact with the *n-* layer. The virtual contact depletes the *n-* layer in the same way as the $p+$ layer in the top illustration. Similarity between the middle illustration and the FDSOI MOSFET can be readily seen—both devices have a middle region of low electron concentration with a region of higher electron concentration to the right.

The potential profile of the channel at the right-edge of the $p+$ layer (or alternatively, the right-edge of the virtual contact) is of particular importance in determining the likelihood of parasitic diagonal tunneling paths discussed in §5.2 and shown in Figure 5.2. Tunneling probability

decreases exponentially with tunneling distance. Therefore, one would expect minimal impact to the TFET subthreshold behavior if the potential decays very slowly from the right-edge of the $p+$ layer; however, if the potential decays quickly, as shown by the Si CB plotted in Figure 5.2c, diagonal tunneling can become problematic as the device turns on right-to-left, as depicted in Figure 5.3, and the subthreshold swing is degraded.

The characteristic length over which the potential in the channel varies with position is the same for the TFET as it is for the FDSOI MOSFET. The expression is restated for clarity:

$$\lambda_{TFET} = \lambda_{FDSOI} \tag{5.5}$$

The rationale is explained as follows: the virtual contact of the middle illustration of Figure 5.5 can be thought of as a source contact since it sets the potential of the bottom surface of the *n*- layer.[‡] The lateral potential change from the right-edge of the virtual contact to the gated *n*- layer near the drain is analogous with the potential change from the right-edge of a doped-source region to the gated *n*- region of an FDSOI MOSFET.

While a small λ is advantageous for mitigating short-channel effects in scaled MOSFETs, smaller λ for TFETs, which corresponds to more spatially abrupt potential change, suggests that the parasitic diagonal tunneling shown in Figure 5.2c could become more problematic as the parasitic tunneling distance becomes shorter.

Increasing λ to decrease parasitic tunneling is problematic: one straightforward technique to increase λ in perpendicular TFET designs is to increase either the oxide thickness or semiconductor body thickness; however this approach is undesirable since increasing the oxide thickness decreases gate efficiency and increasing the body thickness increases the tunneling distance for all paths, including the desired perpendicular tunneling, significantly reducing on-current. Additionally, increased λ limits the scalability of the device.

Another method that could be used to reduce lateral potential variation across the device is to have a continuous $p+$ layer in which the doping gradually decreases as it approaches the drain; however, such a structure would be extremely difficult to realize. In the following section, a bilayer TFET design that uses *electrostatic* doping is presented. In such a device, the electrostatic doping

[‡] In an abrupt *p*+*n*- junction, nearly all of the built-in potential is dropped across the *n*- region.

can be made to gradually decrease through the use of a thick back-gate dielectric. The bilayer design can significantly reduce the lateral potential variation, but scalability of such a structure remains a problem.

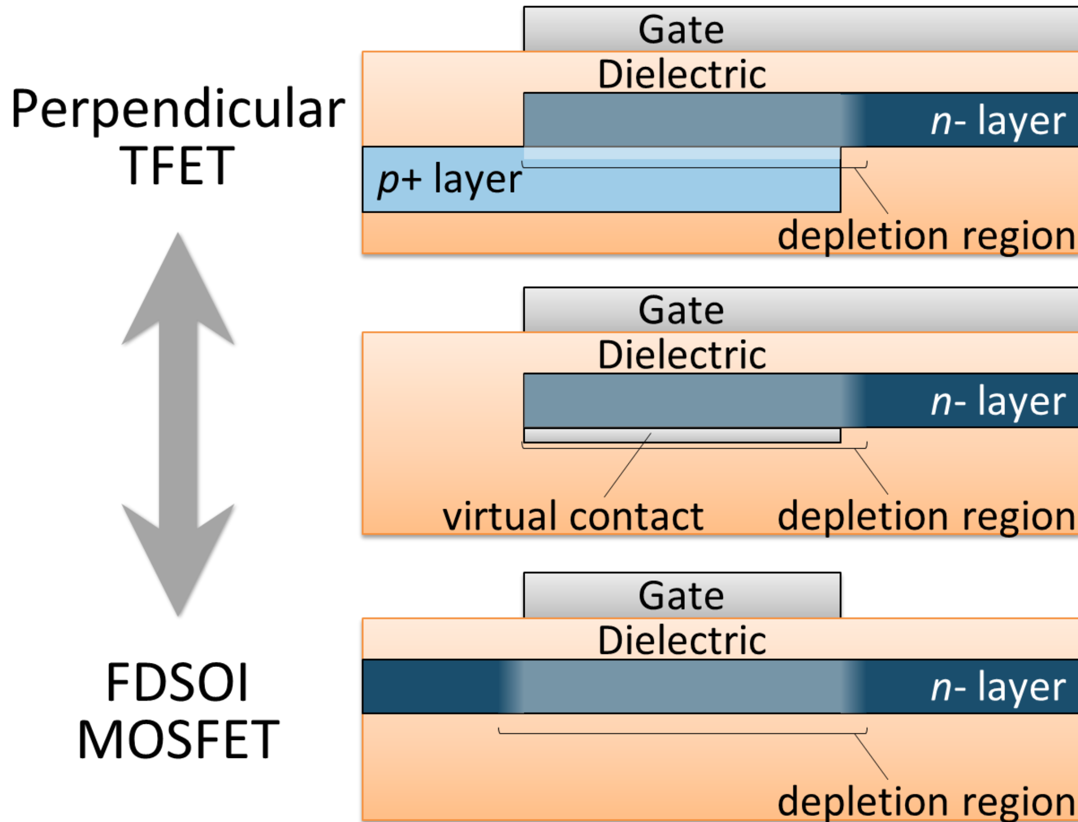

Figure 5.5. Illustration highlighting the relationship between the perpendicular TFET and the FDSOI MOSFET. The middle illustration represents a conceptualized device where the *p+* layer of the perpendicular TFET is replaced with a *virtual* contact in intimate contact with the *n-* layer. The virtual contact depletes the *n-* layer in the same way as the *pn* junction in the perpendicular TFET. The bottom illustration shows an *n*-type FDSOI, where the channel is depleted of electrons. Similarities of the structures allow the short-channel framework for the FDSOI MOSFET to be applied to the perpendicular TFET to study the potential variations at the right-edge of the *p+* layer.

5.4 Optimized Bilayer TFET Design

The bilayer device, depicted in Figure 5.6a, could be used to overcome the challenges of parasitic tunneling paths enabling study of the fundamental switching abruptness of tunneling devices. The device is *electrostatically* doped through the use of top and bottom gates. The *electrostatic* doping

prevents long band-tails introduced by heavy acceptor and donor doping, and also allows lateral control of the hole-rich layer at the bottom of the device through the design of the bottom gate. Increasing the thickness of the bottom oxide reduces the lateral field at the right edge of the bottom gate, which helps prevent diagonal tunneling. The energy band diagram of the structure (Figure 5.6b) shows that lateral tunneling can be greatly reduced through the use of a thick bottom dielectric that significantly reduces λ, the characteristic length for potential variations.

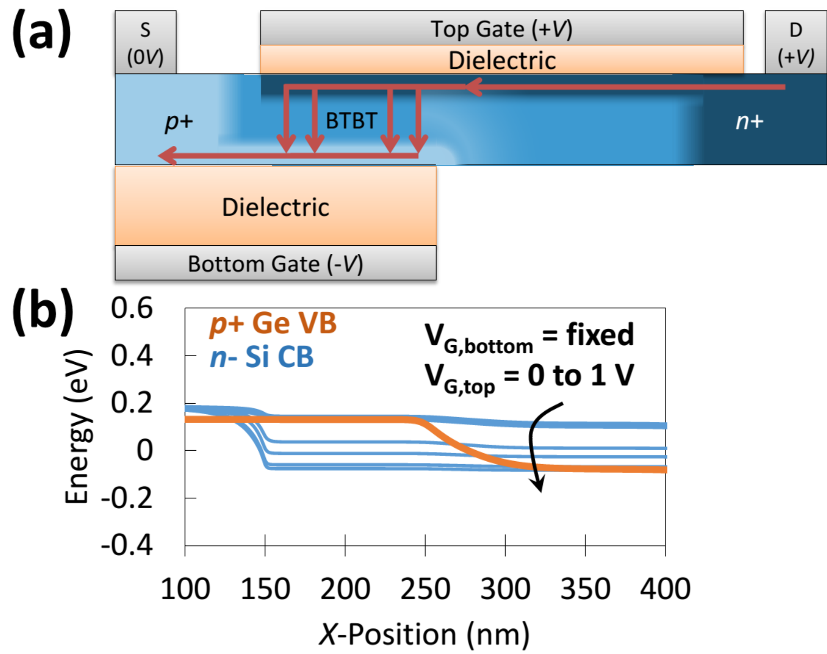

Figure 5.6. (a) Bilayer TFET structure. The top and bottom gate are biased oppositely in order to create an electron-rich layer near the top gate and a hole-rich layer near the bottom gate. BTBT occurs when a sufficiently large bias is applied between the top and bottom gates such that the CB near the top and VB near the bottom overlap in energy. The red arrows indicate the current path. A thicker dielectric is used for the bottom gate to minimize the lateral field at the right side of the bottom gate. Minimizing the lateral field minimizes parasitic diagonal tunneling. (b) Energy band diagram of the structure shown in (a). The parasitic diagonal tunneling path has been greatly mitigated through optimal electrostatic design of the bilayer structure.

5.5 Summary

Non-uniform 2D electrostatics in perpendicular TFETs can lead to parasitic tunneling paths that can seriously degrade the subthreshold swing of the device. Non-uniform electrostatics result from the abrupt termination of a bottom $p+$ layer in many perpendicular TFET designs and can cause large lateral potential variations in the structure that give rise to parasitic tunneling. The characteristic length λ for perpendicular TFET designs is found to be the same as for FDSOI MOSFETs. The bilayer device design is suggested to minimize parasitic diagonal tunneling so that the fundamental switching abruptness of perpendicular TFETs can be effectively studied.

Chapter 6: Fabrication of the 3Gate Strained-Si/strained-Ge Bilayer TFET

The 3Gate strained-Si/strained-Ge bilayer TFET provides many benefits for studying tunneling, as discussed in previous chapters, but the structure requires complex fabrication. Some of the features that make the fabrication challenging include (1) the heterostructure device body, (2) highly strained layers, (3) planarization of a bottom gate, (4) wafer bonding, (5) etch-back of the bonded wafer to a very thin layer, (6) two top-side gate stacks, (7) separate source and drain implants, (8) dopant activation with a constrained thermal budget to prevent strain relaxation, and (9) via etch and ohmic contact formation on a very thin semiconductor layer.

This chapter details the growth of the epitaxial wafers, the wafer bonding and etch-back process, and the fabrication process to create the devices.

6.1 Epitaxial Growth of Wafers

The epitaxial growths are performed in an Applied Materials Epi Centura low-pressure chemical-vapor-deposition (LPCVD) system using six-inch *p*- Si wafers with a (100) surface as the starting substrate. Table 6.1 details the thickness, growth temperature, and SiGe fraction of the various layers for four splits that were run in this experiment, and the leftmost illustration of Figure 6.1 shows the final epitaxial structure.

A high quality Ge layer cannot be grown directly on unstrained Si because the lattice mismatch between Si and Ge is too large (4% mismatch), and the growth seeds many dislocations in the Ge film. Therefore, to create a high quality strained-Si/strained-Ge heterostructure, a substrate with a lattice constant between Si and Ge is used. In this work, a SiGe virtual substrate with a 50% Ge fraction is created to allow growth of a high quality strained-Si/strained-Ge heterostructure.

The SiGe virtual substrate is created by growing a SiGe graded buffer layer followed by a SiGe relaxed layer on a *p*- Si substrate. The Ge fraction in the graded buffer layer is linearly graded from 0 to 50% at the rate of 10% Ge fraction per 1 μm of growth. The slow grade and high temperature (936 °C) allow for strain relaxation without the creation of a high density of threading dislocations [96]. The high temperature creates a high dislocation velocity so that misfit dislocations can grow very long such that a single dislocation can relieve a significant amount of

mismatch strain. Quoting from Fitzgerald et al. [96], "Thus, by compositionally grading at a rate where the strain level in the structure never reaches a high value, and by growing at a high temperature, dislocation nucleation should be suppressed but relaxation from existing dislocation should be quite rapid."

After the growth of the 0 to 50% SiGe[*] graded buffer layer, a 1-µm thick 50% SiGe relaxed buffer layer is grown. The relaxed buffer layer is used to separate the defective graded buffer layer (defective from long misfit dislocations) from the device layer of interest, and the Ge fraction is not varied within the layer. The graded buffer layer and the relaxed buffer comprise the SiGe virtual substrate.

On top of the virtual substrate, an 8-nm thick strained-Si etch-stop layer is grown. The use of this layer as an etch-stop during the etch-back process is described in detail in §6.3. Next, 100 nm of relaxed 50% SiGe is grown at a lower temperature than before (525 as opposed to 936 °C) in order to prevent strain relaxation of the buried strained-Si layer.

Finally, a strained-Si, strained-Ge, and superficial strained-Si layer are grown. These final three layers of the epitaxial structure are the only layers that will remain after the etch-back process detailed in §6.3. The superficial strained-Si layer is only used to ensure a high quality dielectric interface at the top inference (which will become the bottom interface after the wafer is flipped during the wafer bonding process). The thicknesses of the strained-Si and strained-Ge were varied across the wafer lot, but their total thickness was constrained to prevent relaxation in the highly strained layers. Table 6.1 provides the thickness of the strained-Si and strained-Ge layers for the different growth splits performed in this experiment.

Table 6.1. Layer thickness and growth temperature for the four splits that were run in this experiment. The layers with a light gray background are removed during the etch-back process described in §6.3.

Layers (in order from top to bottom)	Split A	Split B	Split C	Split D
strained-Si 625 °C	2 nm			

[*] The "% SiGe" refers to the Ge fraction. For example, 10% SiGe means a 10% Ge fraction, or equivalently a $Si_{0.9}Ge_{0.1}$ alloy.

strained-Ge 365 °C	5 nm	7 nm	7 nm	5 nm
strained-Si 625 °C	7 nm	7 nm	9 nm	9 nm
relaxed 50% SiGe 525 °C	100 nm			
strained-Si (etch-stop layer) 625 °C	8 nm			
relaxed buffer layer (50% SiGe) 936 °C	1 µm			
graded buffer layer (0 to 50% SiGe) 936 °C	5 µm			
***p*- Si substrate** (6-inch wafer with (100) surface)	thick			

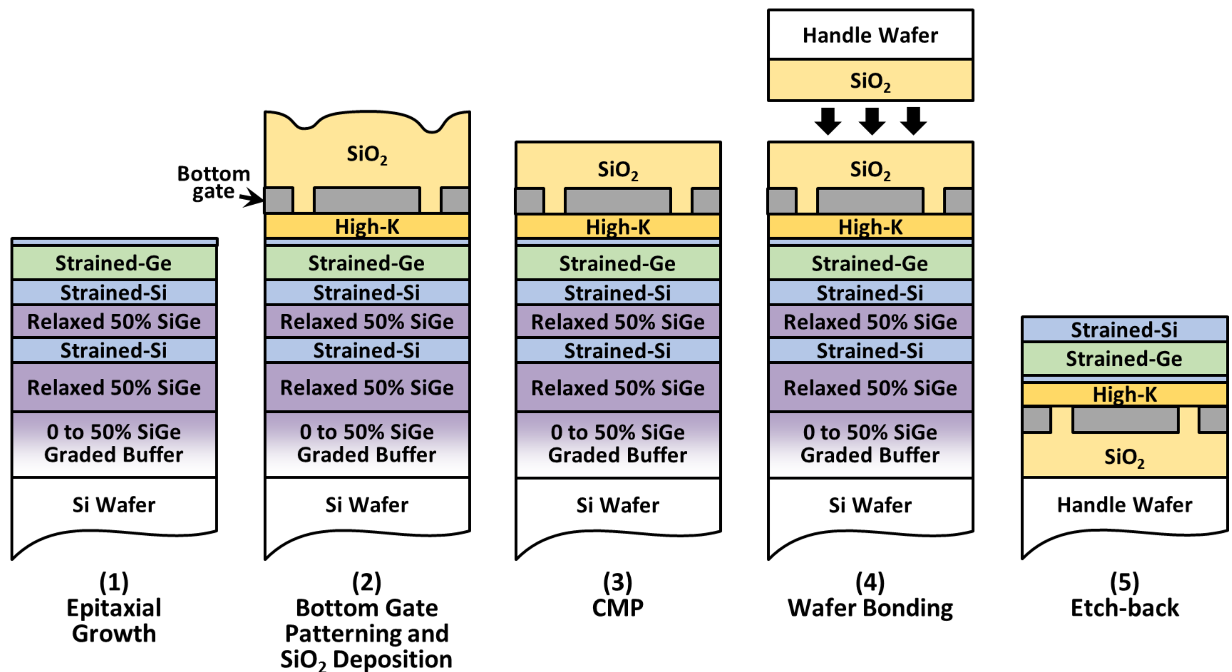

Figure 6.1. Illustration of the experimental structure at different points along the fabrication process. (1) Structure after epitaxial growth. The thin blue layer at the top is a superficial strained-Si layer to improve the dielectric interface at that surface. (2) Structure after bottom gate patterning and SiO_2 deposition. The SiO_2 is nonplanar due to the patterned bottom gate. (3) Structure after CMP. Excellent planarization across the entire wafer is achieved by using a dummy fill pattern for the bottom gate. (4) Bonding of the epitaxial wafer to the handle wafer. (5) Structure after etch-back. All layers of the original epitaxial structure from (1) are removed except for the top three strained-Si, strained-Ge, and superficial strained-Si layer at the bottom. The bond and etch-back process yields a strained-Si/strained-Ge heterostructure directly-on-insulator with a buried bottom gate. (Illustrations not drawn to scale.)

6.2 Patterning and Planarization of the Bottom Gate

Immediately after each epitaxial growth, the wafer was placed in an Oxford Instruments FlexAL ALD. In the ALD, the wafer was first exposed to a 1-minute ozone treatment, followed by 245 cycles of Al_2O_3 (nominally 20 nm), and 1435 cycles of TiN (nominally 50 nm). All ALD steps were performed at 300 °C. In the final device structure, the Al_2O_3 and TiN serve as the bottom gate dielectric and gate metal, respectively.

The TiN metal was patterned using a bottom gate mask that included a dummy fill pattern in the areas without a bottom gate. The dummy fill is necessary in order to achieve a uniform surface

after chemical-mechanical polishing (CMP). An almost perfectly planar surface (RMS roughness less than 10 Å) is necessary for the wafer bonding process detailed in §6.3. If a wafer has a sparse pattern, as shown in Figure 6.2, planarization is inefficient because the CMP polishing pad can bend to match the surface contours. This occurs because the polishing pad is not completely rigid and pressure is placed on the pad during the process in order to planarize the surface. A solution to this problem is to fill-in the sparse areas of the mask with a *dummy fill* so that large spaces do not exist between features. An example of the bottom gate pattern used in this work with and without the dummy fill is shown in Figure 6.3. The dummy fill was designed so that the spacing between bottom gate features was less than 3 µm.

The bottom gate mask that is patterned onto the wafers is mirrored during the wafer bonding step that occurs later in the process. Taking this into account, the pattern that is initially printed onto the wafer must be initially mirrored so that the wafer bonding step un-mirrors the pattern. To achieve this, the bottom gate mask was mirrored in the mask layout software, and the masks were then produced by a commercial vendor.

After patterning the bottom gate and performing a double 10-minute nanostrip clean, ~515 nm of low-temperature oxide (LTO) was deposited on the wafer with a total process runtime of ~4.5 hours at 400 °C. Next, a densification anneal was performed for 30 miuntes at 550 °C in a nitrogen environment.

The wafers were then shipped to Entrepix for CMP foundry services. The CMP process is used to remove surface variations due to the buried bottom gate and cross-hatch roughness from the virtual SiGe substrate. The wafers were polished for 1 minute with a final roughness of 7 to 9 Å R_a.† Approximately 250 nm of SiO_2 was removed from the wafer as measured by weight loss. After the wafers were received, a double 10-minute piranha clean (3:1 H_2SO_4:H_2O_2) was performed, but no HF dip was done. This was followed by an SC2 clean (6:1:1 DI H_2O:HCl:H_2O_2) at 80 °C for 10 minutes.

Next, the wafers undergo wafer bonding and etch-back, which is detailed in the next section.

† R_a is the arithmetic average of absolute values of vertical distance, given by $R_a = \frac{1}{n}\sum_{i=1}^{n}|y_i|$, where y_i is the vertical distance of the ith measurement and n is the total number of measurements.

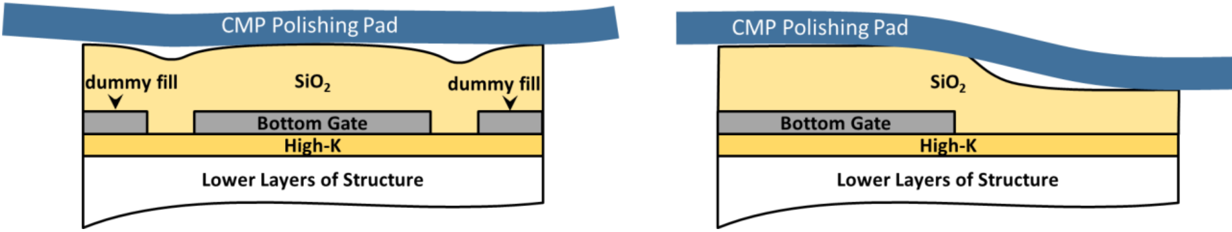

Figure 6.2. Illustration of a polishing pad on the surface of a wafer during the CMP process. (left) Wafer with bottom gate dummy fill pattern. The polishing pad bends, but good planarization is achieved because the pad preferentially removes the highest surfaces. (right) Wafer without dummy fill. Features are spaced widely apart on the wafer, and the polishing pad is able to bend to match the surface contours. Material from both the high and low surfaces are removed at similar rates, preventing effective planarization. This can be avoided if features are placed closer together than the bending curvature of the polishing pad.

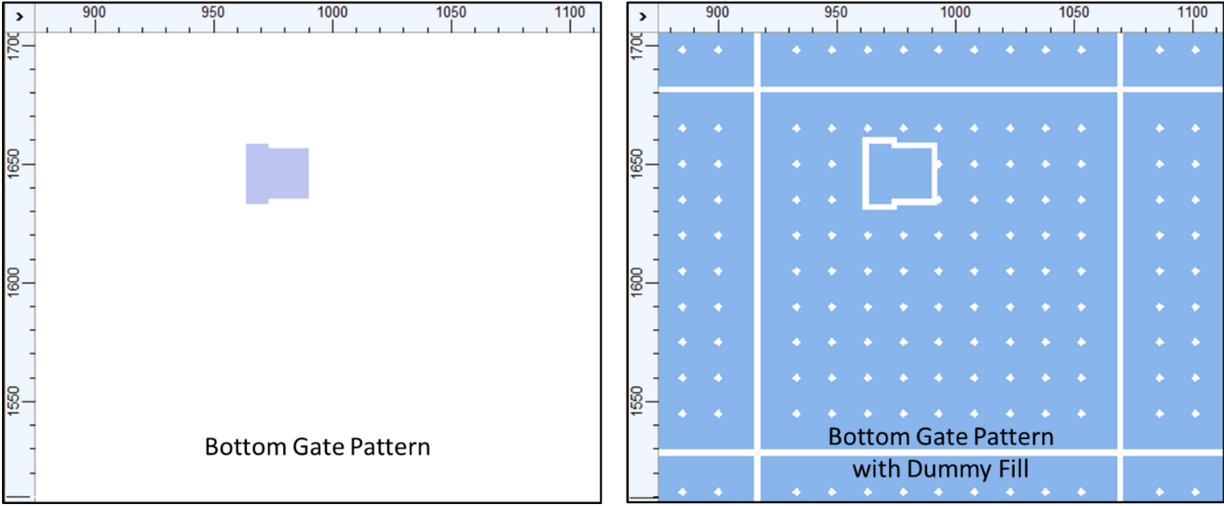

Figure 6.3. (left) Mask layout of original bottom gate pattern. (right) Bottom gate with added dummy fill pattern. The grid and dots of the dummy fill allow it to be distinguished from the actual devices. The dummy fill pattern is necessary to achieve a planar surface after CMP to allow wafer bonding. (Units of axes are in μm.)

6.3 Wafer Bonding and Etch-back

Wafer bonding and etch-back is used to create a highly strained-Si/strained-Ge heterostructure directly-on-insulator. In the process, an epitaxial wafer is bonded to a handle wafer, and nearly all of the epitaxial wafer is subsequently removed both physically, through wafer grinding, and chemically, through etch back processes, preserving only the thin device layers of strained-Si and

strained-Ge. The procedure followed for wafer bonding and etch-back is similar to the process described in [97].

A high quality thermal oxide is formed on both sides of a set of handle wafers using standard processes. Both the handle wafers and the epitaxial wafers are exposed to a 20-second oxygen plasma to create dangling bonds on the SiO_2 surface so that bonding will occur.

Next an oxide-to-oxide bond between a handle wafer and an epitaxial wafer is formed by forced contact using an EV620 contact aligner. Care is taken to align the wafer flats with each other as carefully as possible. A post-bond anneal is then performed for 5 hours at 300 °C in a nitrogen environment.

The bonded wafers were then sent to Silicon Quest International (SQI) for commercial wafer grinding to remove the bulk of the epitaxial wafer. Around 500 μm of the epitaxial wafer was removed by mechanical grinding for final bonded wafer thickness of 800 ± 25 μm.

The etch-back process is used to remove the epitaxial substrate except for the thin strained-Si and strained-Ge layers directly above the insulating layer. The etch-back process is described below.

6.3.1 Removal of Remaining Si Substrate (~150 μm)

Dilute 50:1 DI H_2O:HF is used to remove any native oxide from the remaining substrate of the epitaxial wafer, since tetramethylammonium hydroxide (TMAH) etches SiO_2 very slowly. The wafer is removed from the dilute HF solution, verifying that the surface is hydrophobic indicating the removal any SiO_2.

TMAH was heated in a water bath to 95 °C. The bonded wafers were placed in the heated TMAH for 10 hours until the cross-hatch could be faintly seen, along with a very faded pink bulls-eye pattern. The TMAH etch is highly selective to the Ge fraction, and the etch should stop on around 20% SiGe with a high selectivity (around 20:1) [98].

6.3.2 Removal of SiGe Buffer Layers (5 μm)

To remove the graded and relaxed buffers, a solution of 900 ml acetic acid, 600 ml of H_2O_2, 100 ml of HF, and 200 ml of DI H_2O were mixed and allowed to stabilize for 2 hours. The etch rate is

~40 nm/min with a selectivity of 23:1 for 30% SiGe:Si [97], [99]. The wafers were placed in the solution for 35 to 45 minutes until the surface color stabilized. The edge color of the wafer should change from gray to orange and the etch should stop on the strained-Si etch-stop layer. It is important that the wafers are not left in this solution too long after the color stops changing, otherwise the strained-Si etch-stop will be etched through.

6.3.3 Removal of Strained-Si Etch-stop (8 nm)

The removal of the strained-Si etch-stop occurs very quickly. TMAH is heated on a hot plate to 80 °C. The Si etch-stop is removed after ~45 seconds when the color of the wafer stops changing and the surface becomes hydrophilic.

6.3.4 Removal of Relaxed SiGe (100 nm)

The wafer was placed back in the 900 ml acetic acid, 600 ml of H_2O_2, 100 ml of HF, and 200 ml of DI H_2O solution to remove the 100-nm layer of relaxed 50% SiGe. The etch completed in ~30 seconds when the surface color of the wafer stopped changing.

6.4 Device Patterning and Processing

After etch-back, only a thin layer (~15 nm) of strained semiconductor remains on the insulating substrate. The next steps in the process are to

- pattern top gate 1
- pattern top gate 2
- implant the *n*+ drain
- implant the *p*+ source
- open vias to the bottom gate
- open vias to the source, drain, and top gate 1
- deposit interlayer dielectric (ILD)
- open vias in the ILD
- deposit and pattern metal contacts

An illustration of the final structure is shown in Figure 6.4, and the detailed process steps are provided in Appendix C: *Detailed Process Flow for the 3Gate Strained-Si/strained-Ge Bilayer TFET*.

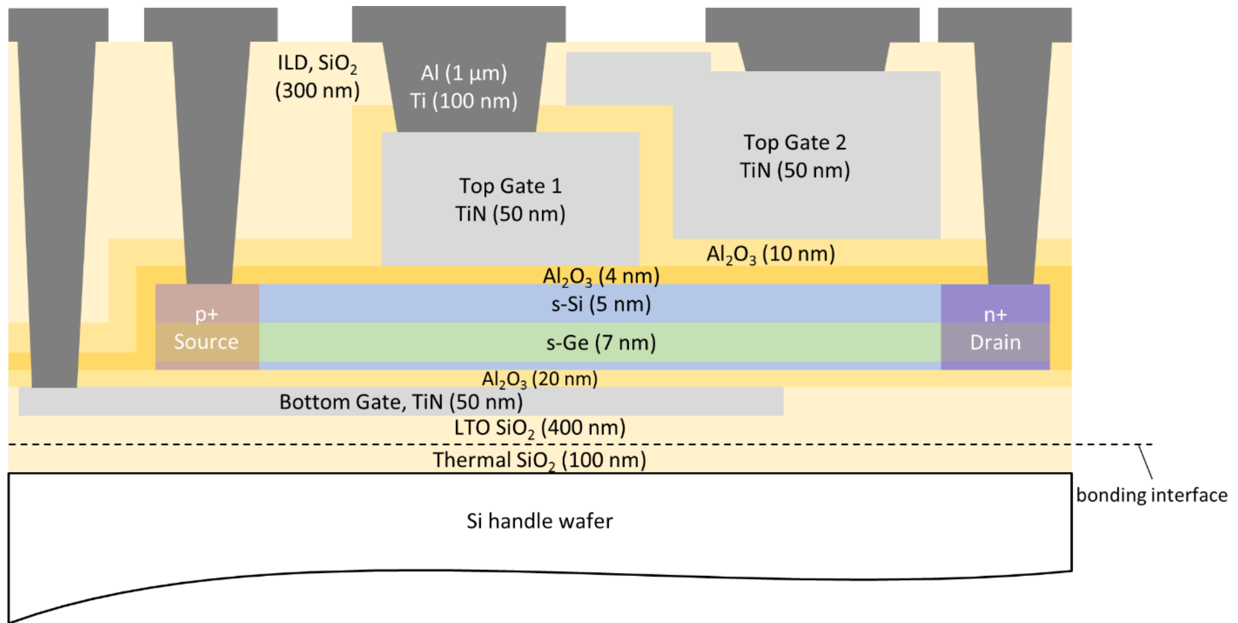

Figure 6.4. Illustration of the 3Gate strained-Si/strained-Ge bilayer TFET device structure.

Chapter 7: Suggestions for Future Work

The focus of this thesis is on the design and development of the bilayer TFET. Future work includes finishing the fabrication of the 3Gate strained-Si/strained-Ge bilayer TFET and then electrically characterizing the device.

Once completed, several biasing schemes are of interest in the experimental device. In the standard bottom-gate biasing configuration, application of a large negative potential creates a degenerate hole layer that pins the surface potential along the bottom gate. By pinning the surface potential at the bottom of the device, any voltage applied to top gate 1 or 2 must appear solely across the semiconductor body and top gate oxide. If the bottom-side surface potential is not pinned, then application of a top gate bias can change the surface potential at the bottom of the device, which leads to a fraction of the top gate bias being dropped across the bottom oxide (reducing gate efficiency at overlapping the bands).

Below are several bias configurations that can be used to analyze the device.

Test Configuration A: to study tunneling between holes near the bottom gate to the electron well created by top gate 1. The bias on top gate 2 is used to create a channel for electrons to make it from the top gate 1 well to the drain. The bottom gate is held at a large negative potential as discussed above. The voltage of top gate 1 is swept for both low and high drain bias. Additionally, top gate 2 should be biased in various ways: at different multiples of the top gate 1 bias and at different constant biases. Also the constant bottom-gate bias should be varied as well.

Test Configuration B: to study tunneling between the hole-rich layer induced by the bottom gate and electron-rich layer created by top gate 2. The gate voltage for top gate 2 is swept for both low and high drain biases. The voltage of top gate 1 is kept constant such that tunneling dues not in the region beneath it. The bias of the constant bottom-gate should be varied as well.

Test Configuration C: to study tunneling between a hole-rich layer induced by top gate 1 and an electron-rich layer created by top gate 2. This test configuration might be difficult to achieve in experimental devices due to the large field required between top gate 1 and 2, which may lead to significant leakage current between the metal/insulator/metal structure of top gate 1/top gate 2 dielectric/top gate 2. The bottom gate is biased to create a sufficient hole channel from the source

to top gate 1, but not large enough to create tunneling from the semiconductor surface near the bottom gate to the semiconductor surface near top gate 2. The voltage of top gate 2 is swept to study parallel tunneling from top gate 1 to top gate 2.

Test Configuration D: to study tunneling between the hole-rich surface near the bottom gate and the electron-rich well created by top gate 1. This is similar to Test Configuration A, but the bottom gate voltage is swept instead of top gate 1. In this configuration, a large positive bias is applied to top gate 1 to create a degenerate electron concentration, and a smaller positive bias is applied to top gate 2 to create a channel to the drain. The voltage on the bottom gate is swept for both low and high drain bias, and for different constant biases applied to top gate 1 and 2.

Of special interest is the comparison of the measured electrical characteristics of Test Configuration A and B, after accounting for the differences in effective oxide thickness of the two gate stacks. The way the device is designed, for Test Configuration A, nearly all diagonal parasitic paths are eliminated leaving only pure perpendicular tunneling. Whereas in Test Configuration B, parasitic diagonal tunneling can occur. Differences between these two results may allow for a definitive statement on the impact of diagonal tunneling on the abruptness of switching characteristics for tunneling transistors.

Table 7.1. Suggested test configurations for electrical measurements of the 3Gate strained-Si/strained-Ge bilayer TFET device.

Test Configuration	Bottom Gate (carried type)	Top Gate 1 (carried type)	Top Gate 2 (carried type)	Source	Drain
A	constant (holes)	swept (electrons)	varied, either proportional to top gate 1 or constant	0	Lo/Hi
B	constant (holes)	constant (none)	swept (electrons)	0	Lo/Hi
C	constant (holes)	constant (holes)	swept (electrons)	0	Lo/Hi
D	swept (holes)	constant (electrons)	constant (electrons)	0	Lo/Hi

Appendix A: Deformation Potentials for Si and Ge

As indicated in §3.1 *Calculation of Energy Band Alignments*, the use of several deformation potentials with different degrees of uncertainty is unavoidable when analyzing Si-Ge heterostructures. The most important parameters that affect this work's calculations are given in Table 3.2. It should be stressed, however, that this work's main conclusion, namely that the Si-Ge valence band offset is larger than hitherto assumed, is not significantly affected by the particular choice of deformation potentials. For example, using the *theoretical* deformation potentials from Van de Walle [44], and following the same procedure used above, it is found that the offset that reproduces Thewalt's photoluminescence results [51] is $\Delta E_{v,av}$ = 720 meV, which is also very large. When applied to this work's s-Si/s-Ge heterostructure, this model gives somewhat better effective band gaps and somewhat worse band offsets. Nevertheless, the authors believe that the deformation potentials presented in Table 3.2 represent a better choice, and here it is briefly summarized how they were obtained.

For the absolute deformation potentials, the analysis starts with the experimental pressure dependence of the direct band gap E_0 in Ge, as measured by Goñi et al. [100]. They find that the resulting volume dependence of the band gap energy is not exactly linear, so a linear expression is fitted over the range of volume changes (~0 to 2.5%) likely to be found in epitaxially strained systems. A band gap volume deformation potential, $a_c - a_v$ = -9.47 eV, is obtained. Here, the band gap deformation potential is expressed in terms of the absolute deformation potentials for the conduction and valence bands at the Γ-point of the Brillouin zone, a_c and a_v. These have been calculated theoretically by several groups. The values from Li et al. [101] are used who obtain a_c = -7.83 eV and a_v = 2.23 eV, in good agreement with Ge band gap data ($a_c - a_v$ = -10.06 eV). The residual small deviation is corrected by multiplying the theoretical values by a factor $9.47/10.06 = 0.94$ to match the band gap data exactly. This gives the value listed in Table 3.2, a_v = 2.10. For Si, there are no pressure dependence studies of E_0. Therefore, the value of a_v from [78] is used and "renormalized" with the same factor used for Ge. The resulting absolute deformation potentials in Table 3.2 are in excellent agreement with the values needed to fit the hole mobilities in Si and Ge [102].

From the pressure dependence of the fundamental band gap of Si [103], the hydrostatic deformation potential, $\left(\Xi_d + \frac{1}{3}\Xi_u - a_v\right)^\Delta$ = 1.47 eV, is obtained for Si. The pressure dependence of the indirect gap associated with the Δ-valley in Ge has been measured by Ahmad and Adams [53], and from their measurements $\left(\Xi_d + \frac{1}{3}\Xi_u - a_v\right)^\Delta$ = 1.80 eV is obtained for Ge.

The shear deformation potentials that give the splitting of bands due to the traceless component of the strain tensor are traditionally measured in uniaxial stress experiments, which potentially suffer from stress calibration issues, as suggested by the fact that Raman phonon Grüneisen parameters obtained from such experiments do not agree very well with direct hydrostatic pressure measurements in diamond anvil cells [104]–[107]. In the case of the valence band shear deformation potential, Liu et al. [108] recently determined b = 1.88 eV for Ge using strained-layer Ge films in which the strain was measured with high-resolution x-ray diffraction. It is interesting to point out that the hydrostatic deformation potential obtained by these authors agrees exactly with the value obtained from Goñi et al. [100] when the data from the latter is fit over the same volume change range. Liu's value is used for Ge, and for Si, the Ge value is taken for b and multiplied times the theoretically predicted ratio of this quantity for Si and Ge [44]. Finally, for the shear deformation potential for Si associated with the Δ-minimum of the conduction band, the value measured by Laude et al. [109], Ξ_u = 8.7 eV is used. There are no equivalent measurements for Ge, but most theoretical calculations give values slightly larger than similar calculations for Si that are in good agreement with the experimental data. Accordingly, Ξ_u = 8.95 eV is used for Ge, which follows from multiplying the Si value from Laude [109] times the theoretical ratio for Ξ_u for Ge and Si [44]. Assuming linear interpolation of the deformation potentials for $Si_{1-x}Ge_x$, the predicted dependence of the split indirect band gaps in $Si_{1-x}Ge_x$ alloys pseudomorphic to Si substrates is compared with experimental data in Figure A.1.

As a final comment, it is pointed out that in 1991, Li and coworkers [110] introduced a capacitance method from which the shear deformation potential Ξ_u can be obtained quite straightforwardly from samples under uniaxial stress. They find Ξ_u = 11.3 eV for Si, significantly larger than the value above from Laude [109], and they present a very thorough discussion of the errors associated with different experiments. The authors suspect that the discrepancies between different works are due in part to differences in the calibration of their stress apparatuses, as suggested above. In the case of Laude, the hydrostatic deformation potentials deduced from their

experiment agree very well with the direct hydrostatic pressure measurements in [102], suggesting small stress calibration errors. No corresponding hydrostatic data comparison is presented by Li. Moreover, if Li's value for Ξ_u is used, the agreement between theory and experiment in Figure A.1 worsens, so the authors prefer to use Laude's value until Li's shear deformation potential value is confirmed by new experiments.

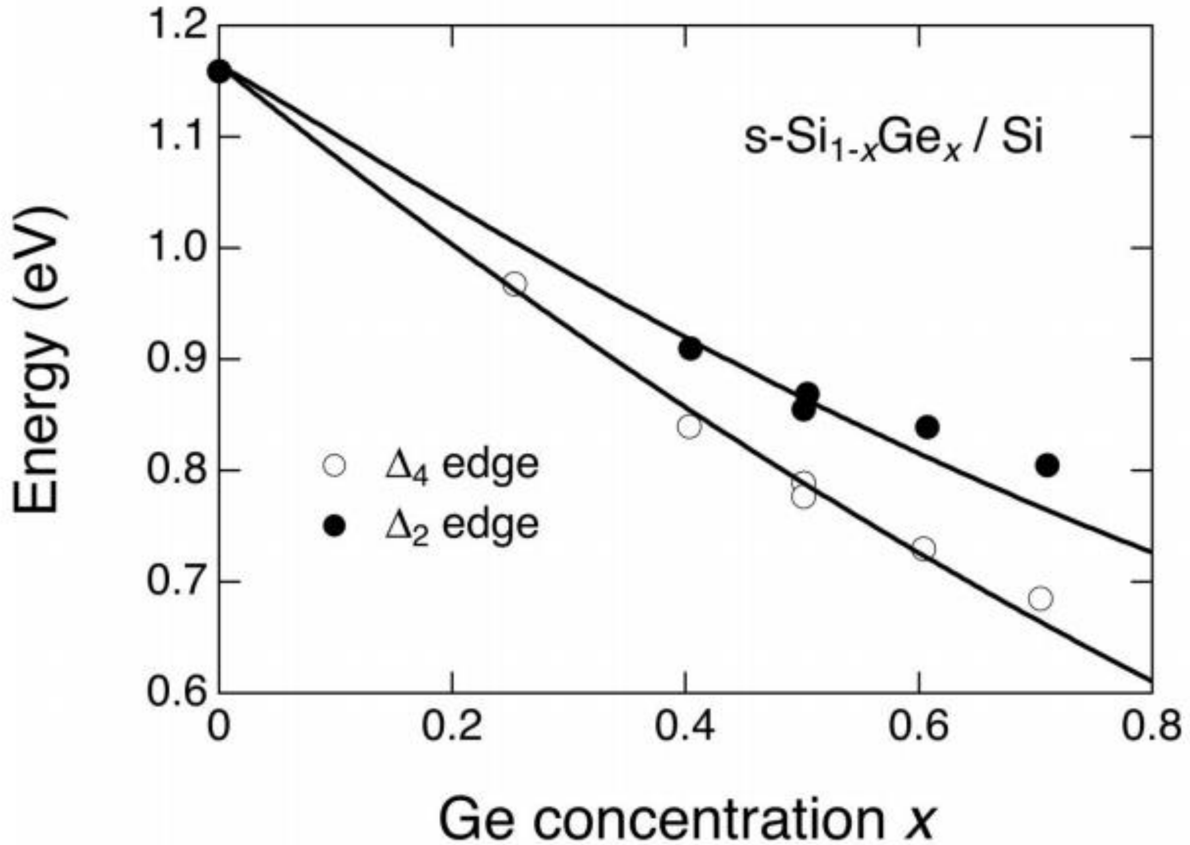

Figure A.1. Experimental Δ-like absorption edges of strained $Si_{1-x}Ge_x$ alloys on relaxed Si substrates from Lang et al. [111] (circles), and this work's calculation of these edges (lines) using the experimental compositional dependence of the band gap in relaxed $Si_{1-x}Ge_x$ alloys from [112] and the deformation potentials in Table 3.2.

Appendix B: Impact of Asymmetric Strain on Band Structure and Transport

B.1 Preface

Although the work presented in this section does not relate directly to the study of the TFET devices in this thesis, it is included here because it would become relevant if Si/Ge strained heterostructure TFETs were to be miniaturized to dimensions compatible with future generations of CMOS.

B.2 Abstract

The impact of asymmetric strain in Ge nanowire (NW) trigate *p*-MOSFETs with record measured hole mobility [113] is simulated. Contrary to previous studies of uniaxial and biaxial strain, the impact of very large (2.4%), non-uniform asymmetric strain (achieved by patterning-induced lateral relaxation) is studied through NW simulations. Asymmetric strain significantly warps the valence band (VB), reducing the hole effective mass in the transport direction, and increasing the ballistic velocity ($v_\theta \propto 1/\sqrt{m^*}$ [114], [115]) compared to biaxial strain. Consistent with previous mobility measurements [113], analysis of the VB structure reveals a 1.6× increase in the inverse effective mass for a 49-nm wide asymmetrically-strained Ge NW compared to planar biaxially strained Ge (s-Ge) with 2.4% compressive strain. Ballistic velocity, v_θ, improves in narrow NWs due to lateral strain relaxation that reduces the transport effective mass. A v_θ enhancement of 2.8× relative to unstrained Si (1.6× relative to 1% uniaxially strained Si) is predicted for 10-nm wide s-Ge NWs suggesting a scalable transport enhancement technique for future technology nodes.

B.3 Strain for Mobility Enhancement

In modern *p*-MOSFETs, uniaxial compression in strained Si (s-Si) warps the VB and improves transport. Strained-Ge is an attractive channel material due to its superior hole mobility compared to s-Si. Extremely high hole mobility has been reported in s-Ge/high-κ/metal gate planar [56], [116] and non-planar [113], [117] *p*-MOSFETs. Relaxation of lateral strain from an initial biaxial state has been experimentally shown to increase hole mobility in s-Ge NW trigates [113] and to produce high current drive (and hole source injection velocity) in SiGe trigates [118]. In this work, insights into the measured mobility enhancement for asymmetrically strained Ge NW *p*-MOSFETs

reported in [113] are obtained using strain-dependent 6×6 $k \cdot p$ band structure and quantum mechanical electrostatic simulations. The simulations are extended to predict the ballistic velocity enhancement for NW widths suitable for ultra-scaled s-Ge p-MOSFETs.

B.4 Device Structure

Figure B.1 shows the NW device structure fabricated in [113]. NWs were produced with widths (w_{NW}) from 18 to 49 nm. The material structure was created by a bond-and-etch-back process [113] which yielded compressive biaxially strained Ge (psuedomorphic to $Si_{0.6}Ge_{0.4}$) directly on HfO_2 dielectric with a tensilely strained Si capping layer. Five nm of HfO_2 (κ = 18) gate dielectric was used in the simulated structures.

Patterning the biaxially strained material into NWs creates free surfaces at the sidewalls that relieve some of the lateral strain, so that the resulting strain is neither biaxial nor uniaxial, but asymmetric. The lattice mismatch compared to the $Si_{0.6}Ge_{0.4}$ virtual substrate (which was removed during the bond-and-etch-back process) was extracted for the 18-nm wide NW from the HRTEM of Figure B.1(c) using the method given in [119]. Figure B.2 shows the spatial distribution of the measured and simulated lattice mismatch, and the agreement supports the strain-based band structure simulations presented in this work.

The simulated strain profiles are shown in Figure B.3. The device is assumed to be long so that strain along the channel direction (ϵ_{zz}) does not relax. Source/drain stressors of physical devices can be engineered to help maintain channel-directed strain for short channel structures. Significant lateral strain relaxation occurs near the NW sidewalls (Figure B.3(a)).

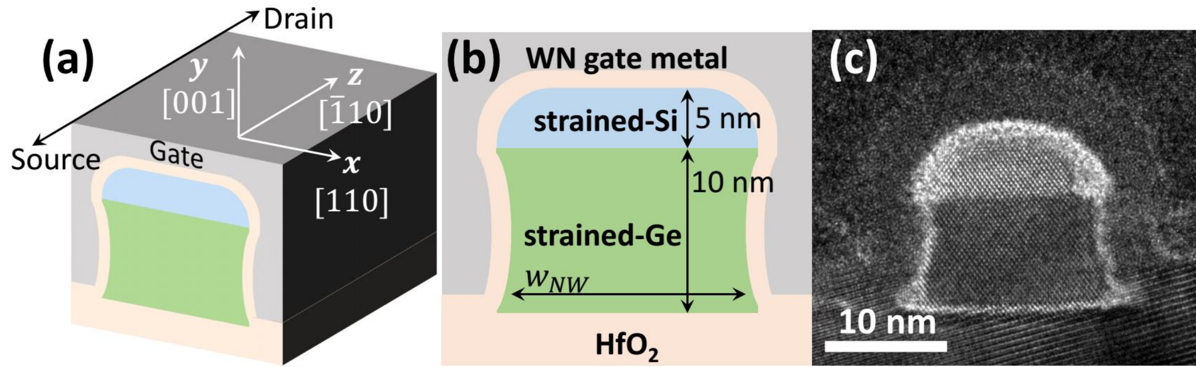

Figure B.1. (a) 3D schematic of the device structure with crystal Miller directions indicated for the different directions. x, y, and z correspond to the lateral, vertical, and channel/transport directions used throughout the paper. (b) Cross-section of the trigate structure. w_{NW} was varied from 5 to 49 nm in the simulations. (c) HRTEM of the experimental device [113]. Five-nm thick HfO_2 was used as the gate dielectric.

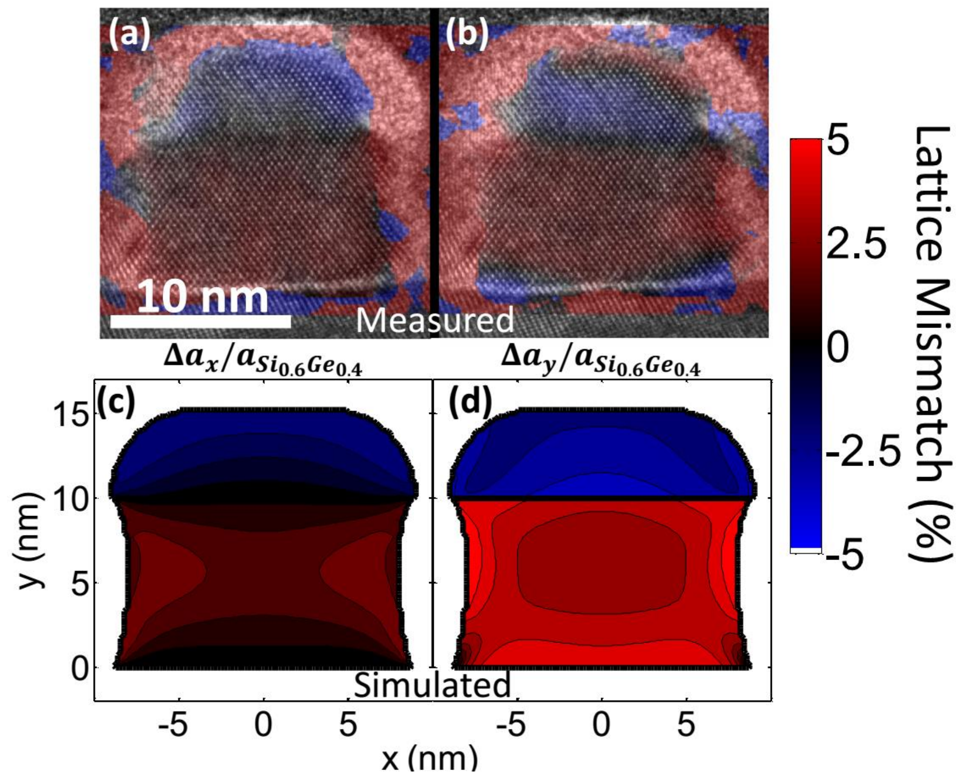

Figure B.2. (a-b) Overlay of the HRTEM from Figure B.1(c) with the measured lattice mismatch m (with respect to a relaxed $Si_{0.6}Ge_{0.4}$ virtual substrate) extracted from the HRTEM using the FFT technique described in [119]. (c-d) Simulated m calculated by elastic energy minimization of the structure [73]. (a) and (c) show m in the x-direction, and (b) and (d) show m in the y-direction.

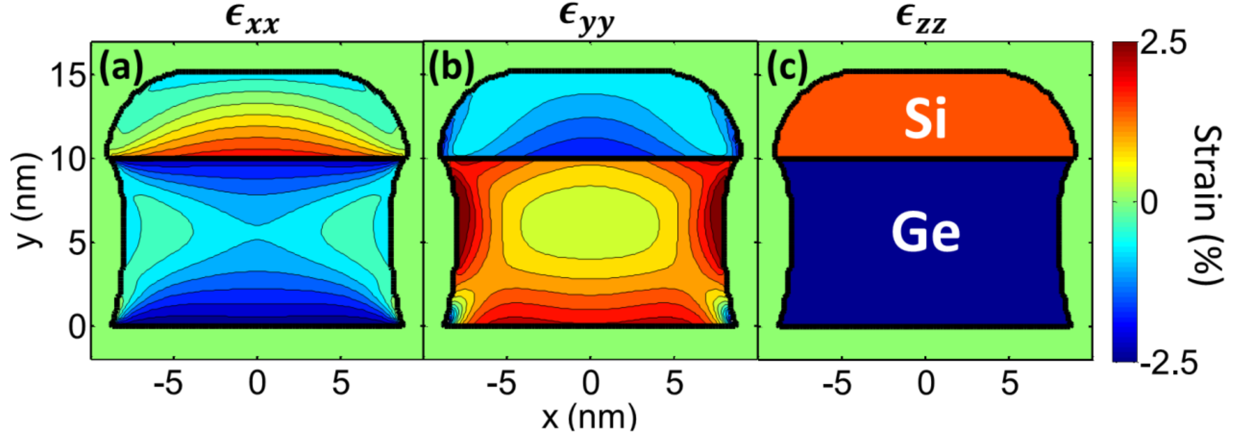

Figure B.3. Simulated strain profile calculated by elastic energy minimization of the structure [73] for w_{NW} = 18 nm. The (a) lateral strain ϵ_{xx}, (b) vertical strain ϵ_{yy}, and (c) strain along the channel ϵ_{zz} are shown. The simulation assumes no relaxation along the channel direction. The lateral strain ϵ_{xx} relaxes near the sidewalls due to the free surface.

B.5 Electrostatic Simulations

Two-dimensional self-consistent coupled Poisson-Schrödinger electrostatic simulations [73] of the NW structure were performed. Strain causes splitting and mixing of the light hole and heavy hole bands, which significantly changes the VB structure. Deformation potentials from [21] were used to calculate the band-edge movement due to strain. Figure B.4 shows the topmost VB with no applied gate bias. The VB energy peaks near the sidewalls due to lateral strain relaxation, drawing holes to the gated sidewalls.

Two-dimensional quantization of holes in the Ge layer was modeled using a strain-dependent 6×6 $k \cdot p$ Hamiltonian for which 80 eigenstates were calculated for various gate voltages. The wavefunction probability density Ψ^2 for the first eigenstate is shown in Figure B.5(a), and the hole density as a function of position is shown in Figure B.5(b) for w_{NW} = 18 nm. Holes accumulate near the sidewalls due to the smaller effective dielectric thickness (the s-Si acts as a dielectric due to its large 770 meV VB offset with s-Ge [21]) and the lateral strain relaxation discussed above. The E-k_z dispersion for all 80 eigenstates is shown in Figure B.6. The holes are quantized in the x- and y-directions, and therefore do not have a dispersion relation along these directions.

The average inverse effective mass in the transport direction $\langle\langle 1/m_z \rangle\rangle$ was computed by taking an occupancy-weighted average of the inverse effective mass for each k-state:

$$\langle\langle \frac{1}{m_z} \rangle\rangle = \frac{\sum_i \langle \frac{1}{m_z} \rangle_i F_i}{\sum_i F_i} \tag{B.1}$$

where

$$F_i = \sum_k f(k) \tag{B.2}$$

and

$$\langle \frac{1}{m_z} \rangle_i = \frac{\sum_k \frac{v_z}{p_z} f(k)}{\sum_k f(k)} = \frac{\sum_k \frac{\partial E / \partial \hbar k_z}{\hbar k_z} f(k)}{\sum_k f(k)} \tag{B.3}$$

The average inverse effective mass for the ith eigenstate is given by $\langle 1/m_z \rangle_i$, the Fermi occupation of state k is $f(k)$, and F_i is the occupancy sum for all k-states in ith eigenstate. The channel-directed velocity, momentum, and k-vector for a particular k-state are given by v_z, p_z, and k_z respectively.

The inverse effective mass as a function of position is calculated from an occupancy-weighted methodology similar to Eq. (B.1) given by

$$\frac{1}{m_z}(x,y) = \frac{\sum_{i,k} \left(\frac{1}{m_z}\right)_{i,k} f(i,k) \cdot \Psi_{i,k}^2(x,y)}{\sum_{i,k} f(i,k) \cdot \Psi_{i,k}^2(x,y)} \tag{B.4}$$

Here, $\Psi_{i,k}^2(x,y)$ is the wave function probability density function for the ith eigenstate with crystal momentum k along the transport direction. The inverse effective mass as a function of position is shown for w_{NW} = 18 nm in Figure B.7. As seen in the plot, the inverse effective mass is boosted in the sidewall regions where lateral strain relaxation has occurred.

The impact of lateral relaxation on effective mass was also studied by performing 6×6 $k \cdot p$ simulations for bulk Ge under varying strain conditions. The E-k dispersion for Ge biaxially strained to $Si_{0.6}Ge_{0.4}$ is plotted in Figure B.8(a). Figure B.8(b-f) show the impact of reducing the magnitude of lateral strain $|\epsilon_{xx}|$ while keeping ϵ_{yy} and ϵ_{zz} at their biaxial values. Reduction of $|\epsilon_{xx}|$ greatly reduces the effective mass in the transport (z-) direction. In contrast, modification of

$|\epsilon_{yy}|$ (vertical direction) does not significantly change the transport effective mass (Figure B.8(g-h)).

The ballistic velocity v_θ was computed from the average inverse effective mass using the following relation

$$v_\theta = \sqrt{2kT\langle\langle 1/m_z\rangle\rangle/\pi} \quad \text{(B.5)}$$

which is valid for the non-degenerate regime [114], [115]. kT is the thermal energy. Figure B.9 shows the increase in $\langle\langle 1/m_z\rangle\rangle$ and v_θ with lateral strain relaxation of 10-nm thick biaxially strained Ge planar FETs. The computed values for unstrained and strained Si are also shown for reference. As shown in the figure, a significant increase in v_θ is predicted as the lateral strain is relaxed. In NW devices with initial biaxial strain, the magnitude of lateral strain $|\epsilon_{xx}|$ can be reduced by decreasing the NW width as shown in Figure B.10.

Figure B.11 shows $\langle\langle 1/m_z\rangle\rangle$ as a function of w_{NW} compared to 10 nm-thick planar Si and Ge. The inverse effective mass increases as w_{NW} decreases due to decreasing $|\epsilon_{xx}|$ in narrow NWs. Experimentally, a 2.0× mobility improvement was measured (μ = 1490 $cm^2/(V{\cdot}s)$ at $N_{inv} = 7\times10^{12}$ cm^{-2}) in a 49-nm wide NW compared to an on-chip biaxially strained Ge *p*-MOSFET [113], consistent with the 1.6× computed $\langle\langle 1/m_z\rangle\rangle$ ratio. Though mobility reduction with decreasing w_{NW} was measured experimentally [113], this is likely due to un-optimized sidewall gate dielectric and large line edge roughness (~1.2 nm RMS). Indeed, high hole source injection velocity exceeding 10^7 cm/s has recently been demonstrated in short-channel NW trigate *p*-MOSFETs with a strained $Si_{0.73}Ge_{0.27}$ channel and w_{NW} = 10 nm [118], indicating that v_θ enhancement is achievable at small NW widths.

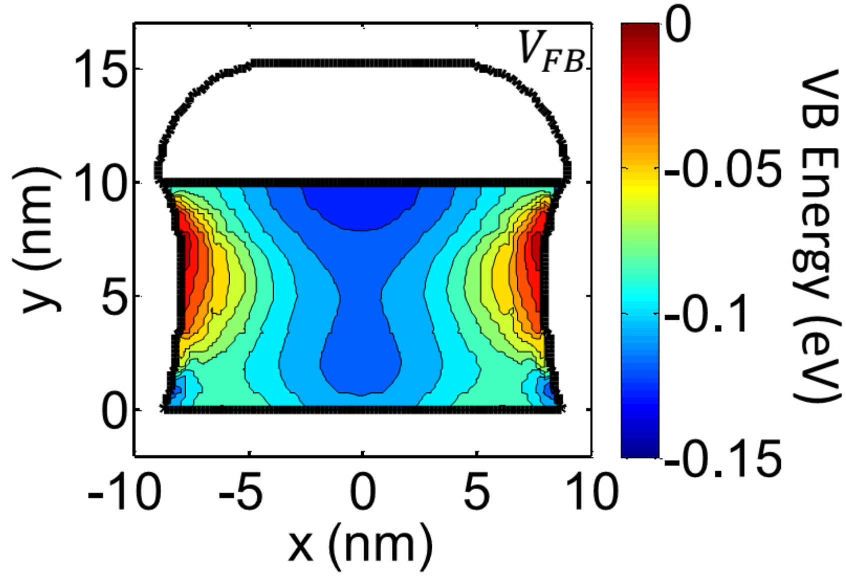

Figure B.4. Topmost valence band (VB) edge at V_{FB} for w_{NW} = 18 nm. The gradient in the VB is due to lateral strain relaxation near the sidewalls. The VB is a mix of *heavy*- and *light-hole* character (highlighted in Figure B.6) due to strain.

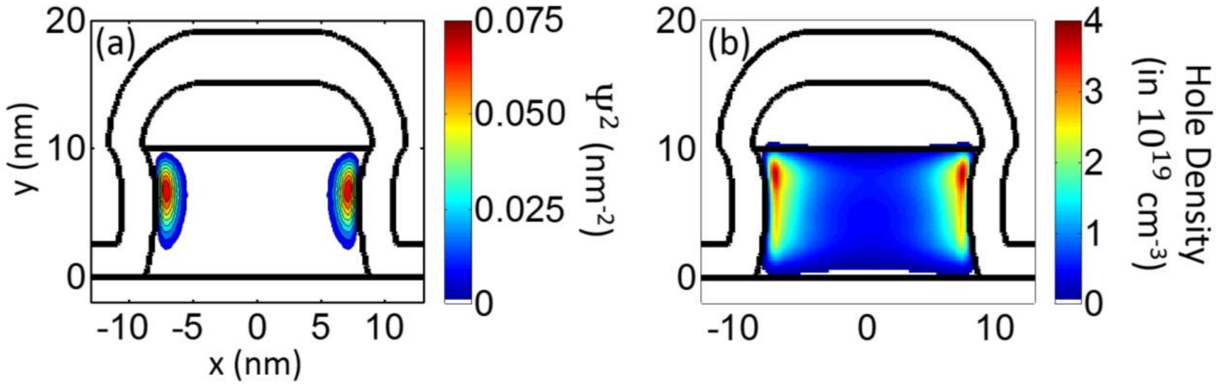

Figure B.5. (a) Wave function probability density Ψ^2 for the first eigenstate and (b) hole density at V_{FB} – 0.5 V for w_{NW} = 18 nm. At this bias, the hole density per channel length is 1.4×10^7 holes/cm, and the sheet density (normalized by gate perimeter) is N_{inv} = 2.9×10^{12} holes/cm^2.

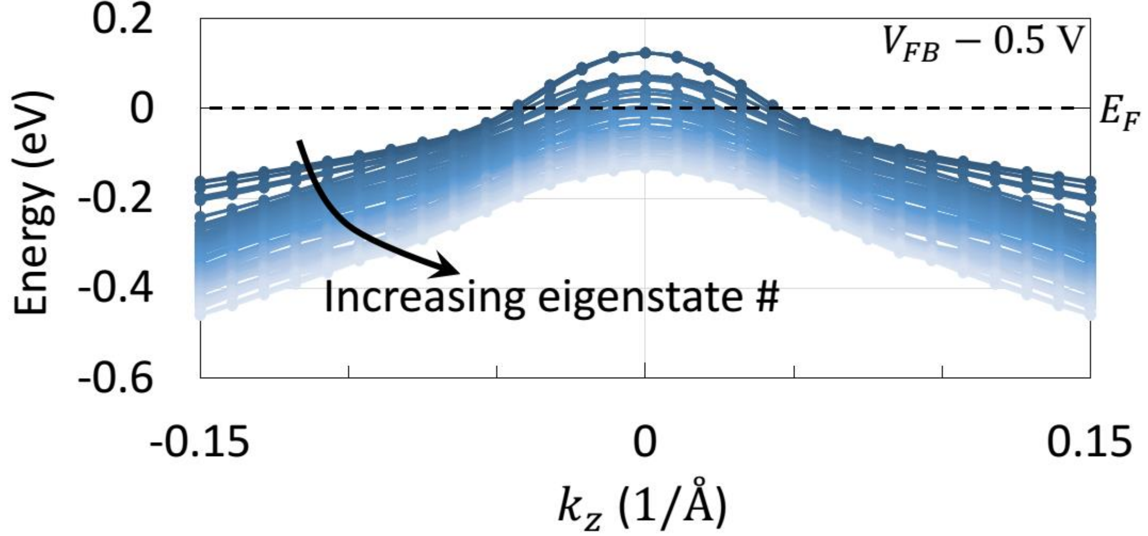

Figure B.6. E-k_z **dispersion for all 80 simulated eigenstates at** V_{FB} **– 0.5 V. The dispersion has a** ***light-hole*** **character for small** $|k_z|$ **and a** ***heavy-hole*** **character for large** $|k_z|$ **due to band mixing caused by strain.**

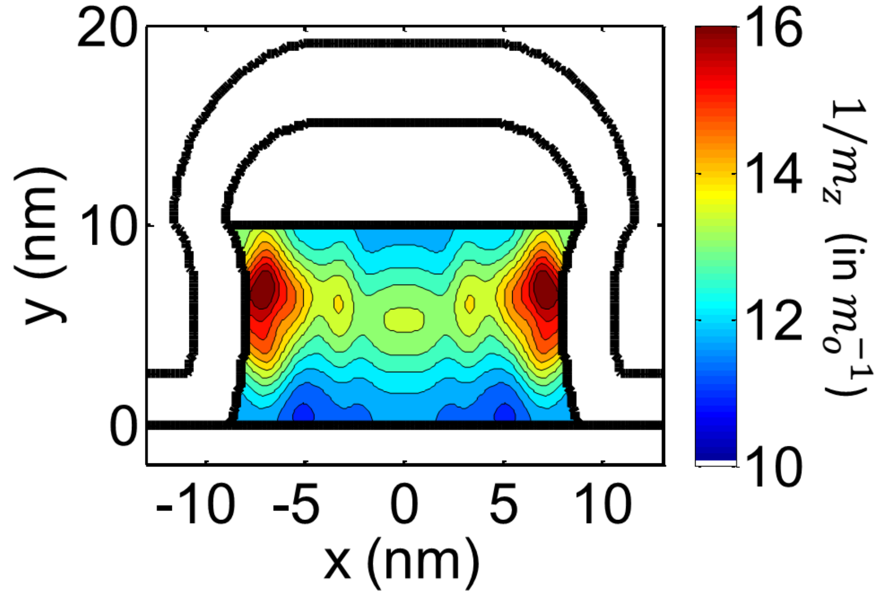

Figure B.7. Hole inverse effective mass $1/m_z$ **as a function of position in the Ge layer for** w_{NW} **= 18 nm and** N_{inv} **= 2.9×10^{12} holes/cm^2. The inverse effective mass is calculated for each** k_z**-state, and an occupancy-weighted average over these states is calculated as a function of position as given by Eq. (B.4). The inverse effective mass peaks near the sidewalls where** $|\epsilon_{xx}|$ **is reduced.**

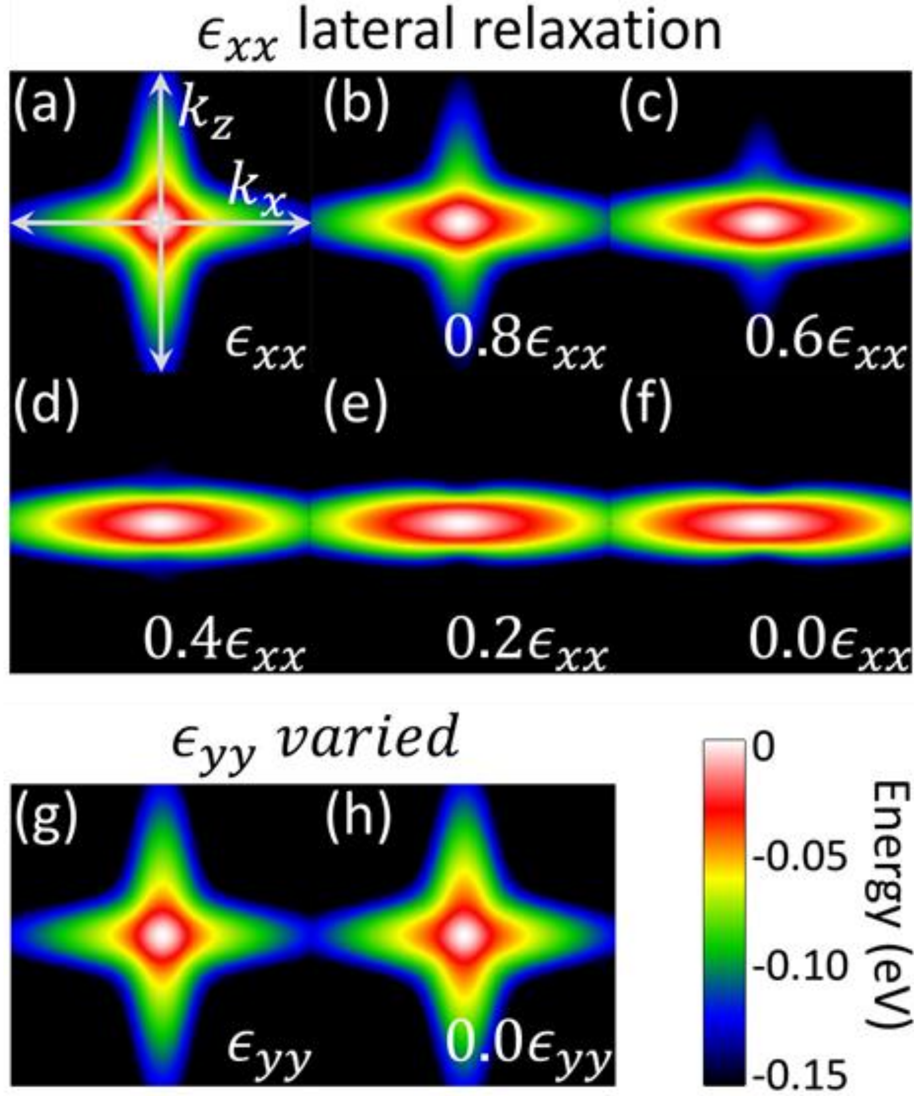

Figure B.8. ***E*-*k* dispersion for bulk Ge with (a-f) varying ϵ_{xx} lateral strain and (g-h) varying ϵ_{yy} vertical strain. (x, y, and z correspond to the lateral, vertical, and channel/transport directions shown in Figure B.1.) (a) and (g) correspond to Ge biaxially strained to a $Si_{0.6}Ge_{0.4}$ substrate (ϵ_{xx} = ϵ_{zz} = -2.4%, ϵ_{yy} = 1.8%). (b-f) ϵ_{xx} is reduced as indicated; ϵ_{yy} and ϵ_{zz} are fixed at 1.8 and -2.4%, respectively. (h) ϵ_{yy} is reduced to 0%; ϵ_{xx} = ϵ_{zz} = -2.4%. The effective mass in the z-direction significantly reduces as $|\epsilon_{xx}|$ is decreased. In contrast, reducing $|\epsilon_{yy}|$ does not markedly alter the transport effective mass. The *E*-*k* dispersion is shown for k_y = 0 with k_x and k_z in the interval [-0.15, 0.15] (1/Å).**

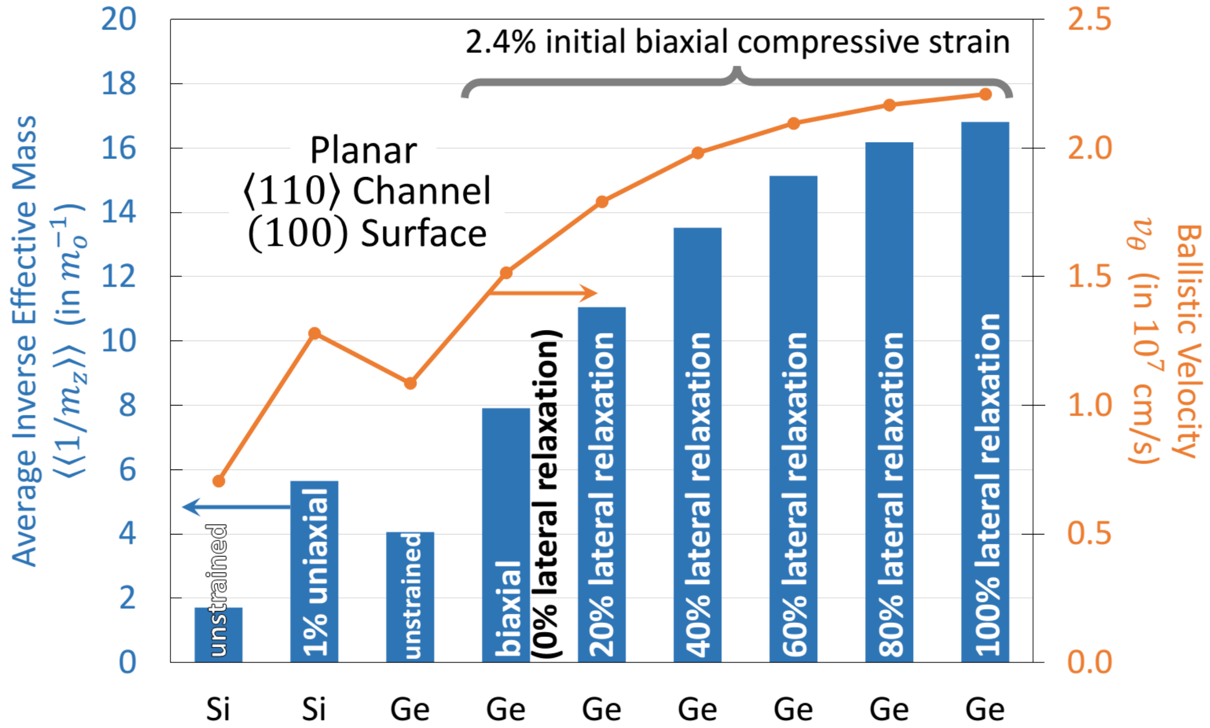

Figure B.9. Average hole inverse effective mass and ballistic velocity for 10-nm thick planar MOSFETs with varying strain and channel material at N_{inv} = 2.5×10^{12} cm^{-2}. The ballistic velocity is calculated from Eq. (B.5). *Si 1% uniaxial* refers to compressive uniaxial stress along the channel where ϵ_{xx} = 0.06%, ϵ_{yy} = 0.36%, and ϵ_{zz} = -1%. The values for *2.4% initial biaxial compressive strain* in Ge are ϵ_{xx} = ϵ_{zz} = -2.4% and ϵ_{yy} = 1.8%. *Lateral relaxation* refers to a hypothetical case where ϵ_{xx} relaxes by the specified amount, but ϵ_{yy} and ϵ_{zz} remain at their biaxial values. As also shown qualitatively in Figure B.8, $\langle\langle 1/m_z \rangle\rangle$ and v_θ significantly improve as $|\epsilon_{xx}|$ is reduced in asymmetrically strained Ge.

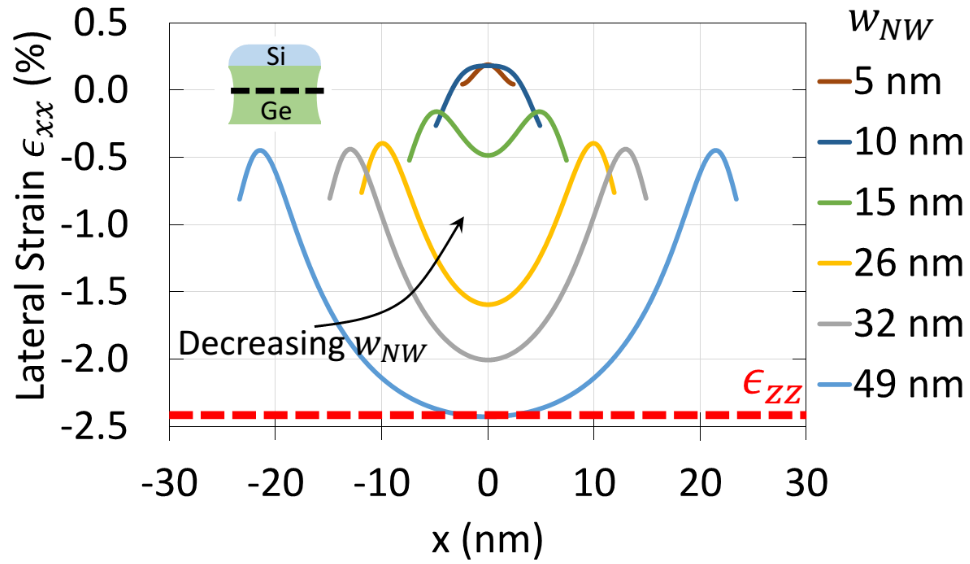

Figure B.10. Lateral strain (ϵ_{xx}) for w_{NW} = 5 to 49 nm for a lateral cut across the middle of the Ge layer at y = 5 nm (see inset). Significant lateral strain relaxation occurs as the NW width is decreased. For $w_{NW} \leq$ 10 nm, the lateral strain becomes tensile due to the Poisson effect associated with the large compressive ϵ_{zz}.

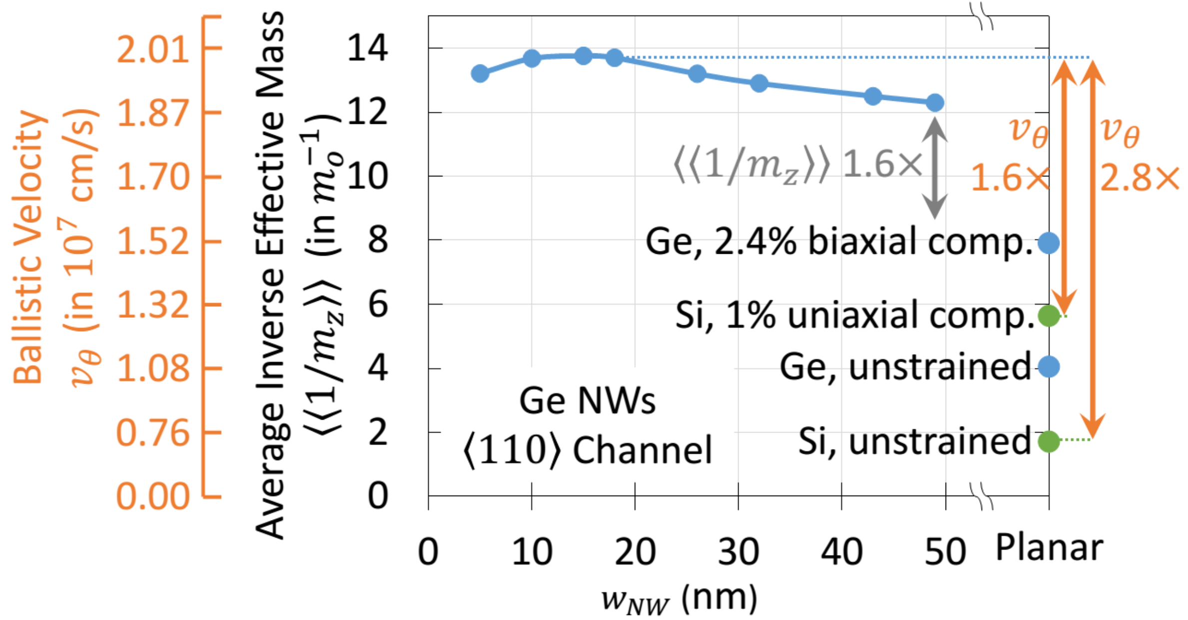

Figure B.11. Simulated inverse effective mass $\langle\langle 1/m^* \rangle\rangle$ and ballistic velocity v_θ for various s-Ge NW widths. v_θ is calculated from Eq. (B.5). $|\epsilon_{xx}|$ decreases as w_{NW} decreases, which causes $\langle\langle 1/m^* \rangle\rangle$ to increase (see Figure B.8 and Figure B.9). Overall, the ballistic velocity enhancement of asymmetrically strained Ge NWs is maintained to w_{NW} = 5 nm. For w_{NW} = 5 nm, increased lateral quantization causes higher $|k_z|$ states to become populated which have a lower inverse effective mass (Figure B.6), which causes a slight decline in $\langle\langle 1/m^* \rangle\rangle$. A 1.6× improvement in $\langle\langle 1/m^* \rangle\rangle$ is calculated for w_{NW} =49 nm compared to planar biaxially strained Ge, which compares well with the measured mobility enhancement of 2.0× [113]. Additionally, a v_θ enhancement of 2.8× relative to unstrained Si (1.6× relative to 1% uniaxial Si) is predicted for 10-nm wide s-Ge NWs. Simulations were performed at N_{inv} ~ 3×10^{12} cm^{-2}.

B.6 Summary

Analysis of the VB structure reveals a 1.6× increase in the inverse effective mass for a 49-nm wide asymmetrically-strained Ge NW compared to planar biaxially strained Ge with 2.4% compressive strain, consistent with previous mobility measurements. In addition, a ballistic velocity enhancement of 1.6× relative to 1% uniaxially strained Si planar *p*-MOSFETs is predicted for 10-nm wide s-Ge NWs with 2.4% compressive strain along the ⟨110⟩ channel. The combination of hole ballistic velocity enhancement and reduced backscattering at the source (inferred from the highly enhanced experimental s-Ge hole mobility) is expected to increase current drive by at least 2× compared to 1% uniaxially strained Si.

Appendix C: Detailed Process Flow for the 3Gate Strained-Si/strained-Ge Bilayer TFET

The process flow below in the table below was used for the fabrication of the 3Gate strained-Si/strained-Ge bilayer TFET making use of the ICL (class 10) and TRL (class 100) cleanrooms that are part of MIT's Microsystems Technology Laboratories.

Table C.1. Detailed process flow for the 3Gate strained-Si/strained-Ge bilayer TFET.

Step	Mask	Process	Steps	Tool
1		RCA clean		RCA-ICL
2		Epitaxial growth		
3		ALD for bottom gate (now on top)	1 minute of O3	ALD-Oxford
4			20 nm Al2O3	ALD-Oxford
5			50 nm TiN	ALD-Oxford
6	Bottom gate	Pattern bottom gate (now on top)	Coat	Coater6
7			Expose	iStepper
8			Develop	Coater6
9			Etch WN (SF6 dry etch)	Rainbow
10			Ash	Asher-ICL
11			Nanostrip, 10 minutes (use own quartzware)	Acidhood-2-TRL
12		Deposit LTO	1 um of LTO (ALD cage)	LTO Tube 6c
13		Densification anneal	500C, 30 minuntes	Tube A2 TRL
14		CMP (Entrepix)	CMP from 600 nm to 400 nm, roughness not to exceed 7 Å	
15		Bond wafers	Double piranha clean	Pre-metal Piranha
16			Thermal oxidiation of RCA cleaned wafer	Tube 5A ICL
17			Activate SiO2 for bonding (both wafers)	AME5000
18			Piranha clean (both wafers)	Acidhood-2-TRL
19			Bond wafers	UV620
20			Anneal bond	Tube A2 TRL
21		Mechanical grinding (SQI)	removal of epitaxial substrate on bonded wafer	
22		Etch-back (stop on s-Si)	Double piranha clean	Pre-metal Piranha
23			Deposit 1 um SiO2 on backside	DCVD
24			TMAH 80C, 10 hrs	TMAH-KOH-ICL
25			Acetic-H2O2-HF, 16 min	Acidhood-2-TRL

26			Etch s-Si etch stop, 80C TMAH	Acidhood-2-TRL
27			SC1	Acidhood-2-TRL
28	Mesa	Mesa isolation	Coat	Coater6
29			Expose	iStepper
30			Develop	Coater6
31			Etch semiconductor body (Cl_2,HBr)	AME5000
32			Ash	Asher-ICL
33			Pure H_2SO_4 (96%) followed by HF dip	Acidhood-2-TRL
34		ALD for top gate 1	1 minute of O_3	ALD-Oxford
35			6 nm HfO_2	ALD-Oxford
36			100 nm TiN	ALD-Oxford
37	Top gate 1	Pattern top gate 1	Coat	Coater6
38			Expose	iStepper
39			Develop	Coater6
40			Etch TiN (SF_6)	Rainbow
41			Ash	Asher-ICL
42			Nanostrip, 10 minutes (use own quartzware)	Acidhood-2-TRL
43		ALD for top gate 2	10 nm Al_2O_3	ALD-Oxford
44			100 nm TiN	ALD-Oxford
45	Top gate 2 drain	Pattern drain-side of top gate 2	Coat	Coater6
46			Expose	iStepper
47			Develop	Coater6
48			Etch TiN (SF_6)	Rainbow
49		n+ drain implant (self-aligned to top gate 2)	Implant phosphorus	
50			Ash	Asher-ICL
51	Top gate 2 left-side	Pattern left-side of top gate 2	Coat	Coater6
52			Expose	iStepper
53			Develop	Coater6
54			Etch TiN (SF_6)	Rainbow
55			Ash	Asher-ICL
56	Source implant	Pattern source implant	Coat	Coater6
57			Expose	iStepper
58			Develop	Coater6
59		p+ source implant (not self-aligned)	Implant boron	
60			Ash	Asher-ICL
61			Nanostrip, 10 minutes	Acidhood-2-TRL
62	Bottom gate via	Pattern bottom gate via	Coat	Coater6
63			Expose	iStepper
64			Develop	Coater6
65			Etch Al_2O_3 (Cl_2, BCl_3)	Rainbow
66			Etch HfO_2 (Cl_2, BCl_3)	Rainbow

67				
68			HF dip to remove Al2O3	Acidhood-2-TRL
69	2 masks:	Pattern S/D/TG1 vias	Coat	Coater6
70	S/D vias		Double exposure for S/D + TG1	iStepper
71	TG1 via		Develop	Coater6
72			HF 50:1 to etch through Al2O3, HfO2	Acidhood-2-TRL
73			Ash	Asher-ICL
74			Nanostrip (maybe) or 10:1 NH4:OH	Acidhood-2-TRL
75		Deposit ILD	300 nm SiO2	DCVD
76		Activation/anneal	600C, ~30 min	Tube A3 Sinter
77	ILD via	Pattern ILD via	Coat	Coater6
78			Expose	iStepper
79			Develop	Coater6
80			Etch ILD for all vias (timed CF4 dry etch)	AME5000
81			Ash	Asher-ICL
82			Green piranha (10 min), HF dip to contact all	Pre-metal
83		Deposit contact metal	100 nm Ti	Endura
84			1 um Al	Endura
85	Metal	Pattern contact metal	Coat	Coater6
86			Expose	iStepper
87			Develop	Coater6
88			Etch Ti/Al (Cl2)	Rainbow
89			Ash	Asher-ICL
90		Sinter	450C, 30 min, forming gas	Tube A3 Sinter

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