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High quality Ge on Si by epitaxial necking
Defects reduction of Ge epitaxial film in a germanium-on-insulator wafer by annealing in oxygen ambient

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A method to remove the misfit dislocations and reduce the threading dislocations density (TDD) in the germanium (Ge) epilayer growth on a silicon (Si) substrate is presented. The Ge epitaxial film is grown directly on the Si (001) donor wafer using a “three-step growth” approach in a reduced pressure chemical vapour deposition. The Ge epilayer is then bonded and transferred to another Si (001) handle wafer to form a germanium-on-insulator (GOI) substrate. The misfit dislocations, which are initially hidden along the Ge/Si interface, are now accessible from the top surface. These misfit dislocations are then removed by annealing the GOI substrate. After the annealing, the TDD of the Ge epilayer can be reduced by at least two orders of magnitude to $<5 \times 10^6$ cm$^{-2}$.

High quality Germanium (Ge) has been studied extensively since the late 1980s. Ge is suitable for photo-detector application for wavelength $>1.2$ µm as well as laser application. In addition, Ge has higher carrier mobility than that of silicon (Si), making it a suitable candidate to augment Si. Furthermore, Ge has a lattice constant that is perfectly matched to gallium arsenide (GaAs) (0.07% at 300 K), which can be used as a buffer layer for integration of GaAs based devices on Si substrate.1–4

One of the important parameters in determining the device worthiness of epitaxially deposited layers is the epilayers’ threading dislocation density (TDD). Due to a large lattice mismatch between Ge and Si, a large number of misfit dislocations (MD) and TDD, on the order of $10^{10}$ cm$^{-2}$, may be generated in the heterostructure when Ge is grown directly on Si substrate.

There are reports on high quality of Ge epitaxial layer grown on Si with TDD $>5 \times 10^6$ cm$^{-2}$.$^{5,6}$ Subsequently, the same group has combined the chemical mechanical planarization (CMP) and re-growth method to annihilate the dislocations to provide a lower TDD of $\sim 2 \times 10^6$ cm$^{-2}$.$^{7}$ However, both of the methods require a thick (~10 µm) graded SiGe buffer layer prior to Ge deposition.$^{7}$ Thin buffer layer has also been reported by growing a thin Si$_{0.5}$Ge$_{0.5}$ buffer layer (~10 nm) followed by two-step Ge growth and annealing. However, the reported TDD is $<1 \times 10^7$ cm$^{-2}$.$^{8}$ Another approach is to deposit Ge directly on Si substrate and then introduce annealing step during and/or after the Ge growth to reduce the TDD.$^{9–15}$ However, this approach results in a much higher TDD of $>10^7$ cm$^{-2}$ (Refs. 16–18) and severe Si/Ge inter-mixing at the in growth interface.

In this letter, a method combining direct Ge on Si growth, wafer bonding, and layer transfer for germanium-on-insulator (GOI) substrate fabrication is discussed. This method has resulted in
significant improvement in the TDD of the Ge film after proper heat treatment. The GOI platform not only can be used as a “passive” buffer layer for III-V materials integration on Si but also has applications as active layer in advanced complementary metal-oxide-semiconductor (CMOS) circuit and silicon-based photonics.

A three-step Ge growth was introduced to grow Ge epilayer directly on a Si donor wafer. The three steps in the growth sequence were: (i) low temperature growth at 400 °C to obtain a rather smooth and continuous Ge seed layer as growth template; (ii) low to high temperature ramping from 400 °C to 600 °C at a ramping rate of 6.5 °C/min; (iii) high temperature growth at 600 °C. The details of the buffer-less Ge on Si growth can be found in Refs. 16–18. After that, aluminum oxide (Al$_2$O$_3$) with thickness of ∼10 nm was deposited on both Ge/Si (donor wafer) and Si (001) substrate (handle wafer) by the atomic layer deposition (ALD) method. Al$_2$O$_3$ was chosen due to its higher thermal conductivity than that of SiO$_2$ (30 W m$^{-1}$ K$^{-1}$ vs. 1.4 W m$^{-1}$ K$^{-1}$). Prior to bonding, both wafers were subjected to O$_2$ plasma exposure for 15 s, rinsed with deionized water and then spin-dried. The Al$_2$O$_3$ containing surfaces of the two wafers were then brought into contact. After bonding, the wafer pair was annealed at 300 °C in an atmospheric N$_2$ ambient for 3 h to further enhance the bond strength.

The bonded pair of wafer was sent for grinding to thin the donor Si wafer down to ∼50 µm. ProTEK® B3-25 was spin coated on the backside of the handle wafer to act as a protection layer during the tetramethyl-ammonium hydroxide (TMAH) etching of the Si. The remaining 50 µm of Si was then removed by submerging the bonded pair of wafer into the TMAH solution at 80 °C and etch stop on the Ge layer. The ProTEK B3-25 protective coating was removed in O$_2$ plasma with a power of 800 W. The details of the fabrication process can be found in the Ref. 19.

The GOI substrate was then subjected to annealing at 850 °C in O$_2$ environment for 4 h. After that, the sample was etched in HF solution (49% HF:H$_2$O = 1:20, by volume) for 30 s to remove the oxidized Ge layer.

The qualities of the Ge epitaxial film on the GOI substrate after annealing were characterized by various techniques. The transmission electron microscopy (TEM; Philips CM200) with operating voltage of 200 kV was used to study the dislocations along the Ge/Si interface as well as the threading dislocations on the Ge surface. The strain and quality of the Ge film is measured by Raman using a WITec confocal Raman microscope alpha 300. The excitation laser wavelength of 532 nm was used with both the focus length and objective lens magnification at 80 cm and 100×, respectively. To further confirm the crystallinity and strain level of the Ge epilayer, high resolution x-ray diffraction (HRXRD) was collected using PANalytical X’Pert PRO. Rocking curve based on Si (004) was used in the HRXRD measurement.

The cross-sectional bright field TEM images in Fig. 1 show the cross-sectional view of the GOI before and after annealing. Fig. 1(a) shows the GOI substrate after layer transfer. As can be seen, the misfit dislocations, which are previously confined along the Ge/Si interface, are now accessible from the top surface. This provides the ease to remove the exposed misfit dislocations by chemical mechanical polishing (CMP) or annealing. In this study, O$_2$ annealing is chosen because it serves two purposes: (i) oxidation of the Si/Ge intermixed layer and Ge layer to remove the misfit dislocations and (ii) removal of the threading dislocations, once the misfit dislocations are eliminated. Hence, from Fig. 1(b), it shows that the misfit dislocations are removed and the threading dislocations are reduced as predicted. In addition, the thickness of Ge film is also reduced by ∼300 nm after O$_2$ annealing due to the oxide formation on the Si/Ge intermixed layer and top Ge layer.

The TDD can be determined from the plan-view TEM by estimating the dislocations in a given area at a number of locations across the samples as shown in Figs. 2(a) and 2(b). The estimated TDD is 7.69 ± 0.583 × 10$^4$ cm$^{-2}$ and 6.41 ± 0.548 × 10$^4$ cm$^{-2}$, for samples before and after annealing, respectively. The TDD value is estimated based on an average of 20 plan-view TEM images for accuracy. Due to the limitation of the TEM, image with a smaller magnification is impossible. Hence, the TDD values are over estimated.

To quantify the TDD with lower magnification images, field emission scanning electron microscope (FESEM) is used. The samples are etched in iodine solution for 1 s to delineate the threading dislocations. Since the dislocations are etched much faster in the etchant, etch pits can be observed. Before annealing, the density of threading dislocations is so high that etch pits are observed across
FIG. 1. Cross-sectional TEM bright field images show the overall view of GOI substrate for (a) before annealing and (b) after O$_2$ annealing.

the entire sample, and some of the etch pits merge together and form larger pits, as shown in Fig. 2(c). After annealing, the sample exhibits much lower etch pit density, most of them have square shape as shown in Fig. 2(d). Within some of these square etch regions, one can observe circular pits. The estimated etch pit density (EPD) of the GOI sample before and after O$_2$ annealing is 5.2 $\pm$ 0.45 $\times$ 10$^8$ cm$^{-2}$ and 2.5 $\pm$ 0.4 $\times$ 10$^6$ cm$^{-2}$, respectively. It is clearly shown that the EPD is reduced by two orders of magnitude after O$_2$ annealing compared to the unannealed sample. The reason why the defected regions have a square shape is because of the circular pits are located on the crosshatch lines which are often oriented along the two orthogonal $\langle 110 \rangle$ directions. The crosshatch pattern is often observed in a low misfit system (below 2%), or in samples with low TDD ($10^6$ cm$^{-2}$), which is applicable in this case.

FIG. 2. Plan view TEM images show the threading dislocations on the Ge surface from GOI for (a) before annealing and (b) after O$_2$ annealing at 850 $^\circ$C for 3 h. The EPD determination for (c) before annealing and (d) after O$_2$ annealing.
To reduce the total TDD, fusion and annihilation reactions are important. When two threading dislocations (TDs) fuse (e.g., two nearly coplanar 60° dislocations interact to form an edge dislocation, \( \frac{a}{2} [110] + \frac{a}{2} [101] \rightarrow \frac{a}{2} [011] \)), they produce a single resultant TD. Although formation of this type of edge dislocation threading segment reduces the threading dislocation density by 50%, the resulting sessile edge dislocation has little chance of ever exiting the system. Thus, it is a permanent threading dislocation. Annihilation, however, is only possible for TDs with opposite sign. These reactions can take place when the distance between interacting dislocations become smaller than the characteristic cross-section of a specific reaction.\(^{21}\) Both the motion and reaction (fusion and annihilation) of the TDs can be assisted by external and internal factors such as temperature, film growth geometry, internal and externally imposed stress, and point defects.

For every misfit dislocation, there are always two corresponding TDs at the end of the misfit, which must thread to a free surface. Hence, it is also possible to reduce the TDD by spreading the misfits out so that when the threads glide, they can easily thread to the edge of the wafer and not interact with any other dislocations.

In our method, since the top surface that contains most of the misfit dislocations is consumed during oxidation, the threading dislocations are not necessarily forming a loop. In addition, the remaining TDs inside the film are not sessile and able to move readily (as they are not constraint by the misfit) closer to another TD, so that annihilation can be occurred under thermal treatment.

Raman spectroscopy is used to determine the strain level of the Ge epitaxial film. In Fig. 3, no signal originated from the Si-Ge vibration mode is observed after O\(_2\) annealing, indicating that the Si from the Si/Ge intermixed layer is removed. From the inset of Fig. 3, a blue shift of Ge-Ge vibration peak position is clearly observed from 295.58 cm\(^{-1}\) (without annealing) to 301.72 cm\(^{-1}\) (after O\(_2\) annealing). The Ge-Ge peak for GOI after O\(_2\) annealing is very close to the bulk Ge reference (peak at 301.09 cm\(^{-1}\)), indicating the Ge film of the GOI is nearly stress free.

HRXRD is used to determine the strain level of the Ge epitaxial film as well. The XRD analysis in Fig. 4 shows that the Ge epilayer for GOI before annealing is shifted to the right with reference to the Ge bulk substrate as a result of a tensile strain (\(\sim 0.35\%\)). In addition, the Ge signal curve is asymmetric and shows a clear shoulder at the side towards higher incidence angles. This is due to Ge/Si intermixing at the interface during thermal processing that perturbs the abrupt interface, which results in an intermediate Si\(_{1-x}\)Ge\(_x\) layer. However, the Ge epilayer for GOI after annealing is left shifted and moved closer to the Ge bulk substrate, indicating that a much lesser tensile strain (0.07%) in the Ge epilayer. This observation is consistent with the Raman analysis. Furthermore,
FIG. 4. HRXRD profile illustrates the crystallinity and the strain state of the Ge epitaxial films with reference to bulk Ge.

the Ge signal curve is symmetrical, which suggests that the intermediate Si$_{1-x}$Ge$_x$ layer is removed after annealing.

The linear coefficients of thermal expansion (CTEs) of Si, Ge, and Al$_2$O$_3$ are 2.6, 5.9, and 8.1 ppm/°C, respectively. When the Ge is grown on the Si substrate at high temperature, the Ge film is essentially stress-free. During cooling down to room temperature, the Ge layer tends to shrink more than Si as the Ge has higher CTE than that of Si. Since the Ge layer is constraint by the Si substrate, it experiences tensile strain. There are two root-causes that can be used to explain the stress-free state of the Ge film on the GOI wafer after annealing.

(i) The amorphous nature of the Al$_2$O$_3$, deposited by ALD at low temperature, acts as a stress buffer layer to accommodate the stress generated due to the CTE mismatch between the materials. COMSOL modeling is used to further verify this explanation. The fitting parameters are shown in Table I. The simulation results are shown in Fig. 5. When the Ge epilayer on Si substrate is cooled from high temperature, the Ge epilayer experiences a higher tensile stress than Si substrate as shown in Figs. 5(a) and 5(b). After annealing, the Ge film in the GOI sample has similar or lower stress level than that of Si substrate indicating that the Ge epilayer is not constraint by Si and almost stress-free as shown in Figs. 5(c) and 5(d). In addition, the Al$_2$O$_3$ layer has the highest stress among the various layers after annealing. This confirms that the Al$_2$O$_3$ layer acts as a stress buffer to accommodate the stress induced due to the CTE mismatch between the materials.

(ii) Since the Si donor wafer is removed and subsequently the Ge/Si intermixed layer is consumed during annealing in O$_2$, the Ge layer is no longer constraint by the Si and therefore it is able to assume a nearly stress-free state.

TABLE I. Fitting parameters for COMSOL simulation.

<table>
<thead>
<tr>
<th>Materials’ properties</th>
<th>Ge</th>
<th>Al$_2$O$_3$</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coefficient of thermal expansion (ppm/°C)</td>
<td>5.9</td>
<td>8.1</td>
<td>2.6</td>
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<tr>
<td>Density (kg/m$^3$)</td>
<td>5323</td>
<td>3965</td>
<td>2330</td>
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<tr>
<td>Young’s modulus (Pa)</td>
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<td>$400 \times 10^9$</td>
<td>$131 \times 10^9$</td>
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<tr>
<td>Poisson’s ratio</td>
<td>0.26</td>
<td>0.22</td>
<td>0.27</td>
</tr>
</tbody>
</table>
FIG. 5. COMSOL simulation on (a) and (b) Ge on Si after cooling from high temperature growth (650 °C); (c) and (d) GOI substrate after cooling from O₂ annealing. The stress profile of the Ge on Si and GOI substrate along y-direction of the (a) and (c) is shown in (b) and (d), respectively.

In summary, annealing at 850 °C in O₂ environment improves the overall quality of the Ge epitaxial film on the GOI substrate. The TDD is reduced by at least two orders of magnitude to <5 × 10⁶ cm⁻² due to the removal of misfit dislocations. In addition, the Ge film on the GOI substrate is nearly stress free after annealing. Hence, good quality of the Ge epilayer could be useful for any subsequent III-V materials integration and devices fabrication. Moreover, the GOI platform will benefit the future semiconductor technology because of the reduction in parasitic and also short channel effects.

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