High-frequency isolated ac-dc converter with stacked architecture

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Abstract—This paper presents a new isolated ac-dc power converter achieving both high power factor and converter miniaturization suitable for many low power ac-dc applications. The proposed ac-dc converter architecture comprises a line-frequency rectifier, a stack of capacitors, a set of regulating converters, and a multi-input isolated bus converter. Among many suitable circuit implementations, the prototype system utilizes the resonant-transition buck converter as a regulating converter, and the capacitively-aided isolated bus converter for the isolated bus converter. The converter is miniaturized by operating at high frequency (1 – 10 MHz range), and it buffers the ac-line frequency energy with a pair of stacked ceramic capacitors (1 \(\mu\)F and 150 \(\mu\)F, 100 V rating) without a requirement for electrolytic capacitors. The prototype converter is implemented to operate from 120 V\(_{\text{ac}}\) to 12 V, and up to 50 W output as an example isolated ac-dc converter for power supply applications. The prototype converter demonstrates with 88% efficiency and 0.86 power factor, and provides 50 W/in\(^3\) power density, which is five times higher than the power density of typical conventional designs.

I. INTRODUCTION

Achieving high efficiency and high power density are definite goals for the ac-dc power supplies. Moreover, while power factor has been traditionally considered important mainly at high power levels to best convey real power from the ac grid to a dc load [1], [2], it is of increasing concern at low power levels as well (e.g., 10s of watts) to reduce the conduction loss and voltage distortion in the grid.

To explore the performance of conventional ac-dc converters, we investigated a group of commercial isolated ac-dc portable device/laptop battery chargers as shown in Table I. The measured specifications illustrate that most of the commercial converters do not achieve both high efficiency and high power factor (e.g., efficiencies in the range of 73 – 88% and power factors of 0.59 – 0.63); Moreover, isolated ac-dc converters at this power level remain bulky and the power densities are in the range of 10 W/in\(^3\) and below though research designs are starting to appear that have higher power density [3].

Most of the ac-dc isolated converters at 10’s of watts utilize the flyback converter topology operated from a line-rectified dc bus. This flyback design, however, provides low power factor and is largely dominated by passive components including the EMI filter, energy buffer capacitor, magnetic transformer, and output capacitors, and thus results in large volume. At higher power levels (e.g., 75 watts and above) and in specific applications such as LED drivers, there are requirements on harmonic content or power factor [4], [5]. One common method to achieve better line waveforms is to cascade a “Power Factor Correction (PFC)” circuit, a large electrolytic capacitor, and a dc-dc converter as illustrated in [1], [2]. In this approach, a front-end PFC circuit modulates the switch(es) so that it shapes the input current waveform over the ac-line cycle for high power factor (often providing a sine-wave or clipped-sine-wave input current waveform), and the associated twice-line frequency power fluctuation is then buffered by its large output capacitor (typically implemented with an electrolytic capacitor). The following dc-dc converter then takes the voltage across the energy buffer capacitor and supplies and regulates the system output voltage.

There are many converter topology options for the front-end PFC circuit including the boost converter [1], [2], [6] and buck converter [7]–[10]. However, these approaches are not amenable to converter miniaturization because: 1) it is hard to greatly reduce the volume of the converter through high-frequency operation owing to loss limits, large inductance (i.e., high characteristic impedance level), and large parasitic capacitance levels (e.g., large output capacitance of the switch) [11]–[13]; 2) the volume of the energy buffer capacitor is large, and 3) for a boost front end, the following dc-dc converter must operate at high voltage when it is tied to the stepped up (high) voltage after the boost PFC converter, and has a large step-down voltage conversion ratio (especially for low output voltage application), so that it is again difficult to be realized at high frequency with small volume.

Here we present an isolated ac-dc converter with a stacked architecture [14], [15] and utilizing a inverted resonant transition buck converter and a capacitively-aided isolated bus converter [16] to provide galvanic isolation and voltage transformation. The proposed ac-dc converter addresses converter miniaturization through high-frequency operation while main-
taining good efficiency, and achieves reasonably high power factor consistent with line harmonic requirements [5], while dynamically buffering twice-line frequency energy at moderate voltages with large voltage swings [17]–[23]. Section II of the paper describes the structure and operation of the proposed stacked ac-dc architecture. Section III and IV of the paper present a circuit implementation and experimental results demonstrating the proposed system. Finally, Section V concludes the paper.

II. STACKED AC-DC CONVERTER ARCHITECTURE

The proposed stacked ac-dc architecture is illustrated in Fig. 1 along with the feedback approach used to provide output voltage control [15]. The system architecture comprises a line-frequency rectifier, a stack of capacitors across the rectifier output, a set of regulating converters having inputs connected to capacitors on the capacitor stack, and a multi-input isolated bus converter that combines the power from the outputs of the regulating converters to provide a single output.

The line-frequency rectifier draws current from the grid during a portion of the cycle, based on how the regulating converters are controlled. The converter can provide high power factor while capacitor $C_2$ (which is much larger than capacitor $C_1$) provides the twice-line-frequency energy buffering over the line cycle.

Regulating converters provide regulated outputs and ultimately regulate the system output under control of the feedback circuitry. Because the regulating converters operate from voltages that are much smaller than the total line voltage, they can be designed to switch at much higher frequencies than conventionally used for converter miniaturization (e.g., as described in [12] [24]). Among many regulating converter topology options, the resonant-transition inverted buck converter can be very effectively utilized [24]. This topology enables converter miniaturization with high-frequency operation (3 – 10 MHz), high efficiency, low device voltage stress, small component size, and good control capability without the need for a current sensor.

The isolated bus converter has two inputs connected to the outputs of the regulating converters, wherein it draws energy from the two regulating converter outputs. The isolated bus converter provides galvanic isolation, voltage transformation while delivering combined power to the converter system output. With the stacked ac-dc architecture and the feedback control of the regulating converters, the isolated converter operates from a low/narrow-range input voltage, and does not need to provide regulation capability; thus the isolated converter can be designed to be very compact operating at high frequency [11] using a capacitively-aided isolated bus converter [16]. The selected capacitively-aided isolated bus converter maintains ZVS condition for all the primary and secondary switches independent of the power level, which thus provides high efficiency with high frequency operation.

A. Operation

Before introducing an example implementation with a specific regulating and isolated bus converter circuit topology, we show how the stacked ac-dc converter structure operates while buffering twice-line-frequency energy at capacitor $C_2$. This approach is related to that of our earlier work [15].

Fig. 2 shows the operating states of the proposed converter with the example operating waveforms. During state 1, the instantaneous amplitude of the ac input voltage is lower than the total voltage of the stacked capacitors; the full-bridge rectifier is off and there is no current drawn from the grid. During this state, the bottom regulating converter (regulating converter 2) delivers and supplies the system power using the stored energy in the energy buffer capacitor $C_2$. When the instantaneous amplitude of the ac input voltage reaches the total capacitor stack voltage, the full-bridge rectifier turns on and the circuit enters state 2. During state 2, the top regulating converter (regulating converter 1) delivers the power while the total voltage of stack capacitors tracks the rectified ac input voltage. The full-bridge turns on and conducts the input current, and capacitor $C_2$ charges up during state 2. After a certain conduction time, the top regulating converter is turned
off and the bottom regulating converter is turned on, and the circuit enters state 1 and the cycle repeats (in state 3, the ac voltage is simply opposite polarity to the state 2, but the converter operation is the same as in state 2).

The proposed architecture accomplishes three functions: First, it draws power from the line with large conduction duration with good power factor. Second, it dynamically buffers twice-line-frequency energy from the line on the capacitor $C_2$, with a significant swing on the voltage of $C_2$ enabling utilization of a large percentage of its energy storage capability in buffering twice-line-frequency power variations from the line. Lastly, while it is not explicitly shown above, the regulating converter steps down the large input voltage, and provides narrow-range regulated outputs (i.e., regulates system output voltage) for the following isolated converter.

**B. System Characteristics, Design Tradeoffs, and Converter Design**

The proposed grid interface architecture we adopt has significant advantages for converter miniaturization through high frequency operation. In addition, there are many tradeoffs among the design parameters including stack capacitance values, power level, capacitor voltage swing variation over line cycle, regulating converter operating range, and power factor. Thus, selecting appropriate topologies, design values, and operating voltage / current waveforms is essential.

One key design parameter is selection of the stack capacitor value $C_1$. A preferred approach is to size the capacitors asymmetrically (one large, one small), such that one of the capacitors (e.g., large $C_2$) buffers most of the twice-line-frequency energy, while the other capacitor (e.g., small $C_1$) is much smaller and simply acts as a bypass capacitor for its associated high-frequency switching stage. One capacitor (e.g., $C_2$) is thus sized principally based on line-frequency energy buffering, while the other capacitor (e.g., $C_1$) can be designed to have a small value and is used for filtering the converter’s switching ripple current. In addition, it should be noted that there is a motivation not to make this bypass capacitor ($C_1$) too large, as the capacitor draws an input current component owing to the ac voltage envelope as illustrated in equation (1), and (capacitively) degrades power factor.

$$i_{C1}(t) \text{ when stack of capacitor tracks ac voltage envelop}$$

$$= C_1 \frac{dV_{C1}}{dt} \simeq C_1 \omega_{ac} V \cos \omega_{ac} t \ll P_o/V \quad (1)$$

Fig. 3 further describes the relation between achievable power factor and the $C_1$ values for a given output power (e.g., $K_{c1p} = C_1 / P_{out}$) when the $K_{c2p} = C_2 / P_{out} = 2 \mu F / W$ and it operates at 120 Vac line voltage. This example shows the detailed effect of $C_1$ capacitance values on the achievable power factor, such that larger $C_1$ value degrades power factor for a given power level and $C_2$ capacitance value. Based on the considerations shown in equation (1) and Fig. 3, it is desirable to make this bypass capacitor ($C_1$) small enough that this capacitive current component is small compared to the active line current that is drawn. We typically select the bypass capacitor to be $K_{c1p} = C_1 / P_{out} = 0.01 – 0.1$. (e.g., for the 50 W ac-dc voltage regulated system implementation shown in section III, we used a capacitor in the range of 1 $\mu F$ for $C_1$.)

Next, several design factors need to be considered for the energy buffer capacitor $C_2$. Capacitor $C_2$ mainly buffers the twice-line-frequency energy of the converter, and the voltage across it fluctuates over the line cycle. We select its value such that it can buffer the needed amount of energy at maximum power operation while having an acceptable voltage swing across which the following regulating converters can operate.

If we make the simplifying assumption of ideal unity power factor, the voltage fluctuation follows equation (2):

$$ac \text{ buffer energy} = P_o / \omega_{ac} = \frac{1}{2} C_2 V_{max}^2 - \frac{1}{2} C_2 V_{min}^2 \quad (2)$$

Fig. 4 further describes the detailed simulation results between voltage swing and the main energy buffer capacitor $C_2$ value (e.g., $K_{c2p} = C_2 / P_{out}$) of the proposed architecture shown in
Fig. 3. The figure shows the achievable power factor of the voltage-regulated system with different $C_1$ values at the given power level (e.g., $K_{c1p} = C_1 / P_{out}$) when $K_{c2p} = C_2 / P_{out} = 2 \mu F/W$. This figure illustrates the effect of small capacitance values (i.e., $C_1$, the capacitor stacked with the main energy buffer capacitor $C_2$) on the achievable power factor. It can be seen that larger $C_1$ values degrades power factor for a given power level and $C_2$ capacitance value.

Fig. 4. This figure illustrates the relation between the voltage swing across the energy buffer capacitor and its capacitance (e.g., $K_{c2p} = C_2 / P_{out}$) when the $K_{c1p} = C_1 / P_{out} = 0.2 \mu F/W$ and the converter operates at 120 V$_{ac}$ input voltage and dc output power $P_{out}$. As shown in the graph, a smaller energy buffer capacitor increases the voltage fluctuation over the line cycle, such that the following regulating converters need to operate across wider voltage ranges.

III. IMPLEMENTATION

Fig. 5 illustrates the implementation of the ac-dc isolated converter. It comprises a line-frequency rectifier, an EMI filter, a stack of capacitors, a set of inverted resonant buck converters having inputs connected to the stack capacitors, and a capacitively-aided isolated bus converter [16]. The two power flow paths from the stacked regulating converters are coupled capacitively with dc blocking capacitors in the isolated bus converter, which combines the power from the regulating converters to supply a single system output. The converter operates at 120 Vac and supplies up to 50 W power at 12 V output, which fits isolated ac-dc applications such as power supplies.

To address the design considerations and achieve high efficiency and high power density, the regulating converters are designed as inverted resonant-transition buck converters as shown in Fig. 5. The regulating converter is designed with single switch, diode, and small inductor, and operates around 3–10 MHz frequency similar to the regulation-stage design illustrated in [12], [13], [15]. It is an “inverted” circuit in the sense that it is designed with “common positives” (i.e., the positive node of the converter’s input voltage is common...
Fig. 5. This figure shows the implementation of the ac-dc isolated converter using a stacked grid interface architecture [15]. The regulating converters are designed as resonant-transition inverted buck converters operating at high frequency, and a multi-input capacitively-aided bus converter is utilized as a dc transformer [16]. The isolated bus converter is coupled with capacitor to combine the power from two regulating converters and supply the single system output.

Fig. 6. The figure shows the layer configuration of the planar transformer for the isolated bus converter (prototype shown in Fig. 9), with the windings implemented as pcb traces in the 12-layer board (with 2 oz/in² of copper). The primary side is realized as 8 turns around the core by parallel-connecting two sets of 2 layers, each having 4 turns/layer, and the secondary is wound with 3 turns by series connecting 3 single turn traces on different layers.

Fig. 7. The figure shows the PI compensator design with isolated error amplifier (Adum3190 from Analog devices which also provides a 1.225 V reference voltage). The voltage divider values are selected such that $V_{out} = 1.225 V$ and the transfer function of this compensator is as shown in Fig. 8.

Fig. 8. This figure shows the asymptotes and intercept of the transfer function of the proposed PI compensator (H(s)) shown in Fig. 7.

(For much of its operating range, the topology acts like a quasi-square-wave ZVS buck converter with a low ratio of switching to resonant frequency [25]. Each regulating converter takes as an input one of the capacitor voltages (from the stack of capacitors) and provides a regulated voltage across its output capacitor. This regulating converter design has several benefits. First, it operates efficiently with ZVS or near-ZVS switching conditions across a wide 35 – 100 V input voltage range. Second, the single common-referenced switch (referenced to a slowly-moving potential) makes it suitable for operation at HF (3 – 30 MHz). It should be noted that in our prototype converter, the regulating converter is designed with a flip-chip Gallium nitride (GaN) on silicon switch; this yields small on-resistance and parasitic capacitance and a compact device size, facilitating high frequency operation. Third, it requires only a single, small-valued inductor. Furthermore, it has very fast response (near single cycle) to input voltage transients and changes in the output current command. Finally, for a given input voltage, the output current is directly related (roughly proportional) to...
the processed information is then delivered to the micro-
sensed, compared, and processed with the compensator, and
the galvanic isolation barrier. The system output voltage is
illustrates how the feedback circuitry is designed to cross
top or bottom regulating converter at any given time. Fig. 7
switch drive circuitry over the line cycle using either the
Then microcontroller regulates the system output voltage using
and processes it with a PI compensator and microcontroller;
voltage. The feedback circuitry senses the system output voltage
we designed feedback circuitry to regulate the system output
regulation) such that the input voltage of the power combining
converters decreases at heavy load (e.g., load
it is biased at 75 V. As can be seen, the size of the inductors
frequency operation of the front-end regulating converters.
for the regulating converters are very small owing to the high

controller across isolation barrier. To accomplish this, we
utilized an isolated PI compensator with the isolated error
amplifier IC (ADuM3190, Analog Device) as illustrated in
Fig. 7. We used a simple PI compensator; its transfer function
is shown in Fig. 8. It should be noted that the sensed output
time information and compensator circuitry should cross
the galvanic isolation and control the front-end regulating
converters with microcontroller and switch drive circuitry, such
that voltage isolation is also required for the compensator
circuitry.

Fig. 9 shows a photograph of the prototype converter
along with a description of the components; and the proto-
type converter is implemented within a 2.1 in (x) × 1.95
in (y) × 0.22 in (z) converter “box volume”. We used 570 µF X7S 100V Ceramic capacitor

In this isolated ac-dc prototype converter implementation,
we designed feedback circuitry to regulate the system output
voltage. The feedback circuitry senses the system output voltage
and processes it with a PI compensator and microcontroller;
Then microcontroller regulates the system output voltage using
switch drive circuitry over the line cycle using either the
top or bottom regulating converter at any given time. Fig. 7
illustrates how the feedback circuitry is designed to cross
the galvanic isolation barrier. The system output voltage is
sensed, compared, and processed with the compensator, and
the processed information is then delivered to the micro-

transistor on-time, allowing a variety of control schemes to be
employed. The details of the design including operation and
drive circuitry is well illustrated in [15].

For the isolated bus converter, we selected an 8:3 trans-
former turns ratio and designed a planar transformer as illustrated in Fig. 6. The turns ratio of the transformer also sets the
e voltage transformation ratio of the capacitively-aided isolated
bus converter, such that the input of the isolated bus converter
(e.g., output of the inverted resonant-transition buck converter)
is roughly around 32 V at 12 V system output voltage. It was
found that for fixed input voltage, the output voltage of the power combining converter decreases at heavy load (e.g., load
regulation) such that the input voltage of the power combining
converter increases up to 36 V to regulate the system output
voltage to 12 V at heavy load. Even though the intermediate
e voltage (e.g., the output voltage of the regulating converter
bus converter, such that the input of the isolated bus converter

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circuitry.

IV. EXPERIMENTAL RESULTS

The ac-dc isolated prototype converter is tested from a
120 V ac power source (Agilent, 6812B) into an resistive
load. One external 5V power supply (xantrex, XPH series) is
used for the hotel power supply to drive logic components,
and used this voltage to bootstrap and make the floating
5V logic voltages. The voltage, current, power, and power
factor are measured with an ac power meter (Yokogawa,
WT1800), and an oscilloscope (Tektronix, MSO4104) and


table

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
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<tr>
<td>Input Voltage</td>
<td>120 Vac</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>12 Vdc</td>
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<tr>
<td>Output Power</td>
<td>48 W</td>
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<tr>
<td>ac Energy Buffer</td>
<td>570 µF (15 µF × 38) X7S 100V Ceramic capacitor</td>
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<th>Regulating Converter</th>
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<tr>
<td>Switch</td>
<td>GaN switch EPC 2010C EPC</td>
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<tr>
<td>Diode</td>
<td>Silicon Schottky diode STPS30120DF ST</td>
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<tr>
<td>Inductor</td>
<td>800 nH; 10 turns on a Micrometals P68-106 core</td>
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<th>Power Combining Converter</th>
<th>Value</th>
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<tr>
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<tr>
<td>Output Power</td>
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<tr>
<td>Energy Buffer Capacitor</td>
<td>570 µF (15 µF × 38) X7S 100V Ceramic capacitor</td>
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<th>Control</th>
<th>Value</th>
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<tr>
<td>Microcontroller</td>
<td>TMS320F28035, TI</td>
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<tr>
<td>Feedback isolated error amplifier</td>
<td>ADuM3190, Analog Device</td>
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</table>
In this paper, we propose an isolated ac-dc converter for power supply applications that uses a stacked grid interface architecture operating at high frequency. This helps address the need for both high power density and good efficiency in ac-dc applications. The proposed approach can achieve reasonably high power factor above 0.8, while dynamically buffering twice-line frequency energy using small capacitors operating with large voltage swings over the ac line cycles without requiring electrolytic capacitors. Regulating converters are designed with the inverted resonant buck converters and operated at high-frequency (3–10 MHz) with significantly reduced voltage stress of the active and passive devices and zero-voltage switching (ZVS) conditions, enabling significant converter size reduction while maintaining high efficiency. The galvanic isolation stage is designed with a capacitively-aided isolated bus converter achieving ZVS for all the primary and secondary switches. Experimental prototypes have been built and evaluated from 120 \text{V}_{\text{ac}} and 12 \text{V}, 50 \text{W} output, and the converter shows that excellent combinations of power density, efficiency, and power factor can be realized with this approach.

V. CONCLUSION

In this paper, we propose an isolated ac-dc converter for power supply applications that uses a stacked grid interface architecture operating at high frequency. This helps address the need for both high power density and good efficiency in ac-dc applications. The proposed approach can achieve reasonably high power factor above 0.8, while dynamically buffering twice-line frequency energy using small capacitors operating with large voltage swings over the ac line cycles without requiring electrolytic capacitors. Regulating converters are designed with the inverted resonant buck converters and operated at high-frequency (3–10 MHz) with significantly reduced voltage stress of the active and passive devices and zero-voltage switching (ZVS) conditions, enabling significant converter size reduction while maintaining high efficiency. The galvanic isolation stage is designed with a capacitively-aided isolated bus converter achieving ZVS for all the primary and secondary switches. Experimental prototypes have been built and evaluated from 120 \text{V}_{\text{ac}} and 12 \text{V}, 50 \text{W} output, and the converter shows that excellent combinations of power density, efficiency, and power factor can be realized with this approach.

ACKNOWLEDGMENT

The authors gratefully acknowledge the support of Texas Instruments for this project.
TABLE III
PERFORMANCE COMPARISON OF THE ISOLATED AC-DC CONVERTERS

<table>
<thead>
<tr>
<th>Reference</th>
<th>[26]</th>
<th>[27]</th>
<th>[28]</th>
<th>[3]</th>
<th>This work</th>
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<tbody>
<tr>
<td>Topology</td>
<td>boost PFC + isolated Converter</td>
<td>clamped series resonant</td>
<td>Flyback</td>
<td>boost PFC + LLC isolated + isolated bus</td>
<td>stacked resonant buck</td>
</tr>
<tr>
<td>Input voltage</td>
<td>120 V_{ac}</td>
<td>120 – 240 V_{ac}</td>
<td>120 – 265 V_{ac}</td>
<td>12 V_{ac}</td>
<td></td>
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<tr>
<td>Output voltage</td>
<td>12 V_{dc}</td>
<td>19.5 V</td>
<td>20 V</td>
<td>12 V_{dc}</td>
<td></td>
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<tr>
<td>Output power</td>
<td>120 W</td>
<td>65 W</td>
<td>65 W</td>
<td>50 W</td>
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<tr>
<td>Switching frequency</td>
<td>135 kHz</td>
<td>1 MHz</td>
<td>800 kHz</td>
<td>3 – 10 MHz (buck dc-dc)</td>
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<td>Transformer</td>
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<td>345 µH</td>
<td>unknown</td>
<td>12 µH, 95 µH</td>
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<tr>
<td>capacitor</td>
<td>200 µF electrolytic (estimated)</td>
<td>76 µF electrolytic</td>
<td>94 µF electrolytic</td>
<td>33 µF</td>
<td></td>
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<tr>
<td>Peak Efficiency</td>
<td>91 %</td>
<td>92.5 %</td>
<td>92 %</td>
<td>94 %</td>
<td></td>
</tr>
<tr>
<td>Power factor</td>
<td>0.99</td>
<td>0.99</td>
<td>0.6 (estimated)</td>
<td>unknown</td>
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<tr>
<td>Box Power density</td>
<td>13 W/in³</td>
<td>7.5 W/in³</td>
<td>25 W/in³</td>
<td>44 W/in³</td>
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REFERENCES


