Reduction of on-resistance and current crowding in quasi-vertical GaN power diodes

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Yuhao Zhang, Min Sun, Daniel Piedra, Jonas Hennig, Armin Dadgar, and Tomás Palacios

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Reduction of on-resistance and current crowding in quasi-vertical GaN power diodes

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This paper studies the key parameters affecting on-resistance and current crowding in quasi-vertical GaN power devices by experiment and simulation. The current distribution in the drift region, n'-GaN, was found to be mainly determined by the sheet resistance of the current spreading layer, n'-GaN. The actual on-resistance of the drift region significantly depends on this current distribution rather than the intrinsic resistivity of the drift layer. As a result, the specific on-resistance of quasi-vertical diodes shows a strong correlation with the device area and sheet resistance of the current spreading layer. By reducing the sheet resistance of the current spreading layer, the specific on-resistance of quasi-vertical GaN-on-Si power diodes has been reduced from ~10 mΩ cm⁻² to below 1 mΩ cm⁻². Design space of the specific on-resistance at different breakdown voltage levels has also been revealed in optimized quasi-vertical GaN power diodes. Published by AIP Publishing. https://doi.org/10.1063/1.4989599

Gallium nitride (GaN)-based vertical power devices have attracted increasing attention, due to their advantages over GaN lateral devices, including high breakdown voltage (BV) and current capability for a given chip size, and superior thermal performance.1 Recent demonstrations of high-performance vertical GaN diodes2–4 and transistors5–7 have made vertical structures very promising. However, the high cost and small diameter of GaN substrates are important obstacles for the commercialization of vertical GaN power devices. Vertical GaN devices on low-cost and large-scale substrates are therefore highly desired. Recently, vertical GaN power devices have been demonstrated on Si,13,14 and sapphire12–14 substrates. Due to the use of insulating substrates (e.g., sapphire) or transition layers, many vertical GaN devices on Si and sapphire substrates have used a quasi-vertical structure, where a mesa structure is formed with the top electrodes and the bottom electrode located on the same side of the wafer. This is in contrast to the fully vertical structure, typically adopted in GaN-on-GaN devices, where the top and bottom electrodes are located on different sides of the wafer.

Although excellent blocking characteristics at the 500–600 V level have been demonstrated in quasi-vertical GaN-on-Si and GaN-on-sapphire devices,3,13 their on-resistance (R_on) is typically much larger than R_on in fully vertical GaN-on-GaN devices. This large R_on is possibly due to the current crowding effects in quasi-vertical structures, as suggested by studies on GaN-based light emitting diodes (LEDs).15–17 However, the epitaxial structures used in quasi-vertical power devices are different from those in LEDs. LED structures mainly consist of a p-GaN layer and an n⁻-GaN current spreading layer. Quasi-vertical power diodes have an additional thick and lightly doped n⁻-GaN drift layer (or i-GaN) between p-GaN and n⁻-GaN, which is designed to sustain high reverse voltage. This thick n⁻-GaN layer makes the current distribution and R_on composition more complicated. In this letter, we present a quantitative and comprehensive study of R_on and current crowding in quasi-vertical GaN power diodes. By optimizing the current spreading layer, this letter demonstrates a reduction of R_on in quasi-vertical GaN-on-Si power diodes by one order of magnitude, with respect to the previous state of the art.

Figure 1(a) shows the schematic of a quasi-vertical GaN-on-Si pin diode, and Fig. 1(b) shows a representative cross-sectional scanning electron microscopy (SEM) image of the wafer. The wafer structure consists of a p-GaN layer,

![Figure 1](image-url)

FIG. 1. (a) Schematic cross-sections of quasi-vertical GaN-on-Si pin diodes with passivation and field plate structures. (b) Cross-sectional SEM images of top GaN layers in the GaN-on-Si wafer. (c) Net ionized donor/acceptor concentration as a function of depth in a GaN-on-Si wafer structure, revealed by the Electrochemical C-V (ECV) measurement. To avoid the impact of possible p-GaN residues during the ECV measurement, the N_D profile in n⁻-GaN was measured after a complete removal of the p-GaN layer. The N_D profile in the first top ~1 μm of GaN is difficult to measure, due to the depletion region of the Schottky tip.
TABLE I. Thickness and donor concentration of n⁻-GaN and n⁺-GaN layers, as well as sheet resistance of n⁻-GaN and total device $R_{on}$ in GaN-on-Si wafers I-IV.

<table>
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<tr>
<th>Wafer No.</th>
<th>I</th>
<th>II</th>
<th>III</th>
<th>IV</th>
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<tr>
<td>n⁻-GaN</td>
<td>$t$ (µm)</td>
<td>$N_D$ (cm⁻³)</td>
<td>$R_{on}$ ($Ω/µm²$)</td>
<td>$R_{on}$ ($Ω/µm²$)</td>
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<tr>
<td>n⁺-GaN</td>
<td>$t$ (µm)</td>
<td>$N_D$ (cm⁻³)</td>
<td>$R_{on}$ ($Ω/µm²$)</td>
<td>$R_{on}$ ($Ω/µm²$)</td>
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$R_{on}$ is the sheet resistance obtained from the TLM measurement.

$R_{on}$ is the diode specific $R_{on}$ extracted from forward I-V characteristics at a relative large forward bias (7 V), to avoid the impact of non-ideal contact resistance.

FIG. 2. (a) Dependence of specific contact resistance on current density, obtained from the TLM measurements. Inset: I-V characteristic measured on two p-GaN contacts separated by 15 µm. (b) Simulated and experimental forward I-V characteristics of quasi-vertical pin diodes fabricated on four GaN-on-Si wafers.

TCAD simulations were then performed using a Silvaco ATLAS simulator, based on the models developed for GaN power devices in our previous works. As shown in Fig. 2(a), due to a slight non-linearity in the I-V characteristics of the p-GaN contacts, the extracted specific contact resistance shows a dependence on current density. This dependence was fitted by a polynomial expression and then incorporated into the simulation model. The dependence of electron mobility on $N_D$ was described by Caughey-Thomas approximation: $\mu(N_D) = \mu_{min} + (\mu_{max} - \mu_{min})/(1 + N_D/N_F)$. The values of $\mu_{max}$ and $\mu_{min}$ were optimized by a polynomial expression fitted to the experimental data.

An n⁻-GaN drift layer, an n⁺-GaN current spreading layer, and an iron-doped semi-insulating (Si) GaN layer, all grown by metal-organic chemical vapor deposition (MOCVD) on (111) Si substrates. Four GaN-on-Si wafers have been grown, with different n⁻-GaN and n⁺-GaN layers and the same thickness and doping as p-GaN and Si GaN. The acceptor/donor (N_A/N_D) profile as a function of depth in four wafers was revealed by the electrochemical C-V (ECV) measurement, with a representative profile shown in Fig. 1(c).

The thickness $(t)$ and $N_D$ of n⁻-GaN and n⁺-GaN layers in four wafers are summarized in Table I. Wafers I and II have the same n⁻-GaN but different $N_D$ in n⁺-GaN. Wafers I and III have the same n⁻-GaN but different $t$ in n⁺-GaN. In wafers I-III, the high $N_D > 10^{19}$ cm⁻³ in n⁻-GaN was realized by Germanium doping. In wafer II, the low $N_D \sim 1 \times 10^{16}$ cm⁻³ was achieved by lightly carbon doping to compensate the non-intentional-doping. Wafer IV was used as a reference, and it was not optimized to lower the $N_D$ in n⁻-GaN and increase $N_D$ in n⁺-GaN. This wafer was also used to calibrate our simulation model for a large range of variations in device structures.

In each wafer, quasi-vertical GaN-on-Si pin diodes have been fabricated [Fig. 1(a)], with detailed fabrication processes reported elsewhere. Transmission line measurement (TLM) patterns were fabricated in the p-GaN anode region and the n⁻-GaN cathode region to evaluate the contact resistance and sheet resistance ($R_{sh}$) in these regions. The revealed $R_{sh}$ of n⁺-GaN is summarized in Table I. The specific $R_{on}$ values of quasi-vertical pin diodes were also extracted from the experimental forward I-V characteristics. All the fabricated diodes have circular anodes on p-GaN and ring-shaped cathodes on n-GaN surrounding the circular anodes. According to studies on LEDs, this electrode design set is optimized in geometry for current spreading in quasi-vertical diodes.

FIG. 3. (a)–(c) Simulated current density distribution in the quasi-vertical pin diodes A–C with different n⁻-GaN doping levels and thicknesses, at a forward bias of 10 V; the anode radius is 100 µm in the simulated structures. (d) and (e) Current density along cutlines #1 and #2 in the simulation results presented in (a)–(c). The locations of cutlines #1 and #2 are shown in (a). (f) Exponential fitting for the lateral current distribution along cutline #1, for devices A–C.
\(\mu_{\text{min}}, \mu_{\text{max}},\) and \(N_d\) were fitted as 55 cm\(^2/V\) s, 1000 cm\(^2/V\) s, and \(2 \times 10^{17} \text{cm}^{-3}\), respectively, from Hall and TLM measurements. With these models, a good agreement has been achieved between simulation and experiment for diodes fabricated on four wafers, as shown in Fig. 2(b).

Figures 3(a)–3(c) show the simulated current density distribution in quasi-vertical pin diodes, for three structures with different n\(^+\)-GaN layers. Device A [Fig. 3(a)] has the same \(r\) but a lower \(N_d\) in the n\(^-\)-GaN layer than device B [Fig. 3(b)]. As shown, the current distribution is much more uniform across the n\(^-\)-GaN and n\(^+\)-GaN layers than that in device B. The n\(^-\)-GaN layers of devices B and C have different \(t_c\) and \(N_c\) but the same \(R_{sh} (=1/q\mu t_N D)\). As shown, the current distribution in devices B and C is identical. We then obtained the normalized current density distribution along two cutlines [locations shown in Fig. 3(a)] for devices A–C and plotted the distribution in Figs. 3(d) and 3(e). As shown, \(R_{sh}\) of the n\(^+\)-GaN layer determines the current distribution in the drift region. This can be understood when considering the major current paths flowing vertically in n\(^-\)-GaN and then laterally in n\(^-\)-GaN; if \(R_{sh}\) of n\(^+\)-GaN is small enough, the resistance is similar for the current paths either close to or far away from the anode edge; therefore, current tends to spread away from the anode edge.

Figure 3(f) shows that the lateral current spreading in the n\(^-\)-GaN can be approximated by an exponential function. This exponential distribution was also reported for LEDs.\(^{15}\) From the exponential fitting, we can define a current spreading length, \(L_s\), as the length where the current density has dropped to the 1/e value of the current density at the edge. From simulation, it is found that the extracted \(L_s\) is mainly dependent on \(R_{sh}\) of the n\(^-\)-GaN layer and shows little dependence on the n\(^-\)-GaN layer [Fig. 4(a)]. Similarly, the specific \(R_m\) of pin diodes shows almost no dependence on the doping density of the n\(^-\)-GaN layer [Fig. 4(b)]. This indicates that the actual resistance of n\(^+\)-GaN is mainly determined by the current distribution rather than its resistivity.

The dependence of the specific \(R_m\) of pin diodes on the anode radius is shown in Fig. 4(c). For the large anode radii, the diode specific \(R_m\) linearly increases with the anode radius. If the anode radius is comparable to or below \(L_a\) (\(\sim 30 \mu\text{m}\) in wafers I and III; \(\sim 8 \mu\text{m}\) in wafer IV), the diode specific \(R_m\) becomes independent of the anode radius. This indicates that the current can be regarded as “uniformly distributed” in quasi-vertical devices, similar to that in fully vertical devices, when the anode radius is below \(L_s\). In this case, the total current would scale up with the anode area. However, when the anode radius is larger than \(L_a\), the total current would scale up with the anode perimeter instead of the area.

Finally, the design space of \(R_m\) at different breakdown voltage (BV) levels was simulated for quasi-vertical pin diodes with an optimized n\(^+\)-GaN layer \((N_D = 10^{20} \text{cm}^{-3}\) and \(t = 1 \mu\text{m}\) [Fig. 4(d)]. The BV was modulated by changing the thickness of n\(^-\)-GaN \((t_{-\text{GaN}} = 1-11 \mu\text{m})\) based on the approximation:\(^{8}\) \(BV = 1/2 E_{\text{peak}} N_D G_{\text{GaN}} + 1/2 (2E_{\text{peak}} - qN_D^{\text{GaN}} G_{\text{GaN}} / e)_{\text{GaN}} - G_{\text{GaN}}\). The \(N_D\) value of n\(^+\)-GaN \((N_D^{\text{GaN}})\) and the peak electrical field \((E_{\text{peak}})\) were set as \(10^{16} \text{cm}^{-3}\) and 2.5 MV/cm\(^3\), respectively. As shown, \(R_m\) of these optimized quasi-vertical pin diodes is not sensitive to the drift region thickness and is quite small (\(\sim 0.5 \text{m}\Omega \text{cm}^2\) and \(\sim 2 \text{m}\Omega \text{cm}^2\) for radii of 50 and 300 \(\mu\text{m}\)) for 200–1600 V voltage designs.

In conclusion, this work shows that the \(R_{sh}\) of the current spreading layer is a key factor in current distribution and total device \(R_m\) in quasi-vertical power devices. This finding provides important guidelines to the design of high-current and high-voltage quasi-vertical GaN power devices: (a) although the total thickness of the GaN layers grown on foreign substrates is limited due to the lattice and thermal mismatch, adequate thickness and high doping should be guaranteed for the current spreading layer; (b) total current can be effectively scaled up with the device area when the anode radius is comparable to or smaller than \(L_a\); otherwise,
the current would scale up with the device perimeter. An effective mask for current scaling-up in a quasi-vertical power device may be “multi-finger” mesa strips with the strip width comparable to $2L_s$; (c) fully vertical structures allow for current scale-up with the device area all the time. The feasibility of making fully vertical power devices on foreign substrates has been recently demonstrated by layer transfer technologies or highly doped conductive buffer layers.

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