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Process-to-Panel Modeling of a-Si/c-Si Heterojunction Solar Cells

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Abstract — The cell-to-panel efficiency gap observed in a-Si/c-Si heterojunction solar cells is one of the key challenges of this technology. To systematically address this issue, we describe an end-to-end modeling framework to explore the implications of process and device variation at the module level. First, a process model is developed to connect the a-Si deposition parameters to the device parameters. Next, a physics based device model is presented which captures the essential features of photo-current and diode injection current using the thermionic-diffusion theory. Using the process and device models, the effects of process conditions on cell performance are explored. Finally, the performance of the panel as a function of device and process parameters is explored to establish panel limits. The insights developed through this process-to-panel modeling framework will improve the understanding of the cell-to-panel efficiency gap of this commercially promising cell technology.

I. INTRODUCTION

The a-Si/c-Si heterojunction (HJ) solar cell promises to capture a significant portion of the PV market [1] due to several advantages, such as, better temperature coefficient, possibility for bifacial design, and lower processing temperature. However, the panel performance (and the prospect of large-scale deployment) is still very sensitive to process variations during a-Si deposition. These variations can alter the deposited a-Si film properties, such as, the band-gap, doping etc., which can significantly affect the cell performance, ultimately inducing cell-to-cell efficiency variations. This cell-to-cell variation is the main source of cell-to-panel efficiency gap, an important concern for this emerging technology.

It requires careful and self-consistent modeling and optimization at the process, device, and panel levels to reduce the cell-to-panel efficiency gap due to process variability. Hence, a multi-scale modeling framework is needed to explore the implications of process-device optimization on device-module optimization. The connection between the key process parameters, the device parameters and the module parameters can help establish the ultimate performance limit and commercial viability of a PV technology [2], [3].

Towards this goal, an end-to-end compact modeling framework to integrate the process, device and panel stages of the HIT cell technology (see Fig. 1) is presented. Here, we will study the sensitivities of process/device parameters at the module level and explore the optimization procedures essential for reducing the cell-to-panel efficiency gap. This study may also serve as an illustrative example for process-to-panel optimization flow for other PV technologies.

II. AMORPHOUS SILICON PROCESS MODEL

As discussed in section I, the deposition of a-Si on the c-Si wafer can introduce significant process variations which can ultimately impact the cell-to-panel efficiency gap. For example, a small change in deposition temperature/pressure can significantly affect the a-Si/c-Si band-offset ($\Delta E_V$) (see Fig. 2(a)) which in-turn reduces collection efficiency and the fill-factor ($FF$). Both the front and back a-Si layers can impact the performance of the cell, however, in good quality cells, the impact of front a-Si layer is dominant. Further, given the maturity of process-control of c-Si wafer to provide reproducible cell parameters (doping, bandgap, lifetime, etc.), this is not the dominant source of the cell-to-panel efficiency gap. Here, the a-Si process model which can predict the cell parameters (such as $\Delta E_V$, emitter doping ($N_A$), etc.) based on the a-Si deposition conditions is presented.

A. Process Compact Model

An empirical model connecting the deposition parameters of plasma enhanced chemical vapor deposition (PECVD) of hydrogenated amorphous silicon (a-Si) to the material properties of the created films is developed. This model

![Fig. 2. (a) Schematic of energy band diagram indicating the process dependent a-Si/c-Si band offset $\Delta E_V$. (b) The deposition temperature ($T_p$) and pressure ($P_p$) dependence on the a-Si bandgap ($E_{gsi}^{as}$).](image-url)
incorporates both measured relationships as well as those from the literature to predict film properties such as the material band gap \([4] - [6]\), refractive index, optical constants, conductivity, hole mobility, density and stress, as well as the deposition rate \([7]\) for given process conditions. The included conditions allow for variations in process pressure \((P_p)\), power density, deposition time and temperature \((T_p)\) \([8]\), as well as dopant gas incorporation \([9]\). Relationships are extrapolated or estimated analytically to allow for an increased number of simulated conditions, or computed from a connected parameter, where appropriate (e.g. density and refractive index).

**B. Influence of Process Parameters**

Here, as an illustrative example, the dependence of the a-Si bandgap \(E_{g}^{Sa}\) as a function of deposition temperature \(T_p\) and pressure \(P_p\) is presented, see Fig. 2(b). Typical values of other process parameters discussed in section II A are used in this example. The material band gap is calculated by first starting with a standard baseline condition \((200^\circ C, 400 mTorr, etc.)\), and the influence of the variance of the simulated deposition parameters \((T_p and P_p)\) from this baseline condition are estimated to calculate the a-Si band gap. While \(T_p\) and \(P_p\) are the only process parameters considered here, this general procedure would allow one to calculate the influence of any combination of process parameters of the simulated material.  

*The experimental validation of the process model will be presented in the full paper.*

**III. HETEROJUNCTION DEVICE MODEL**

In this section, we analyze the influence of process parameters on the efficiency of the HIT cell. As mentioned in section I, the properties of the a-Si/c-Si HJ cause several non-ideal effects in the even in good quality cells, thereby degrading their efficiencies. The non-ideal features in the experimental IV characteristics, such as, failure of superposition, injection limited transport in diode current \(J_{Diode}(I)\) \([10]\), occurrence of S-type curve in photo-current \(J_{Pho}(I)\) \([10], [11]\) are all attributed to the presence of large \(\Delta E_p\) at the HJ and low \(N_A\). These non-ideal features are well understood and modelled using numerical simulations (see Fig. 3(a-c)) \([10], [11]\). However, these models cannot be scaled to the panel level due to their inherent complexity. Hence, we need to develop a physics-based compact model to capture the distinctive features of I-V characteristics and relate it to the HJ properties such as \(\Delta E_p\), \(N_A\) etc. Using this compact model, along with the process model described in section II, we can explore the process sensitivity of cell-level performance parameters.

**A. Device Compact Model**

To capture the above mentioned features, \(J_{Pho}\), \(J_{Diode}\) are modelled using diffusion-thermionic emission theory \([12]\). The mathematical formulation will be discussed in the full paper. Here we present the final expression for \(J_{Pho}\), given by

\[
J_{Pho} = qG_{Total}\left(\frac{v_a^{-1} + v_b^{-1}}{v_{f1}^{-1} + v_{a1}^{-1} + v_{b1}^{-1}}\right)
\]

\(1\)

**Fig. 3.** The \(J_{Diode}\) obtained from numerical simulation (□) and compact model (●), indicating the current saturation at \(V_{park}^B\). (b) The corresponding \(J_{Pho}\) also indicates the expected shift in S-type rollover at \(V_{Light}\). (c) The corresponding \(J_{cell}\) is plotted along with \(J_{Diode}\) and \(J_{Pho}\). (d) The schematic of the compact model of the cell with the intrinsic and extrinsic components.

Here, \(G_{Total}\) is the effective generation rate inside the absorber layer (assuming a uniform generation profile), \(v_b\) is the surface recombination velocity at the back interface, \(v_a\) is the diffusion velocity given by \(v_a = D_n/W_c\), where \(D_n\) is the diffusion coefficient for holes and \(W_c\) is the thickness of the absorber region. The \(v_f\) is the emission velocity given by \(v_f = v_n e^{(V-V_{Light})/k_B T}\), where \(v_n\) is the diffusion velocity in the a-Si layer, and \(V_{Light} = \phi_N - \Delta E_p = (\phi_N (V = 0) - \beta V) - \Delta E_p\), \(\beta (0 < \beta < 1)\) is the ratio of potential developed in the absorber to the applied voltage \(V\), \(\Delta E_p\) is the a-Si/c-Si valence band-offset and \(\phi_N\) is the electrostatic potential in the absorber under illumination.

Similarly, the minority carrier current \(J_{Diode}\), is given by

\[
J_{Diode} = q n_c^2 \left(\frac{1}{v_f^{-1} + v_a^{-1}}\right) \left(e^{qV/k_B T} - 1\right)
\]

\(2\)

Here, \(n_c\) is the intrinsic carrier concentration in the absorber layer, \(v_f = v_n e^{-(V-V_{park}^B)/k_B T}\). Note that, at high bias, there can be an additional current component due to the majority carrier transport, *which will be discussed in the full paper.*

A close match between the numerical and the compact model is presented in the Fig. 3 (a-c). The compact model accurately captures the effect of current saturation of \(J_{Diode}\) above \(V_{park}^B\), which is due to injection-limited transport in HJ (see Fig. 3(b)). Further, it also accounts for the S-type curve of \(J_{Pho}\) above \(V_{Light}\), which is due to the HJ barrier for minority carrier collection (see Fig. 3(a)). *The experimental validation of the compact model will be presented in the full paper.*

**B. Influence of Process Parameters**

Based on the process dependence of \(E_{g}^{Sa}\) as described in Fig. 2(b), we explore the corresponding process dependence of \(FF\)...
of the device in Fig. 4. Note that this difference in FF is due to the degree by which the $\Delta E_F$ effects the $J_{cell}$ through the S-type curve of $J_{pho}$. The FF starts to drop-off rapidly for $T_p < 200^\circ C$. Above these values, the FF remains $> 70\%$, as the $J_{cell}$ is now limited by the $J_{diode}$. In the full paper, additional device level effects such as emitter doping ($N_A$), a-Si mobility ($\mu_{Si}$) will be discussed. The sensitivity of process parameters on cell efficiency will be explored.

IV. PANEL PERFORMANCE

A. Module Compact Model

The compact model used to model each cell is shown in Fig. 3(d). The intrinsic components ($J_{photo}$ and $J_{diode}$) are obtained from device model as discussed in section III A. The extrinsic components, which are $R_{shunt}$ and $R_{series}$ are added at the panel level to model the shunt and series resistance of the cells. The cells are connected in series configuration to form a panel of size 12x6. In the full paper, we will the effects of distributed resistances and shunts for more accurate modeling.

B. Influence of Process Parameters

In section III B, we discussed the influence of $P_p$ and $T_p$ on FF of the cell. Here, we will extend this discussion to understand the influence of process parameters at the panel level. $P_p$ and $T_p$ are assumed to vary around a mean values of 760mTorr and 200$^\circ$C with a small variance of 15mTorr and $10^\circ$C respectively. The resulting variation in the normalized cell efficiency at the panel level is presented in Fig. 5. For the assumed process conditions, the optimal cell which has an efficiency of 21.4% (see Fig. 5 (a)), with mean at 20.9% and the overall panel efficiency is 20.5%. Even for such excellent process control, the cell-to-panel efficiency gap is significant (~1%). In practice, however, the process variations are much higher, resulting in a large cell-to-panel efficiency gap. In the full paper, the effect of full process parameter variation space along with, log-normal shunt distributions, etc. on the cell-to-panel efficiency gap will be explored.

V. SUMMARY

A multi-scale end-to-end modeling framework integrating the process, device and panel stages of the a-Si/c-Si HJ technology is presented. The framework provides a unique opportunity to analyze the process parameter sensitivities at the device and the panel level. Using this framework, the cell-to-panel efficiency gap, which is the key challenge to this technology, can be addressed. In particular, the influence of several process parameters ($P_{p}, T_{p}$) on the cell parameters ($E_{G}^{Si}$) the FF of the device is presented as an illustrative example. The physics based device model is extended to the panel level. Then, the cell-to-panel efficiency gap is extracted for a sample process parameter set ($P_{p}, T_{p}$) to illustrate the usefulness of the method. Using this end-to-end framework, the process parameter space will be further explored to understand the origin of the cell-to-panel efficiency gap in a-Si/c-Si HJ solar cells.

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Fig. 4. The deposition temperature ($T_p$) and process pressure ($P_p$) dependence on the FF of the cell.

Fig. 5. (a) The panel simulation shows the normalized efficiency of the cells connected in series configuration obtained for ($P_p,T_p$) of (760mTorr, 200$^\circ$C) and a variance of (15mTorr, $10^\circ$C). (b) The histogram indicates the cell-to-panel efficiency gap of about ~1%, even for excellent process control.