A Simple Semiempirical Short-Channel MOSFET Current-Voltage Model Continuous Across All Regions of Operation and Employing Only Physical Parameters

A Simple Semiempirical Short-Channel MOSFET Current–Voltage Model Continuous Across All Regions of Operation and Employing Only Physical Parameters

Ali Khakifirooz, *Member, IEEE*, Osama M. Nayfeh, *Member, IEEE*, and Dimitri Antoniadis, *Fellow, IEEE*

***Abstract*—A simple semiempirical model $I_D(V_{GS}, V_{DS})$ for short-channel MOSFETs applicable in all regions of device operation is presented. The model is based on the so-called "top-of-the-barrier-transport" model, and we refer to it as the "virtual source" (VS) model. The simplicity of the model comes from the fact that only ten parameters are used. Of these parameters, six are directly obtainable from standard device measurements: 1) gate capacitance in strong inversion conditions (typically at maximum voltage $V_{GS} = V_{dd}$); 2) subthreshold swing; 3) drain-induced barrier lowering (DIBL) coefficient; 4) current in weak inversion (typically $I_{\rm off}$ at $V_{GS} = 0$ V) and at high V_{DS}; 5) total resistance at $V_{DS} = 0$ V and $V_{GS} = V_{dd}$ and 6), effective channel length. Three fitted physical parameters are as follows: 1) carrier low-field effective mobility; 2) parasitic source/drain resistance, 3) the saturation region carrier velocity at the so-called virtual source. Lastly, a constrained saturation-transition-region empirical parameter is also fitted. The modeled current versus voltage characteristics and their derivatives are continuous from weak to strong inversion and from the linear to saturation regimes of operation. Remarkable agreement with published state-of-the-art planar short-channel strained devices is demonstrated using physically meaningful values of the fitted physical parameters. Moreover, the model allows for good physical insight in device performance properties, such as extraction of the VSV, which is a parameter of critical technological importance that allows for continued MOSFET performance scaling. The simplicity of the model and the fact that it only uses physically meaningful parameters provides an easy way for technology benchmarking and performance projection.**

***Index Terms*—CMOS scaling, inversion charge density, MOSFET compact modeling, virtual source velocity.**

I. Introduction

MOSFET compact modeling has been the subject of a vast amount of technical literature, and models of various degrees of complexity and accuracy exist. Conceptually, compact models can be considered to consist of a multilevel hierarchy. At the first level are the carrier charge and transport models, in which some parameters are represented by second-level models of geometry-dependent electrostatics and even by third-level models that capture layout dependencies. While the majority of compact models are concerned with computer-aided-design applications and with accurate and detailed fittings to device characteristics over a range of geometry and layout features, the model presented in this paper belongs strictly to the first level with the goal of providing a simple and intuitive understanding of the underlying carrier transport in modern short-channel planar MOSFETs with the capability, for example, of extracting the virtual source carrier velocity. The "new" semiempirical model describes the short-channel MOSFET current versus voltage characteristics and is valid in all regions of operation, with continuity of both current and its derivatives. To demonstrate the model, this paper also presents some example fittings to state-of-the-art MOSFETs. The model is very simple and reasonably accurate and is based on the physics of short-channel device transport with only physical quantities that are either known, e.g., gate length, or are easily obtainable from standard output and transfer characteristics. While much of the parameter reduction in this model compared to standard compact models comes primarily from the fact that this is only a first level model, still, by adopting a rather simple physical concept as its basis, even at this level, the model has inherent simplicity and requires few fitting parameters. The key value of the model is that it allows extraction of the so-called virtual-source carrier velocity, which is a parameter of great technological importance [1] that cannot be obtained via direct measurement. Moreover, the fact that the model is based only on a limited number of physically meaningful parameters allows for easy technology benchmarking and performance projection [1]. The term "new" here is used with some hesitation because, practically, all ideas used in the model have been discussed in one form or another in the vast topical literature, but to the best of our knowledge, they have never been combined in the way done in this paper. For reasons that will become obvious in Section II, we refer to this model as the virtual source (VS) model.

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II. VS Model in Saturation

In the "charge-sheet approximation," the drain current normalized by width (I_D/W) of a MOSFET can be described by

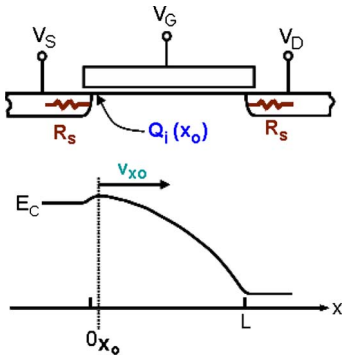

Fig. 1. Virtual source point x_o in the channel of a modern short-channel MOSFET. The carrier charge and velocity, used in (1) and through this work, are defined at this point (at the peak of the conduction band profile).

the product of the local charge areal density times the local carrier velocity anywhere in the channel. It is particularly useful to write this expression at the location of the "virtual source," i.e., at the location of the top of the energy barrier ($x = x_o$) between the source and channel (see Fig. 1) because the channel charge density there Q_{ix_o}, is easiest to model [2], [3], i.e.,

$$I_D/W = Q_{ix_o} v_{x_o}. \tag{1}$$

For short-channel devices, the virtual source velocity, v_{x_o} is related to the so-called unidirectional thermal velocity, or ballistic velocity v_θ, as has been discussed at length elsewhere [2], [3]. It turns out, as will be shown later in this paper by direct comparison with measured data in the literature, that v_{x_o} is weakly dependent on either V_{GS} or V_{DS}, provided that the device is biased in saturation (in either strong or weak inversion). In fact, it has been shown that in the saturation regime, the ballistic velocity and the inversion charge density at the virtual source [except for drain-induced barrier lowering (DIBL) dependence] are independent of V_{DS} [3]. It is further demonstrated that even at the nonballistic regime inversion charge density at the top of the barrier Q_{ix_o} and carrier velocity at this point v_{x_o} are almost independent of V_{DS} if the device operates in the saturation region. On the other hand, while the ballistic velocity increases monotonically with V_{GS} [3], Monte Carlo simulations demonstrate that the virtual source velocity is almost constant at high V_{GS} [1] since carrier scattering also increases with the gate voltage.

Note that instead of using the ballistic velocity along with the backscattering coefficient to describe the I_D–V_{GS} characteristics in saturation, as done, for example, in [3], we opt to use the average velocity of carriers at the virtual source v_{x_o} to avoid the complication caused by exact dependencies of the backscattering coefficient on device parameters and bias, and the ambiguity of the k_BT layer.

The virtual-source charge density can be approximated quite closely by the new empirical function in (2). This expression allows for a continuous expression for the inversion charge density at the virtual source from weak to strong inversion. The form of the expression (i.e., without the new α term in the exponential) was first proposed by Wright [4] as follows:

$$Q_{ix_o} = C_{\rm inv} n\phi_t \ln\left(1 + \exp\frac{V'_{GS} - (V_T - \alpha\phi_t F_f)}{n\phi_t}\right) \tag{2}$$

where $C_{\rm inv}$ is the effective gate-to-channel capacitance per unit area in strong inversion, ϕ_t is the thermal voltage (k_BT/q), V'_{GS} is the internal gate–source voltage, i.e., corrected for the voltage drop on the source resistance R_S and is given by $V'_{GS} = V_{GS} - I_D R_S$, n is the subthreshold coefficient, which is related to the so-called "subthreshold swing" by $S = n\phi_t \ln 10$, and

$$V_T = V_{T0} - \delta V'_{DS} \tag{3}$$

where V_{T0} is the strong-inversion threshold voltage at $V_{DS} = 0$, V'_{DS} accounts for the voltage drop on both R_S and R_D (drain resistance) as $V'_{DS} = V_{DS} - I_D(R_S + R_D)$, and δ is the DIBL coefficient in V/V. Note that DIBL is the only term that introduces dependency of Q_{ix_o} on V_{DS}. The term following V_T in (2) allows for the requirement of different values of threshold voltage (better stated as "reference voltage") in strong and weak inversion, as discussed at length in the literature, e.g., [5]–[7]. It was found empirically in this work that a shift of V_T by $3.5\phi_t$ is a very good approximation, and hence, $\alpha = 3.5$ in (2) is used in this work. The following "inversion transition" function F_f is a Fermi function that allows for a smooth transition between the two values of reference voltage and is centered at the point halfway between them:

$$F_f = \frac{1}{1 + \exp\left(\frac{V'_{GS} - (V_T - \alpha\phi_t/2)}{\alpha\phi_t}\right)}. \tag{4}$$

Fig. 2 compares the approximate solution of (2) with $\alpha = 3.5$ to the exact solution from a 1-D Poisson solution (e.g., [7]) under the sheet-charge approximation and assuming nondegenerate conditions for different values of the body factor: $\gamma = \sqrt{2q\varepsilon_{\rm Si}N}/C_g$. As can be seen in the figure, the approximation in (2) produces an error less than 15% over seven orders of magnitude of channel-charge number-density up to a maximum of 2.5×10^{13} cm^{-2}, which is a sufficient range for most MOSFET applications. Moreover, note that the error in the strong-inversion region is below 5% for more technologically reasonable values of body factor in the range of 0.1–1 V$^{1/2}$. It was found that the errors remained nearly unchanged with temperatures over a wide range, e.g., form -20 °C to 100 °C.

Of course, the virtual source charge density of a short-channel device can only be derived from a 2-D Poisson solution. In the 2-D case, the subthreshold swing is dictated by a combination of doping and geometrical electrostatics. However, the overall shape of the charge versus V_{GS} characteristics does not change, and comparisons with 2-D device simulations, including degenerate conditions (not shown here), indicate that (2)–(4) still yield a good approximation to the charge density with errors no larger than that shown in Fig. 2. All that is required is that $C_{\rm inv}$ at maximum V_{GS}, n, and the value of the charge Q_{ix_o} at a particular value of V_{GS} in weak inversion be all matched to the theoretically calculated (or simulated) charge. Note that matching these three parameters to data uniquely determines the value of V_T. Similarly, it was found by comparisons to theoretical calculations that included the inversion layer quantum-mechanical effect [8] and reasonable amounts of poly depletion [8] that (2)–(4) are still an excellent approximation, provided the above three parameters are matched.

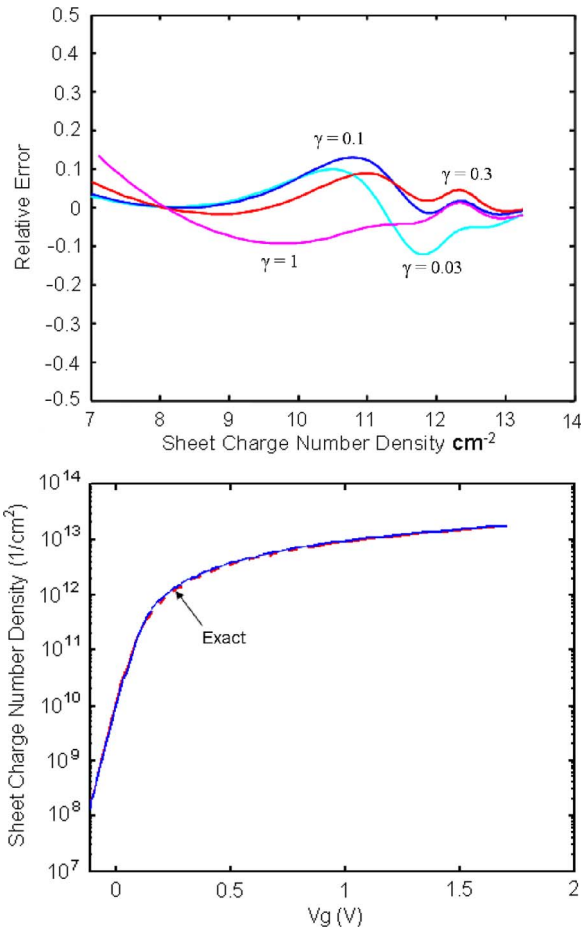

Fig. 2. (a) Relative error of the approximate solution for charge using (2) with $\alpha = 3.5$ as compared to 1-D Poisson solution under the charge-sheet approximation. For comparison, the value of V_{T0} was fitted to match the value of V_{GS} at a charge density of 10^8 cm^{-2} in the exact and approximate solutions. The subthreshold swing was calculated from the classical expression $n = 1 + \gamma/2\sqrt{2\phi_F}$. C_g was matched to the theoretically calculated value at $V_{GS} = 1.2$ V, which was set to 1.9 μF/cm^2 in the theoretical calculation while the body factor γ (in V$^{1/2}$), was varied by changing doping from 10^{16} to 10^{19} cm^{-3}. (b) Model versus exact charge solution for "worst case" approximation for $\gamma = 0.03$.

III. Nonsaturation

To account for the nonsaturation region, the velocity v_{x_o} in (1) is multiplied by a "saturation function" F_s, which increases smoothly from 0, at $V'_{DS} = 0$, to 1, at $V'_{DS} > V_{\rm DSAT}$, where $V_{\rm DSAT}$ is the saturation voltage. Equation (1) is then generalized to (5), given as follows, which is valid over all regions of operation:

$$I_D/W = Q_{ix_o} v_{x_o} F_s \tag{5}$$

$$F_s = \frac{V'_{DS}/V_{\rm DSAT}}{\left(1 + (V'_{DS}/V_{\rm DSAT})^{\beta}\right)^{1/\beta}}. \tag{6}$$

This F_s function is akin to the carrier velocity saturation function used elsewhere [9], [10], but here, it serves to empirically reproduce the nonsaturation behavior of the I–V characteristics. At $V_{DS} = 0$, F_s is 0, while it becomes equal to 1 for $V'_{DS} \gg V_{\rm DSAT}$ and, hence, allows the full value of v_{x_o} in (5). In principle, β is a saturation-transition-region fitting parameter, but it was generally found in this work that excellent fits to measured modern MOSFET data, as will be discussed later, can be obtained with $\beta = 1.8$ for nFETs and $\beta = 1.4$ for pFETs. It is interesting to note that typical values of β when (6) has been used to model carrier velocity saturation are 2 for electrons and 1 for holes [10], [11].

Returning to (6), it is noted that the derivative of this equation with respect to V'_{DS} at $V'_{DS} = 0$ is $1/V_{\rm DSAT}$, irrespective of the value of β, and therefore, we have

$$\frac{1}{W}\frac{\partial I_D}{\partial V'_{DS}}\bigg|_{V_{DS}=0} \cong \frac{Q_{ix_o}(V_{DS}=0) v_{x_o}}{V_{\rm DSAT}} \equiv \frac{1}{W R_{C\,\rm min}}. \tag{7}$$

Here, the approximate sign is used because of the assumption that the V_{DS} dependency of both v_{x_o} and Q'_{ix_o} is negligible. $W R_{C\,\rm min}$ is the width-normalized resistance of the channel at $V_{DS} = 0$ (in ohm centimeters), where it has its minimum value for any given value of V_{GS}, i.e.,

$$W R_{C\,\rm min} = \frac{L_C}{Q_{ix_o 0}\mu} \tag{8}$$

where $L_C = L_G - 2L_{\rm ov}$ is the effective channel length obtained from the gate length, accounting for source and drain overlap $(L_{\rm ov})$, μ is the channel carrier effective mobility at $V_{DS} = 0$ V, which, of course, is a function of V_{GS} but is assumed constant to the first order, and $Q_{ix_o 0} \equiv Q'_{ix_o}(V_{DS} = 0)$ is defined for convenience. Using (8) in (7) determines the value of $V_{\rm DSAT} = V_{\rm DSATs}$ in strong inversion, which is independent of β and only dependent on physical parameters, i.e.,

$$V_{\rm DSATs} = \frac{v_{x_o} L_C}{\mu}. \tag{9}$$

To properly account for saturation in weak inversion, $V_{\rm DSAT}$ in (6) in that region should be equal to ϕ_t. While this is an approximation because F_s is not exactly equal to $1 - \exp(-V_{DS}/\phi_t)$ as it should be in weak inversion, the resulting error is less than about 10% for a range of β values from 1.4 to 2.5 (not shown). Finally, to allow a smooth transition between the strong- and weak-inversion values of the saturation voltage, a generalized form of the saturation voltage is introduced by employing again the inversion transition function F_f, defined by (4), as follows:

$$V_{\rm DSAT} = V_{\rm DSATs}(1 - F_f) + \phi_t F_f. \tag{10}$$

It can easily be seen from (4) that F_f in strong inversion tends to zero, while in weak inversion, it tends to unity, and thus, $V_{\rm DSAT}$ correspondingly varies smoothly from $V_{\rm DSATs}$ to ϕ_t. Fig. 3 exemplifies the behavior of the model over the complete range of operation of a MOSFET. The smooth transition of the saturation voltage from weak inversion to strong inversion is clearly evident.

It should be emphasized that (6) and (10) are heuristic. It can be easily shown from (1), (8), and (9) that $V_{\rm DSATs}$ is approximately equal to the value of V_{DS} where the current through the resistor $R_{C\,\rm min}$ is equal to the saturation current, i.e., it is determined by the intercept of the $1/W R_{C\,\rm min}$ and $Q_{ix_o 0} v_{x_o}$ loci in the I_D/W versus V_{DS} plane. While this is appealing, it is not physically rigorous. In addition, the form of

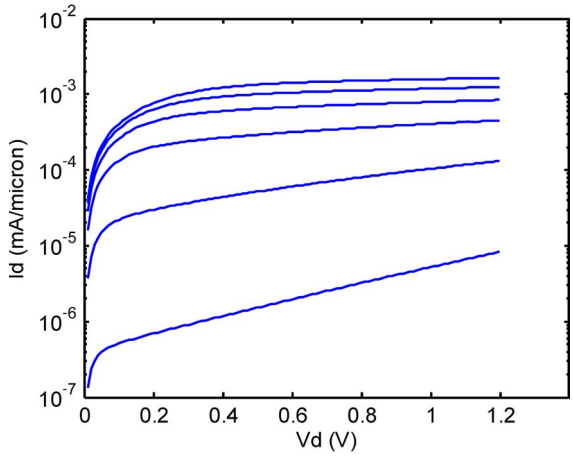

Fig. 3. Model output characteristics as in Fig. 4(a) in a semilog plot to illustrate the continuity of the model from weak to strong inversion and from linear to saturation regions.

(6) is not fully physically justified, even though it is borrowed from the velocity saturation expression [9], [10]—it is not justifiable to assume that the lateral electric field is given by V_{DS}/L_C under all conditions in strong inversion, as actually implied by (6). Nevertheless, as can be seen in Section IV, the fitting of the VS model to real device data is very good and comes with physically justifiable parameters.

IV. Approximate Evaluation of the Model

It is clear from the fact that the internal voltages V'_{GS} and V'_{DS} are required in (5) and (6) that explicit solution of the model equations requires iterations in order to obtain self-consistent values of $V'_{GS} = V_{GS} - I_D R_S$ and $V'_{DS} = V_{DS} - I_D(R_S + R_D)$. However, iterations can be avoided with relatively little loss of accuracy by simply replacing the internal voltages in (2)–(5) by the applied external ones, namely, V_{GS} and V_{DS}, while replacing the virtual-source velocity in (5) by the effective velocity v, which is given by:

$$v = \left(F_f + \frac{1 - F_f}{1 + W R_S C_g (1 + 2\delta) v_{x_o}} \right) v_{x_o}. \qquad (11)$$

As in the case of (10), the Fermi function F_f, which is given in (4), allows for a smooth transition of v from a value of v_{x_o} in weak inversion ($F_f \sim 1$), where there is no degradation due to the presence of R_S, to the value that is appropriately degraded in strong inversion ($F_f \sim 0$). The derivation of the second term in the right-hand side of (11) for the case of operation only in the strong-inversion region and, therefore, for $F_f = 0$ has been discussed in [12] and [13]. In addition, $R_S + R_D$ must be added explicitly to the right-hand side of (8) so that the correct total resistance at $V_{DS} = 0$ V can be obtained. Then, the strong-inversion saturation voltage becomes

$$V_{DSATs} = (R_S + R_D) W Q_{ix_o 0} v + \frac{v L_C}{\mu}. \qquad (12)$$

Finally, it is found that for this implicit solution, the β factor in the saturation function F_s [see (6)] should be set to approximately 2.5 for nFETs and 2.0 pFETs. The model implementation in this approximate form is entirely closed form, which is useful for some applications, but in Section V, only the exact explicit solution given by (1)–(10) is used.

V. Comparison of the Model to Data and Discussion

Example fits to device data of a modern uniaxially strained 65- and 32-nm node technologies [14], [15] are shown in Figs. 4 and 5. As can be seen, the model description of the data is very good over a broad range and of bias values, and over two different technologies, i.e., with poly-SiON and high-k metal-gate stacks. Table I shows the device parameters that can be considered as given for this model, i.e., $C_{\rm inv}$, $I_{\rm off}(V_{GS}, V_{DS})$, S, δ, and L_G. Since the data come from the literature, a value for $L_{\rm ov} = 5$ nm had to be assumed—the same for both technologies. This assumption does affect somewhat the extracted value of μ, as will be discussed next. The extracted parameters are v_{x_o}, WR_S, μ, and β. As can be seen from the table, the extracted values are physically reasonable and come with the correct trend between the two technologies.

The methodology for fitting can be accomplished manually with little iteration, although standard optimization methods can also be used. First, the capacitance $C_{\rm inv}$ is set to the strong-inversion value measured at $V_{GS} = V_{dd}$, which is typically reported. Second, the subthreshold swing parameter n, $I_{\rm off}$ (typically at $V_{GS} = 0$ V and $V_{DS} = V_{dd}$), and the DIBL coefficient δ are obtained directly from the measured transfer characteristics of the device. Naturally, in order to match the calculated $I_{\rm off}$ to the measured value, an initial guess for v_{x_o} is required; a good starting value is $v_{x_o} = 10^7$ cm/s, and it is then refined as described later. Note that this process sets the value of V_T and establishes the correct electrostatic behavior of the device. Third, from the I_D versus V_{DS} output curve for $V_{GS} = V_{dd}$, the total resistance $2R_S + R_{C\,\rm min}$ is obtained from the slope $dI_D/dV_{DS}|_{V_{DS}=0}$ at $V_{DS} = 0$ V—it can typically be assumed that $R_S = R_D$ for symmetric devices. At this point, an assumption about L_C and μ is required in order to isolate and extract R_S. A good typical value for $L_{\rm ov}$ is $\sim 0.15\times$ the nominal short-channel L_G, and $\mu \sim 200{-}300$ cm^2/V $\cdot$ s for electrons and $\mu \sim 100{-}250$ cm^2/V $\cdot$ s for holes in strained Si. Finally, the velocity v_{x_o} is adjusted by comparing model results in saturation with measured data at $V_{DS} = V_{dd}$ and at various V_{GS} values. The model is quite constrained, and therefore, relatively minor adjustments of the initial parameter values are typically required or are, indeed, possible. Typically, in nominal short-channel devices, the parasitic resistance dominates at the highest value of V_{GS}, and therefore, errors in the assumptions for $L_{\rm ov}$ and μ are not very critical for the extraction of R_S, which, in turn, is critical for obtaining an accurate value for v_{x_o}. With some experience and good engineering judgment, very reasonable physical parameters can be obtained, as can be seen in Figs. 4 and 5 and Table I; it should be noted that these particular MOSFETs exhibit the lowest values of R_S in the authors' experience, but they are well within the physical range for well-engineered devices. Furthermore, although the values of carrier velocity may appear high, it should be noted that the devices have

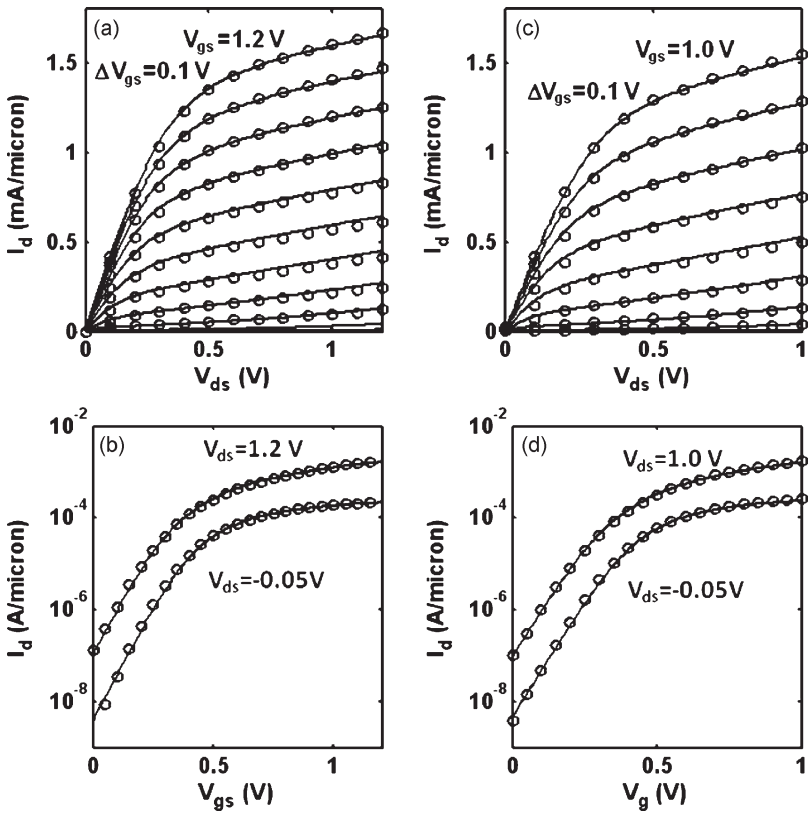

Fig. 4. Comparison of model current (lines) with data (circles). (a) and (b) For a 65-nm technology uniaxially strained nFET technology with poly-SiON gate stack [13] and gate length $L_G = 35$ nm. (c) and (d) For a 32-nm technology uniaxially strained nFET with a metal-gate high-k stack [14] and gate length $L_G = 32$ nm. Device parameters are given in Table I.

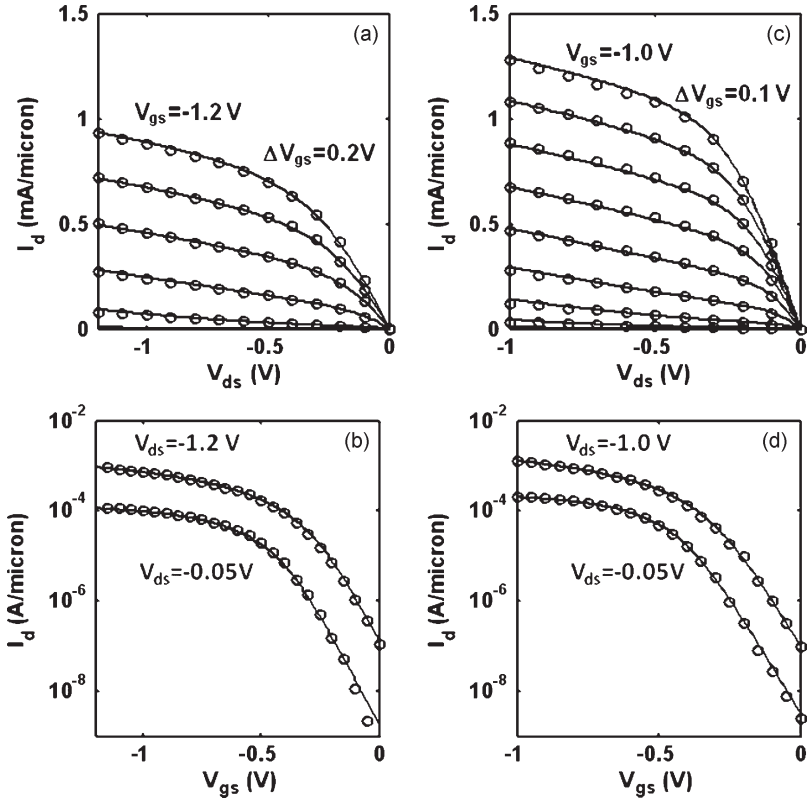

Fig. 5. Comparison of model current (lines) with data (circles). (a) and (b) For a 65-nm technology uniaxially strained pFET technology with poly-SiON gate stack [13] and gate length $L_g = 35$ nm. (c) and (d) For a 32-nm technology uniaxially strained nFET with a metal-gate high-k stack [Intel IeDM 08] and gate length $L_g = 32$ nm. Device parameters are given in Table I.

TABLE I
MOSFET DEVICE PARAMETERS

	65-nm CMOS nFET	32-nm CMOS nFET	65-nm CMOS pFET	32-nm CMOS pFET
C_{inv} [μF/cm^2]	1.83	2.65	1.70	2.60
L_G [nm]	35	32	35	32
L_{ov} [nm]	5	5	5	5
S [V/decade]	0.10	0.098	0.095	0.095
δ [V/V]	0.12	0.13	0.155	0.145
$I_{off}(V_{GS}$=0, $V_{dd})$ [nA/μm]	120	100	135	100
V_{dd} [V]	1.2	1.0	1.2	1.0
v_{xo} [10^7 cm/s]	1.4	1.35	0.85	1.03
WR_S [Ω.μm]	75	80	130	80
μ [cm^2/V.s]	250	250	140	210
β	1.8	1.8	1.5	1.7

been shown to be nonballistic; the thermal velocity (ballistic limit) in these uniaxially strained devices has been shown theoretically to be significantly increased compared to relaxed Si values [1].

The quality of agreement shown in Figs. 4 and 5 was found to hold over numerous devices from the literature as well as experimental devices in the authors' laboratory. Interestingly, the model produces good agreement even with non-MOSFET FETs, such as 50-nm-gate-length InGaAs HEMTs [16] using the same parameter β as for Si nFETs but with suitably increased electron mobility and velocity, as expected for III–V channel materials.

As discussed in Section I, the VS model in this paper was developed primarily in order to allow for simple and largely unequivocal characterization of the historical evolution of virtual source carrier velocity in Si-CMOS FETs operating in the saturation region and to permit extrapolation of future requirements, e.g., as done by Khakifirooz and Antoniadis [17], [18]. Nevertheless, it is rather remarkable that this minimalist model describes very well the I–V behavior of modern MOSFETs over their full range of operation and with only few physical parameters, which, moreover, are held constant. Of course, the model is not predictive in the sense that it requires the electrostatics ($C_{\rm inv}$, S, δ, and $I_{\rm off}$—i.e., V_T) and virtual source carrier velocity and mobility as input parameters either from measurements or device simulations, or simply from educated guesses about future device structures and materials. On the other hand, if gate-length dependence of the electrostatics is available, the model can help in understanding the significance of the effects of the key MOSFET parameters and their variations over a range for gate lengths. As an example, Fig. 6 shows the VS model "predicted" $I_{\rm off}(V_{GS}=0\ {\rm V}, V_{DS}=1.2\ {\rm V})$ versus $I_{\rm on}(V_{GS}=1.2\ {\rm V}, V_{DS}=1.2\ {\rm V})$ for the nFET technology in Fig. 4 [14]. The calculations were made by varying L_G in the model from 30 to 65 nm. For these calculations, the variation of $V_{T_{\rm sat}}$ and $V_{T_{\rm lin}}$ (the typical constant-current threshold voltages at $V_{DS}=1.0$ V and 0.05 V, respectively) versus L_G in [14, Fig. 3] was used to reproduce the DIBL parameter $\delta(L_G)$ and V_{T0} versus L_G dependence in the model. Note that for V_{T0} only the variation with L_G was used from the data because the definitions of V_{T0} here, and $V_{T_{\rm lin}}$ in that paper are different. As can be seen in the figure, even with no other L_G parameter dependences in the model, the calculated $I_{\rm on}$ versus $I_{\rm off}$ (dashes) is in good agreement with the data. Next, since some increase of S with decreasing length can be expected even for these evidently very well engineered devices, a linear $S(L_G)$ dependency on $\delta(L_G)$ was assumed (empirically) as follows: $S(L_G)=S(35\ {\rm nm})+(0.1\ {\rm V/dec})(\delta(L_G)(\delta(35\ {\rm nm}))$. The result is depicted in the dotted line. Finally, a good match to the data is achieved (solid line) by assuming a linear variation of $v_{x_o}(L_G)$ as follows: $v_{x_o}(L_G)=v_{x_o}(35\ {\rm nm})+(10^7\ {\rm cm/s})(\delta(L_G)-\delta(35\ {\rm nm}))$. This form of dependency of velocity for short-channel MOSFETs has been shown in the literature [19], [20], and the coefficient here is quite reasonable. Of course, it cannot be claimed here that the modeled velocity dependency on DIBL is physically correct because the $S(L_G)$ dependency via DIBL was assumed empirically—the data are not available in the literature. On the other hand, $S(L_G)$ is often available from measurements, and if so, then the $v_{x_o}(L_G)$ would have real physical significance, for example, in quantifying the effectiveness of strain engineering in a particular technology.

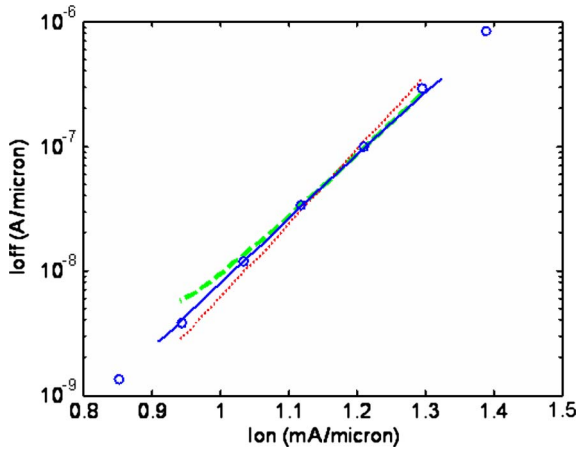

Fig. 6. Modeled versus measured $I_{\rm off}(V_{GS}=0\ {\rm V}, V_{DS}=1.2\ {\rm V})$ versus $I_{\rm on}(V_{GS}=1.2\ {\rm V}, V_{DS}=1.2\ {\rm V})$ for the nFET technology in Fig. 3. Data from [13] are depicted by points. For details of the model-calculated lines, refer to the text.

VI. Conclusion

A minimalist MOSFET model that describes the I–V behavior of short-channel MOSFETs over the complete region of operation has been developed. In addition to physical parameters that are easily obtained from measurements, a minimum set of physically meaningful parameters, all assumed constant over the region of operation, is included, and a methodology for extracting them from data has been presented. The model is suitable for analyzing the effect of variation of these parameters and for technology road-mapping exercises. In addition, the model can form the basis of a compact model for circuit simulation with the addition of models relating its parameters to physical device dimensions and/or layout properties.

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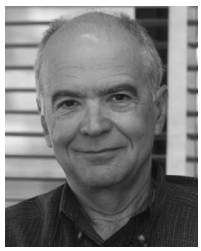

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