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Measurement and Analysis of Contact Plug Resistance Variability

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Abstract—The impact of contacts on device and circuit performance is becoming larger with technology scaling because of higher resistance as well as increased variability. Thus, techniques are needed for measurement, analysis, and modeling of variation in contacts, and for devices, interconnects, and circuits in general, in order to ensure robust circuit design. A test chip for characterizing contact plug resistance variability is designed in a 90nm CMOS process. Each chip is capable of characterizing over 35,000 devices under test. Statistical analysis of the measurement results show that the contact plug resistance changes as a function of key layout parameters, such as the distance from the contact to the polysilicon gate and the distance from the contact to the edge of the diffusion region. Spatial variation analysis shows that the resistance distribution has a systematic die-to-die pattern, possibly caused by variability in the lithography process. Spatial correlation analysis is also performed to identify the possibility of additional systematic trends or separation-distance dependent correlated random variation. Results of these analyses motivate the need for both numerical and compact models for contacts which incorporate variability information.

I. INTRODUCTION

Variability characterization and modeling in advanced technologies are needed to ensure robust performance as well as improved process capability – and methods for the measurement, analysis, and mitigation of variation in devices, interconnects, and circuits are starting to emerge [1] [2]. Key elements of these “statistical metrology” methods include test structure and test circuit designs to gather the large amounts of data required; statistical analysis techniques, including identification of significant effects in spatial design of experiments, variation decomposition, and spatial correlation approaches to quantify variation and its sources; and finally, modeling to understand the impact and implications of variation on devices, circuits, and systems. In this paper, we review and extend these approaches for one important component: contact plug resistance in advanced MOSFETs.

A great deal of work focuses on the characterization and modeling of variability in MOSFETs. In particular, threshold voltage and channel length are two device parameters which have been studied extensively. With increased scaling, however, the parasitic components of the MOSFET are playing a more significant role in determining the performance of a device. Parasitic resistance components resulting from the gate-to-source/drain overlap regions, source/drain extensions, and contact regions are growing in magnitude relative to the intrinsic resistance associated with the channel of the MOSFET. High frequency device characteristics are also increasingly determined by parasitic capacitances associated with the charge storage not only in the channel, but elsewhere in the device as well. As new materials and processing techniques are being investigated to reduce these parasitic effects, it will become important to accurately assess and model the variability in these contacts.

The interface between the device and local metallization layers is critical in understanding the performance and robustness of a MOSFET. Consequently, increasing attention has been paid to the analysis of contact resistance, which represents a growing proportion of the total on-resistance associated with a transistor. ITRS projections predict that the contact resistance will double every technology generation [3]. This is partially due to the higher aspect ratios required for contact plugs in advanced technologies. Methods for contact characterization and analysis can be categorized into four areas: fabrication and measurement of individual contacts, failure and defect analysis, analytical modeling, and arrayed test structures for characterization of parametric variability.

The rest of the paper is organized as follows. Section II reviews existing methods for contact resistance characterization and modeling. Section III describes a new arrayed test structure for contact plug resistance variability characterization, and applies a variety of statistical analysis techniques to understand the measurement results. Section IV underscores the need for variability-based models, and Section V presents some conclusions.

II. BACKGROUND WORK

A. Individual Contact Measurement

A key step in the development of any process involves the characterization of individual components, such as transistors, diffusion resistors, or metallization layers. In this context, the fabrication of contacts and the measurement of its resistance has been performed and reported in the literature several times. Measurement techniques for the measurement of a single contact can generally be classified as using either a) the transfer-length method, or b) the four-terminal probe method, both of which will be described in the following subsections. In addition to these techniques, SEM images can be used to inspect the physical quality of an individual contact. Contact chains can also be used to measure the series resistance of multiple contacts and therefore obtain an average contact resistance [4]. These techniques involving individual contact measurements tend to consume a great
deal of both on-chip and off-chip resources due to the use of large, dedicated pad structures; as a result, opportunities for variability characterization, which requires measurements of many contacts, are limited.

1) Transfer Length Method: In terms of characterizing contact resistivity, one of the first major breakthroughs was the transfer-length method, or TLM, which enabled the determination of contact resistivity by obtaining the resistances of many different sized contacts and using analytical equations to determine the resistivity [5]. The derivation of the analytical equation stems from a resistor-grid model of the metal-semiconductor contact interface as shown in Figure 1.

![Resistor-grid model of metal-semiconductor contact](image)

Here $R'$ is the resistivity of the doped silicon source/drain junction, and $G'$ is the resistivity of metal-semiconductor contact interface. The metal resistivity is negligible compared to the other two, so it is neglected in this analysis. Based on simple Kirchoff’s law current equations, the contact resistance, $R_c$, is

$$R_c = \frac{R_{sc} L_T}{W_c} \coth \frac{d}{L_T}$$

where $L_T = \sqrt{\rho_c R_{sc}}$ is the characteristic contact transfer length, $R_{sc}$ is the sheet resistance of the diffusion layer directly beneath the contact area, $W_c$ is the contact width, and $d$ is the contact length [6]. The transfer length method was extended for the analysis of silicided diffusion regions in [7]. More recently, technology scaling has demanded smaller dimensions for contacts, as well as design rules which allow for only one specific contact size. Nevertheless, recent efforts to accurately characterize the contact resistivity have been successful despite these trends [8]. For example, in [9], the TLM was combined with analysis of various geometries to determine the specific contact resistance of NiSi and PtSi silicides.

2) Four-Terminal Probe Method: Another common method used to determine contact resistances is the four-terminal Kelvin resistor method. This test structure uses four terminals which are all connected to the device under test — in this case, a contact [10]. With this structure, it is relatively simple to obtain the contact resistance, but more difficult to obtain the specific contact resistivity. This is because the current flow through the contact is nonuniformly distributed throughout its area, which presents problems when coupling this method with the TLM in order to obtain $\rho_c$. A test structure was developed in a 0.8μm technology to determine the distribution of contact resistances for an array of 4k contacts in [11]. The results indicated a Gaussian distribution of contact resistances for any given contact size. Some work has also focused on refining each of these methods by eliminating parasitic components which could lessen the accuracy of the resistivity measurement, or on developing a unified approach to accurately extract specific contact resistivity [12] [13].

B. Failure and Defect Analysis

A more comprehensive approach for individual contact characterization is failure and defect analysis, which is useful for functional yield estimation. Thus, a variety of test structures are available to characterize resistances, in order to quantify the failure or defect rate of contacts or vias. These structures seek to capture the functional yield of the contacts, e.g., by detecting open contacts with extremely high resistance, rather than trying to determine parametric yield by obtaining a distribution of individual contact resistances. The advent of these types of test structures has been due to the increasing complexity and density of integrated circuits and the possibility that a small number of contact or via failures could jeopardize proper operation. In [14], a passive multiplexing approach was developed in order to quickly and accurately characterize contact and via fail-rates. Using bit-lines and word-lines and testing a number of combinations of interconnect paths, highly resistive contacts were detected. The cause for the open contact and via failures was found to be partly due to a lack of tungsten within the plug which was to be filled. Another test structure, described in [15], implemented an efficient methodology to characterize open contact and via failures by using a pyramidal architecture scheme. SEM results indicated that the highly resistive contacts and vias were caused by three major process failures: voiding failures, etching failures, and resistive failures. These techniques for failure and defect analysis are useful in capturing functional yield, but the increasing parametric variability in advanced technologies requires other techniques for parametric variability characterization.

C. Analytical Modeling

For contact resistance modeling, the TLM remains useful as an accurate method for modeling contact resistance. However, due to the differences in device geometries as a result of scaling, such models have been adjusted to include sidewall interface resistance, dopant redistribution calculations, and various nuances in process steps. For example, in [16], the contact resistance is modeled as part of an effort to accurately model the entire series resistance of a device. An effort to include the sidewall contact resistance contribution is made in [17], since the contact width is shrinking. Analytical modeling of contact resistance is oftentimes folded into the analytical modeling of extrinsic resistance in a MOSFET. Such modeling efforts are beneficial in understanding the physical nature of the contact resistance and its interactions with other variables, but it is also important for these efforts to be extended to account...
for the increasing variability which is present in advanced technologies.

D. Arrayed Test Structures

Arrayed test structures are helpful in gathering variability data for contact resistances. In [18], a test structure was designed to assess the resistance of individual contacts located within transistors. Results showed that the distribution of resistances is Gaussian, but that the means can also change due to different device layout configurations. When the data gathering process is sufficiently fast, this rapid characterization of many contacts can be helpful in assessing variability. The next section will focus on the results obtained from a test chip which is also designed for contact plug resistance variability characterization purposes.

III. TEST STRUCTURE FOR CONTACT PLUG RESISTANCE VARIABILITY CHARACTERIZATION

A. Description of Test Circuit

A test chip has been implemented in a 90nm CMOS technology to determine the characteristics of contact plug resistance variability and the layout-based design parameters which can affect it. The resistance is obtained by a current-force, voltage-sense approach, similar to the four-terminal probe method used for individual contact characterization, which is multiplexed across over 35,000 devices under test. Design steps are taken to ensure that leakage current paths do not adversely impact the measurement results beyond the desired measurement resolution capability. Figure 2 shows a three-dimensional view of the device under test and the current flow through it. The current is forced into the silicide region through one contact and out of the region through the other contact (yellow), which is the contact to be characterized. The voltage is tapped across the two terminals of the contact, emanating in the two voltage outputs, $V_{OUTL}$ and $V_{OUTH}$. The current is guided to a sink device transistor where it then flows to ground. The resistance is directly proportional to $V_{OUTH} - V_{OUTL}$ with a proportionality constant of $1/I_F$, the inverse of the forced current. The multiplexing scheme, shown in Figure 3, features three DUT access transmission gates which are enabled by the outputs of row and column decoders. In addition to this scheme, each row contains its own high-$V_T$ transmission gate to adequately minimize leakage current paths. The analog-to-digital conversion of the voltage outputs is performed off-chip, and digital output enables fast characterization of contact plug resistances.

B. Design of Experiments

The design of experiments for this test chip includes five key layout design parameters: contact-to-gate distance ($d_{cg}$), contact-to-diffusion edge distance ($d_{cd}$), metallization layer to contact overlap for the y-dimension ($d_o$), the number of contacts in the source diffusion region ($N_s$), and the number of contacts in the drain diffusion region ($N_d$). In addition, DUTs with contacts located in both NMOS and PMOS transistors are used. The contact which is measured is always on the drain side of the device. A DUT type is one which consists of some particular combination of these five layout design parameters. The chip contains a total of 55 types of devices under test. The chip also contains 256 rows and 144 columns of DUTs, for a total of 36,864 resistance measurements.

C. Statistical Analysis Results

Measurement results are reported for a total of 23 die. The results will be described in four sections: layout-dependent trends, die-to-die systematic trends, wafer-level edge effect trends, and spatial correlation analysis.
1) Layout Dependence: The first statistical analysis is to identify which effects are significant, arising from the design of experiments in layout parameters. Because a large number of replicated DUT types are available (both within each die, and for 23 die), it is possible to obtain quite tight confidence intervals on the estimation of mean and variance of resistance for each DUT type, enabling us to identify any systematic effect of different layout parameters on the mean and variance of the contact plug resistance. Two notable effects are those of $d_{cg}$ and $d_{cd}$. Figure 4 shows the resistance mean and standard deviation as a function of the distance between the contact and the polysilicon gate with all other layout parameters held constant. Figure 5 shows the normalized resistance mean and normalized standard deviation as a function of the distance between the contact and the edge of the diffusion region. Both the mean and standard deviation are plotted with 95% confidence intervals. The other layout parameters are $d_{cd} = 0.08 \mu m$, $d_o = 0.01 \mu m$, and $N_s = N_d = 3$, and only contacts within NMOS devices are included. Resistance values are normalized to the global wafer mean.

Results show an increase in resistance with both increasing $d_{cg}$ and $d_{cd}$. However, there appears to be no clear significant change in the variance when plotted against these distances.

2) Die-to-Die Trends: The next statistical analysis seeks to identify any systematic die-to-die trends. When the systematic layout-dependent induced variability components (summarized in the previous section) are subtracted off the total resistance distribution die pattern, the remaining portion of the data exposes any systematic (repeatable) die-to-die trends. To do this, the type mean-subtracted resistance is computed for each DUT. The type mean-subtracted resistance is the measured resistance minus the average resistance of all DUTs of the same type as itself. Some insight is obtained when the resulting mean-subtracted resistance is plotted for each column, with all DUTs in that column averaged. This is done in Figure 6 for each of the 144 rows with 95% confidence intervals on the column averages. The resistances are plotted as a fraction shift from the wafer global mean. Clearly, two regions of resistance exist with a sharp change at around $x = 1210 \mu m$. The average over all contact plugs on the left side of the chip, where $x < 1210 \mu m$, is noticeably greater than the average over all devices on the right side of the chip, where $x > 1210 \mu m$. Furthermore, the change in average plug resistance is quite abrupt. While all of the previously seen trends with regards to layout design parameters can still be seen for DUTs in each of the two sides of the chip, there appears to be an offset. The average resistance measured for DUTs on the right side of the chip is 1.3% lower than those located on the left side of the chip.

These results appear to be consistent with variability re-
resulting from a step-and-scan exposure system used during lithography processes [19]. Because the variability only occurs in the x-direction and not in the y-direction, this leads us to believe that the optical scan direction is the vertical y direction, while the slits are organized in the horizontal x direction. The two distinctly different regions in terms of contact plug resistance suggest that a total of two slits were part of this particular die (part of a larger multiproject die) on the reticle. The resulting effect is a critical dimension change from one side of the die to the other side of the die. This critical dimension change may then manifest itself in terms of a change in the cross-sectional area of the contact plug, thus changing the total resistance. If this is indeed the case, the contact width would have changed by approximately 0.7% in order to explain the observed resistance change.

3) Wafer-Level Edge Effects: Wafer-level edge effects can also have an impact on the contact plug resistance. The examination of one particular die which is near the edge of the wafer reveals some interesting trends. While nearly all of the other die show a systematic pattern similar to that seen in Figure 7(a), the particular die located at the edge of the wafer shows a systematic pattern as depicted in Figure 7(b). This indicates that some wafer-level or wafer-edge variation may be affecting the contact plug resistance in this die.

4) Distance-Dependent Spatial Correlation Analysis: While the examination of systematic components of contact plug resistance variability is important, the analysis of random components is also critical for both modeling and for understanding the variation sources. When the systematic components are mean-subtracted from the resistance data, as was done in Section III-C2, what remains is “unexplained” or random variation in contact plug resistance. To analyze the nature of this variability, and in particular to understand if some remaining correlated spatial variation remains, contact-to-contact spatial separation distance correlation analyses can be performed. An important observation below is that systematic spatial trends (such as those discussed earlier) can appear to be spatially correlated variations, if they are not previously identified and removed. Thus, spatial correlation analysis can serve as a tool by which potential spatial trends can be “flagged” for investigation, removal, or mitigation.

First, to understand the effects of unremoved systematic components on spatial correlation analysis, the distance-dependent spatial correlation coefficient has been plotted for the nominal device type on all die with 95% confidence intervals on each coefficient in Figure 8(a). Because the systematic die-to-die component is not removed (mean-subtracted), we see some small positive correlation for small distances as well as some small negative correlation for large distances. In this case, what appears to be spatially correlated random variation is actually systematic variation which has not been removed prior to the correlation analysis.

In Figure 8(b), the same analysis is done, except the $(x, y)$ location mean is subtracted from each point before the correlation is computed. Here, the small positive correlation at small distances could be the result of either some subtle systematic trends which have not been accounted for, or truly spatial correlation. An illustration of the effect of a substantial spatial trend is seen in Figure 8(c), which shows the correlation coefficient as a function of separation distance for contacts located only on the die which is at the edge of the wafer. The 95% confidence intervals in this plot are substantially wider, because the data set includes resistance values from only one die as opposed to all the die. Here, we see both positive correlation at small separation distances and negative correlation at large separation distances, despite the fact that the location means have been subtracted off. This large spatial correlation is due to the unique systematic gradient in contact plug resistance on this die, shown earlier in Figure 7(b).

IV. NEED FOR VARIABILITY MODELS

Results from the previous section motivate the need for variability models which can capture systematic effects in contacts accurately, including small but important choices made in the local layout. As technology scales, parameters such as contact resistance are becoming more critical to the operation of the transistor. The issues of increasing contact plug resistance and higher variability have presented concerns that scaling past
the 65nm node while continuing with the same contact plug process steps may result in intolerably high resistances [20]. While efforts have been made to improve the materials and process steps which are used to form these contacts, parallel efforts are needed to model the variability present in these contacts. Advances in both numerical modeling and compact modeling are necessary to capture these variations.

Current state-of-the-art device models for transistors such as BSIM are lacking in their ability to adequately model contact resistance variability as part of the transistor. While some functionality exists in terms of choosing some geometric parameters such as the type of contact (wide or point contact) and type of connection to the source/drain regions (isolated or shared), a more accurate variation-aware model will be needed to capture the impact of all these layout configurations on variability. In addition, many layout parasitic extraction tools do not consider the impact of the source/drain contacts during their analysis.

In terms of analytical or numerical modeling of contacts, work has been done to model the total extrinsic resistance of a MOSFET [21][22]. In addition, analytical models have been derived for accurately determining the parasitic capacitances associated with the source/drain contacts [23]. The analytical models were verified by 3-D Monte Carlo simulation results. Work has also been done to perform sensitivity analysis of contacts with respect to different geometries using device simulations [24]. In addition, methods for fast variation-aware extraction of capacitances have been proposed which effectively take into account geometric perturbations [25]. Fast variation-aware extraction tools such as these will be necessary in the future due to increased variability and aggressive scaling. More work is necessary, however, to generate accurate variability-based models for contacts and to integrate them into the design framework.

**V. Conclusions**

Because of the growing impact of contact variability in advanced technologies, it is necessary to understand the nature of this variability. While several methods have been developed to study individual contact resistance, as well as to understand failures and defects, new methods are necessary to accurately analyze the parametric variability in these structures. In this context, a test structure has been designed, fabricated, and measured which enables the characterization of contact plug resistance variability. The application of statistical analysis techniques reveal both die-to-die and within-die variability, as well as wafer-level edge effects, affecting contact plug resistance. In addition, spatial correlation analysis was performed to uncover further possible trends in the data. For future technologies, it will become necessary to have adequate numerical and compact models for robust design.

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