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A Low Temperature Fully Lithographic Process For Metal–Oxide Field-Effect Transistors

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Abstract—We report a low temperature (~100 °C) lithographic method for fabricating hybrid metal oxide/organic field-effect transistors (FETs) that combine a zinc–indium–oxide (ZIO) semiconductor channel and organic, parylene, dielectric layer. The transistors show a field-effect mobility of (12 ± 0.8) cm²V⁻¹s⁻¹, on/off ratio of 10⁶ and turn-off voltage of V₉off = −1 V. This work demonstrates that organic and inorganic layers can be deposited and patterned using a low temperature budget, integrated lithographic process to make FETs suitable for large area electronic applications.

Index Terms—Thin-film transistors (TFTs), amorphous semiconductors.

I. INTRODUCTION

A MORPHOUS wide bandgap (~3 eV) metal–oxide thin films have been investigated by many researchers as semiconducting layers in field-effect transistors (FETs) [1]–[5]. Metal–oxide-based FETs have been demonstrated with higher charge carrier mobilities, higher current densities, and faster response performance than amorphous silicon (a-Si) FETs, which are the dominant technology used in display backplanes. Furthermore, the optically transparent semiconducting oxide films can be deposited in a near-room-temperature process, making the materials compatible with future generations of large-area electronics technologies that require use of flexible substrates. In this study we present a fully photolithographic, low temperature process for fabricating metal–oxide FETs, consisting of zinc indium oxide (ZIO) semiconductor and parylene dielectric layers, in a top gate configuration. This technique enables processing of complex multilayer structures at low temperatures, as needed for large area electronic applications on low thermal budget substrates such as heat-sensitive plastic foils.

Amorphous n-type ZIO films can be deposited at room temperature by sputter deposition, a process suitable for large scale processing of uniform thin films. In addition, by controlling oxygen partial pressure during deposition, the carrier concentration of deposited films can be varied from sufficiently low values to generate insulating films to higher than 10¹⁹ cm⁻³ [6], [7]. The high mobility of amorphous metal oxides compared to a-Si is attributed to the direct overlap of spherically symmetric metal s orbitals [3], [8]. FET performance is not solely determined by the semiconductor mobility, however, and the selection of an appropriate dielectric material strongly affects FET performance. Amorphous Si FETs in large area display applications, for example, utilize SiNₓ as a dielectric material. SiNₓ can be deposited by plasma-enhanced chemical-vapor deposition (PECVD) methods, which typically require temperatures around 300 °C and hence are not suitable for deposition on heat sensitive substrates [9]. In the fully lithographic process for ZnO FETs demonstrated by Hsieh et al., the SiNₓ layers used as dielectric were deposited by PECVD at 200 °C [10].

As an alternative to high temperature deposition processes, we demonstrate use of a room temperature-deposited polymer, parylene-C, as the dielectric layer. In the chemical-vapor deposition (CVD) process, parylene dimer is cleaved in a vacuum pyrolysis furnace (T ~ 700 °C) into monomer units which are flowed into a room-temperature deposition chamber to adsorb and polymerize on the substrate. Unlike spin-coated or solution-processed films, no annealing is required after deposition. The conformal, transparent films have a dielectric constant of ε ~ 3.9 and a breakdown voltage of 3 MV/cm [11]. Their pinhole-free structure enables their use as low leakedielectric thin films necessary for FET fabrication.

II. PROCESS FLOW

A schematic illustration of the lithographic process flow for fabricating ZIO/parylene FETs is shown in Fig. 1. Photolithography allows subtractive patterning by liftoff or by etching, but liftoff is considered less desirable for sputtered films because of their increased step coverage and hence liftoff was avoided here. The process was run on 100-nm borosilicate glass wafers, which were cleaned in a piranha bath (3:1 H₂SO₄:H₂O₂) before starting device fabrication. The maximum process temperatures (~100 °C) were dictated by photoresist baking steps. No intentional annealing of the electrode, semiconductor, or dielectric layers was performed.

A. Source/Drain Layer

After piranha cleaning, a 100-nm-thick layer of indium–tin–oxide (ITO) was sputter-deposited in Ar onto the substrates. During deposition, the chamber pressure was kept at 4 mTorr and the unheated substrate holder rotated for uniformity in thickness of the deposited films. The source/drain
electrodes were then dry-etched in a CH\textsubscript{3}/H\textsubscript{2}/Ar mixture (1.7:3:4 ratio) at 80 °C in a reactive ion etching system.

**B. Semiconductor Layer**

After patterning of the source/drain contacts, the substrates were returned to the sputtering chamber for semiconductor deposition. A 50-nm-thick layer of ZIO was RF sputtered from a mixed oxide target (2:1 ZnO:In\textsubscript{2}O\textsubscript{3}, AJA International) at room temperature in 15% oxygen. A deposition pressure and power of 5 mTorr and 50 W, respectively, were used.

Fig. 2 shows a typical X-ray diffraction (XRD) pattern collected in a Bragg-Brantano geometry with a CuK\textsubscript{α} radiation at 40 kV and 40 mA for a 50-nm-thick ZIO film, deposited on a glass substrate using RF magnetron sputtering. The absence of sharp diffraction peaks in Fig. 2 indicates that the material is fully amorphous.

Since ZIO is easily wet-etched compared to ITO, patterning of the semiconductor was performed in a very dilute hydrochloric acid solution (400:1 H\textsubscript{2}O:HCl). Patterning the semiconductor is desirable to isolate the devices from each other, thereby avoiding current leakage between transistors and other circuit elements.

**C. Dielectric/Via Layer**

It is known that parylene does not adhere readily on inorganic substrates [11]. Especially in a lithographic process, where multiple patterning steps follow parylene deposition, avoiding parylene delamination is crucial for repeatable fabrication of the integrated circuits. Thus, immediately prior to parylene deposition, the substrates were treated briefly in an oxygen plasma to functionalize the surface before being exposed to vinyltrimethoxysilane, an adhesion promoter, in vapor form for 2 h. Parylene-C was then deposited by CVD (di-XC dimer, Daisan Kasei Company) to form a 250-nm-thick dielectric layer. During the deposition process, the substrate itself remains at room temperature. Finally, similar to the process outlined by Kymissis et al., vias were opened through the parylene using an oxygen reactive ion etch [12]. Parylene’s relative insolubility allows for use of standard photolithography solvents.

**D. Gate Layer**

After via definition, a chromium/gold (Cr/Au) thin film was e-beam evaporated onto the substrates for gate electrodes and probe pads. The 10-nm-thick Cr layer serves as adhesion layer for the 100-nm-thick Au film. The two metal layers were then wet-etched in two steps, first a potassium-iodide-based etch (Transene TFA) to pattern the gold, then Cr-7 chromium etchant (Cyantek) to remove the exposed chromium.

Fig. 3 shows a completed array of single transistors of varying channel lengths. The inset shows a magnified view of a single FET ($W/L = 100 \mu m/100 \mu m$).

**III. DEVICE CHARACTERIZATION**

Electrical characterization of the fabricated devices was performed using an Agilent 4156C semiconductor parameter analyzer. Fig. 4(a) shows output–voltage ($I$–$V$) characteristics for a typical enhancement mode transistor with $W/L = 100 \mu m/100 \mu m$. The corresponding saturation region transfer characteristics (solid line), linear region transfer characteristic (dashed line) and gate currents (dotted lines) are shown in Fig. 4(c). From the saturation transfer characteristic the extracted subthreshold slope is 0.7 V/dec and the current
on/off ratio is $\sim 10^8$. The turn-off voltage, $V_{\text{off}}$, where the drain current falls below gate leakage current, is close to 0 V. The low leakage through parylene is shown by the low gate current which, normalized for area, is $< 9 \times 10^{-8}$ A/cm² at $V_{\text{GS}} = 20$ V. The channel capacitance, as measured in the quasi-static capacitance-voltage (C–V) curve shown in Fig. 4(b), was 19 nF/cm² and the overlap capacitance normalized for width, is $<5$ fF/µm.

Several methods for extracting effective carrier mobility in amorphous semiconductor FETs have been reported in literature. It is common to report mobility values calculated from saturation region transfer characteristics, borrowing the definition of saturation mobility from crystalline Si models. However, as noted by Hoffman [13] for oxide FETs and by Ryu et al. [14] for organic FETs, the assumptions of the ideal crystalline Si conduction models may not hold true for disordered semiconductors.

The mobility extraction method developed by Hoffman calculates an average mobility, $\mu_{\text{avg}}$, from the channel conduction assuming drift-dominated charge transport. Noting the difficulty in estimating the induced charge in the channel, $Q_{\text{ind}}$, from a frequency-dependent measured capacitance, this derivation calculates $Q_{\text{ind}}$ from simple electrostatics to be $Q_{\text{ind}} = C_{\text{ins}}(V_{\text{GS}} - V_{\text{on,H}})$, where $C_{\text{ins}}$ is the insulator capacitance and $V_{\text{GS}}$ the gate-to-source bias. The parameter $V_{\text{on,H}}$ is defined as the gate voltage at which drain current begins to increase exponentially from the off-state. (An ‘H’ subscript was added to $V_{\text{on}}$ to differentiate the parameter $V_{\text{on}}$, defined by Hoffman from that defined by Ryu et al. Note that when gate leakage current is sufficiently low, $V_{\text{on,H}}$ is the same as the previously defined $V_{\text{off}}$.) Combining expressions for channel conductance and induced channel charge yields the following equation for average mobility at low drain-to-source bias ($V_{\text{DS}} \rightarrow 0$):

$$
\mu_{\text{avg}} = \frac{G_{\text{ch}}(V_{\text{GS}})}{L C_{\text{ins}}(V_{\text{GS}} - V_{\text{on,H}})}
\quad (1)
$$

where $G_{\text{ch}}$ is the channel conductance as a function of $V_{\text{GS}}$.

As Hoffman notes, this expression appears almost the same as that for Si MOSFET mobility in the linear regime, $\mu_{\text{eff}}$, except that threshold voltage, $V_{\text{T,Lin}}$, is replaced here by $V_{\text{on,H}}$. Fig. 5 plots the linear region transfer characteristic for a 100 µm x 100 µm FET on both log and linear scales and compares $V_{\text{T,Lin}}$, found by the commonly-used linear extrapolation method, with $V_{\text{on,H}}$. As shown, $V_{\text{on,H}} = 0$ V is several volts lower than $V_{\text{T,Lin}} = 3.8$ V. The higher calculated value of $\mu_{\text{eff}} = 15 \text{ cm}^2/\text{V} \cdot \text{s}^{-1}$ compared to $\mu_{\text{avg}} = 12 \text{ cm}^2/\text{V} \cdot \text{s}^{-1}$ results from an understimation of induced channel charge, which must be accurately determined for mobility calculations.

The method proposed by Ryu et al. [14] also starts from simple electrostatics but calculates the total sheet charge density by integrating over the quasi-static C–V curve, $Q = \int_{-\infty}^{V_{\text{GS}}}(C_{\text{ch}})/(WL)dv$, where the channel capacitance, $C_{\text{ch}}$, is the capacitance due to charge induced in the semiconductor. In this derivation, the model parameter $V_{\text{on,R}}$ can be defined from the C–V characteristic such that the total integrated charge $Q = -(C_{\text{ch,accumulated}})/(WL)(V_{\text{GS}} - V_{\text{on,R}})$. 

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**Fig. 3.** Micrograph of a fabricated array of single devices with varying channel lengths. The inset gives a larger view of a single field effect transistor ($W/L = 100 \mu m/100 \mu m$).

**Fig. 4.** (a) Output I–V characteristics for a W/L = 100 µm/100 µm zinc-indium-oxide FET. (b) Quasi-static C–V characteristics of the same device. The overlap capacitance $C_{\text{overlap}}$ is 0.5 pF. (c) Transfer I–V characteristics for the same device shown in (a) and (b), double-swept from negative to positive and back. Both the linear region (dashed line) and saturation region (solid line) characteristics in (c) show a turn-off voltage, $V_{\text{off}}$, close to 0 V. Gate leakage currents (dotted lines) were $<1$ pA.

**Fig. 5.** Transfer I–V characteristics for a W/L = 100 µm/100 µm zinc-indium oxide FET at $V_{\text{DS}} = 1$ V. The same curve is plotted on both log and linear scales, and $V_{\text{on,eff}}$ and $V_{\text{T,Lin}}$, are pointed out for comparison. The 3.8 V difference between $V_{\text{on,H}}$, the gate voltage at which drain current beings to increase exponentially from the off-state, and $V_{\text{T,Lin}}$, as commonly found by linear extrapolation method, leads to a discrepancy in the calculated channel charge used in mobility calculations.
Fig. 6. The table summarizes mobility values calculated in the linear region ($V_{DS} = 100$ mV) with $V_{GS} = 20$ V for 50, 100, 150, and 200 μm channel length FETs. Two methods used to calculate mobility (following Hoffman [13] and Ryu et al. [14]) are compared. The channel width for all devices was 100 μm.

Table: Charge mobility (cm²/V·s)

<table>
<thead>
<tr>
<th>L (μm)</th>
<th>Hoffman (μavg)</th>
<th>Ryu, et al. (μ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>13.1</td>
<td>12.7</td>
</tr>
<tr>
<td>100</td>
<td>11.8</td>
<td>11.4</td>
</tr>
<tr>
<td>150</td>
<td>11.2</td>
<td>11.2</td>
</tr>
<tr>
<td>200</td>
<td>11.2</td>
<td>10.8</td>
</tr>
</tbody>
</table>

(An ‘R’ subscript was added to $V_{on}$ to differentiate the parameter ‘$V_{on}$’ defined by Ryu et al. from that defined by Hoffman.)

The calculated channel mobility, $\mu$, is given by

$$\mu = \frac{I_D}{W \int_{V_{GS}}^{V_{on}} \left( \frac{C_T}{C_W} \right) dV \left( \frac{L}{V_{DS}} \right)}.$$  

The calculated channel mobility is then an average mobility over the total gate-bias induced charge, which includes free and trapped charges.

A comparison of the mobility values obtained using each of these methods is shown in Fig. 6. The table lists values for devices with channel width of 100 μm and four different channel lengths (50, 100, 150, and 200 μm); the reported values were taken near $V_{GS} = 20$ V when $V_{DS} = 100$ V. For all channel length devices, both the Hoffman ($\mu_{avg}$) and Ryu et al. ($\mu$) methods give similar values. The slightly lower $\mu$ values suggest that not all the channel charge is accounted for in $\mu_{avg}$, but for $V_{GS} \gg V_{on}$ the difference does not appear significant. Overall, the calculated mobility values are very similar for transistors of different channel lengths. Both $\mu_{avg}$ and $\mu$ are ($12 \pm 0.8$) cm²/V·s across the four different channel length transistors shown in Fig. 6.

IV. CONCLUSION

In this study we demonstrate that parylene dielectric and ZIO semiconducting layers can be integrated in a fully lithographic process to fabricate high performance field effect transistors. The steps of the photolithographic process flow are described and device characteristics are reported. Field effect mobility values in the linear region are extracted by employing $I$-$V$ and $C$-$V$ measurements and are found to be ($12 \pm 0.8$) cm²/V·s across the channel on the Hoffman and Ryu et al. models. In summary, the low temperature ($\leq 100$ °C) processing of these devices along with their superior characteristics compared to a-Si based FETs hold promise for future large area electronic applications.

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REFERENCES


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Prof. Bulovic is a recipient of the U.S. Presidential Early Career Award for Scientist and Engineers, the National Science Foundation Career Award, and was named to Technology Review TR100 List.

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