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Seamless On-wafer Integration of GaN HEMTs and Si(100) MOSFETs

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The integration of III-V compound semiconductors and silicon (100) CMOS technologies has been a long pursued goal. A robust low-cost heterogeneous integration technology would make the outstanding analog and mixed-signal performance of compound semiconductor electronics available on an as-needed basis to realize key functions on VLSI chips that are difficult to implement in Si technology. In this paper, we demonstrate the first on-wafer integration of AlGaN/GaN high electron mobility transistors (HEMTs) with Si(100) MOSFETs.

The AlGaN/GaN transistor structures used in this work were grown on Si(111) substrates by metal-organic chemical vapor deposition (MOCVD) at Nitronex Corporation. In these samples, the AlGaN barrier had a total thickness of 175 Å and an Al composition of 26%. Our technology removes the Si(111) substrate (not useful by Si electronics due to its high density of surface states) and it uses two different wafer bonding steps to fabricate a Si(100)-GaN-Si(100) virtual substrate as shown in Figure 1. The top Si(100) layer has a 200 nm thickness and a donor doping concentration of $10^{15}$ cm$^{-3}$. Our wafer bonding technology has been described in [1] and it is based on the use of a hydrogen silsesquioxane (HSQ) interlayer. HSQ is a flowable oxide with excellent thermal stability, which withstands the high thermal budget required during the processing of both Si and GaN devices (i.e. >1000°C). Once the virtual substrate has been fabricated, device processing starts with the fabrication of Si p-MOSFETs following a standard SOI MOSFET processing. Device isolation was achieved by field oxide and a 10 nm gate oxide was formed by a plasma enhanced chemical vapor deposition (PECVD). Undoped polycrystalline Si was subsequently deposited and anisotropically etched in a Cl$_2$ plasma to form the gate contact. The source, drain and gate implantation was achieved at the same time with a species of BF$_2$, a dose of $4\times10^{15}$ cm$^{-2}$, and an implantation energy of 10 KeV. In order to fabricate GaN HEMTs, the AlGaN/GaN layer embedded in the virtual substrate was exposed by etching away the top Si(100) and HSQ layers using SF$_6$ plasma in those regions where GaN devices are needed. The etch selectivity between Si/SiO$_2$ and AlGaN is excellent and a smooth AlGaN surface was obtained after the etch. Once the AlGaN/GaN layer is exposed, the fabrication of GaN HEMTs is identical to a standard GaN HEMT processing. A Ti/Al/Ni/Au multilayer was first deposited for the ohmic contacts. Ohmic metal alloying of GaN HEMTs and dopant activation of Si p-MOSFETs were simultaneously accomplished by rapid thermal annealing at 870°C for 30s in N$_2$ atmosphere. The bonding between GaN and Si(100) was mechanically stable up to 1000°C for a few seconds, a sufficient thermal budget for Si and GaN processing. A Cl$_2$/BCl$_3$ plasma was used for the mesa isolation, and then a 2–3 μm-long gate was formed by photolithography and Ni/Au/Ni metallization. Figure 2 shows a scanning electron micrograph image of typical Si p-MOSFETs and GaN HEMTs after this step. The separation between these two devices is just 4 μm. It should be noted that nitride-based semiconductors are ideal candidates for this heterogeneous integration due to their excellent thermal stability which stands the high thermal budget of Si processing.

The drain current versus drain voltage characteristics as well as the transfer characteristics of a Si p-MOSFET and a GaN HEMT fabricated using the technology described in this paper are shown in Figure 3 and Figure 4, respectively. Both devices show excellent modulation of the drain current by the gate contact as well as low off-currents. The effect of the entire fabrication process to the transport properties of the AlGaN/GaN epilayer was evaluated by transfer length measurements (TLM) (Figure 5). The contact resistance ($R_c$) was almost constant (0.3–0.4 Ω-mm), however the sheet resistance ($R_{sh}$) is reduced by 24%, from 476 Ω/sq to 364 Ω/sq. This improvement in $R_{sh}$ is due to the layer transfer process and it was also reported in [1].

In conclusion, we have demonstrated the first seamless on-wafer integration of GaN-based devices and Si(100) electronics through a fully Si-compatible process. This integration allows transistor-level integration of compound semiconductors and Si-based devices to enable revolutionary advances in circuits and systems. Some of the applications envisioned for this integration include high power integrated wireless transmitters, power gating and power conversion circuits, and in-chip optical interconnections where the optoelectronic devices are made of nitride semiconductors and the digital circuit is based on Si devices.


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Figure 1. a) Main processing steps in the fabrication of Si(100)-GaN-Si(100) virtual substrates through the layer transfer technology described in [1]. The thin top Si(100) layer is obtained from the active Si layer of an SOI wafer. The doping of this layer sets the nMOS or pMOS character of the fabricated devices. b) A cross-section scanning electron microscope (SEM) image of the virtual substrate.

Figure 2. a) A cross-section schematic of fabricated Si p-MOSFETs and GaN HEMTs. b) A top SEM view of the fabricated transistors.

Figure 3. DC current-voltage characteristics (left) and transfer curve (right) of a long channel Si p-MOSFET (L_G=8 μm). The use of shorter gate lengths and higher doping levels in the thin-Si layer are expected to improve the performance of these MOSFETs even further and it is part of our on-going work.

Figure 4. DC current-voltage characteristics (left) and transfer curve (right) of a GaN HEMT (L_G=2 μm).

Figure 5. Contact resistance (R_c) and sheet resistance (R_sh) of unpassivated GaN HEMTs after their integration with Si devices. These results are compared to standard GaN HEMT structures grown on Si (111). R_c is almost constant, however R_sh reduces ~24% during the fabrication of virtual Si-GaN-Si wafers.