**Critical Voltage for Electrical Reliability of GaN High Electron Mobility Transistors on Si Substrate**

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**Detailed Terms**

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Critical Voltage for Electrical Reliability of GaN High Electron Mobility Transistors on Si Substrate

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Abstract
We have evaluated the electrical reliability of GaN HEMTs on Si by carrying out V_{DS} = 0 V step-stress experiments. We have found that these devices show a degradation pattern that is very similar to that of devices on SiC with a critical voltage at which a sudden degradation of the gate current takes place. In general, devices on Si have a relatively high critical voltage although its distribution on a wafer is fairly broad even on a short-range scale.

Introduction
GaN High Electron Mobility Transistors are promising devices for high power and high frequency applications. SiC is the most broadly used substrate for GaN HEMTs. Recently, Si has emerged as an attractive substrate because of lower cost, availability in large diameters and sophisticated technology base. However, reliability becomes a bigger concern with larger lattice and thermal mismatch between GaN and Si as compared to SiC. This has been reported to cause more defects in GaN-on-Si devices when compared with devices on SiC (2x10^9 vs. ~10^8 cm^{-2} range) [1-2] and results in prominent trapping even before applying electrical stress [3]. Nevertheless, excellent electrical reliability has been reported in GaN on Si HEMTs with a lifetime greater than 10^7 h at T_j=150 °C at 28 V [4-6].

In this work we study the electrical degradation of GaN-on-Si HEMTs using techniques that we have developed to study GaN on SiC devices in reverse bias regime [7-8]. In particular, we have step-stressed the devices under V_{DS} = 0 V condition, a harsh stress condition relative to the targeted operating conditions for these devices. We find a pattern of degradation under these step-stress tests that in several ways resembles that of GaN-on-SiC HEMTs, although there are some salient differences.

Experimental
We studied experimental Al_xGa_{1-x}N/GaN HEMTs on Si with a 17.5 nm thick x=0.26 AlGaN barrier fabricated by Nitronex [4-5]. These devices yield P_{out} = 3.9 W/mm and PAE = 62% at 2.14 GHz under V_{DS} = 28 V. The gate-source and gate-drain separation, and the gate length are 1, 3 and 0.5 μm respectively. Although the devices used in this study are engineering devices specially produced for reliability studies, they have capabilities representative of the technology.

In the stress experiments performed in this study, the drain is shorted to the source and the gate voltage is stepped down from -5 V to -80 V. The device is at ambient temperature. Since in this experiment, negligible current flows, the device does not suffer from self heating. Throughout the experiment we measure several figures of merit (I_{D\text{MAX}}, I_{GOFF}, R_D, R_S and V_T) by interrupting the stress every 30 seconds.

We have contrasted the results from these experiments on GaN-on-Si devices with HEMTs fabricated on SiC substrate that we have studied before under identical conditions.
conditions [7-8]. These devices on SiC have a relatively similar barrier design and therefore should constitute a reasonable reference.

Results

Fig. 1 compares the results of a typical stress experiment in GaN-on-Si HEMT and a GaN-on SiC HEMT as reference. This experiment stops at -40 V. In the GaN-on-Si HEMT from the very beginning of the stress test, $R_D$ and $R_S$ start increasing and $I_{DMAX}$ starts decreasing. $I_{GOFF}$ also decreases up to a certain voltage. In contrast, for the GaN HEMT on SiC, $R_S$, $R_D$ and $I_{DMAX}$ remain stable up to about 20 V of $|V_{GS}|$. In both devices, at a certain voltage, there is a relatively sharp rise of the gate leakage current. This is what we term the critical voltage, $V_{CRIT}$ [9].

Below the critical voltage, there is a marked difference in the behavior of both devices. There seems to be degradation in GaN-on-Si even before reaching the critical voltage, while the GaN-on-SiC devices remain stable. In order to understand this apparent degradation below $V_{CRIT}$, a five-phase experiment was performed on Si (Fig. 2). Phase 1 consisted of continuous characterization without stress. In Phase 2, $V_{DS} = 0$ V step stress from $V_{GS} = -1$ V to -20 V was applied (this is below $V_{CRIT}$). In this phase, we see degradation in $R_S$, $R_D$ and $I_{DMAX}$, consistent with the results in Fig. 1.

In Phase 3, the device was allowed to rest in the dark without stress and the FOMs were observed to recover sluggishly suggesting slow detrapping from deep traps. $I_{DMAX}$ recovered to 86% of its original value. In Phase 4, detrapping was enhanced with the device at rest but under UV light illumination (365 nm). After turning off UV in Phase 5, $I_{DMAX}$ reached 95% of initial value. $I_{GOFF}$ is also observed to recover in a very similar manner.

To further understand this experiment, we have performed current collapse measurements before and after it. These show that there was no significant increase in the number of traps. All together, this indicates that the apparent degradation in GaN-on-Si HEMTs in the stress regime below $V_{CRIT}$ that is observed in Fig. 1 is the consequence of electron trapping in pre-existing traps in the fresh device. UV is
effective in recovering the device to its virgin state through electron detrapping. The fact that $I_{GOFF}$ decreases with trapping is consistent with a gate leakage mechanism through partially filled traps in the AlGaN barrier [8]. When the traps fill up, current conduction is blocked and $I_{GOFF}$ decreases. The increase in $R_D$ and $R_S$ and the decrease in $I_{DMAX}$ stem from the electrostatic suppression of the 2DEG in the intrinsic region of the device by the trapped electrons. $V_T$ also shifts positive consistent with increased trapping. The fact that no such effects are observed on SiC below $V_{CRIT}$ is consistent with the existence of fewer traps on SiC in the fresh state compared to Si. Burn-in, as commonly performed in industry [5] might mitigate this problem. We have not investigated this possibility.

A remarkable result is that some GaN HEMTs on Si exhibit high values of $V_{CRIT}$, sometimes exceeding 70 V. Similar devices on SiC devices have $V_{CRIT}$ values in the 15-30 V range [7-8]. Another interesting difference is that on Si, the distribution of $V_{CRIT}$ is broad even for devices in the same reticle (Fig. 3). In our studies, the average $V_{CRIT}$ for $V_{DS} = 0$ V step-stress experiments for 59 samples is 37 V with $\sigma=13.1$ V. On SiC, we often observed much tighter $V_{CRIT}$ distributions over a wafer with $\sigma = 1-2$ V range.

**Discussion**

Our observations on Si are consistent with a degradation mechanism for devices on Si that seems similar to the one we have observed in SiC devices: defect formation induced by excessive mechanical stress introduced at high voltages through the inverse piezoelectric effect [7]. The unique aspect of Si is the large amount of trapping centers that virgin devices seem to have. Current collapse right after a -10 V gate pulse under $V_{DS} = 0$ V condition is almost 5x larger on Si as compared to SiC (Fig. 4). This large amount of traps might be related to the lesser amount of initial strain in the AlGaN barrier as evidenced from the relatively smaller values of $I_{DMAX}$ (~800 vs ~1100 mA/mm) and more positive $V_T$ (-1.3 vs -3.5 V) when compared with typical SiC devices [10-11]. This reduced initial strain translates into a higher value of $V_{CRIT}$ as higher voltages are needed to accumulate the critical elastic energy that triggers the onset of defect formation [12]. The broad range of $V_{CRIT}$ values for the devices on Si might
reflect an uneven distribution of initial strain on the wafer.

Conclusion
We have evaluated the reliability of GaN HEMTs on Si under harsh $V_{DS} = 0$ V step-stress conditions. We find that HEMTs on Si exhibit a pattern for degradation that is characterized by a critical voltage, just as devices on SiC. Apparent device degradation for GaN-on-Si HEMTs for stress voltages below the critical voltage is due to traps that already exist in the fresh device and is not real physical degradation. We have also found that $V_{CRIT}$ on GaN on Si HEMTs can be quite high but with a relatively broad distribution of values on a wafer.

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References


