Temperature Dependence of Digital Single-Event Transients in Bulk and Fully-Depleted SOI Technologies

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***Abstract*—Factors that affect single-event transient pulse widths, such as drift, diffusion, and parasitic bipolar transistor parameters, are also strong functions of operating temperature. In this paper, SET pulse-width measurements are performed over a wide temperature range in both bulk and fully-depleted SOI (silicon on insulator) technologies. The average pulse-width increases with temperature for the bulk process, but not for the FDSOI process.**

***Index Terms*—Heavy ions, ion radiation effects, silicon-on-insulator technology, single event upset (SEU), single event transients.**

I. Introduction

SPACE-BORNE electronic circuits are often required to operate in high radiation, extreme temperature environments. Single-event error rates for these circuits are a strong function of single-event transient (SET) pulse widths [1], [2], and parameters that control SET pulse widths (drift, diffusion, bipolar effects, etc.) are strong functions of operating temperature. Experimental measurements of SET pulse widths over a wide temperature range are of vital importance to the radiation effects community. However, to date, very little research has been performed in this area. Simulation results, carried out by Shuming *et al.* [3] over a large temperature range in 180-nm bulk and 180-nm partially depleted SOI (silicon-on-insulator) processes show that SET pulse widths are expected to increase with temperature in bulk technologies, but not for SOI technologies. The main reason for the increase in the pulse width for the bulk process was suggested to be an increase in parasitic bipolar effects with increasing temperatures. In this paper, an on-chip, autonomous SET pulse-width measurement circuit is used to measure the SET pulse-width distribution as a function of operating temperature for 130-nm bulk and 180-nm fully-depleted SOI CMOS technologies. Experimental and 3D TCAD simulation results show an increase in SET pulse widths with temperature for the bulk process, but not for the SOI process. This is the first time SET pulse-widths have been experimentally measured as a function of IC temperature in these technologies.

Manuscript received July 17, 2009; revised September 10, 2009 and October 02, 2009. Current version published December 09, 2009.

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Digital Object Identifier 10.1109/TNS.2009.2034150

II. 130-nm Bulk Process

The test circuit used to characterize SET pulses was fabricated in a 130-nm bulk CMOS technology from IBM. The test circuit measures the SET pulse-width in terms of inverter delays. The circuit is based on the principle that within an inverter chain, an SET pulse will affect a given number of inverters directly related to the pulse width of the SET [4]. For the bulk 130-nm device, two target circuits, each consisting of a linear chain of 100 minimum drive-strength inverters, are used to generate SETs. The W/L for the pMOS transistor is 720 nm/120 nm, and the W/L for the nMOS is 240 nm/120 nm. The total drain area for both the nMOS and pMOS transistors is approximately $0.76\mu m^2$. The drain areas of the inverters were enlarged to increase the size of the sensitive volume. In one target circuit, guard bands are placed around each transistor in the inverter chain, while the other target circuit has no guard bands around the inverters [5]. Details of the layout (along with an illustration that shows the enlarged drain areas) of the guard band and non-guard band circuit can also be found in [5]. Following the 100 inverter chain, 32 inverter stages are connected to latches to store the number of inverters affected by each SET. An SET pulse detection circuit is used to trigger the latches. With the individual inverter stage delay at room temperature of about 100 ps, this circuit allows measurement of SET pulses ranging from 100 ps to 2 ns with a 50 ps measurement resolution [5]–[7]. A more complete description of the test circuit can be found in the work by Narasimham *et al.* [4]–[7].

A ring oscillator consisting of pulse measurement circuit latch stages was fabricated to obtain the precise delay of an individual latch stage. Since SET measurements were going to be performed over a wide range of temperatures, it was imperative to measure the change in stage delay with temperature. Using the same test setup used for the heavy ion testing, the ring

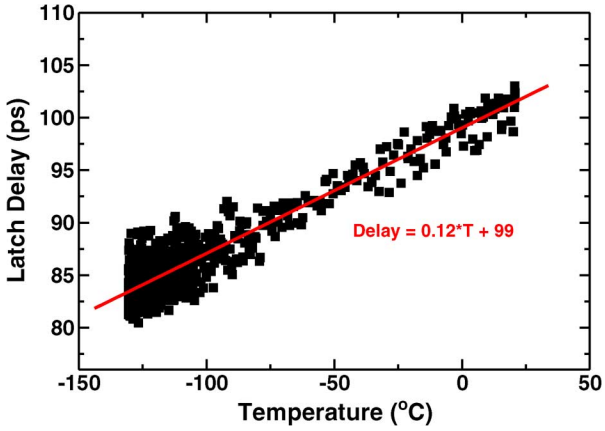

Fig. 1. 130-nm stage delay as a function of temperature.

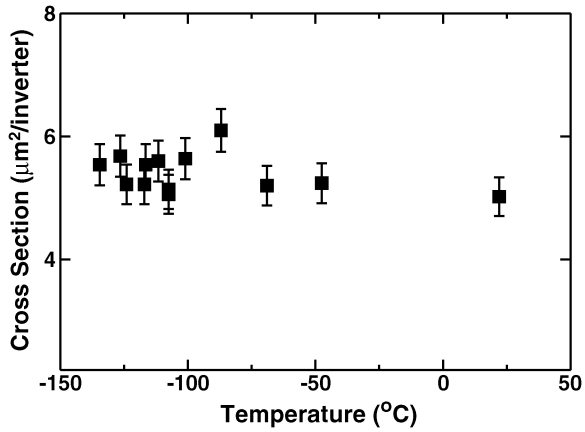

Fig. 2. SET cross section as a function of temperature.

oscillator frequency was measured as a function of operating temperature. As seen in Fig. 1, the stage delay is approximately linear with temperature in the range considered here. For these measurements, multiple data points were recorded at each temperature for a single ring oscillator. The variation in the data is due to jitter in the ring oscillator.

A. Reduced Temperature Experimental Results

To explore the effect of temperature on SET pulse widths in this 130-nm technology, radiation testing was performed using a customized cryogenic single event test system [8]. The bulk 130-nm test circuits were tested with heavy ions at the Texas A&M University Cyclotron facility over a temperature ranging from -135 °C up to room temperature (20 °C). The temperature of the IC was controlled in the test system via a cold finger (this cold finger is a piece of copper). One end of the cold finger contacted the package of the device under test, while the other end was connected to a liquid nitrogen vessel. The cold finger transferred heat between the device under test and the liquid nitrogen. Temperature measurements were taken using a sensor attached to the cold finger next to the device under test. The temperature reported in this section is the cold finger temperature as measured by the temperature sensor. The entire cryogenic test system runs under vacuum. The ion beam at the Texas A&M cyclotron passes through a thin aramica window before entering the cryogenic test system and striking the device under test. The LET values reported are the LET values at the silicon surface of the die.

Only the target circuit with guard bands was tested in the cryogenic test system. The circuit was tested with 2766 MeV xenon ions at normal incidence with an LET (Linear Energy Transfer) of 40.1 MeV-cm^2/mg.

The circuit was exposed to an ion fluence of 5×10^7 particles/cm^2. This led to approximately 200 SET events being measured at each temperature. The SET cross section per inverter is plotted as a function of temperature in Fig. 2. The SET cross section is equal to the number of SETs measured divided by the particle fluence (and then divided by the number of inverters). The SET cross section did not change significantly with temperature. (The error bars in the cross section are equal to plus/minus the square root of the number of events divided by the fluence.) Note that the cross section is significantly larger than the drain area. This implies that charge is being collected from an area larger than the drain. Since the cross section is not changing with temperature, the area in which charge was collected (around the sensitive drain) is also not changing with temperature.

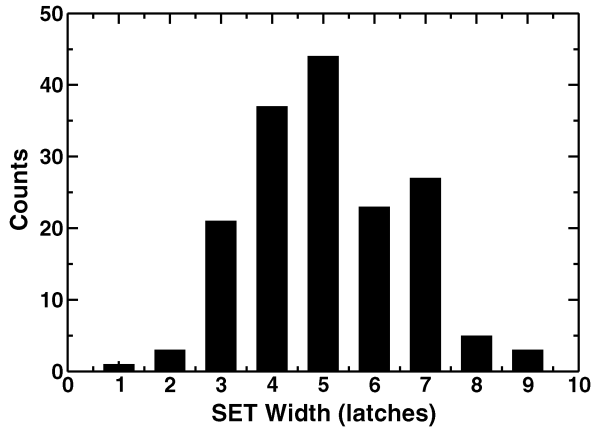

Fig. 3. Measured SET pulse width histogram at room temperature. The histograms (in units of latch delays) were similar for all temperatures.

A histogram of the measured SET pulse width distribution in units of latch delay at room temperature (20 °C) is plotted in Fig. 3. To obtain the SET pulse widths, one multiplies the number of latches by the delay (shown in Fig. 1). The histograms in units of latches were almost identical for each temperature. In Fig. 4, the average number of latch stages affected by SET pulses as a function of temperature is plotted. Note that the average number of latch stages affected shows little change as a function of temperature. The average SET pulse width in picoseconds (found by multiplying the latch delay for a given temperature by the average number of latches) is plotted in Fig. 5. The average SET width increases from 385 ps at -135 °C to over 500 ps at 20 °C. The error bars in Figs. 4–6 represent the standard error. The standard error is found by dividing the standard deviation by the square root of the number of events.

B. Elevated Temperature Experimental Results

The bulk 130-nm test circuits were also tested with heavy ions at the Lawrence Berkeley National Labs cyclotron facility

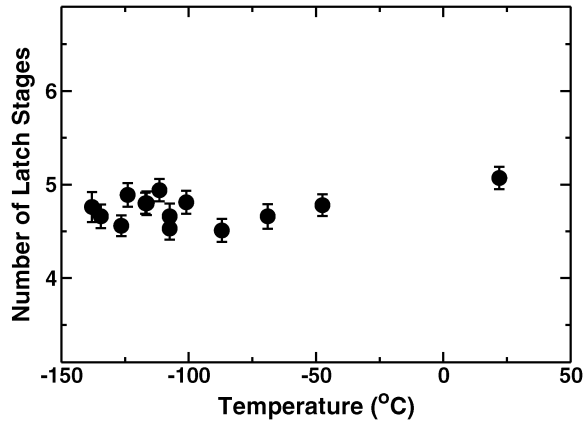

Fig. 4. Average SET pulse width in units of latch delays.

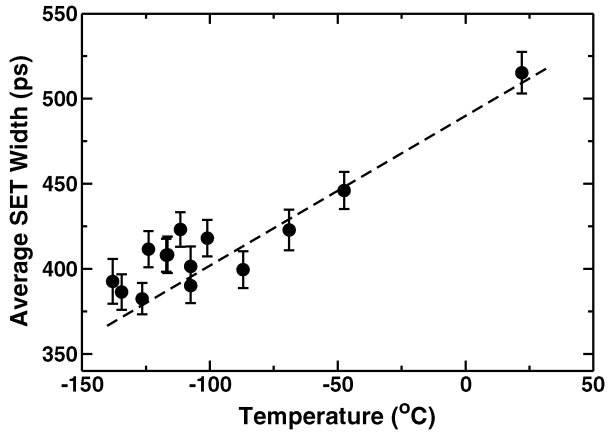

Fig. 5. Average SET pulse width for the cold temperature testing.

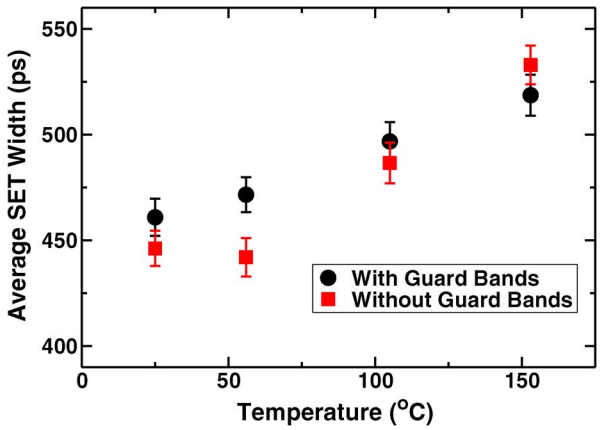

Fig. 6. Average SET pulse width for the elevated temperature testing of the 130-nm test circuits.

at elevated temperatures. Both target circuits (the ones with and without guard bands) were tested. Previous results have shown that the presence of guard bands can mitigate long SETs by reducing the charge collection area per node at extremely high LET values (~ 50 MeV-cm^2/mg) [5]. Both target circuits were tested here for no significant reason other than they were available. For the elevated temperature testing, the circuits were tested with 906 MeV Krypton ions at normal incidence

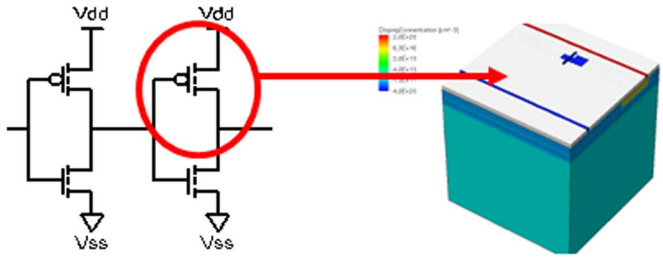

Fig. 7. A 130-nm TCAD model used to study the effect of temperature on SET pulse widths using a mixed mode simulation. For the 130-nm bulk device, either the off state pMOS or nMOS device was modeled in 3D TCAD.

with an LET of 30.9 MeV-cm^2/mg. (Note that this is a slightly lower LET than was used for the cold temperature test.) The temperature of the IC was controlled through a resistive heater attached to the package. Temperature measurements were taken using a resistive sensor attached to the package. Ion exposures were carried out at temperatures of approximately 25 °C, 50°C, 100 °C, and 150 °C. The temperature reported in the following section is the package temperature as measured by the temperature sensor.

A comparison of SET pulse-widths at the four different temperatures for exposures to Krypton ions with LET of 30.9 MeV-cm^2/mg for the 130-nm bulk device is summarized in Fig. 6. The pulse width distribution shifts towards a higher average value as the temperature increases. The same trend observed with the cold temperature data is also seen with elevated temperature data. SET pulse widths increase with temperature. Approximately 200 SET events were measured for each target circuit at each temperature. Each circuit was exposed to an ion fluence of 10^8 particles/cm^2. One item to note from Figs. 4 and 5 is that at room temperature the average SET width is about 50 ps shorter for the elevated temperature experiment. This is due to the fact that the elevated experiment was performed at Berkeley National Labs with an LET of 30.9 MeV-cm^2/mg, whereas the cold temperature test was performed at Texas A&M with an LET of 40.1 MeV-cm^2/mg.

C. Mixed Mode Simulations

Mixed-mode simulations for a string of eight inverters designed using a calibrated 130-nm bulk model were performed to identify the factors responsible for pulse-width variations. For these simulations, both the off-state pMOS and nMOS transistors of the second inverter were modeled using a 3D-TCAD simulator (see Fig. 7). The pMOS transistor has been previously found to be responsible for the longest SETs in this technology [4], [8]. The normally incident ion LET was fixed at 31 MeV-cm^2/mg, which corresponds to about 0.3 pC of deposited charge per micrometer. The ion strike location was the center of the drain region. This is the most sensitive strike location for the device. The temperature in both the TCAD and compact models was varied from -50 °C to 150 °C. For the TCAD simulations, temperature-dependent physical models were used. These physical models included: Fermi-Dirac statistics, SRH recombination, Auger recombination, and the Philips mobility model. The charge deposited by the incident heavy-ions was modeled using a Gaussian radial profile with a characteristic $1/e$ radius

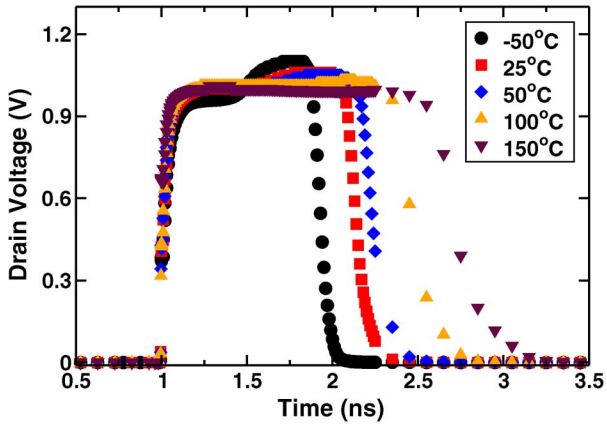

Fig. 8. Results of the 130-nm mixed mode simulation of the pMOS device showing SET pulses on the struck node for five temperatures.

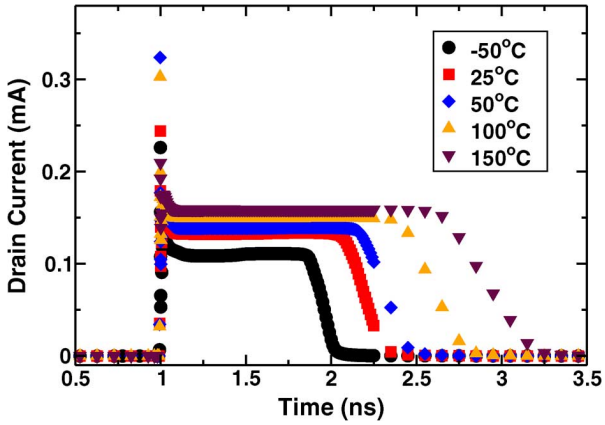

Fig. 10. Results of the 130-nm mixed mode simulation showing the drain current on the struck node of the pMOS device for five temperatures.

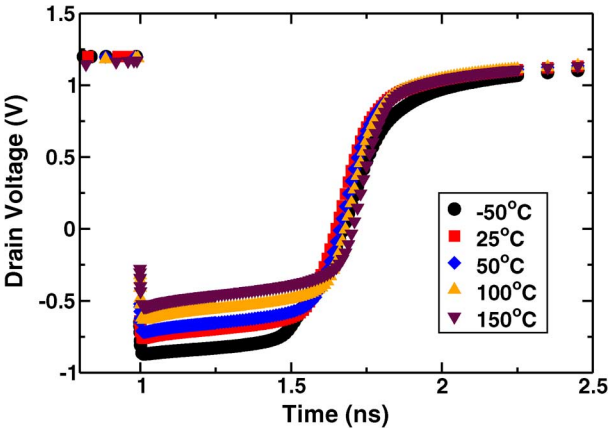

Fig. 9. Results of the 130-nm mixed mode simulation of the nMOS device showing SET pulses on the struck node.

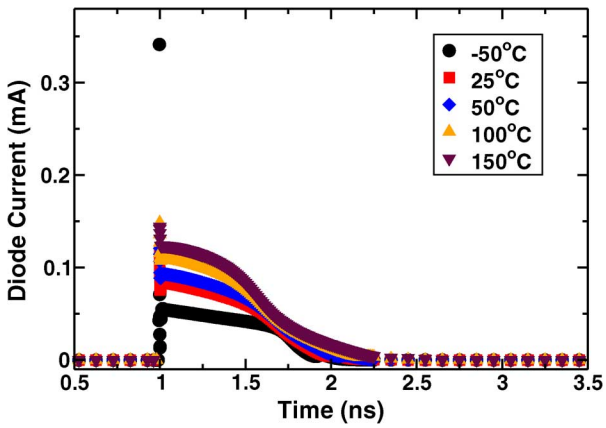

Fig. 11. Results of the 130-nm mixed mode simulation showing the current on the struck node of the p-diode for five temperatures.

of 50 nm, and a Gaussian temporal profile with a characteristic decay time of 2 ps.

Fig. 8 shows a plot of the width of the pulse from a pMOS strike measured at the output of the struck inverter for five different temperatures. The trend for this device is longer pulse widths with higher temperatures. Over the experimentally tested temperature range (25 °C to 150 °C), an increase in pulse width is observed for strikes on the pMOS device. The widths measured for the pMOS strikes are larger than the average SET widths measured with the test circuit. This is primarily due to the fact that the simulations were performed with a worst-case ion strike (i.e. the strike location was the center of the drain) whereas in the broad-beam experiment the ions are actually not likely to strike the worst-case location. SET widths for an nMOS strike are shown in Fig. 9. SETs originating from the nMOS devices show little change with temperature. The combined effect of nMOS and pMOS strikes would lead to an overall increase in average SET pulse widths with temperature. This correlates well with the increase in SET pulse widths seen in the experimental results.

Larger SET pulse widths are observed for the pMOS device than for the nMOS device. The larger SET widths in the pMOS device are due to parasitic bipolar amplification [9], [10]. Parasitic bipolar amplification is more pronounced for a pMOS device in n-well with a p-substrate for a bulk, twin-well CMOS process like the one studied in this work [10].

To explore the effect of bipolar amplification on the pulse width, mixed-mode simulations were performed with the gate and source of the pMOS transistor removed. The remaining circuit is a reverse-biased diode. For this diode, all other charge collection mechanisms except the parasitic-bipolar mechanism will be present. Plots of the simulated drain current at the struck node of the pMOS device and the diode are shown in Figs. 10 and 11. The increase in SET pulse width for the diode with temperature is noticeably smaller than that of the pMOS device. The simulations support the hypothesis that an enhancement in parasitic bipolar amplification with temperature is the primary cause for the increase in SET widths observed with the pMOS device.

Recent work has shown that an increase in resistance from the n-well contact to the pMOS device causes an enhancement in parasitic bipolar amplification [9], [10]. An increase in temperature will increase the resistance (due to a decrease in mobility) in the well from the n-well contact to the pMOS device. This increase in n-well resistance would create a further enhancemant in the parasitic bipolar gain. This also suggests that the increase in SET pulse widths with temperature could be mitigated by increasing the well contact area and/or decreasing the contact placement distance. The drain/source current paths do not de-

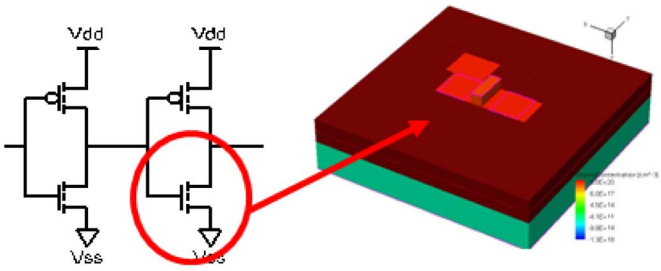

Fig. 12. A 180-nm FDSOI TCAD model used to study the effect of temperature on SET pulse widths using a mixed mode simulation. For the 180-nm FDSOI device, both the off state nMOS and pMOS device were modeled in 3D TCAD.

TABLE I
AVERAGE AND MAXIMUM 180-nm FDSOI SET PULSE WIDTH VALUES FOR Xe (EFFECTIVE LET = 52.3 MeV-cm^2/mg) AT TEMPERATURES OF 25 °C, 50 °C, AND 100 °C

Temperature	Average SET	Max. SET
25° C	670 ps	980 ps
50° C	620 ps	1050 ps
100° C	620 ps	1050 ps

pend on this resistance. The resistance discussed here is from the well contact to the body region of the pMOS device.

III. 180-nm FDSOI

The 180-nm FDSOI test circuit works in a similar fashion to the bulk device with the main differences being that the target circuit consists of a 200-inverter chain and the individual stage delay is only 70 ps [11]. This fully-depleted SOI technology has a silicon thickness of 40 nm, a BOX (buried oxide) thickness of 400 nm, and the transistors in both the target and measurement circuit do not have body ties. The change in individual stage delay over the temperature range of the testing was negligible.

A. Elevated Temperature Experimental Results

The FDSOI 180-nm test circuits were tested with heavy ions at the Texas A&M University Cyclotron facility with 1934 MeV xenon ions at normal incidence with an LET of 52.3 MeV-cm^2/mg. A similar comparison of SET pulse widths over temperature for the 180-nm FDSOI devices was performed as that described for the 130-nm bulk devices. However, for the SOI device, the pulse-width distribution shows very little change as the temperature increases. The average measured SET pulse widths are 670 ps, 620 ps, and 620 ps at 25 °C, 50 °C, and 100 °C, respectively. (Note: These averages include pulse broadening effects. The generated SET width is much smaller than the averages shown in the table. Pulse broadening effects in this device are discussed later in this section.) As with the 130-nm devices, the total number of SET's measured for a given ion fluence does not change with temperature. The operating temperature of the die does not affect the cross section in this technology.

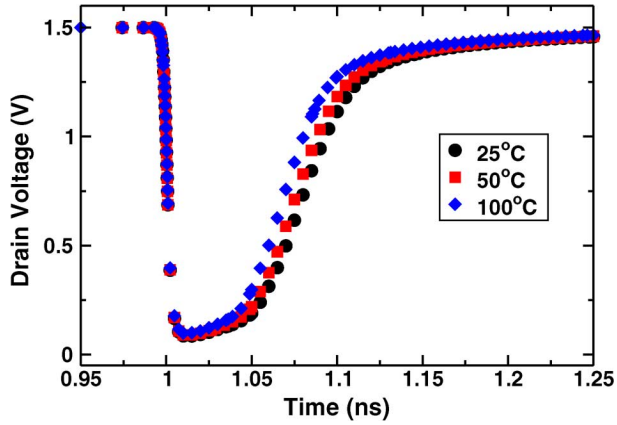

Fig. 13. Results of the 180-nm FDSOI mixed mode simulation for the nMOS device showing SET pulses on the struck node for 25 °C, 50 °C, and 100 °C.

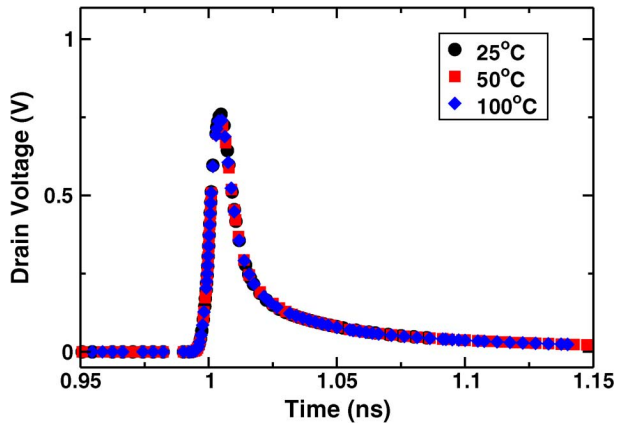

Fig. 14. Results of the 180-nm FDSOI mixed mode simulation for the pMOS device showing SET pulses on the struck node.

B. Mixed Mode Simulations

Mixed-mode simulations for a string of inverters designed using a calibrated 180-nm FDSOI model were performed to further explore the effect of temperature on SET pulse width for this SOI technology. For these simulations, both the off-state pMOS and nMOS transistors of the second inverter were modeled using the same 3D-TCAD simulator used for the bulk TCAD simulations. The ion strike location was the center of the gate (or body region) as this is the most sensitive region for these devices. The normally incident ion LET was fixed at 51 MeV-cm^2/mg (to match the LET used in the heavy ion testing), which corresponds to about 0.5 pC of deposited charge per micrometer.

The SET pulse width at the struck node for the three temperatures in the 180-nm FDSOI TCAD model is shown in Figs. 13 and 14 for the nMOS and pMOS devices, respectively. No significant trend is observed with increasing temperature in this technology. Note that the simulated pulse-widths for the FDSOI technology are less than 100 ps, while the measured SET pulse-widths average more than 600 ps. This can be attributed to "pulse stretching" or "pulse broadening", a well-known issue for floating body SOI devices [12]. Pulse broadening has been experimentally confirmed through laser

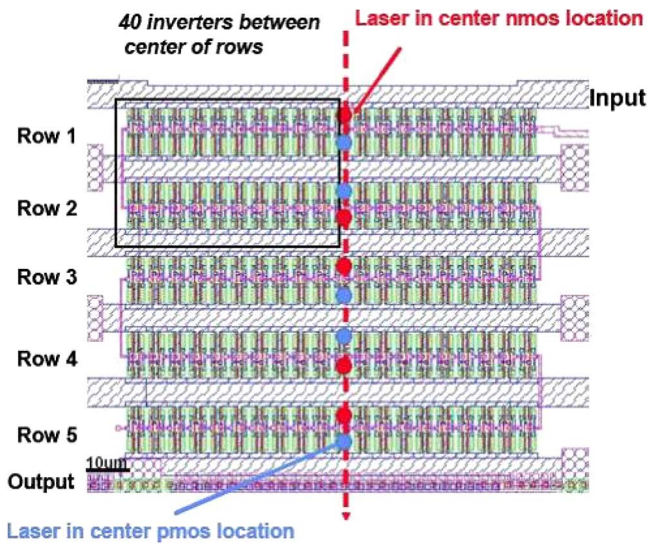

Fig. 15. For the laser testing performed here, the laser strike location was the nMOS device.

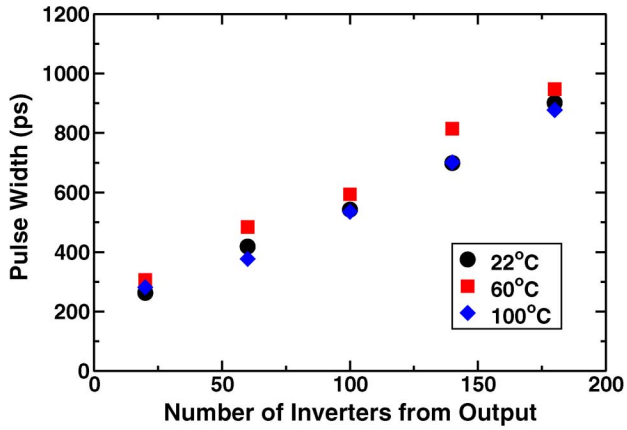

Fig. 16. Laser-induced SET pulse width in a FDSOI process as a function of temperature.

testing in this circuit by Gouker *et al.* [11]. Neither the experimental nor simulation results show a significant change in SET pulse width with temperature.

C. Pulse Broadening at Elevated Temperatures

Since pulse "stretching" or "broadening" is a well-known issue for non-body tied SOI devices, an experiment was performed using a focused laser to explore the effect of temperature on pulse broadening in this process. The test device was heated in a similar way as that used during the heavy ion testing. Using the focused laser pulse [11], nMOS transistors in the inverter chain were struck with the laser in different locations in the target circuit. An illustration of the target circuit is displayed in Fig. 15. Fig. 16 shows the pulse width as a function of laser strike location for three different temperatures. If one extrapolates to an intercept of zero, the SET pulse width at the first inverter would be about 200 ps. This is larger than the simulated SET widths of about 100 ps. Two possible explanations for this discrepancy include: (1) the laser energy used correlated to an LET value much higher than the one used for heavy ion testing, and (2) the simulations were set up to look primarily for trends in SET widths with temperature not necessarily to determine the exact pulse widths (that was the goal of the test structures). The pulse width plotted is the average pulse width of approximately 10000 laser-induced SET events. Two important items to note from this data set are (1) the generated SET pulse width did not change significantly as a function of temperature (this confirms what was observed with the heavy ion testing and the simulations), and (2) the broadening also did not change with temperature. Massengill *et al.* [13] showed that pulse broadening in SOI is due to a body-bias-induced threshold voltage hysteresis. These results show that this hysteresis shows no change with temperature in this FDSOI process.

IV. Discussion

Drift, diffusion, and bipolar-amplification are three temperature-dependent factors affecting radiation-induced charge collection for semiconductor devices. The drift component of charge-collection depends on mobility, which decreases with increasing temperature. However, the drift component of an SET current pulse is typically fairly short (on the order of tens of picoseconds). Thus for a SET lasting several hundred picoseconds, the drift component of charge collection does not significantly impact SET pulse-widths as temperature increases. The effect of temperature on SET pulse width through the diffusion current also tends to be negligible. Previous researchers have found the net effect of temperature on diffusion current resulting from a heavy ion strike to be small [14]. As a result, the increase in bipolar amplification with temperature is the main contributor to the increase in SET pulse widths seen in the 130-nm bulk circuit. Since bipolar amplification is less important for FDSOI devices than for either partially depleted or bulk devices [15], there is no increase in SET pulse width with temperature for the FDSOI test chip.

In addition to the various charge collection mechanisms mentioned, another important factor affecting SET pulse widths is the drive current of the transistor that restores the struck node to its initial state. For an nMOS strike, the restoring transistor in an inverter would be the pMOS device (and vice versa for a pMOS strike). The drive strength of the restoring transistor depends on the channel mobility of the device (which decreases with increasing temperature). If the channel mobility decreases with increasing temperature, the drive strength would also decrease and cause an increase in SET widths for the same amount of generated charge. For our simulations, strikes on the nMOS device (as shown in Fig. 9) show almost no change in temperature. This suggests that if there is a change in drive strength of the pMOS device it's not significantly impacting the SET width. Likewise, in Figs. 10 and 11, the parasitic bipolar is clearly shown to have a major impact on SET widths. While the nMOS drive strength may decrease slightly with increasing temperature, its impact is much smaller than the enhancement of bipolar amplification at the elevated temperatures. Simulations performed by Shuming *et al.* [3] in 180-nm bulk and SOI processes support the same conclusions reached in this work.

V. Conclusion

Soft error rates are a strong function of SET pulse widths. Measurements and TCAD simulations of digital SET pulse widths show that an increase in temperature leads to an increase in SET pulse widths for a 130-nm bulk circuit. Since mitigation approaches, and resulting error rates, are determined by the SET pulse-width distributions, an increase in SET pulse width may negate the mitigation efforts and increase error rates. This will lead to a significantly greater reliability issue for advanced technology ICs operating in high temperature environments. Since bipolar amplification is less significant in the charge collection of the 180-nm FDSOI circuit studied in this work, SET pulse widths for our FDSOI circuit showed little change with temperature. The lack of increase in SET pulse widths with temperature is additional advantage of using a FDSOI technology in a high temperature environment where soft errors will be a concern.

Acknowledgment

The authors would like to thank the Defense Threat Reduction Agency and NASA Johnson Space Center for their support of this effort. The authors would also like to thank NAVSEA Crane for their support through their Ph.D. program.

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