A 10Gb/s compact low-power serial I/O with DFE-IIR equalization in 65nm CMOS

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ISSCC 2009 / SESSION 10 / MULTI-Gb/s SERIAL LINKS AND BUILDING BLOCKS / 10.2

10.2  A 10Gb/s Compact Low-Power Serial I/O with DFE-IIR Equalization in 65nm CMOS

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The design of compact low-power I/O transceivers continues to be a challenge for both chip-to-chip and backplane applications. The introduction of dense fine-pitch silicon packaging technologies, that in principle are capable of supporting tens of thousands of high-data-rate I/O for local chip-to-chip interconnect, will make I/O area and power requirements even more stringent. Figure 10.2.1 depicts two chips mounted on a silicon (Si) carrier [1], an example of such a dense packaging technology, and connected by fine-pitch interconnects. Characteristics of an example 20mm Si carrier channel are shown in Fig. 10.2.1, showing significant (~6dB) DC attenuation as well as 17dB of loss at 5GHz. In the time domain, the response to an isolated ‘1’ applied at 10Gb/s shows many postcursors. A DFE would require many taps to be effective, however, the power and area penalty would be prohibitive in this context. This paper describes an alternative low-power compact I/O transceiver with RX equalization that achieves the required multi-bit postcursor cancellation without the high tap-count DFE. While this work targets data transmission over Si carrier links at rates up to 10Gb/s, it is also relevant to backplane channels.

The RX architecture of Fig. 10.2.2 features a modified DFE with IIR feedback (DFE-IIR), developed as an alternative to using a multi-tap DFE. From the channel characteristics of Fig. 10.2.1, it is observed that the impulse response is well modeled by a decaying exponential at all times more than 2UI after the main cursor. The DFE-IIR treats postcursor ISI from the most recent bit (H1) in the same manner as conventional DFES [2], but departs from this approach for all subsequent postcursors. Specifically, the two half-rate outputs of the DFE are multiplexed and fed back to the summer through a full-rate adjustable CT-IIR filter whose transfer function G(s) is adapted to match the exponentially decaying tail of the channel impulse response [3, 4]. As a result, a single additional feedback tap in the DFE can be employed to compensate several postcursors while consuming less power and area than a conventional multi-tap DFE.

Figure 10.2.3 depicts key circuit schematics of the DFE-IIR RX. As in the DFE summers in [5], the input is sampled and applied to linear transconductors. The summer output current is directly injected into a resettable current-comparator PMOS load acting as a slicer. By using a high (~1kΩ) resistor acting as a protection device is shown to equalize a 17mm channel with a 35% eye opening at 10Gb/s. ThisRX produces a 45% horizontal eye opening at a BER<10-10 with error-free operation in the center of the eye, while drawing 6.8mA from a 1V supply. Figure 10.2.5 summarizes 10Gb/s equalization results over various channels, including a 16inch Tyco backplane with ~27dB of loss at 5GHz. This demonstrates the potential of the DFE-IIR RX for low-power backplane equalization in addition to Si carrier applications. For comparison, a conventional 2-tap DFE is also implemented using the same basic components and power consumption level as the DFE-IIR. As seen in Fig. 10.2.5, the addition of the IIR filter improves performance over all tested channels, highlighting the effectiveness of this equalization scheme.

To test RX performance over the targeted Si carrier channels, test sites are designed in which low-power integrated TX-RX pairs are linked over channels of various lengths. These channels, implemented in the top metal layers of the CMOS backend, are designed so that their frequency responses emulate those of actual Si carrier channels of comparable lengths. Compact CMOS transmitters with low output impedances are designed to launch serial data over the channels. As discussed above, the integrated test site receivers use 1ksymbol period. Figure 10.2.7 shows a die micrograph of the integrated test site which contains 12 TX-RX pairs in various combinations communicating over channels with lengths ranging from 2mm to 40mm. TX and DFE-IIR RX macro layouts are shown as insets and occupy areas of 75x75μm2 and 150x115μm2, respectively. Some of the 12 pairs contain RX blocks without DFE-IIR equalization, enabling comparisons with traditional DFES at 5 and 10Gb/s.

References:
Figure 10.2.1: Conceptual silicon carrier link and characteristics of a 20mm channel.

Figure 10.2.2: Compact I/O DFE-IIR RX architecture.

Figure 10.2.3: DFE-IIR RX circuit schematics.

Figure 10.2.4: $S_{21}$ plots of 30, 40 and 50inch traces and BER bathtub curves equalized by the DFE-IIR RX for 10Gb/s PRBS7 pattern.

Figure 10.2.5: Measured results for stand-alone DFE-IIR RX and 2-tap DFE RX at 10Gb/s.

Figure 10.2.6: $S_{21}$ plots of emulated silicon carrier links in CMOS backend and measured results of TX-RX pairs over these channels.

**Tables**

<table>
<thead>
<tr>
<th>Channels</th>
<th>Horizontal eye opening (BER&lt;10^{-9})</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DFE-IIR</strong></td>
<td><strong>2-tap DFE</strong></td>
</tr>
<tr>
<td>30inch trace</td>
<td>PRBS7</td>
</tr>
<tr>
<td></td>
<td>PRBS31</td>
</tr>
<tr>
<td>40inch trace</td>
<td>PRBS7</td>
</tr>
<tr>
<td></td>
<td>PRBS31</td>
</tr>
<tr>
<td>50inch trace</td>
<td>PRBS7</td>
</tr>
<tr>
<td>16inch Tyco</td>
<td>PRBS7</td>
</tr>
</tbody>
</table>

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Figure 10.2.7: Die micrograph of TX-RX test site with emulated silicon carrier channels.