A 10Gb/s compact low-power serial I/O with DFE-IIR equalization in 65nm CMOS

10.2 A 10Gb/s Compact Low-Power Serial I/O with DFE-IIR Equalization in 65nm CMOS

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The design of compact low-power I/O transceivers continues to be a challenge for both chip-to-chip and backplane applications. The introduction of dense fine-pitch silicon packaging technologies, that in principle are capable of supporting tens of thousands of high-data-rate I/O for local chip-to-chip interconnect, will make I/O area and power requirements even more stringent. Figure 10.2.1 depicts two chips mounted on a silicon (Si) carrier [1], an example of such a dense packaging technology, and connected by fine-pitch interconnects. Characteristics of an example 20mm Si carrier channel are shown in Fig. 10.2.1, showing significant (~6dB) DC attenuation as well as 17dB of loss at 5GHz. In the time domain, the response to an isolated '1' applied at 10Gb/s shows many postcursors. A DFE would require many taps to be effective, however, the power and area penalty would be prohibitive in this context. This paper describes an alternative low-power compact I/O transceiver with RX equalization that achieves the required multi-bit postcursor cancellation without a high tap-count DFE. While this work targets data transmission over Si carrier links at rates up to 10Gb/s, it is also relevant to backplane channels.

The RX architecture of Fig. 10.2.2 features a modified DFE with IIR feedback (DFE-IIR), developed as an alternative to using a multi-tap DFE. From the channel characteristics of Fig. 10.2.1, it is observed that the impulse response is well modeled by a decaying exponential at all times more than 2UI after the main cursor. The DFE-IIR treats postcursor ISI from the most recent bit (H1) in the same manner as conventional DFEs [2], but departs from this approach for all subsequent postcursors. Specifically, the two half-rate outputs of the DFE are multiplexed and fed back to the summer through a full-rate adjustable CT-IIR filter whose transfer function G(s) is adapted to match the exponentially decaying tail of the channel impulse response [3, 4]. As a result, a single additional feedback tap in the DFE can be employed to compensate several postcursors while consuming less power and area than a conventional multi-tap DFE.

Figure 10.2.3 depicts key circuit schematics of the DFE-IIR RX. As in the DFE summers in [5], the input is sampled and applied to linear transconductors. The summer output current is directly injected into a resettable current-comparator PMOS load acting as a slicer. By using a high (~1kΩ) RX termination impedance, R_{TERM}, in conjunction with a low TX output impedance, the voltage drop across the resistive channel can be mitigated while also reducing power dissipation. While reflections will result from the impedance mismatch created by this approach, the high channel losses will lessen their impact on signal integrity. The output of the merged summer/slicer stage is further regenerated by a two-stage latch. The first stage is designed for high-speed signal regeneration, while the second stage sets an output common-mode level appropriate for CML DFE feedback circuits. The CT-IIR filter with integrated MUX adopts a fully differential structure. Its time constant can be adjusted from 40ps to 1ns (i.e., 0.4UI to 10UI at 10Gb/s) by tuning on-chip resistors R_D and capacitor C_D with 1b and 5b resolution, respectively. Adjusting a common-mode current (I_{CM}) ensures a constant common-mode output level from the IIR filter as R_D is varied. The IIR filter output is fed to a linear transconductor within the summer that is matched to the input transconductor.

To evaluate the DFE-IIR RX performance, stand-alone test sites are implemented in a 65nm bulk CMOS technology. To improve testability, 50Ω RX input termination is used instead of the high-impedance termination discussed earlier. This DFE-IIR has an input sensitivity of $64mV_{pp\text{-}diff}$ at 10Gb/s (BER<10^{-9}) and operates error-free up to 13Gb/s with ISI-free input data. Equalization capabilities are tested by transmitting data over 30, 40 and 50inch traces on a high-quality PCB board, with frequency rolloff characteristics similar to those expected in Si carrier links. S_{21} data for these channels are shown in Fig. 10.2.4. Including ~2dB of loss from SMA cables, the channels losses are 15.5, 19.6d and 23.2dB at 5GHz, respectively. RX bathtub curves when equalizing 10Gb/s PRBS7 data are also shown in Fig. 10.2.4. For the 50inch trace, the RX produces a 45% horizontal eye opening at a BER=10^{-9} with error-free operation in the center of the eye, while drawing 6.8mA from a 1V supply. Figure 10.2.5 summarizes 10Gb/s equalization results over various channels, including a 16inch Tyco backplane with ~27dB of loss at 5GHz. This demonstrates the potential of the DFE-IIR RX for low-power backplane equalization in addition to Si carrier applications. For comparison, a conventional 2-tap DFE is also implemented using the same base components and power consumption level as the DFE-IIR. As seen in Fig. 10.2.5, the addition of the IIR filter improves performance over all tested channels, highlighting the effectiveness of this equalization scheme.

To test RX performance over the targeted Si carrier channels, test sites are designed in which low-power integrated TX-RX pairs are linked over channels of various lengths. These channels, implemented in the top metal layers of the CMOS backend, are designed so that their frequency responses emulate those of actual Si carrier channels of comparable lengths. Compact CMOS transmitters with low output impedances are designed to launch serial data over the channels. As discussed above, the integrated test site receivers use 1kΩ termination. Figure 10.2.7 shows a die micrograph of the integrated test site which contains 12 TX-RX pairs in various combinations communicating over channels with lengths ranging from 2mm to 40mm. TX and DFE-IIR RX macro layouts are shown as insets and occupy areas of 75×75μm² and 150×115μm², respectively. Some of the 12 pairs contain RX blocks without DFE-IIR equalization, enabling comparisons with traditional DFEs at 5 and 10Gb/s.

S_{21} data for 25 and 40mm CMOS backend channels (both extrapolated from measurements of a 2.5mm line) are compared with their measured Si carrier counterparts in Fig. 10.2.6, showing similar frequency rolloff behavior albeit with slightly more loss for the Si carrier channels. Equalization results are also reported in Fig. 10.2.6. Over a 40mm link with 19dB rolloff at 4.45GHz, the 1V TX-RX pair operates at 8.9Gb/s with a 15% eye opening while consuming 17mW (5.4mW from RX and 11.6mW from TX). When equalizing 9.5Gb/s data transmitted over a 25mm link, the DFE-IIR shows superior performance as compared to a 2-tap DFE. Additionally, a DFE-IIR RX with a 550fF input ESD protection device is shown to equalize a 17mm channel with a 35% eye opening at 10Gb/s. These results demonstrate the feasibility of the DFE-IIR for use in low-power compact Si carrier link receivers.

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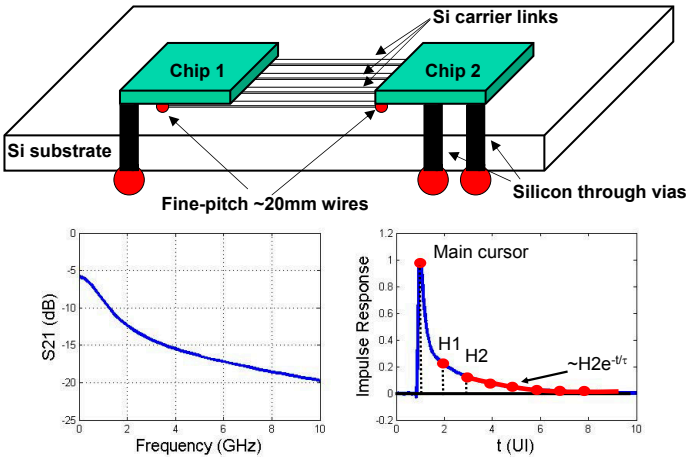

Figure 10.2.1: Conceptual silicon carrier link and characteristics of a 20mm channel.

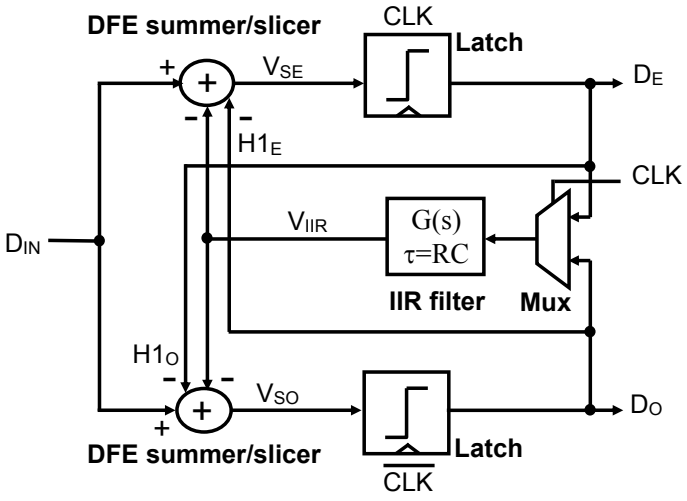

Figure 10.2.2: Compact I/O DFE-IIR RX architecture.

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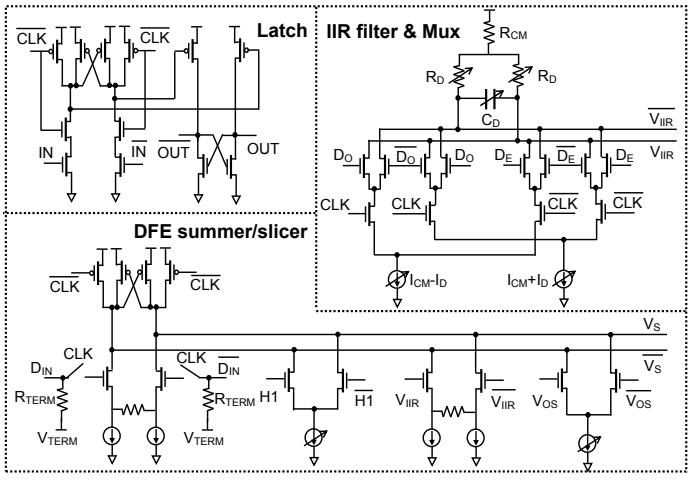


Figure 10.2.3: DFE-IIR RX circuit schematics.

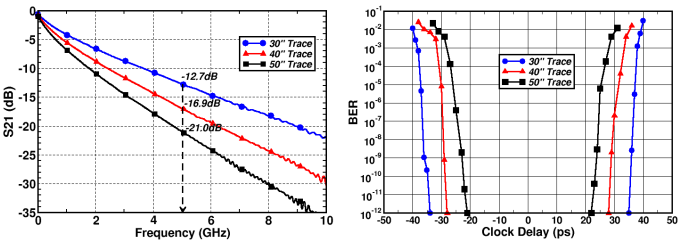
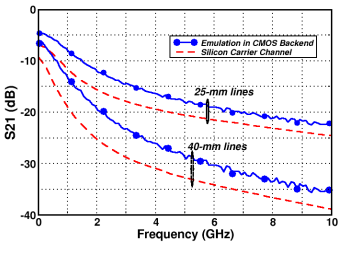


Figure 10.2.4: S_{21} plots of 30, 40 and 50inch traces and BER bathtub curves equalized by the DFE-IIR RX for 10Gb/s PRBS7 pattern.

Channels		Horizontal eye opening (BER<10^{-9})	
		DFE-IIR	2-tap DFE
30inch trace	PRBS7	71%	47%
	PRBS31	57%	24%
40inch trace	PRBS7	57%	28%
	PRBS31	41%	Closed eye
50inch trace	PRBS7	45%	Closed eye
16inch Tyco	PRBS7	28%	Closed eye

Figure 10.2.5: Measured results for stand-alone DFE-IIR RX and 2-tap DFE RX at 10Gb/s.



Channels		Horizontal eye opening (BER<10^{-9}) at PRBS7	
		DFE-IIR	2-tap DFE
17mm + ESD	10Gb/s	35%	n/a
25mm	9.5Gb/s	14%	Closed eye
40mm	8.9Gb/s	15%	n/a

Figure 10.2.6: S_{21} plots of emulated silicon carrier links in CMOS backend and measured results of TX-RX pairs over these channels.

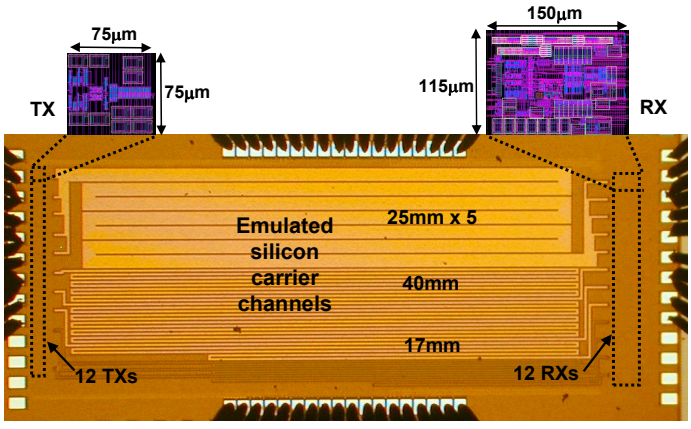


Figure 10.2.7: Die micrograph of TX-RX test site with emulated silicon carrier channels.

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