Dual Threshold Voltage Integrated Organic Technology for Ultralow-power Circuits

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Dual Threshold Voltage Integrated Organic Technology for Ultralow-power Circuits

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Abstract

For the first time, we demonstrate control of organic thin-film transistor’s (OTFT) threshold voltage ($V_T$) by modifying the gate work function. We present a near-room-temperature, fully lithographic process to fabricate integrated pentacene dual $V_T$ OTFTs suitable for large-area and flexible mixed signal circuits. Platinum and aluminum are used as the gate metals for the high $V_T$ (more depletion-like) and low $V_T$ (more enhancement-like) p-channel devices, respectively. The availability of a high $V_T$ device enables area-efficient zero-$V_{GS}$ current source loads. We demonstrate positive noise margin inverters which use pico Watts of power and a 3 V supply. Compared to a single $V_T$ implementation, the dual $V_T$ inverter occupies an area that is 30x smaller, and is 17x faster. These results show that p-channel only organic technologies can produce functional and low-power circuits without integrating a complementary device.

Introduction

Organic thin-film transistors can enable large-area and flexible electronics because their low processing temperatures ensure their compatibility with polymer substrates. Although individual p-channel OTFTs have been demonstrated with impressive mobilities ($\mu_{\text{hole}} \geq 1 \text{ cm}^2/\text{Vs}$), positive noise margins in OTFT digital circuits have been difficult to achieve due to the absence of a complementary device, the value of the $V_T$, and the lack of resistors (1,2). We have addressed this problem by creating a dual $V_T$ process, with the addition of only one mask to pattern a second gate metal. By using low and high work function metal gates, we are able to fabricate nominally identical devices whose $V_T$’s are shifted by an amount of $\Delta V_T$. To the best of our knowledge, this is the first demonstration of OTFT $V_T$ control by changing gate materials. The availability of two threshold voltages reduces the inverter area by 30x and increases inverter speed 17x compared to a single $V_T$ implementation. We present positive noise margin inverters which use pico Watts of power and a near rail-to-rail ring oscillator, both powered by a 3 V supply. The 3 V $V_{DD}$ is an order of magnitude lower than what has been reported for other photolithographic integrated organic circuits, which typically use at least 25-30 Volts (2,3). The dual $V_T$ circuits also use 10,000x lower switching current, and 10x-20x less static power than state-of-the-art complementary organic circuits at 3 V (4).

Experimental: Process Technology

We have developed a near room-temperature, completely photolithographic dual threshold voltage process to fabricate large-area, flexible organic integrated circuits. Dual threshold voltages are obtained by using two different gate metals: aluminum for the low (more enhancement-like) $V_T$ device and platinum for the high (more depletion-like) $V_T$ OTFT. The addition of a second gate metal adds only one mask compared to the conventional process.

We can write the threshold voltage equation for this system as follows,

$$ V_T = \left( \Phi_{\text{gate}} - \Phi_{\text{semiconductor}} \right) - \frac{Q_I}{C_{\text{ox}}} \tag{1} $$

where $\Phi_{\text{gate}}$ and $\Phi_{\text{semiconductor}}$ are the potentials of the gate and semiconductor, $Q_I$ the fixed charge per unit area at the gate dielectric/semiconductor interface, and $C_{\text{ox}}$ the gate capacitance per unit area.

Although this equation is technically for the flatband voltage, since these devices operate in accumulation, OTFT literature commonly refers to this voltage as the threshold voltage. Therefore, we will refer to this quantity as $V_T$ for consistency.

Since the gate dielectric and semiconductor deposition steps for both devices are done at the same time, we expect nominally the same $\Phi_{\text{semiconductor}}$ and $Q_I/C_{\text{ox}}$ for the aluminum and platinum gate OTFTs. Therefore, the $V_T$ of both devices should be shifted by the difference in gate work function. For the case of aluminum and platinum gates, theoretically we should expect a difference in threshold voltage, which we call $\Delta V_T$, of $\approx 1.3$ V.

The low temperature ($\leq 95^\circ\text{C}$) process is pictured in Figure 1. All processing steps are done in a class 100 clean room. The process flow produces p-channel devices with two different threshold voltages, and two metal interconnect layers. The gate metals are patterned by lift-off. Both $V_T$ devices employ an organic polymer (parylene-C) dielectric and pentacene as the channel material (5).

The current-voltage characteristics of fabricated devices are pictured in Figure 2. We observe that the current-voltage characteristics of aluminum and platinum gate devices are nominally identical, shifted by a threshold voltage difference, $\Delta V_T$. Statistics of the threshold voltages of Al and Pt devices over three wafers are shown in Figure 3. A consistent $\Delta V_T$ between the Al and Pt devices of $\approx 0.6$ V was measured over multiple wafers and lots. We do not observe any difference
in mobility, $C_{ox}$, or subthreshold slope between Al-gate and Pt-gate devices. The mobility and other device parameters are consistent with what we observe in our standard Au-gate, single $V_T$ process (6).

It was found that lift-off patterning the gates was necessary to obtain reproducible $V_T$’s and $\Delta V_T$’s. Two reasons are suggested for the difference between the measured and theoretical $\Delta V_T$. First, it is known that the presence of water on a metal surface can alter the surface potential (7,8). Contamination of the metal surfaces by processing, or residual water layers on the metal gates may lead to the effective work function difference of 0.6 V.

### Dual $V_T$ Digital Circuits

In the p-channel only OTFT technology, we can choose between using a diode-connected or zero-$V_{GS}$ load. Since the diode-loaded inverter suffers from asymmetric voltage transfer curves and low gain, we focus our analysis on the zero-$V_{GS}$ topology (9). Given the gate voltage dependent mobility in OTFTs, the zero-$V_{GS}$ load must be significantly wider than the driver to achieve positive noise margins (10,11). Not only does this make the area of the inverter large, it also increases the $C_{GD}$ of the load transistor, decreasing inverter speed. A dual threshold voltage technology solves this problem by enabling area-efficient, high output resistance zero-$V_{GS}$ current sources. The availability of a high $V_T$ (i.e. more depletion-like) device reduces the load’s size by two orders of magnitude.

Using an inverter topology with a high $V_T$ device as the load and with a low $V_T$ driver, one obtains substantial area and power savings, as well as shorter propagation delays while maintaining high noise margins. The inverter was sized to maximize noise margins by locating the trip voltage at $V_{DD}/2$, and also to minimize inverter area. The inverter schematic and measured inverter transfer characteristics are shown in Figure 4. We demonstrate positive noise margin ($NM_{H}=0.3$ V, $NM_{L}=1.3$ V, $V_{DD}=3$ V) inverters using this process. The inverter transfer curve is asymmetric, since the $V_T$ of the zero-$V_{GS}$ load was $\approx 200$ mV more negative than was used in the hand calculations.

The measured dual $V_T$ inverter uses pico Watts of power, and occupies an area that is 30 times smaller than an Al-only topology. An 11-stage ring oscillator with an output buffer was fabricated and tested. Powered by a 3 V supply, the oscillator swings near rail-to-rail (0.05 V to 2.85 V) with a propagation delay of 27 ms, as seen in Figure 5. This is one of the few near rail-to-rail integrated OTFT ring oscillators reported in literature. Near rail-to-rail operation is necessary to accurately extract the inverter propagation delay.

These results compare favorably with state-of-the-art organic digital circuits. The dual $V_T$ inverters here use 40x less area, 10,000x less dynamic power, and 10x-20x less static power than the 3 V shadow-masked complementary inverters reported by Klauk, et al. (4). The dual $V_T$ inverter has a power delay product of $5.6 \times 10^{-13}$ J, compared to an estimated power-delay product of $3 \times 10^{-11}$ J of Klauk’s 3 V inverters.

### Conclusions

In summary, we have demonstrated the first dual threshold voltage integrated OTFT technology suitable for mixed signal organic circuits. This fully photolithographic technology enables area-efficient zero-$V_{GS}$ current source loads. We have fabricated and tested digital logic using this process, and have measured positive noise margin inverters and near rail-to-rail ring oscillators using a 3 V power supply. This is the lowest $V_{DD}$ reported for photolithographically processed organic integrated circuits. Not only does lowering $V_{DD}$ reduce power consumption, it also improves circuit lifetime by decreasing the gate-field dependent bias-stress effects (12). Lastly, a 3 V $V_{DD}$ could enable interfacing with silicon ICs without the requirement of level-shifting.

### Acknowledgements

This work was funded in part by the FCRP Focus Center for Circuit & System Solutions (C2S2), under contract 2003-CT-888. Ivan Nausieda acknowledges financial support from the Martin Family Fellowship for Sustainability. This research has taken place at the Microsystems Technology Laboratories of MIT.

### References

Figure 1: Process flow for the integrated dual $V_T$ OTFT technology. All patterning steps are done with photolithography.

Figure 2: Linear and semi-log I-V’s of Al and Pt gate devices, W/L=200 µm/15 µm, $V_{DS}=-1$ V. $V_T$’s are extracted using a straight-line fit to the subthreshold region and marking where the I-V pulls away from the fit. Here, $V_{T,Al}=-0.5$ V, $V_{T,Pt}=0.1$V. The Pt device conducts 100x more current at $V_{GS}=0$ than the Al device.
Figure 3: Statistics of $V_T$ and $\Delta V_T$ for wafers fabricated using dual $V_T$ OTFT process. $V_T$’s extracted by method in Figure 2. 4-5 dies are measured per wafer.

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Figure 4: (a) Dual $V_T$ inverter schematic. (b) Measured inverter characteristics, $V_{\text{trip}}=1.8$ V, $I_{\text{trip}}=8$ pA, $I_{\text{off}}$ ($V_{\text{IN}}=V_{\text{DD}}$)=480 fA, $A_v=-7$ V/V, $V_{\text{DD}}=3$ V.

Figure 5: (a) Dual $V_T$ 11-stage ring oscillator and output buffer. (b) The measured output waveform at a frequency of 1.7 Hz, corresponding to an inverter propagation delay of 27 ms. $V_{\text{DD}}=3$ V.