# High-Performance Integrated Dual-Gate AlGaN/GaN Enhancement-Mode Transistor

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<td>As Published</td>
<td><a href="http://dx.doi.org/10.1109/led.2010.2055825">http://dx.doi.org/10.1109/led.2010.2055825</a></td>
</tr>
<tr>
<td>Publisher</td>
<td>Institute of Electrical and Electronics Engineers</td>
</tr>
<tr>
<td>Version</td>
<td>Final published version</td>
</tr>
<tr>
<td>Accessed</td>
<td>Wed Mar 16 09:57:45 EDT 2016</td>
</tr>
<tr>
<td>Citable Link</td>
<td><a href="http://hdl.handle.net/1721.1/70906">http://hdl.handle.net/1721.1/70906</a></td>
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High-Performance Integrated Dual-Gate AlGaN/GaN Enhancement-Mode Transistor

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Abstract—In this letter, we present a new AlGaN/GaN enhancement-mode (E-mode) transistor based on a dual-gate structure. The dual gate allows the transistor to combine an E-mode behavior with low on-resistance and very high breakdown voltage. The device utilizes an integrated gate structure with a short gate controlling the threshold voltage and a long gate supporting the high-voltage drop from the drain. Using this new dual-gate technology, AlGaN/GaN E-mode transistors grown on a Si substrate have demonstrated a high threshold voltage of 2.9 V with a maximum drain current of 434 mA/mm and a specific on-resistance of 4.3 mΩ·cm² at a breakdown voltage of 643 V.

Index Terms—AlGaN/GaN, dual-gate, enhancement-mode (E-mode), high-electron-mobility transistor (HEMT), power electronics.

I. INTRODUCTION

AlGaN/GaN high-electron-mobility transistors (HEMTs) have attracted a great interest for power electronics applications. A standard AlGaN/GaN HEMT is a depletion-mode (D-mode) device due to the large 2-D electron gas induced by the polarization charge at the AlGaN/GaN interface [1]. However, enhancement-mode (E-mode) AlGaN/GaN HEMTs are highly desirable for power electronics as they can greatly simplify circuit designs and improve system reliability.

Several approaches have been reported in the past for fabricating normally-off GaN transistors, including gate recess [2], fluorine/hydrogen plasma treatment [3]–[5], p-type gate injection [6], engineering the surface potential with dielectrics [7], [8], dipole engineering [9], [10], and GaN MOSFETs [11]–[14]. However, it is difficult to use these methods to fabricate devices that simultaneously have large threshold voltage, low on-resistance, and high breakdown voltage. In this letter, we report the use of a new integrated dual-gate technology on a standard AlGaN/GaN D-mode HEMT structure that allows the fabrication of state-of-the-art AlGaN/GaN E-mode power transistors with high threshold voltage (> 2.8 V), high drain current (> 400 mA/mm), and high breakdown voltage (643 V).

The concept of the dual-gate technology is based on the circuit topology shown in Fig. 1(a). High-performance E-mode operation can be achieved by connecting a high-voltage D-mode AlGaN/GaN HEMT with a low-voltage short-gate E-mode device, which can be a Si MOSFET or an E-mode GaN-based transistor. This circuit topology can be integrated into a single device on an AlGaN/GaN structure—the integrated dual-gate transistor—as shown in the device schematic in Fig. 1(b), where the E-mode gate is implemented by gate recess. Although two separated gate fingers can be used, the integrated dual-gate structure gives the smallest form factor when the two gates are biased at the same voltage.

When the device is in the pinchoff, the channel underneath the D-mode gate will be depleted, and the short E-mode gate will be shielded from the large drain voltage. Only a voltage that is equal to the threshold voltage of the D-mode gate ($|V_{th}|$) is dropped across the E-mode short gate, as shown by the simulation of the potential distribution in the integrated dual-gate normally-off transistor with $V_{DS} = 0$ V and $V_{DS} = 100$ V.

![Fig. 1](image-url)
be carefully designed so that the following will be achieved: 1) the gate length of the E-mode gate [shown in the SEM image in Fig. 1(b)] should be as short as possible to reduce its impact on the device total on-resistance; 2) the D-mode gate needs to be long enough (∼1 μm in our devices) to support the high drain voltage; and 3) the pinchoff voltage of the D-mode gate should not exceed the drain punchthrough voltage of the E-mode gate, which requires the D-mode gate to be as close to the channel as possible.

II. Device Fabrication

The devices used in this letter were fabricated on an AlGaN/GaN heterostructure grown on a 4-in Si (111) substrate by Nitronex Corporation. The structure has an ∼1.8-μm undoped GaN/AlGaN buffer and a 17-nm Al_{0.26}Ga_{0.74}N barrier. Ti/Al/Ni/Au alloyed source and drain ohmic contacts were formed by rapid thermal annealing (RTA). Mesa isolation was achieved by BCl_{3}/Cl_{2} plasma etching, then, the short E-mode gate (L_{g} = 95 ± 10 nm) was patterned with electron beam lithography, and the AlGaN barrier was fully recessed to achieve the high drain punchthrough voltage of the E-mode gate. The first knee voltage is at 5 V of the E-mode dual-gate device is ≈1.8μm gate dielectric was then deposited by atomic layer deposition, followed by 90-s RTA at 700 °C. Finally, a 2-μm-long Ni/Al/Ni gate electrode was deposited, overlapping with the first gate-recess region. The 2-μm gate was shifted ∼1 μm toward the drain side forming the D-mode gate in the integrated dual-gate structure, as shown in the SEM image in Fig. 1(b). The gate was annealed at 500 °C for 3 min. Standard D-mode transistors were also fabricated at the same time as a reference on the same sample without the gate recess. The breakdown voltage was measured using a Tektronix curve tracer connected to Agilent 34401A multimeters. The breakdown voltage is defined as the voltage when the leakage current reaches 1 mA/mm.

III. Experimental Results

The dc characteristics of a normally-off integrated dual-gate device with L_{gdr} = 5 μm are shown in Fig. 2. The maximum forward gate bias voltage (V_{gs}) of the fabricated devices is 7 V, beyond which the gate dielectric breaks. The maximum drain current at V_{gs} = 7 V of the E-mode dual-gate device is 434 mA/mm [Fig. 2(a)]. The transfer characteristics of the E- and D-mode devices are shown in Fig. 2(b). The E-mode device has a threshold voltage of −2.9 V, while the D-mode device has a threshold voltage of −3.5 V, which is also the pinchoff voltage of the D-mode gate in the integrated dual-gate device. Measurements from five E-mode devices on the sample give an average threshold voltage of 2.9 V with a standard deviation σ of 0.10 V, which is comparable to the one in D-mode devices (σ = 0.13 V). The integrated dual-gate E-mode and standard D-mode transistors reach maximum transconductances (g_{m}S) of 124 and 134 mS/mm, respectively, which are limited by the access resistance.

The I_{d}−V_{ds} curves in Fig. 2(a) show two knee voltages that are a unique characteristic of the dual-gate devices. The first knee voltage is at V_{ds} = V_{gs} − V_{th,E−mode}, where V_{th,E−mode} = 2.9 V, the E-mode gate threshold voltage. The second knee voltage is at V_{ds} = V_{gs} − V_{th,D−mode}, where V_{th,D−mode} = −3.5 V, the D-mode gate threshold voltage. The output conductance between the two knee voltages is due to the short-channel effect of the 95-nm E-mode gate.

A maximum 643-V three-terminal breakdown voltage is achieved on a dual-gate E-mode device at V_{gs} = 0 V with L_{gdr} = 18 μm (shown in Fig. 3). Its specific on-resistance (R_{sp,on}) is extracted to be 4.3 mΩ⋅cm², with L_{gdr} = 24 μm (including a 2-μm transfer length from the source and drain contacts). A device with L_{gdr} = 15 μm has a breakdown of 567 V and a R_{sp,on} of 3.4 mΩ⋅cm². The breakdown curves of a standard D-mode device with the same L_{gdr} biased at V_{gs} = −8 V and −6.8 V are compared with that of the E-mode device in Fig. 3. Both E- and D-mode devices reach the same breakdown voltage at I_{d} = 1 mA/mm, which is limited by the Si substrate. However, the E-mode device has higher drain leakage than the D-mode device biased at V_{gs} = −8 V. A
device performance can be further improved by increasing the Al$_2$O$_3$/GaN interface mobility.

**IV. SUMMARY**

This letter has demonstrated the concept of an integrated dual-gate structure for E-mode GaN transistors where a short gate controls the threshold voltage and a longer gate supports the drain voltage drops. Using gate recess and Al$_2$O$_3$ gate dielectric, the fabricated dual-gate E-mode AlGaN/GaN on Si transistors show a threshold voltage of 2.9 V, a maximum drain current of 434 mA/mm, and a $R_{sp, on}$ of 4.3 m$\Omega$·cm$^2$ with a breakdown voltage of 643 V. The proposed integrated dual-gate transistor is therefore a very promising approach to achieving high breakdown and threshold voltage with minimum impact on on-resistance. These three properties are important requirements for the use of GaN transistors in high-performance power electronics.

**REFERENCES**


