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High-Performance Integrated Dual-Gate AlGaN/GaN Enhancement-Mode Transistor

Bin Lu, Student Member, IEEE, Omair Irfan Saadat, Student Member, IEEE, and Tomás Palacios, Member, IEEE

Abstract—In this letter, we present a new AlGaN/GaN enhancement-mode (E-mode) transistor based on a dual-gate structure. The dual gate allows the transistor to combine an E-mode behavior with low on-resistance and very high breakdown voltage. The device utilizes an integrated gate structure with a short gate controlling the threshold voltage and a long gate supporting the high-voltage drop from the drain. Using this new dual-gate technology, AlGaN/GaN E-mode transistors grown on a Si substrate have demonstrated a high threshold voltage of 2.9 V with a maximum drain current of 434 mA/mm and a specific on-resistance of 4.3 mΩ·cm² at a breakdown voltage of 643 V.

Index Terms—AlGaN/GaN, dual-gate, enhancement-mode (E-mode), high-electron-mobility transistor (HEMT), power electronics.

I. INTRODUCTION

AlGaN/GaN high-electron-mobility transistors (HEMTs) have attracted a great interest for power electronics applications. A standard AlGaN/GaN HEMT is a depletion-mode (D-mode) device due to the large 2-D electron gas induced by the polarization charge at the AlGaN/GaN interface [1]. However, enhancement-mode (E-mode) AlGaN/GaN HEMTs are highly desirable for power electronics as they can greatly simplify circuit designs and improve system reliability.

Several approaches have been reported in the past for fabricating normally-off GaN transistors, including gate recess [2], fluorine/hydrogen plasma treatment [3]–[5], p-type gate injection [6], engineering the surface potential with dielectrics [7], [8], dipole engineering [9], [10], and GaN MOSFETs [11]–[14]. However, it is difficult to use these methods to fabricate devices that simultaneously have large threshold voltage, low on-resistance, and high breakdown voltage. In this letter, we report the use of a new integrated dual-gate technology on a standard AlGaN/GaN D-mode HEMT structure that allows the fabrication of state-of-the-art AlGaN/GaN E-mode power transistors with high threshold voltage (> 2.8 V), high drain current (> 400 mA/mm), and high breakdown voltage (643 V).

The concept of the dual-gate technology is based on the circuit topology shown in Fig. 1(a). High-performance E-mode operation can be achieved by connecting a high-voltage D-mode AlGaN/GaN HEMT with a low-voltage short-gate E-mode device, which can be a Si MOSFET or an E-mode GaN-based transistor. This circuit topology can be integrated into a single device on an AlGaN/GaN structure—the integrated dual-gate transistor— as shown in the device schematic in Fig. 1(b), where the E-mode gate is implemented by gate recess. Although two separated gate fingers can be used, the integrated dual-gate structure gives the smallest form factor when the two gates are biased at the same voltage.

When the device is in the pinchoff, the channel underneath the D-mode gate will be depleted, and the short E-mode gate will be shielded from the large drain voltage. Only a voltage that is equal to the threshold voltage of the D-mode gate (|Vth|) is dropped across the E-mode short gate, as shown by the simulation of the potential distribution in the integrated dual-gate normally-off transistor with Vgs = 0 V and Vds = 100 V.

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be carefully designed so that the following will be achieved: 1) the gate length of the E-mode gate [shown in the SEM image in Fig. 1(b)] should be as short as possible to reduce its impact on the device total on-resistance; 2) the D-mode gate needs to be long enough (~1 μm in our devices) to support the high drain voltage; and 3) the pinchoff voltage of the D-mode gate should not exceed the drain punchthrough voltage of the E-mode gate, which requires the D-mode gate to be as close to the channel as possible.

II. DEVICE FABRICATION

The devices used in this letter were fabricated on an Al-GaN/GaN heterostructure grown on a 4-in Si (111) substrate by Nitronex Corporation. The structure has an ~1.8-μm undoped GaN/AlGaN buffer and a 17-nm AlGaN barrier. Ti/Al/Ni/Au alloyed source and drain ohmic contacts were formed by rapid thermal annealing (RTA). Mesa isolation was achieved by BCl3/Cl2 plasma etching. Then, the short E-mode gate ($L_g = 95 \pm 10$ nm) was patterned with electron beam lithography, and the AlGaN barrier was fully recessed with low-damage BCl3/Cl2 plasma etching. A 14-nm Al2O3 gate dielectric was then deposited by atomic layer deposition, followed by 90-s RTA at 700 °C. Finally, a 2-μm-long Ni/Au/Ni gate electrode was deposited, overlapping with the first gate-recess region. The 2-μm gate was shifted ~1 μm toward the drain side forming the D-mode gate in the integrated dual-gate structure, as shown in the SEM image in Fig. 1(b). The gate was annealed at 500 °C for 3 min. Standard D-mode transistors were also fabricated at the same time as a reference on the same sample without the gate recess. The breakdown voltage was measured using a Tektronix curve tracer connected to Agilent 34401A multimeters. The breakdown voltage is defined as the voltage when the leakage current reaches 1 mA/mm.

III. EXPERIMENTAL RESULTS

The dc characteristics of a normally-off integrated dual-gate device with $L_{gd} = 5$ μm are shown in Fig. 2. The maximum forward gate bias voltage ($V_{gs}$) of the fabricated devices is 7 V, beyond which the gate dielectric breaks. The maximum drain current at $V_{gs} = 7$ V of the E-mode dual-gate device is 434 mA/mm [Fig. 2(a)]. The transfer characteristics of the E- and D-mode devices are shown in Fig. 2(b). The E-mode device has a threshold voltage of 2.9 V, while the D-mode device has a threshold voltage of ~3.5 V, which is also the pinchoff voltage of the D-mode gate in the integrated dual-gate device. Measurements from five E-mode devices on the sample give an average threshold voltage of 2.9 V with a standard deviation $\sigma$ of 0.10 V, which is comparable to the one in D-mode devices ($\sigma = 0.13$ V). The integrated dual-gate E-mode and standard D-mode transistors reach maximum transconductances ($g_m$’s) of 143 and 134 mS/mm, respectively, which are limited by the access resistance.

The $I_d$-$V_{ds}$ curves in Fig. 2(a) show two knee voltages that are a unique characteristic of the dual-gate devices. The first knee voltage is at $V_{ds} = V_{gs} - V_{th,E-mode}$, where $V_{th,E-mode} = 2.9$ V, the E-mode gate threshold voltage. The second knee voltage is at $V_{ds} = V_{gs} - V_{th,D-mode}$, where $V_{th,D-mode} = -3.5$ V, the D-mode gate threshold voltage. The output conductance between the two knee voltages is due to the short-channel effect of the 95-nm E-mode gate.

A maximum 643-V three-terminal breakdown voltage is achieved on a dual-gate E-mode device at $V_{gs} = 0$ V with $L_{gd} = 18$ μm (shown in Fig. 3). Its specific on-resistance ($R_{on}$) is extracted to be 4.3 mΩ·cm², with $L_{sd} = 24$ μm (including a 2-μm transfer length from the source and drain contacts). A device with $L_{gd} = 15$ μm has a breakdown of 567 V and a $R_{on}$ of 3.4 mΩ·cm². The breakdown curves of a standard D-mode device with the same $L_{gd}$ biased at $V_{gs} = -8$ V and $-6.8$ V are compared with that of the E-mode device in Fig. 3. Both E- and D-mode devices reach the same breakdown voltage at $I_d = 1$ mA/mm, which is limited by the Si substrate. However, the E-mode device has higher drain leakage than the D-mode device biased at $V_{gs} = -8$ V. A
similar trend is also reported in [14]. The higher drain leakage associated with the E-mode device is due to its insufficient electron blocking barrier in the channel at the $V_{GS} = 0$-V pinchoff condition. Similarly, lowering the electron blocking barrier in the D-mode device by increasing the gate bias from $-8$ to $-6.8$ V increases its drain leakage as well (as shown in Fig. 3). Improving the electron confinement by using a back barrier in the AlGaN/GaN structures would reduce the drain leakage of the E-mode transistor.

By varying the recessed gate lengths in the integrated dual-gate structure, the resistance from the gate-recessed region can be extracted from the on-resistance ($R_{on}$) versus recessed-gate-length curve in Fig. 4, where the $R_{on}$ of these devices is calculated from the $I$–$V$ characteristics at a gate bias of 7 V. The slope of the curve gives a sheet resistance of 32.5 kΩ/□ in the recessed region. Therefore, the 95-nm recessed gate region contributes only 17% of the total device resistance of the 643-V E-mode device with $L_{gd} = 18$ μm. The dual-gate design allows the decoupling of the E-mode recessed region from the D-mode high-voltage region, which significantly improves the on-resistance and the maximum current of the devices, as shown in Fig. 5, where the combination of the maximum drain current, $R_{sp, on}$, and threshold voltage for several published E-mode GaN transistors with a breakdown voltage over 500 V is benchmarked.

The relatively high sheet resistance of the recess region is due to the low electron mobility in that region. The electron mobility at the Al$_2$O$_3$/GaN interface in the recessed region of the dual-gate E-mode transistors is $16 \pm 2$ cm$^2$/V·s (extracted from the $g_{m0} - V_g$ characteristics), while the extracted mobility for the D-mode device is $1045 \pm 79$ cm$^2$/V·s. The device performance can be further improved by increasing the Al$_2$O$_3$/GaN interface mobility.

IV. SUMMARY

This letter has demonstrated the concept of an integrated dual-gate structure for E-mode GaN transistors where a short gate controls the threshold voltage and a longer gate supports the drain voltage drops. Using gate recess and Al$_2$O$_3$ gate dielectric, the fabricated dual-gate E-mode AlGaN/GaN on Si transistors show a threshold voltage of 2.9 V, a maximum drain current of 434 mA/mm, and a $R_{sp, on}$ of 4.3 mΩ·cm$^2$ with a breakdown voltage of 643 V. The proposed integrated dual-gate transistor is therefore a very promising approach to achieving high breakdown and threshold voltage with minimum impact on on-resistance. These three properties are important requirements for the use of GaN transistors in high-performance power electronics.

REFERENCES


