High-speed graphene interconnects monolithically integrated with CMOS ring oscillators operating at 1.3GHz

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Abstract

We have successfully experimentally integrated graphene interconnects with commercial 0.25 μm technology CMOS ring oscillator circuit using conventional fabrication techniques, and demonstrated high speed on-chip graphene interconnects that operates above 1GHz.

Device Fabrication

(1) Graphene synthesis and transfer

Large area graphene films are grown by chemical vapor deposition (CVD), and then transferred to a 5mm×5mm CMOS chip following the procedure developed by Reina et al. [4]. The graphene synthesis and transfer is described below in brief. A 500nm Ni film is evaporated on a SiO2/Si substrate and thermally annealed. The growth is carried out for 5 minutes at 1000°C, with 5 sccm and 1300 sccm flow of CH4 and H2, respectively. After the growth process, poly(methyl methacrylate) (PMMA) is spin-coated on the graphene/Ni film. The substrate is subsequently placed in a 10% HCl aqueous solution, which etches away the underlying Ni film and releases the graphene film. Once the PMMA/graphene film is placed on the target substrate, the PMMA layer is removed by acetone [4]. The described process flow of material synthesis and transfer is shown in Fig. 1. An average sheet resistance of ~700ohms/sq was extracted for graphene before post-transfer process by transferring graphene films onto SiO2/Si test substrates.

(2) Integration with CMOS circuit

The CMOS chip was fabricated using a 0.25 μm CMOS technology. Each of the arrays of 256 ring oscillators was designed with a missing interconnect wire onto which a graphene interconnect wire was subsequently integrated. Fig. 2 illustrates the process flow for post-transfer processing. The
graphene sheet is first patterned into stripes using optical lithography and oxygen plasma dry etching. Gold electrodes are then deposited as contacts. Then via holes are formed by etching through the CMOS passivation layer, reaching down to the topmost aluminum metal layer (M3) of the chip. Finally via contacts are formed by filling the via holes with 100nm of titanium (Fig.3). MWCNT interconnects are integrated in a similar approach [5] for comparison.

Electrical Testing

The oscillator circuit on chip was implemented as a 5-stage ring oscillator with 4 inverters and one differential amplifier [6] at the receiving end of the interconnect line, as shown in Fig.4c.

(1) DC characterization

The statistics of DC resistivity in Fig. 5(a) shows that the average sheet resistivity remains about 700Ω/sq after post-transfer processing, indicating that the quality of the

Fig.3 Optical images of graphene on top of CMOS chip. (a) Graphene film after being transferred onto a CMOS chip. (b) One fabricated graphene interconnect on top of CMOS ring oscillator array. The lines that appear black in the middle of Ti via contacts are M3 Al lines. Inset: AFM image of graphene stripe on SiO2/Si test substrate.
graphene film is preserved after transfer and post processing. Sheet resistances data of graphene prepared by a variety of synthesis techniques are extracted from previous literature, and compared in Table 1. We can see that a few to several layers of graphene is generally more favorable for obtaining low sheet resistance for high-speed interconnects. Contact resistance extracted from Fig. 5b was negligible compared to interconnect resistance. Along with the linear I-V curves shown in Fig. 5b, it is clear to see that we have obtained near-ideal ohmic contacts, a key requirement for interconnect technology. The distribution of resistivity is probably due to material nonuniformity.

(2) RF characterization

Oscillation frequency \( f \) of the ring oscillator circuit is determined by RC delay expressed by Eq. (1). If capacitance associated with graphene, \( C_g \) dominates the total capacitance \( C_{tot} \), \( f \) is then expressed by Eq. (2):

\[
\begin{align*}
\frac{1}{RC} & \propto \frac{W}{L \cdot C} \quad (1) \\
\frac{1}{RC} & \propto \frac{1}{L^2} \quad (2)
\end{align*}
\]

where \( L \) is the interconnect length, and \( W \) is the width. Experimental results (Fig.6) show that frequency is directly correlated with \( W \), and inversely correlated with \( L/W \) ratio as it is in Eq.(1), which means \( C_{tot} \) is not dominated by \( C_g \).

Comparison of RF performances between graphene and MWCNT is shown in Fig.7. For the same ring oscillator circuit design, graphene interconnects have lower resistance and thus offered a higher oscillation frequency. However at the same resistance value, MWCNT tends to have better performance. This is probably due to the larger capacitance associated with wide graphene stripes. Therefore narrower, multi-layered graphene with smaller RC delay should be more desirable for RF applications. Currently, RF performance of MWCNT is mainly limited by the difficulty in achieving Ohmic contacts to all the shells for maximum conductance.

<table>
<thead>
<tr>
<th>( R_{sheet} ) (K(\Omega)/sq)</th>
<th># of layers</th>
<th>Synthesis</th>
<th>Reference</th>
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<tr>
<td>~0.28</td>
<td>~6-10</td>
<td>CVD growth on Ni</td>
<td>[7]K. S. Kim et. al., Nature, 457, 2009</td>
</tr>
<tr>
<td>~1.8</td>
<td>~10.1nm*</td>
<td>Graphene oxide reduction</td>
<td>[10]X. Wang et. al., Nanoletters, 8, 2008</td>
</tr>
<tr>
<td>~0.7</td>
<td>~10nm*</td>
<td>CVD growth on Ni</td>
<td>*this work</td>
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*The film thickness is reported in lieu of the number of layers
Conclusions

The demonstration of monolithic integration of graphene with CMOS using conventional fabrication processes represents an important step forward for potential VLSI application of graphene for nanoelectronics that is scalable to any CMOS technology and arbitrary wafer sizes. Additionally, the observation of GHz operation in graphene stripes with length as long as 80 μm indicates the promising future of graphene for local and semi-global high-speed interconnects.

Acknowledgements

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Reference


Fig. 6 (a) Oscillation frequency for various interconnect lengths and widths. GHz range operation frequency is observed for interconnects up to ~80 μm long; (b) Oscillation frequency and resistance as functions of L/W ratio indicative of the # of squares. Symbols are experimental data, bold lines are a visual guides.

Fig. 7 Oscillation period as a function of interconnect resistance for CMOS reference interconnect (aluminum), MWCNT, and graphene. For the same ring oscillator circuit, graphene offers higher speed operation compared to MWCNT. However, at the same resistance value MWCNT interconnects are faster most likely due to their smaller capacitance.