Investigation of hole mobility in gate-all-around Si nanowire p-MOSFETs with high-k/metal-gate: Effects of hydrogen thermal annealing and nanowire shape

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Investigation of Hole Mobility in Gate-All-Around Si Nanowire p-MOSFETs with High-κ/Metal-Gate: Effects of Hydrogen Thermal Annealing and Nanowire Shape

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Abstract

A detailed study of hole mobility is presented for gate-all-around Si nanowire p-MOSFETs with conformal high-κ/MG and various high-temperature hydrogen annealing processes. Hole mobility enhancement relative to planar SOI devices and universal (100) is observed for 15 nm-diameter circular Si nanowires, due to an optimized anneal process which smooths and reshapes the suspended nanowires. Increasing hole mobility is experimentally observed with decreasing nanowire width down to 12 nm. The measured inversion capacitance-voltage characteristics are in excellent agreement with quantum mechanical simulations. In addition, a method to extract areal inversion charge density in Si nanowires is introduced and its impact on the mobility of Si nanowires with various shapes is explored.

Introduction

Gate-All-Around (GAA) Si nanowire (NW) MOSFETs are excellent candidates for future CMOS integration due to their ideal electrostatics and immunity to short channel effects [1, 2]. Effective hole mobility (μeff) for Si NWs processed with non-uniform, plane-dependent thermally grown oxide/poly-Si gates is reduced for decreasing NW size, as a result of non-ideal NW sidewalls [3, 4]. Maskless hydrogen anneal (H2A) is shown to smooth and/or reshape suspended NWs [5] and has recently been combined with oxidation to form GAA NW MOSFETs with excellent current drive [2]. The effect of H2A on the electron mobility of 20 nm wide NWs has recently been reported [6]. In this work, for the first time, effective hole mobility of GAA Si NWs with high-κ/MG is investigated in detail. The conformal dielectric ensures that the entire perimeter is uniformly gated. The impact of high-temperature (>850°C) H2A on the μeff of Si NWs with different conditions that smooth and reshape the NWs is investigated. Increasing hole mobility with decreasing NW width down to 12 nm is observed for NWs subjected to H2A. Quantum-mechanical (QM) simulation is utilized to verify the capacitance measurements and mobility extraction method.

Device Fabrication and Characterization

Fig. 1 shows the schematic and SEM images of high-κ/MG GAA NW p-MOSFETs fabricated along the <110> direction on (100) thin body SOI. GAA devices with LNW=0.6-1.2 μm and 500 parallel NWs were fabricated to accurately measure the inversion capacitance and hole mobility. The process flow and SEM images of NWs before and after H2A are shown in Fig. 2. Table I summarizes the H2A process splits utilized after NW suspension. Extremely smooth sidewalls for various NW dimensions are observed in SEM images after the optimized H2A (Fig. 2 and 3). On wafer test structures were designed to calibrate various NW and device dimensions using cross-sectional SEM and TEM. Fig. 3 shows XTEM images of NWs subjected to H2A (condition B), after device completion. NWs are surrounded by the conformal ALD O3-SiO2 (~1 nm)/Al2O3 (5.5 nm)/WN (~30 nm) gate stack. It can also been seen that NW sidewalls are faceted to {311}, {111} and {110} crystallographic planes after the H2A process.

Table I: Process splits for post-suspension NW treatment, indicating pre-dielectric cleaning and H2A conditions.

<table>
<thead>
<tr>
<th>Condition</th>
<th>Suspended Nanowire Process</th>
</tr>
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<tbody>
<tr>
<td>A</td>
<td>No H2 annealing, RCA clean, HF last, ALD</td>
</tr>
<tr>
<td>B</td>
<td>RCA clean, H2 anneal at 850°C, 100 torr, for 2 min, ALD</td>
</tr>
<tr>
<td>C</td>
<td>Condition B + RCA, H2 anneal at 875°C, 100 torr, for 2 min, HF dip, ALD</td>
</tr>
</tbody>
</table>

Results and Discussion

Fig. 4 shows the transfer characteristics of 22×15.6 nm GAA NW p-FETs treated with H2A (condition B) and without H2A, indicating ideal sub-threshold slope, SS=61 mV/dec, and high cut-off ratio (~10^10 order). The variation of SS and threshold voltage (Vth) as a function of WNW is shown in Fig. 5. All devices exhibit near ideal swing indicating very low density of interface traps (Dit) at the Si/dielectric interface. A large Vth roll-off with decreasing WNW is observed, which cannot be explained by QM simulations. The output and transfer characteristics of 22×15.6 nm NWs (Fig. 6 and 7) show more than 60% enhancement in saturation and linear current for H2A relative to NWs without H2A, at a given VGS-Vth.

The low-field effective hole mobility of Si NWs was extracted using measured I-V and split C-V and the 2-FET method [7], utilizing devices with LNW = 0.6 and 1.2 μm. Fig. 8 shows such current and capacitance measurements for 15 nm diameter circular NWs. Excellent agreement between measured and nextnano3 [8] simulated intrinsic capacitance of ~15 nm-diameter circular and 22×15.6 nm elliptical NWs (normalized to the length of the NWs) is shown in Fig. 9,
verifying the mobility extraction method. Only physical dimensions (derived from TEM), \( \kappa \) (extracted from planar C-V measurements) and \( V_{FB} \) were input into the simulations. The upper and lower simulated curves correspond to simulations using a gate metal with high and medium density of states, respectively.

The plots of \( \mu_{\text{eff}} \) as a function of inversion charge density \( (N_{\text{inv}}) \) for NWs without H2A and with H2A (condition B) are shown in Fig. 10 and Fig. 11, respectively. Without H2A, similar hole mobilities are observed at high \( N_{\text{inv}} \) for various \( W_{\text{NW}} \) in the range of 22-72 nm, with an average 20% drop compared to planar SOI devices. On the other hand, \( \mu_{\text{eff}} \) enhancement over planar (100) SOI is observed for sub-40 nm NW widths subjected to H2A (condition B), at high inversion charge densities. In addition, monotonic \( \mu_{\text{eff}} \) enhancement with decreasing NW width can be seen, where the mobility is enhanced by 47% relative to the widest NW and 33% over the planar (100) SOI device at \( N_{\text{inv}}=1.1\times10^{13} \, \text{cm}^{-2} \). Increased contribution of high-mobility sidewalls with reduced sidewall roughness scattering is believed to be responsible for this mobility enhancement with decreasing NW width. Fig. 12 shows the hole \( \mu_{\text{eff}} \) vs. \( N_{\text{inv}} \) for 15 nm-diameter circular NWs, demonstrating mobility enhancement over planar SOI and the highest mobility NWs without H2A. These results demonstrate the highest hole mobility compared to reported data for sub-15 nm thickness NWs [3, 9, 10], particularly at high \( N_{\text{inv}} \) where roughness scattering is important. Fig. 13 shows the width-dependence of hole mobility for NWs subjected to condition A and B. Little dependence on \( W_{\text{NW}} \) is observed without H2A due to a balance between high-hole-mobility non-(100) planes [11] and sidewall roughness scattering, while the latter mechanism is significantly diminished for condition B. Finite-element stress simulations (not shown) do not indicate significant NW width dependence of strain in the channel due to the WN gate intrinsic stress.

Fig. 14 illustrates the QM simulation of hole density in elliptical and circular NWs. Increased charge density at the sidewalls compared to the horizontal (100) surfaces is observed due to the radial electric field, indicating the importance of the sidewall roughness quality. In addition, as the carriers are physically separated from the dielectric interface (particularly at low gate overdrive), the effective perimeter (defined as the locus of the hole centroid, which is displaced from the NW surface by the distance \( \delta_{\text{QM}}(V_{GS}) \), as shown in Fig. 14) should be used to extract the areal \( N_{\text{inv}} \). Fig. 15 shows the mobility of circular and elliptical NWs as a function of \( N_{\text{inv}} \) with and without this QM correction. While the results are close for wide elliptical NWs, major correction is needed for 15nm circular NWs at low \( N_{\text{inv}} \) (< 2 \times 10^{12} \, \text{cm}^{-2} ). For H2A temperatures above 850°C, significant size reduction of the Si NWs is observed (Fig. 16). HR-XSEM images of a NW test structure subjected to H2A (condition C) are shown in Fig. 17, indicating NW circular reshaping and formation of sub-10nm NWs without oxidation. Transfer characteristics, NW capacitance (simulated and measured), and \( \mu_{\text{eff}} \) for NWs subjected to H2A (condition C) are shown in Fig. 18-20. All devices subject to condition C, including on-chip planar MOSFETs, showed high \( D_{\text{Si}} \) (likely due to the HF dip prior to ALD), which generally reduces the mobility compared to condition B. For sub-10 nm NWs, the effective NW diameter, \( d_{\text{NW,eq}} \) (defined as equivalent circular diameter with similar capacitance) was extracted by fitting simulations to the C-V measurements. The diameter dependence of \( \mu_{\text{eff}} \) (condition C) for diameters down to 8 nm is shown in Fig. 20 (b). A peak in mobility is seen for 12 nm-wide NWs. For widths above 12 nm, the increase in \( \mu_{\text{eff}} \) with decreasing width is attributed to the larger contribution of the high-hole-mobility sidewalls. For sub-12 nm diameters, increased phonon scattering associated with carrier confinement as well as diameter-fluctuation scattering effects may contribute to the observed \( \mu_{\text{eff}} \) reduction. To compare the width dependence of the \( \mu_{\text{eff}} \) for various process conditions, the mobilities were normalized by the mobility of on-chip planar SOI devices (extracted for each process condition), as shown in Fig. 21. Interestingly, similar normalized \( \mu_{\text{eff}} \) is observed in the common range of \( W_{\text{NW}} \) for annealed NWs processed under conditions B and C.

### Summary and Conclusion

In summary, for the first time, a detailed study of hole mobility is presented for GAA Si NWs with conformal high-k/MG and various H2A processes. Increasing hole mobility with decreasing NW width down to 12 nm is observed for NWs subjected to H2A. The highest hole mobility is achieved for circular NWs with an optimized process, with 33% mobility enhancement over universal (100) mobility at high \( N_{\text{inv}} \). The results and the new insights obtained are promising for future CMOS applications.

### Acknowledgement

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### References

8. nextnano**: http://www.nextnano.de
Fig. 1: (top) Top-view and cross-sectional schematic of high-k/MG GAA NW p-FETs oriented along <110> fabricated on (100) thin body SOI. The NW dimensions (W_NW, t_NW, L_NW) are defined as shown; (bottom) Tilted (left) and cross-sectional (right) SEM images of the final device structure, with a FIB cut along the suspended NW direction.

Fig. 2: (left) Process flow used to fabricate GAA NW p-FETs with high-k/MG and H2 anneal (H2A) process; (right) schematic and top-view SEM (enhanced for brightness, contrast and shadows) of suspended Si NWs before and after high-temperature H2A. Reduced sidewall roughness is observed after H2A.

Fig. 3: (left) Plan-view SEM images of suspended Si NWs subjected to H2A (condition B), with W_NW = 14-73 nm; (right) XTEM of on-wafer NW test structure (as-patterned W_NW = 20 to 60 nm, step 4 nm) subjected to H2A (condition B), after device completion. NWs are surrounded by conformal 1 nm ALD O_SiO_2/5.5 nm Al_2O_3/30 nm WN gate stack. For wide NWs, t_NW=16 nm; dropping to 13 nm for the circular NW, {110}, {111} and {311} sidewall facets are discernible from the XTEM images.

Fig. 4: Transfer characteristics of 22×15.6 nm GAA NW p-FETs (with N=500 NWs) treated with H2A (condition B) and without H2A (condition A). No hysteresis was observed.

Fig. 5: Typical I_D-V_GS plots of 15nm-diameter circular NWs (with N=500 NWs) with H2A (condition B) and without H2A (condition A), indicating very low D_S.

Fig. 6: Output characteristics of 22×15.6 nm GAA NW p-FETs (with N=500 NWs) with H2A (condition B) and without H2A (condition A), for overdrive V_GS-V_TH = -2 to 0V. Current enhancement of ~1.6X over condition A is observed for the NWs annealed with condition B, due to improved sidewall roughness scattering.

Fig. 7: Plot of I_D vs. gate over-drive voltage, V_GS-V_TH, for 22×15.6 nm GAA NW p-FETs with H2A (condition B) and without H2A (condition A), indicating 1.64X linear current enhancement due to the H2A process.

Fig. 8: Typical I_D-V_GS and split C-V measurements of 15nm-diameter circular NW (with L_NW = 0.6 and 1.2 µm) for mobility extraction using the 2-FET method [7]. Current and capacitance are normalized by the number of NWs (N=500).

Fig. 9: Measured and simulated inversion capacitance of NWs, demonstrating excellent agreement between measured and simulated results, verifying mobility extraction method. Only physical dimensions (derived from TEM), κ (extracted from planar CV measurements) and V_FB were input into the simulations. The upper and lower curves correspond to simulations using a gate metal with high and medium density of states, respectively.
Fig. 10: Effective hole mobility vs. inversion charge density \(N_{inv}\) (normalized by NW circumference) for NWs with \(W_{NW} = 22\)–72 nm, without H2A. Similar mobilities are observed at high \(N_{inv}\) for various \(W_{NW}\), with a ~20% drop compared to planar (100) SOI device.

Fig. 11: Effective hole mobility vs. \(N_{inv}\) (normalized by NW circumference) for NWs with \(W_{NW} = 15\)–72 nm subjected to H2A (condition B). Monotonic mobility enhancement with decreasing NW width is observed.

Fig. 12: Hole mobility vs. \(N_{inv}\) for 15 nm circular NWs (condition B) demonstrating mobility enhancement over planar SOI and the highest mobility NWs without H2A. Significant enhancement is seen relative to published data for sub-15 nm thickness NWs.

Fig. 13: Width-dependence of hole mobility for NWs with and without H2A, at \(N_{inv} = 5 \times 10^{12}\) and \(10^{13}\) cm\(^{-2}\). More than 57% enhancement is observed for NWs subjected to H2A (condition B) for \(W_{NW} < 22\) nm.

Fig. 14: Simulated (nextnano\(^3\)) hole charge density in NWs with elliptical (22×15.7 nm) and circular (15.6×14 nm, \(d_{NW} \approx 15\) nm) cross-sections for \(V_{GS}-V_{FB} = -1.3\) V. Inversion centroid is displaced from NW surface by the distance \(\delta_{QM}(V_{GS})\) which is used in the QM correction to the perimeter (Fig. 15).

Fig. 15: Hole mobility vs. \(N_{inv}\), normalized by NW physical perimeter (dashed line) and with QM correction (symbols) for the NWs shown in Fig. 14. The QM correction to the perimeter was calculated using simulations at each gate bias.

Fig. 16: Top-view SEM image of NW test structure subjected to high temperature H2A at 875°C, showing anisotropic etching of Si NWs.

Fig. 17: HR-FIB-XSEM image of a NW test structure (with as patterned \(W_{NW} = 20\) to 60 nm; step 4 nm) subjected to H2A (condition C), after device completion. NW diameters (\(d_{NW}\), as defined in the SEM image) are scaled from 22 nm down to sub-10 nm, mostly with circular cross sections.

Fig. 18: Transfer characteristics of GAA NW p-FETs (with \(d_{NW} = 8, 10, 12, 17, 22\) nm subjected to H2A (cond. C). Non-ideal swings (>80 mV/dec) suggest that NWs have high \(D_{it}\) due to non-optimized cond. C.

Fig. 19: Measured and simulated intrinsic NW capacitances for \(d_{SOI} = 8\)–17 nm (condition C). \(d_{SOI}\) was measured by HR-XSEM for the 12 and 17 nm NWs. For sub-10 nm NWs, the effective circular diameter (\(d_{eq}\)) was extracted by fitting simulations to the CV data.

Fig. 20: Plots of effective hole mobility vs. \(N_{inv}\), and \(d_{NW}\) (nanowire diameter for NWs subjected to H2A (condition C). Increased mobility is observed by reducing \(d_{NW}\) to 12 nm diameter. However, the mobility of sub-10 nm circular NWs is reduced as \(d_{NW}\) is decreased.

Fig. 21: Comparison of the hole mobility normalized by the mobility of on-chip planar SOI FETs for various post-suspension treatments. Similar normalized mobilities are observed for H2A nanowires processed at cond. B and C, in the common range of \(W_{NW}\).