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Detailed Terms
An Energy Management IC for Bio-Implants Using Ultracapacitors for Energy Storage
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Abstract

We present the first known energy management IC to allow low-power systems, such as biomedical implants, to optimally use ultracapacitors instead of batteries as their chief energy storage elements. The IC, fabricated in a 0.18 μm CMOS process, consists of a switched-capacitor DC-DC converter, a 4 nW bandgap voltage reference, a high-efficiency rectifier to allow wireless recharging of the capacitor bank, and a switch matrix and digital control circuitry to govern the stacking and unstacking of the ultracapacitors. The stacking procedure allows for more than 98% of the initial energy stored in the capacitors to be removed before the output voltage drops unsuitably low. The DC-DC converter achieves a peak efficiency of 51% for loads between 10 and 100 μW, operates for input voltages between 1.25 and 2.5 V.

Introduction

Recent trends in the medical industry have created a growing demand for implantable devices. While traditionally relying on batteries as energy storage elements, there is emerging interest in using ultracapacitors [1]. Ultracapacitors lack the energy density of batteries, at present falling short by approximately an order of magnitude. However, they have several compelling advantages. Chief among them is the promise they hold of being integrated on a chip, as proposed in [1] and as indicated in research in carbon nanotube based ultracapacitors in [2]. In addition to the potential for an extremely small form factor, ultracapacitors also feature: high power density; a practically unlimited number of recharge cycles; extremely rapid recharging; and an uncomplicated relationship between the terminal voltage and its state of charge.

In this paper we present an energy management IC as a solution to many of the engineering challenges posed by using ultracapacitors. A major problem with using any capacitor as an energy source is the fact that its voltage drops so rapidly with decreasing charge. This leaves the circuit to cope with a large supply variation and, worse, can lead to a lot of energy being left on the capacitor when its voltage gets too low. The chip presented here has a switched-capacitor (SC) DC-DC converter to regulate the output voltage, which is referenced to a bandgap reference that draws less than 4 nW. In addition, rather than use a single ultracapacitor, we split it into an array of four capacitors which we progressively stack as energy is drawn out. Finally, we take into account the "start-up" problem, or restoring charge to an ultracapacitor array that has completely lost charge after being implanted. The energy management IC described in this paper is able to recharge from RF energy coupled into an antenna, even from the zero-charge state.

1Note that 100 mV left on a 1 F ultracapacitor translates to 100 nJ, enough to power a 10 μW implant for almost 3 hours.

Architecture and Circuit Implementation

The architecture for the energy management integrated circuit (EMIC) that implements the reconfigurable ultracapacitor bank and power converter is shown in Fig. 1. The general operation of the EMIC is illustrated in Fig. 2. During normal operation, the SC converters step down the ultracapacitor bank and reference voltages to α1 and α2, respectively. When discharging, once α1 falls below the stepped down reference, the comparator trips and the digital logic reconfigures the switch matrix. A similar procedure follows during charging, in which case the comparator trips once α1 > α2 resulting in unstacking. A 4-stage synchronous rectifier [3] is connected to the ultracapacitor bank during wireless recharging in the 900 MHz band.

The load is driven by the output of a 1.5-MHz switched-capacitor regulator whose level is controlled by a 1-V reference voltage generated by the bandgap reference (BGR). In a circuit environment such as this where the supply voltage varies significantly (the supply voltage here is the output of the ultracapacitor array), the BGR provides a stable reference useful for controlling the switch matrix of the reconfigurable capacitor bank. Since the BGR is the only static power draw in the entire architecture, we exploit the fact that the reference is only needed to drive transistor gates...
to allow us to operate the BGR at <4 nW for the highest ultracapacitor voltage of 2.5 V.

Referring to Fig. 2, assuming all the ultracapacitors are equal in size and with $v_{DD,CAP,\text{max}} = 2v_{DD,CAP,\text{min}}$, our stacking strategy results in utilization of 98.4% of the total energy initially stored on the ultracapacitors. In this stacking discipline, moving from one configuration to the other either halves or doubles the number of parallel branches, and is conveniently implemented when the total number of capacitors is a power of two. If this convention is followed, we may write the energy efficiency that results as

$$\eta_E = \frac{E_{\text{delivered}}}{E_0} = 1 - \frac{1}{2^{2(N-1)}} \left(1 - \frac{v_{DD,CAP,\text{min}}}{v_{DD,CAP,\text{max}}}\right)^2$$

where $N$ is the number of distinct stacking configurations and $E_0$ is the total stored energy. In practice, $v_{DD,CAP,\text{max}}$ is set by dielectric breakdown in the ultracapacitors, and $v_{DD,CAP,\text{min}}$ is set by the minimum input voltage of the SC regulator.

**Measurement results**

Conversion efficiency measurements are shown Fig. 3 as a function of output load power for measured versus simulated data for a clock frequency of 1.5 MHz. A peak efficiency of 51% was measured with a load of 63 μA at 1 V±10 mV. This efficiency is comparable to the 56% achieved in [4], which was also designed for biomedical implant applications.

![Fig. 3. Conversion efficiency of measured versus simulation for f_{\text{clk}} = 1.5 MHz.](Image)

Operation of the IC was confirmed using 5-F ultracapacitors from Maxwell Technologies. These capacitors have 0.18 Ω of series resistance, and 40 μA of leakage current. The voltage ripple at the output of the power converter depends on comparator clock rate in relation to the current draw and capacitance at the load. The higher the current demand and/or the smaller the capacitance, the higher the clock rate necessary for a given ripple. Fig. 4 illustrates this, where the clock has been greatly slowed to 50 kHz for illustration purposes. The current draw is 150-200 nA, and the capacitance is 200 pF±5%. Based on these numbers we expect a ripple on the order of 200 mV, which is what we observe from the measurements in Fig. 4.

The stacking and unstacking operations are shown in Fig. 5 using 300-μF electrolytic capacitors for purposes of illustration. Notice that the charging behavior starts successfully even when the ultracapacitor array is almost fully discharged (see Fig. 5 upper right). This is possible because the rectifier is connected directly to the output of the ultracapacitor array. Once the ultracapacitor output exceeds 1.2 V, the BGR and the switched regulator begin to function. The chip occupies a total area of 1.82 mm² (1.3 mm x 1.4 mm) with a 0.39 mm² active area. Fig. 6 shows the IC die photo.

**Conclusion**

We report what to the best of our knowledge is the first power management IC that allows low-power circuits to optimize their use of ultracapacitors as an energy storage element. We use ultra-low power and mixed signal techniques, and introduce a new stacking strategy to maximize the energy usage of the ultracapacitor array. By implementing a reconfigurable ultracapacitor bank to serve as an energy reservoir, greater than 98% of its stored energy is made available. This far outperforms traditional battery technology.

**References**