50-nm E-mode In$_{0.7}$Ga$_{0.3}$As PHEMTs on 100-mm InP substrate with $f_{\text{max}} > 1$ THz

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We have demonstrated 50-nm enhancement-mode (E-mode) In$_{0.7}$Ga$_{0.3}$As PHEMTs with $f_{\text{max}}$ in excess of 1 THz. The devices feature a Pt gate sinking process to effectively thin down the In$_{0.52}$Al$_{0.48}$As barrier layer, together with a two-step recess process. The fabricated device with $L_g = 50$-nm exhibits $V_T = 0.1$ V, $g_{\text{m, max}} = 1.75$ mS/$\mu$m, $f_T = 465$ GHz and $f_{\text{max}} = 1.06$ THz at a moderate value of $V_{\text{DS}} = 0.75$ V. In addition, we have physically modeled the abnormal peaky behavior in Mason’s unilateral gain ($U_g$) at high values of $V_{\text{DS}}$. A revised small signal model that includes a shunting $R_{gd,NDR}$ with negative value successfully describes the behavior of the device from 1 to 67 GHz.

### Introduction

The last few years have witnessed an explosion of interest in devices suitable for ultra high frequency applications, such as in the Tera-Hz regime. To accomplish this, a device technology must rely on boosting high frequency operation by reducing gate length ($L_g$) to sub-50 nm, improving carrier transport in the channel, improving electrostatic integrity and minimizing resistance and capacitance parasitics [1-2].

An additional feature that is highly desirable in future THz circuits is a positive $V_T$. Achieving E-mode PHEMTs is rather difficult as it demands tight control of $t_{\text{ins}}$, especially as $L_g$ approaches to sub-50 nm regime. In this work, we use Pt gate sinking to shift $V_T$ and to thin down the barrier [3]. Pt gate sinking in devices with high InAs compositions in the channel have been demonstrated before [4-5]. What is important in this work is a well balanced device design that pays close attention to short-channel effects and that leads to exceptional high frequency characteristics. In this work, we demonstrate for the first time enhancement-mode In$_{0.7}$Ga$_{0.3}$As PHEMTs with $f_{\text{max}}$ in excess of 1 THz at a moderate value of $V_{\text{DS}} = 0.75$ V.

### Process Technology

Fig. 1 shows a cross section of the device structure. The device architecture brings together unique features designed to minimize parasitics and mitigate short-channel effects, as in [5]. The epitaxial layer structure is similar to [6]. It features a 10-nm thick In$_{0.7}$Ga$_{0.3}$As channel. After a two-step recess process that exposes an InAlAs barrier, a Pt/Ti/Pt/Au (3/30/10/350 nm) gate was created. Subsequently, the devices were annealed at 250 °C for 2 minutes to drive the Pt into the InAlAs barrier. In this way, a gate-to-channel distance ($t_{\text{ins}}$) of about 4-nm was achieved with side-recess spacing ($L_{\text{side}}$) of 150-nm. A range of gate length ($L_g$) in this work was from 200-nm to 50-nm.

### DC & Microwave Characteristics

Fig. 2 shows typical DC output characteristics of In$_{0.7}$Ga$_{0.3}$As PHEMTs with various values of $L_g$. Well-behaved drain current saturation is observed with excellent pinch-off characteristics up to $V_{\text{DS}} = 0.9$ V for all gate lengths. Typical ON-resistance ($R_{\text{ON}}$) is about 0.4 Ω-mm for $L_g = 50$ nm devices. As in the author’s previous work on In$_{0.7}$Ga$_{0.3}$As PHEMTs [5], the devices in this work also show improved current driving capability as $L_g$ scales down to 50 nm.

Fig. 3 plots the transconductance ($g_{\text{m}}$) characteristics of the same devices at $V_{\text{DS}} = 0.5$ V. The devices exhibit a continuously increasing $g_{\text{m}}$ as $L_g$ scales down to 50-nm. Particularly, the device with $L_g = 50$ nm shows $g_{\text{m, max}} = 1.7$ S/mm. These outstanding characteristics arise from improved charge control behavior through the combination of the two-step recess plus buried Pt gate sinking technology.

Fig. 4 plots the sub-threshold and transfer characteristics of all the 50-nm In$_{0.7}$Ga$_{0.3}$As PHEMTs on a 100-mm wafer. The devices offer a true e-mode operation ($V_T = 0.1$ V, defined with a criteria of $I_{\text{D}} = 1$ mA/mm) with excellent $V_T$ uniformity ($\Delta V_T = 28$ mV) across the wafer. Besides, the devices show very sharp subthreshold characteristics, as assessed by a subthreshold-swing = 80 mV/dec and DIBL = 80 mV/V, which are close to those of advanced InGaAs PHEMTs [6]. Besides, these devices do not show excessive gate leakage current. The typical gate turn-ON voltage ($V_{\text{g, ON}}$) was greater than 0.5 V with a criteria of $I_{\text{g}} = 1$ mA/mm, which is highly attractive for e-mode operation.
Microwave performance was characterized using an Agilent precision-network-analyzer (PNA) with a standard Line-Reflection-Reflection-Match (LRRM) calibration from 1 GHz to 67 GHz. On-wafer open and short structures were used to de-embed pad capacitances and inductances. Fig. 5 plots measured (symbols) and small-signal modeled (lines) short-circuit current gain (H21), maximum stable gain (MSG), Mason’s unilateral gain (Ug) and stability factor (k) for the 50-nm device at (a) VGS = 0.5 V and VDS = 0.5 V, and (b) VGS = 0.5 V and VDS = 0.75 V. The transistor fT was determined by extrapolating |H21| with a slope of -20 dB/decade using a least-squares fit. The 50-nm PHEMT in this work exhibits a high value of fT = 465 GHz at VDS = 0.75 V, and over 400 GHz at VDS = 0.5 V. More significantly, the device displays an extremely high value of maximum oscillation frequency (fmax). At VDS = 0.75 V, fmax of 1.06 THz is obtained from extrapolation using the measured Ug.
To accurately extract the value of \( f_{\text{max}} \), we carried out small-signal modeling at different bias conditions, as recently proposed [7]. The estimated \( f_{\text{max}} \) is sensitive to the values of small-signal parameters, such as \( R_g \), \( R_s \) and \( R_d \). To make the small-signal modeling process robust, we carefully extracted all the parasitic resistances [7], used them to derive all the intrinsic parameters, and finally verified the accuracy of the small-signal model at different bias conditions across multiple devices. As shown in Fig. 5, our models predict all the S-parameters, RF gains and \( k \) consistently at both bias conditions. From the model, the 50-nm device yields \( f_{\text{max}} = 1.08 \) THz at \( V_{\text{DS}} = 0.75 \) V, which is very similar to the value from the measured \( U_g \). This is the highest \( f_{\text{max}} \) ever reported in any FET on any material system with E-mode operation.

Increasing \( V_{\text{DS}} \) beyond 0.75 V is likely to yield even better \( f_{\text{max}} \). However, it is very difficult to extract it from either the experimental measurement of \( U_g \) or from the small-signal model. This is because \( U_g \) is apt to show sharp peaky behavior at intermediate frequencies as \( V_{\text{DS}} \) increases. Fig. 6 shows measured and modeled RF gains and \( k \) at \( V_{\text{DS}} = 0.9 \) V. Indeed, \( U_g \) exhibits an anomalously increasing behavior with frequency, and the modeled \( U_g \) fails to describe it. For a given device, we have verified that this behavior is reproducible across different measurement systems. Such behavior has also been observed in high frequency devices by another group [1].

A possible mechanism for this is shown in Fig. 8. As \( V_{\text{DS}} \) increases, high-field effects at the drain-side of the gate, such as hot electron production, become more prevalent. These hot electrons are capable of causing NDR effects between the gate and drain [8]. Fig. 9 shows the measured \( I_g \) as a function of \( V_{\text{DS}} \) for 50-nm devices with different values of \( V_{\text{GS}} \). As \( V_{\text{DS}} \) increases, \( I_g \) initially decreases (due to the reduction and eventual change of sign of the gate-drain gate leakage current), and then increases at \( V_{\text{DS}} = 0.5 \) V for \( V_{\text{GS}} > 0.4 \) V due to real-space transfer of hot electrons from the channel into the gate [7]. This is a region of negative differential resistance in \( I_g \).

**Advanced Small-Signal Model**

In trying to understand the abnormal behavior in \( U_g \), we found that \( U_g \) is actually negative before the peak occurs. From the definition of Mason’s unilateral gain, \( U_g \) takes the sign of its denominator. The expression of \( U_g \) is:

\[
U_g = \frac{|Y_{21} - Y_{12}|^2}{\text{Re}(Y_{11}) \cdot \text{Re}(Y_{22}) - \text{Re}(Y_{12}) \cdot \text{Re}(Y_{21})} \quad (1)
\]

Fig. 7 shows the denominator of the experimental \( U_g \) for the 50-nm device at \( V_{\text{DS}} = 0.5 \) V and 0.9 V. Clearly, a negative value of \( U_g \) arises from its denominator and this occurs at high values of \( V_{\text{DS}} \). Furthermore, the frequency at zero-crossing in \( \text{Den}(U_g) \) is responsible for the abnormal peaky behavior in \( U_g \). Now, the question arises: what is the origin of this? We found that a ‘Negative-Differential-Resistance’ (NDR) effect between gate and drain at high values of \( V_{\text{DS}} \) is responsible for the negative \( U_g \).

**Fig. 6** RF gains (\( H_{21}, U_g \) and MSG), \( k \)-factor, and S-parameters (inset) for 50-nm In\(_{0.7}\)Ga\(_{0.3}\)As PHEMTs vs. frequency at \( V_{\text{GS}} = 0.5 \) V and \( V_{\text{DS}} = 0.9 \) V, together with model predictions.

**Fig. 7** Denominator of \( U_g \) for 50-nm device as a function of frequency at \( V_{\text{DS}} = 0.5 \) V and 0.9 V.

**Fig. 8** Physical origin of NDR effect between gate and drain. As \( V_{\text{DS}} \) increases, there is real-space transfer of hot electrons from the channel into the gate.
From the RF point of view, this phenomenon can be modeled by adding a shunt negative resistance ($R_{gd\text{-NDR}}$) between gate and drain, as shown in Fig. 10. From this model, the denominator of $U_g$ is approximated as $g_0/R_{gs} + g_m/R_{gd\text{,total}}$. If $R_{gd\text{,total}}$ has a negative sign and its absolute value is smaller than $g_mR_{gs}/g_0$, then the denominator of $U_g$ becomes negative. We have used this revised small-signal model to estimate $f_{\text{max}}$. The value of $R_{gd\text{,total}}$ can be obtained from $\text{Re}(Y_{12}) = -R_{gd\text{,total}}$ in the equivalent circuit model. Fig. 11 plots measured and modeled RF gains and k at $V_{DS} = 0.9$ V with the addition of $R_{gd\text{-NDR}}$. Our model predicts the experimental gain characteristics and the k-factor very nicely, including the sharp peak in $U_g$. Using the model, we extrapolated a value of $f_{\text{max}} = 920$ GHz at $V_{DS} = 0.9$ V, which is a bit lower than that at $V_{DS} = 0.75$ V. This is likely due to the drop in $f_T$ that results from the increase in the drain delay as $V_{DS}$ increases.

To see how our devices stand out in comparison to other reports, Fig. 12 plots $f_{\text{max}}$ as a function of $f_T$ for our 50-nm device with $V_{DS} = 0.75$ V, as well as other reports including III-V HBTs and III-V HEMTs. Clearly, the device in this work exhibits a record value of $f_{\text{max}}$ for e-mode operation.

**Conclusions**

In summary, we have demonstrated for the first time 50-nm E-mode InGaAs PHEMTs on a 100-mm InP substrate with $f_{\text{max}} > 1$ THz. We have physically modeled the abnormal peaky behavior in $U_g$ at high values of $V_{DS}$ and successfully revised the small signal model by adding $R_{gd\text{-NDR}}$ with negative value. Without doing this, any attempt on $f_{\text{max}}$ extrapolation at high values of $V_{DS}$ could result in an over-estimation on its value.

**References**


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