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Thermal Considerations for Advanced SOI Substrates Designed for III-V/Si Heterointegration

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Silicon-on-Lattice Engineered Substrates (SOLES) are SOI substrates with embedded Ge layers that facilitate III-V compound integration for advanced integrated circuits. The new materials integration scheme in SOLES requires the analysis of its thermal stability and diffusion barrier properties. In this study, we report on the successful monolithic integration of CMOS/III-V transistors with a reduced CMOS thermal budget. We further investigated the ultimate thermal budget limits for the SOLES platform. We demonstrated a new SOLES structure incorporating a SiN$_x$ interlayer, which adds greater integration flexibility for future circuit applications.

Introduction

The SOLES platform, composed of a germanium layer buried under a silicon-on-insulator (SOI) structure [1], allows the monolithic integration of III-V devices with silicon CMOS technology. The Ge layer provides a suitable lattice constant that serves as a template on which III-V devices can be epitaxially deposited and processed while the surface silicon allows for standard CMOS processing techniques, providing for a truly monolithic III-V/Si integration scheme. AlInGaP LED arrays have been fabricated on the SOLES platform previously [2], establishing its viability for III-V device integration schemes. Here, we present thermal budget analyses (i.e., time-temperature studies) on SOLES variants to map out the process integration space for CMOS on SOLES. We also show that the SOLES platform can exhibit CMOS transistor performance equivalent to that on standard SOI, and can further support the fabrication of an advanced monolithically integrated III-V/Si differential amplifier.

SOLES thermal budget

The commercially available 100 mm SOLES used in this study were fabricated by SOITEC [3]. Cleaved pieces of the SOLES substrate were annealed at various temperatures for 8.5 hours (an approximate total thermal budget time for the CMOS process) to determine the maximum temperature for SOLES before mechanical failure. Because the melting temperature of Ge is 937°C, we performed anneals of 875°C, 900°C, 915°C and 935°C. No morphological changes in the SOLES wafers were seen in cross-sectional TEM for all anneals up to 915°C. Ge agglomeration and delamination occurred at 935°C (see Figure 1). SIMS profiling of Ge diffusion properties showed that a successful thermal budget could be established for the SOLES platform. Extended anneals at 915°C showed Ge diffusion and accumulation at the bonded (i.e., the SiO$_2$/ SiO$_2$) interfaces was exacerbated (see Figure 2). Diffusion of Ge in bulk silicon layer is slow at these temperatures, and therefore the top silicon layer acts as a diffusion barrier to Ge, limiting deleterious effects on CMOS devices.

A properly engineered process integration sequence led to the successful fabrication of InP/Si differential amplifier circuits. Figure 3 is an SEM image of the differential amplifier before final metallization, clearly showing the InP heterojunction bipolar transistors (HBTs) integrated with Si CMOS. Testing of the circuits showed no signs of effects from any mechanical instability or Ge diffusion, demonstrating that monolithic CMOS/III-V integration on SOLES is possible.

SOLES for higher thermal budget applications

Though the CMOS thermal budget can be adjusted to mitigate the effects of Ge diffusion, we also seek to increase the thermal budget of SOLES in order to achieve greater, and more universal, integration flexibility. It is desirable to introduce an additional diffusion barrier into the oxide stack, to intercept any Ge diffusion. Several approaches could be conceived.
to do so, but we believe that a dielectric layer inserted into the SiO$_2$ would be a simplest implementation. To this end, we tested the effect of inserting a SiN$_x$ interlayer in the SOLES structure to limit Ge diffusion without compromising mechanical integrity.

We fabricated the modified SOLES structures by starting with 100 mm, germanium-on-insulator (GeOI) wafers, the bottom half of SOLES, and then deposited various SiO$_2$/SiN$_x$ thin film stacks on the GeOI. We subjected the modified SOLES structures (minus the top Si layer) to anneals up to 915°C for 8.5h. The tensile-strained SiN$_x$, deposited by a Thermco 7000 series vertical thermal CVD reactor, effectively stopped Ge diffusion into the top oxide cap. As shown in Figure 4, Ge diffused through the thin SiO$_2$ immediately adjacent to the Ge layer; however, all the Ge diffusion was effectively stopped at the SiN$_x$ layer. Thus, we demonstrated the potential of SOLES variants containing embedded SiN$_x$ layers as potential improvements to the state-of-the-art, commercially available, SOLES technology.

Further work will explore integration of embedded GaAs into the SOLES platform. As the end-goal is III-V/Si integration, integrating a III-V material directly into the substrate is a logical next step. In addition, the higher melting point of GaAs, as compared to Ge, may accommodate higher thermal budgets.

**Conclusion**

The thermal budget/integration challenges for SOLES have been investigated. A process window has been found that allows for the successful demonstration of a monolithically integrated III-V/Si differential amplifier. A method of increasing the integration flexibility of SOLES by introducing SiN$_x$ interlayers has been demonstrated. Future work will explore the increased thermal budget/integration flexibility of SOLES provided by incorporating embedded GaAs layers.

**Acknowledgements**

This work was funded by the DARPA COSMOS program, ONR contract number N00014-07-C-0629, monitored by Dr. Harry Dietrich, and made use of MIT MTL and CMSE facilities. We would like to thank A. Pitera for valuable discussions.

**References**