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# SI-BASED UNRELEASED HYBRID MEMS-CMOS RESONATORS IN 32NM TECHNOLOGY

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## ABSTRACT

This work presents the first unreleased Silicon resonators fabricated at the transistor level of a standard CMOS process, and realized without any release steps or packaging. These unreleased bulk acoustic resonators are driven capacitively using the thin gate dielectric of the CMOS process, and actively sensed with a Field Effect Transistor (FET) incorporated into the resonant body. FET sensing using the high  $f_T$ , high performance transistors in CMOS amplifies the mechanical signal before the presence of parasitics. This enables RF-MEMS resonators at orders of magnitude higher frequencies than possible with passive devices. First generation CMOS-MEMS Si resonators with Acoustic Bragg Reflectors are demonstrated at 11.1 GHz with  $Q \sim 17$  and a total footprint of  $5\mu\text{m} \times 3\mu\text{m}$  using IBM's 32nm SOI technology.

## INTRODUCTION

### *To integrate or not to integrate...*

The question of direct integration of MEMS with CMOS is of constant debate across a wide range of systems and applications. Efforts directed toward monolithic integration have been motivated primarily by improved size, weight and power (SWaP), reduced parasitics from off-chip connections, and relaxed constraints on impedance matching[1]. However, the majority of electromechanical devices require custom fabrication including a release step to freely suspend the moving structures. This requires costly complex encapsulation methods and restricts MEMS-CMOS integration to back end-of-line (BEOL) processing [2]. Methods for monolithic integration of MEMS and CMOS in the past have focused on MEMS-first or MEMS-last processes. However the increased mask count, complexity and constraints on the process sequence, thermal budget and materials in these processes result in compromised performance, higher cost and reduced yield. Such custom MEMS processes cannot keep up with rapidly changing CMOS technology.

Development of unreleased Si-based MEMS resonators in CMOS as shown in this work overcomes these obstacles and allows for seamless integration into Front End of Line (FEOL) processing with no post-processing or special packaging (Fig. 1).

### *FET sensing for high frequency resonators*

Due to restricted material selection at the transistor level, electrostatic transduction is the optimal choice for low-power resonators fabricated in CMOS. However, *passive* electrostatic resonators are subject to a reduced dynamic range at higher frequencies, owing to high feed-through parasitics which make it difficult to detect RF and mm-wave signals. The authors have previously demonstrated the Resonant Body Transistor (RBT) which

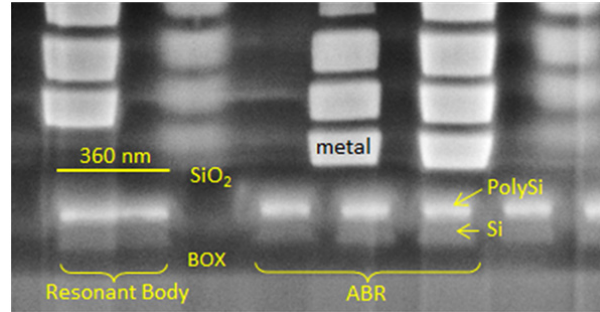


Figure 1: SEM of CMOS stack cross section showing resonator body and adjacent Acoustic Bragg Reflectors (ABRs) obtained using FIB. The device is formed in the SOI device layer, defined using Shallow Trench Isolation (STI), and in the PolySi gate layer.

addresses this obstacle by employing active FET sensing of acoustic vibrations [3]. The FET sensing mechanism allows for amplification of the mechanical signal before parasitics, enabling frequencies of operation previously inaccessible in electrostatic MEMS resonators. Using dielectric drive, RBTs have achieved up to 41 GHz acoustic resonance with  $f \cdot Q$  products in excess of  $10^{13}$  [4]. FET sensing has also been demonstrated using Si-based air-gap transducers up to 71 MHz [5] and in piezoelectrically driven GaN-based MEMS R-HEMTs up to 5 MHz [6].

Realization of the FET-sensed resonators in CMOS technology combines the benefits of a high efficiency sensing mechanism with high-performance transistors of CMOS technology, with major reduction in parasitic effects due to direct integration with surrounding circuitry.

## THE HYBRID CMOS-MEMS RESONATOR

The CMOS-MEMS resonators demonstrated in this work consist of longitudinal-mode bars driven electrostatically and sensed using a FET incorporated into the resonant body, as shown in Fig. 2. On the drive side, acoustic waves are actuated in the Si bar by superimposing DC and RF voltages  $V_A + v_{in}$  across the drive capacitor formed using the Si device layer, gate oxide, and gate polysilicon layers of the CMOS process. On the sense side, the FET is biased into saturation with DC gate and drain voltages,  $V_G$  and  $V_D$ , respectively. The body of the resonator is independently grounded from the source to minimize electrical feed-through. Acoustic resonance is detected in the Si bar through piezoresistive modulation of the drain current  $i_D = I_D + i_{out} e^{j\omega_0 t}$ . In Si, this piezoresistive sensing provides  $>10\times$  boost in transduction efficiency relative to electrostatic sensing. It also decouples the output signal from the input, reducing the effects of feed-through parasitics which can dominate in the GHz regime.

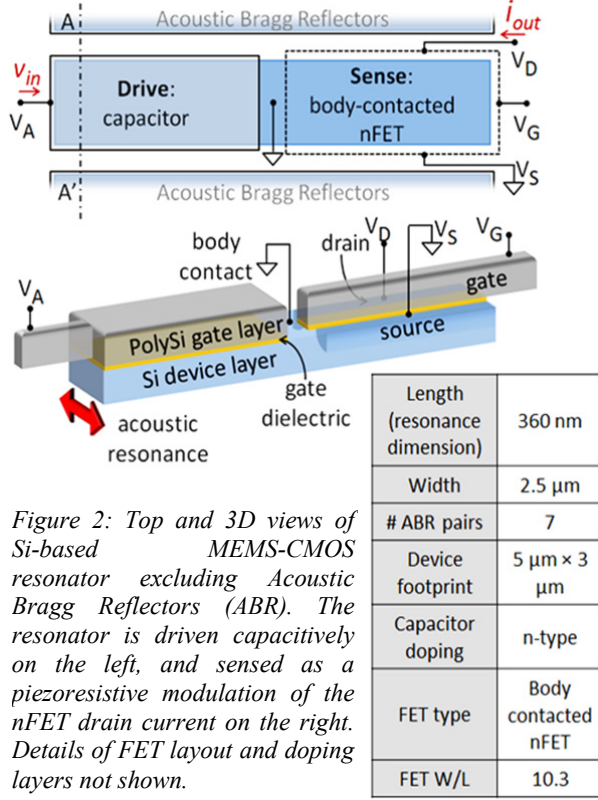


Figure 2: Top and 3D views of Si-based MEMS-CMOS resonator excluding Acoustic Bragg Reflectors (ABR). The resonator is driven capacitively on the left, and sensed as a piezoresistive modulation of the nFET drain current on the right. Details of FET layout and doping layers not shown.

### Design considerations

Design of the CMOS-MEMS resonator involves several geometry and doping modifications to the standard body-contacted analog nFET layout provided by the foundry. The size and shape of the active region and the number of contacts are changed to create longitudinal bar structures. Additional doping layers and Poly gate regions are added to these resonant structures to define acoustic geometry and electric contact for drive and sense.

The acoustic cavity of the unreleased resonator is defined by taking advantage of acoustic impedance mismatch between Si and surrounding materials. Shallow trench isolation (STI) is used to define alternating Si/SiO<sub>2</sub> regions at quarter-wavelength ( $\lambda/4$ ) intervals for the desired frequency (Fig. 3) [7] to generate acoustic Bragg reflectors (ABRs) in the direction of longitudinal resonance. The relative acoustic impedance between these materials is  $Z_{\text{rel}} = Z_{\text{Si}}/Z_{\text{SiO}_2} \sim 1.47$  and the reflection coefficient given by  $R = (Z_{\text{rel}} - 1)/(Z_{\text{rel}} + 1)$  asymptotically converges towards 1 with an increase in the number of ABRs. Considering the tradeoff of total device footprint vs. acoustic reflectivity (and therefore quality factor), these unreleased resonators are designed using 7 pairs of 1D ABRs which provide a reflectivity of 99.4% based on 1D analysis.

Design rule checking (DRC) restrictions of the CMOS process limited the spacing of the ABRs closest to the resonant cavity. To accommodate this rule, the first Bragg reflector is spaced  $3\lambda/4$  away from the resonator, as evident in Fig. 1. This results in a reduced solid angle to the ABRs from the structure which reduces reflection and quality factor in the resonator. It has yet to be determined if this design rule is necessary for FET operation.

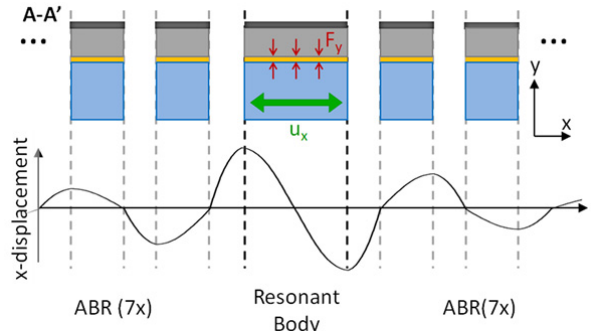


Figure 3: Acoustic mode shape in resonant cavity and surrounding Acoustic Bragg Reflectors (7 ABRs on each side) along A-A'. ABRs provide acoustic localization for the unreleased resonator, surrounded by SiO<sub>2</sub> on all sides.

### SMALL-SIGNAL MODELING

A small-signal equivalent circuit was developed for the hybrid CMOS-MEMS resonator by combining a traditional transistor pi-model with the RLC equivalent circuit of the bulk-acoustic resonator (Fig. 4). Unlike traditional 2-port resonators with passive transduction, the drive and sense for this resonator are not symmetric. To accommodate this, the RLC components defining the motional current  $i_{\text{in}}$  in the model are equivalent to those of a 1-port passive device, and determine the resonance frequency of the system.

The current  $i_{\text{in}}$  is proportional to the velocity of the acoustic mode and may be represented in terms of the driving DC voltage  $V_A$  and the amplitude of vibrations  $U_0$ , resonance frequency  $\omega_0$ , the drive capacitance  $C_0$ :

$$i_{\text{in}} = V_A \frac{dC_0}{dt} = \frac{2j\omega_0 V_A C_0 U_0}{L} \quad (1)$$

The electromechanical transconductance  $g_\alpha$  models the piezoresistive modulation of the DC drain current in the FET at resonance resulting in the AC output current  $i_{\text{out}}$ . This AC modulation of the output current is proportional to the mechanical strain in the channel and is hence in phase with the displacement  $U_0$ . For a piezoresistive coefficient  $\pi_{\text{Si}}$ , Young's modulus  $E_{\text{Si}}$  and mobility in the channel given by  $\mu$ , this may be written as:

$$i_{\text{out}} = \frac{\Delta\mu}{\mu} I_D \propto \pi_{\text{Si}} E_{\text{Si}} U_0 I_D \quad (2)$$

In the RLC mechanical circuit, the amplitude of vibrations is represented the voltage  $V_{C_m}$  across the motional capacitance  $C_m$ . At resonance, this voltage defines the dynamic range of the output current, through a voltage dependent current source with electromechanical transconductance  $g_\alpha$  given by:

$$g_\alpha = \frac{i_{\text{out}}}{V_{C_m}} = \frac{i_{\text{out}}}{i_{\text{in}}} j\omega_0 C_m \quad (3)$$

To assess the transduction efficiency of FET-sensing relative to passive electrostatic sensing, one can look at the effective motional impedance of the active resonator as:

$$\frac{v_{\text{in}}}{i_{\text{out}}} = \frac{v_{\text{in}}}{i_{\text{in}}} \frac{i_{\text{in}}}{i_{\text{out}}} = j \frac{\omega_0 R_m C_m}{g_\alpha} \quad (4)$$

The signal floor is limited by drive electrode feed-through modeled by  $g_\beta$ .

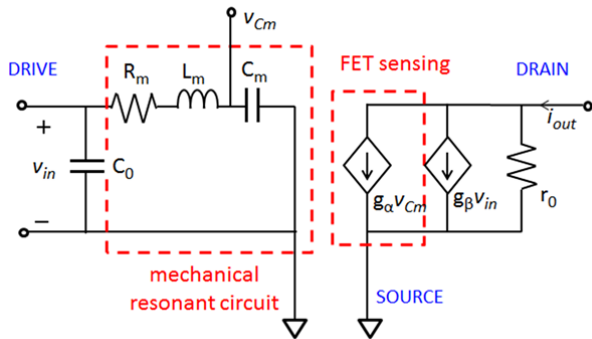


Figure 4: Small-signal model of the 2-port CMOS-MEMS resonator composed of a 1-port RLC mechanical component and an active FET sensing component. The electromechanical transconductance  $g_\alpha$  models the drain current modulation due to piezoresistance. The signal floor is limited by parasitic drive electrode transconductance  $g_\beta$ .

## EXPERIMENTAL RESULTS

The hybrid CMOS-MEMS resonators are tested in a standard two-port configuration in a Cascade PMC200 RF probe system. All measurements are performed at room temperature under  $N_2$  purge to prevent electrostatic discharge (ESD).

In operation, the drive capacitor is biased at  $V_A = 0.5$  V while the FET is biased at a drain voltage  $V_D = 0.6$  V and gate voltage  $V_G = 0.4$  V. Despite modification of the body-contacted NFET layout provided by the foundry, the altered FETs exhibit characteristic DC behavior and show no DC dependence on drive voltage  $V_A$  (Fig. 5).

Standard SOLT calibration is used to de-embed the test setup up to the probe tips. This is followed by open and short structures defined in the CMOS die to de-embed the large probe pads and routing down to the lowest metal layer of each device. RF measurements are taken with -21.9 dBm input power, no averaging, and a 30Hz IF BW using an Agilent PNA-X N5245A. After de-embedding the probe-pads and routing, the electromechanical transconductance  $g_\alpha$  is extracted from the Y-parameters as  $g_\alpha = Y_{21} - Y_{12}$ .

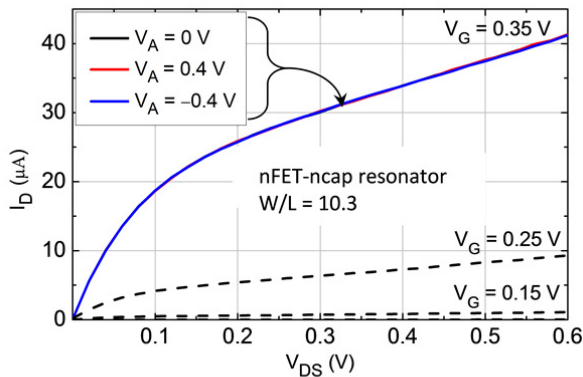


Figure 5: DC response of device with n-type drive and nFET sense (nFET-ncap). DC characteristics are unaffected by the bias voltage on drive capacitor ( $V_A$ ).

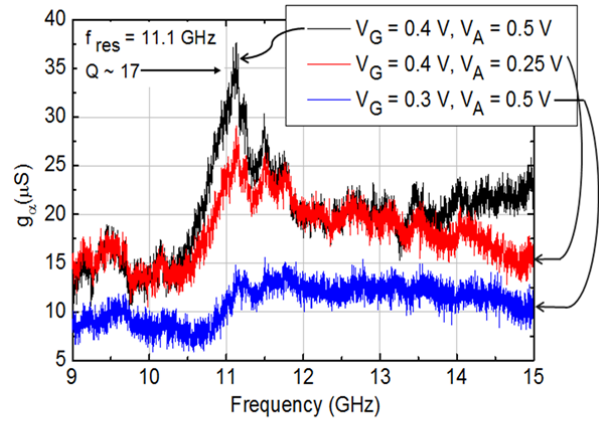


Figure 6: Frequency response of an 11.1 GHz nFET-ncap resonator showing transconductance  $g_\alpha$  and phase under multiple biasing conditions of the drive voltage ( $V_A$ ) and gate voltage ( $V_G$ ).

The frequency response of an 11.1 GHz resonator is shown in Fig. 6. The amplitude of the resonance peak changes for different values of the DC drive voltage  $V_A$ , verifying the mechanical nature of the resonance. The response for the lower FET gate voltage  $V_G$  of 0.3 V corresponds to a small FET amplification factor  $g_\alpha$  resulting in an indistinguishable resonance peak with respect to the feed-through. The DC power consumed at the operating point is 35  $\mu$ W. The device exhibits a  $Q$  of 17 with a total footprint of  $3 \mu\text{m} \times 5 \mu\text{m}$ .

It is important to note that certain acoustic properties of the FEOL stack were unknown or could not be shared by the foundry. Several processing parameters, including STI fill, silicide, stress liners, and metal contacts to Si [8] contribute substantially to the effective acoustic velocity and stress distribution in the resonator and surrounding ABRs. The resonator is designed to operate in a 1D longitudinal mode at 12 GHz assuming Si and  $\text{SiO}_2$  in and around the resonant cavity. The altered acoustic properties of the resonator result in degraded performance of the ABRs, which are also designed for 12 GHz but are not subject to all the same FET processing steps as the resonator body. This resonator-ABR mismatch alters the resonance frequency, amplitude of vibrations, quality factor, and presence of spurious modes.

Additionally, the metal stack directly above the resonant cavity as seen in Fig. 1 has a strong impact on the eigenmodes of the resonator. The metal layers seen above the resonator were not designed for but were generated as part of the CMP fill of the CMOS process. The high acoustic mismatch between the dielectric fill and low-level metals (e.g.  $Z_{\text{Cu}}/Z_{\text{SiO}_2} = 2.45$ ) results in acoustic reflections in the thickness direction. This thickness coupling results in spurious modes near the targeted frequency. The CMP fill can be excluded from the process in localized areas, eliminating this effect in future designs. Alternatively, the metal layers above the resonant structure can be designed to provide 3D ABRs for improved quality factor and reduction of spurious modes.

To characterize the effect of Bragg reflectors and material properties on device performance, ABR geometries were designed for +5% offset (ABR 1.05) and

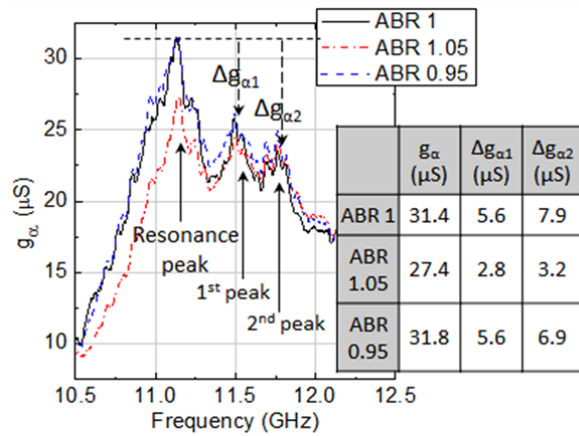


Figure 7: Comparison of three identical resonators with ABRs designed for the resonance frequency (ABR 1), 5% higher frequency (ABR 1.05) and 5% lower frequency (ABR 0.95). The resonator with ABRs designed at the resonance frequency shows best performance for  $g_\alpha$  and spurious mode suppression.

-5% offset (ABR 0.95) from the resonator frequency for a fixed resonator geometry. ABRs show a clear effect on both the amplitude of the resonance peak  $g_\alpha$  and suppression of the 1<sup>st</sup> and 2<sup>nd</sup> spurious modes with respect to the resonance peak,  $\Delta g_{\alpha 1}$  and  $\Delta g_{\alpha 2}$  (Fig. 7) as predicted by theory [7].

Resonators using capacitive drive and sense in IBM's 32nm process were also measured to compare the performance of active FET sensing to that of passive electrostatic sensing. Measurements of passive Si bar resonators driven and sensed with p-doped capacitors showed no discernible resonance peaks due to large feed-through signal at 12 GHz. This highlights the importance of FET sensing in 2-port MEMS resonators at multi-GHz frequencies.

## CONCLUSION

The first hybrid RF CMOS-MEMS resonators are demonstrated at 11.1 GHz with a  $Q$  of 17 in Si at the transistor level of IBM's 32nm SOI CMOS process with no need for any post-processing or packaging. They present the first step toward monolithically integrated RF MEMS building blocks for frequency sources and signal processors for wireless communications, microprocessor clocking, navigation and sensing applications.

Material properties of the composite CMOS stack extracted from measurement of these devices can be used to optimize resonator design for resonance frequency, quality factor, and spurious mode suppression in future designs. Metal layers above the resonant cavity can be effectively used to create 3-D Acoustic Bragg Reflectors for excellent suppression of spurious modes and  $Q$  enhancement.

The FET-based sensing demonstrated in these resonators leverages the excellent transistor performance, high yield, and cutoff frequency optimized for cutting-edge CMOS technology. Seamless integration of MEMS resonators into a standard CMOS process eliminates the complexity of custom MEMS fabrication processes, leveraging the high yield and rapid turnover of CMOS foundries to design low cost, small scale, low power devices. The fabrication of resonators side-by-side with CMOS circuitry greatly reduces parasitics of off-chip access, constraints of limited IO, and power consumption associated with impedance matching networks. These benefits result in increased system speed and dynamic range, particularly at RF and mm-wave frequencies of operation.

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