High Performance Mixed Signal Circuits Enabled by the Direct Monolithic Heterogeneous Integration of InP HBT and Si CMOS on a Silicon Substrate

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High Performance Mixed Signal Circuits Enabled by the Direct Monolithic Heterogeneous Integration of InP HBT and Si CMOS on a Silicon Substrate

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Abstract—In this work we present recent results on the direct heterogeneous integration of InP HBTs and Si CMOS on a silicon template wafer or SOLES (Silicon On Lattice Engineered Substrate). InP HBTs whose performance are comparable to HBTs on the native InP substrates have been repeatedly achieved. 100% heterogeneous interconnect yield has been achieved on daisy chain test structures with CMOS-InP HBT spacing (interconnect length) as small as 2.5µm. In DARPA COSMOS Phase 1 we designed and fabricated a differential amplifier that met the program Go/NoGo metrics with first pass design success. As the COSMOS Phase 2 demonstration vehicle we designed and fabricated a low power dissipation, high resolution, 500MHz bandwidth digital-to-analog converter (DAC).

Keywords—CMOS integrated circuits, Heterojunction bipolar transistors, Indium Phosphide, Monolithic integrated circuits, Silicon

I. INTRODUCTION

As silicon technology is scaled to shorter dimensions and higher frequency operation, silicon integrated circuits (ICs) are beginning to be used in applications traditionally served by III-V compound semiconductors (e.g., microwave/millimeter-wave amplifiers, high-frequency mixed signal ICs and data converters). However, while silicon-based ICs clearly provide more cost-effective solutions and increased integration density, they exhibit significant performance limitations when compared to III-V based ICs. Because of the superior transport properties of III-V materials, III-V devices offer higher gain, efficiency, bandwidth and dynamic range/linearity, and lower noise characteristics and RF loss at relaxed geometries than silicon based devices.

As a result the future of integrated circuits will include the integration of high performance III-V electronic and/or optoelectronic devices with standard Si CMOS. While traditional hybrid approaches, such as wire bonded or flip chip multi-chip assemblies (see Fig. 1, left), may provide short term solutions, the variability, losses and size of the interconnects and the limitation in the placement of III-V devices relative to CMOS transistors limit the performance, utility, size, and cost of these approaches. A more attractive approach is the direct integration of Si CMOS and III-V devices on a common silicon substrate (COMpound Semiconductor Material On Silicon - COSMOS) (Fig. 1, right). In this way circuit performance can be optimized by the strategic placement of high performance III-V devices adjacent to Si CMOS transistors and cells, and the devices and subcircuits can be interconnected using standard semiconductor on-wafer interconnect processes.

Figure 1. Traditional hybrid assembly (left) and direct monolithic integration of III-V devices and silicon CMOS (right).

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In this paper recent progress on the direct heterogeneous integration of InP HBTs and Si CMOS on a silicon substrate are presented. The process is analogous to the SiGe BiCMOS and is essentially a III-V BiCMOS process. As the COSMOS Phase 1 demonstration vehicle, a high-speed, low-power-dissipation differential amplifier, which serves as the basic building block for high-performance mixed-signal circuits such as ADCs and DACs, was designed and fabricated. In COSMOS Phase 2, the technology is being used to design and fabricate a low power dissipation (1.6W), high resolution (13 bit, > 78 dB spur free dynamic range (SFDR)), 500MHz bandwidth digital-to-analog converter (DAC).

II. RESULTS AND DISCUSSION

Our direct integration approach is based on a unique “engineered” silicon substrate which is similar to a standard SOI wafer. The SOLES (Silicon-on-Lattice Engineered Substrate), invented at MIT [1,2] and manufactured by SOITEC using their Smart-Cut™ Process [3,4], contains a buried III-V template layer that enables the direct growth of high quality III-V epitaxial material in windows directly on the silicon substrate (Fig. 2). At present the buried III-V template layer is Ge, although the substrate fabrication process is compatible with GaAs or InP template layers as well. SOLES have been successfully scaled to 200mm diameter wafers and are compatible with and can be readily inserted into a standard silicon CMOS foundry.

While our main efforts have focused on the fabrication of InP HBTs on SOLES, the approach is equally applicable to other III-V electronic (FETs, HEMTs) and opto-electronic (photodiodes, VSCLS) devices. The process flow is similar to a SiGe BiCMOS process flow: 1) Si CMOS device fabrication; 2) HBT epitaxial growth and device fabrication; 3) multilayer interconnect fabrication. In our approach, after the completion of CMOS device fabrication, windows are lithography defined and etched into the SOLES wafer to reveal the III-V template layer. Since the III-V growth windows are defined as part of the CMOS fabrication process, the III-V epitaxial material can be grown selectively and arbitrarily across the substrate as required for the particular circuit or applications. Figure 3 shows an example of a SEM image of a completed InP HBT in close proximity to a CMOS transistor prior to interconnect formation. A detailed report on the growth of high quality InP HBT epitaxial material in windows on SOLES has been previously published [5]. The electrical performance of InP HBTs fabricated on SOLES is comparable to HBTs grown directly on native InP substrates [6]. Figure 4 shows the small signal parameters of a 0.5 x 5 um² emitter HBT grown in a 15 x 15 um² window on a SOLES substrate. Gain (beta), \( f_t \) and \( f_{max} \) of 40, > 200GHz and > 200GHz, respectively, are achieved.

To facilitate the interconnecting of the III-V devices and CMOS transistors, the thickness of the III-V epitaxial layers and depth of the windows are optimized such that the III-V devices and CMOS transistors are planar. With this truly planar approach, 100% heterogeneous interconnect yield has been achieved on daisy chain test structures with CMOS-InP HBT spacing (interconnect length) as small as 2.5um (Fig. 5).

Initial circuit demonstrations were based on 1.2um CMOS and 2um emitter InP HBTs on 100mm diameter SOLES wafers. To facilitate circuit design, a design kit (consisting of CMOS, HBT and Interconnect models, design rules, DRC and LVS) was created and used to design the differential amplifier circuit shown in Figure 6 (COSMOS Phase 1 demonstration circuit). In addition to the core differential amplifier, the
circuit contains a bias circuit and all HBT output buffer. (The role of the output buffer is to attenuate the output of the core differential amplifier to facilitate the characterization of the differential amplifier.) Because of our truly monolithically integrated, planar approach we were able to include multiple differential amplifier design variants within a reticle on a wafer, effectively creating a design optimization design of experiments (DOE) within the reticle. 4-port S-parameter measurements were made to determine the low frequency amplifier gain and unity-gain bandwidth of the differential amplifier. The differential amplifier core was biased at a $V_{ss} = 6V$ and $I_{ss} = 14mA$ ($P_{diss} = 84mW$). Typical differential amplifiers exhibited a peak low frequency gain of 550V/V, a unity-gain frequency of 20 GHz, a voltage swing of 7.5V and a measured slew rate a measured slew rate of $1.25\times10^7$ V/µsec. From the DC-gain measurement, the DC-gain*unity gain bandwidth product is measured to be $1.1\times10^4$ V/V GHz. The differential amplifiers exceeded the DARPA COSMOS Phase 1 performance metrics with first pass design success. Differential amplifiers step and repeated across a 100mm diameter SOLES wafer showed very good yield and uniformity highlighting the manufacturability of our approach. Details on the differential amplifier have been previously reported [7, 8].

As the COSMOS Phase 2 demonstration vehicle, we designed a low power dissipation (1.6W), high resolution (13 bit, > 78 dB spur free dynamic range (SFDR)), 500MHz bandwidth digital-to-analog converter (DAC) (Fig. 7). The DAC uses a return to zero (RZ), current steering (Current-Source-Switch or CSS) architecture and contains on-chip static calibration circuitry. The simulated performance of the DAC is shown in Figure 8. The DAC uses 1.2 µm CMOS and contains over 14,000 silicon CMOS transistors heterogeneously integrated with over 1100 InP HBTs. The DAC is currently being fabricated. More details on the DAC design and performance will be presented in a later work.

With the successful scaling of SOLES to 200mm diameter wafers, we have scaled our monolithic integration approach to more cutting edge CMOS technology and the design kit has been updated to include 180nm CMOS. A 180 nm CMOS version of the DAC has recently been designed and is being fabricated. The new DAC design contains both on-chip static and dynamic calibration circuitry in the same footprint as the 1.2µm CMOS version of the DAC.

III. SUMMARY

In this work we presented an overview of the Raytheon approach to the direct monolithic integration of III-V devices (InP HBTs) and Si CMOS on a common silicon substrate.
(SOLES). The COSMOS Phase 2 DAC is a building block for other types of high speed, high dynamic range, low power dissipation converter circuits including Analog Digital Converters (ADCs) and Direct Digital Synthesizers (DDSs). The next step is to integrate these mixed signal converter circuits with RF transistors (HEMTs and HBTs) to enable single chip Digital Transceivers and Dynamically Reconfigurable Circuits as well as compact circuit elements for Low Cost Panel Arrays.

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REFERENCES


[4] Smart-Cut™ is a registered trademark of Soitec.


