$L_{g}=60\text{nm}$ recessed In$_{0.7}$Ga$_{0.3}$As metal-oxide-semiconductor field-effect transistors with Al$_{2}$O$_{3}$ insulator.
Lg = 60 nm recessed In0.7Ga0.3As metal-oxide-semiconductor field-effect transistors with Al2O3 insulator

D.-H. Kim,1,a) J. A. del Alamo,2 D. A. Antoniadis,2 J. Li,3 J.-M. Kuo,3 P. Pinsukanjana,3 Y.-C. Kao,3 P. Chen,1 A. Papavasiliou,1 C. King,1 E. Regan,1 M. Urteaga,1 B. Brar,1 and T.-W. Kim4,a)
1Teledyne Scientific Company, Thousand Oaks, California 91360, USA
2Microsystmes Technology Laboratories, MIT, Cambridge, Massachusetts 02139, USA
3Intelligent Epitaxy Technology, Richardson, Texas 75081, USA
4SEMATECH, Austin, Texas 78741, USA

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In this Letter, we report on sub-100 nm recessed In0.7Ga0.3As metal-oxide-semiconductor field-effect transistors (MOSFETs) with outstanding logic and high-frequency performance. The device features ex-situ atomic-layer-deposition (ALD) 2-nm Al2O3 layer on a molecular-beam-epitaxy (MBE) 1-nm InP layer and is fabricated through a triple-recess process. An Lg = 60 nm MOSFET exhibits on-resistance (R_ON) = 220 Ω·μm, subthreshold-swing (S) = 110 mV/decade, and drain-induced-barrier-lowering (DIBL) = 200 mV/V at V_DS = 0.5 V, together with enhancement-mode operation. More importantly, this device displays record maximum transconductance (g_m_max = 2000 μS/μm and current-gain cutoff frequency (f_T) = 370 GHz at V_DS = 0.5 V, in any III-V MOSFET technology.

The increasing difficulty in shrinking Si complementary-metal-oxide-semiconductor (CMOS) transistor footprint while managing power consumption and extracting improved performance threatens to bring Moore’s law to a halt. At its heart, the problem is the need to reduce operating voltage and the difficulty of obtaining sufficient drain current drive. A solution to this problem appears in the use of certain III-V compound semiconductors, which are endowed with very high electron mobilities and thermal velocities (Ref. 1 and references therein). Transistors with record high frequency characteristics have been demonstrated.2 Recently, these materials have also shown great promise for a next-generation ultra-low power and high density III-V CMOS logic technology. In the last few years, there has been impressive progress in improving the quality of high-k dielectric/channel interfaces in III-V metal-oxide-semiconductor field-effect transistors (MOSFETs) by atomic-layer-deposition (ALD).3–5 This makes this technology promising for future scaled III-V CMOS devices. A critical problem that has received little attention in these transistors is the source and drain resistance (R_S and R_D). In order to achieve the desired transistor I_ON/I_OFF ratio, sufficiently low R_S and R_D is essential, especially as L_g scales down to the 10 nm regime. This is especially challenging while managing short-channel effects. To date, the best III-V MOSFET features on-resistance (R_ON) = 440 Ω·μm, maximum transconductance (g_m_max) = 1750 μS/μm and subthreshold-swing (S) = 100 mV/dec at V_DS = 0.5 V.3 In this paper, we scale beyond this result and demonstrate L_g = 60 nm In0.7Ga0.3As quantum-well MOSFETs with an equivalent-oxide-thickness (EOT) = 1.2 nm Al2O3/InP composite insulator fabricated through a triple-recess process that yields a very tight side recess spacing. Our enhancement-mode devices exhibit record g_m_max > 2000 μS/μm and current-gain cutoff frequency (f_T) of 370 GHz of any III-V MOSFET. These are accomplished while maintaining excellent short-channel effects, manifested by S = 110 mV/dec at V_DS = 0.5 V. Our work demonstrates the promising potential of III-V MOSFETs for future CMOS logic and sub-millimeter wave applications.

Figure 1(a) shows a cross section of our device structure. From top to bottom, the epitaxial layer structure consists of a heavily doped multi-layer cap (In0.53Ga0.47As/InP/In0.52Al0.48As), 1-nm InP barrier, 10-nm In0.7Ga0.3As channel, 5-nm In0.52Al0.48As spacer, Si δ-doping, and 300-nm In0.52Al0.48As back-barrier on an InP substrate. The measured electron Hall mobility (μ_Hall) is 8000 cm²/V s with n_Hall = 1 × 10¹²/cm² at room temperature, after removal of the heavily doped cap layers.

Device fabrication is somewhat similar to that of conventional high-electron-mobility transistors (HEMTs),8 except for the deposition of a gate oxide prior to gate metal formation. It begins with mesa isolation and non-alloyed S/D ohmic contact with 1 μm spacing. After 20 nm SiO2 deposition by PECVD, a fine gate pattern using a single-layer ZEP-520 A is defined by e-beam lithography. This is transferred to the passivating SiO2 layer by CF4 plasma. Following this, we carry out a triple-recess process, as in Ref. 8. Immediately after removing the e-beam resist, 2-nm of Al2O3 is deposited by ALD at 250°C. Finally, Pal/Au metal gate is formed. In this way, devices with L_g from 60 nm to 150 nm are fabricated. Figures 1(b) and 1(c) show a SEM image after triple-recess process, and a TEM image for the cross section of an L_g = 60 nm device with Al2O3 gate insulator, respectively. The TEM image also shows a tight control of the side recess spacing (L_side), which is around 5 nm on each side of the gate.

Figure 2(a) shows the output characteristics of representative In0.7Ga0.3As MOSFETs with L_g = 60 nm, 100 nm,
and 150 nm. The devices exhibit excellent pinch-off characteristics up to $V_{DS} = 0.5$ V, and a fairly small value of ON-resistance ($R_{ON}$) = 220 $\Omega \cdot \mu$m at $V_{GS} = 0.8$ V for the device with $L_g = 60$ nm. This is mainly the consequence of combining the proposed triple-recess process and the epi layer design with a multi-layer cap, which provides a tight control of the side-recess spacing ($L_{side}$ = 5 nm) on each side of the gate as can be observed in the TEM image of Fig. 1(c).

From transmission line method (TLM) measurements after S/D ohmic, we obtain a contact resistance ($R_c$) to the heavily doped cap of 15 $\Omega \cdot \mu$m and a sheet resistance ($R_{sh}$) of 50 $\Omega$/sq. This outstanding value of $R_{ON}$ yields a maximum transconductance ($g_{m, max}$) of 2000 $\mu$m/A at $V_{DS} = 0.5$ V, which is the highest $g_{m}$ reported in any III-V MOSFET.

Figure 2(b) shows subthreshold characteristics at $V_{DS}$ of 0.5 V, for $L_g = 60, 100$ and 150 nm devices. Using a definition for $V_T$ as the value of $V_{GS}$ that yields $I_D = 1$ mA/mm, the 60 nm device exhibits enhancement-mode operation with $V_T = 0.02$ V at $V_{DS} = 0.5$ V. More importantly, the device exhibits excellent short-channel effects as manifested by a subthreshold-swing (S) of 110 mV/dec and drain-induced-barrier-lowering (DIBL) of 200 mV/V at $V_{DS} = 0.5$ V. These numbers are comparable to the device in Ref. 3, which had $S = 100$ mV/dec and DIBL = 130 mV/V for $L_g = 75$ nm. In addition, we find that the gate leakage current ($I_{GLeak}$) is lower than 0.1 nA/$\mu$m at all the measured bias conditions, and that our device delivers $I_{ON} = 0.27$ mA/$\mu$m at an $I_{OFF} = 100$ nA/$\mu$m with $V_{DS} = 0.5$ V. In other words, an $I_{ON}/I_{OFF}$ ratio is easily in excess of $10^3$ in our devices, even with supply voltage of 0.5 V.

Microwave performance was characterized using a precision-network-analyzer (PNA) system with an off-wafer standard line-reflection-reflection-match (LRRM) calibration from 1 GHz to 50 GHz. We used on-wafer open and short structures to subtract pad capacitances and inductances from the measured device S-parameters. Figure 3 plots $|h_{21}|^2$, maximum-available-gain (MAG) and Mason’s unilateral-gain ($U_g$) against frequency from 1 to 50 GHz for a 60 nm gate length device with $W_G = 2 \times 20$ $\mu$m at $V_{GS} = 0.6$ V and $V_{DS} = 0.5$ V. In this particular measurement, values of $f_T = 370$ GHz and $f_{max} = 280$ GHz were, respectively, obtained by extrapolating $|h_{21}|^2$ and $U_g$ with a slope of $-20$ dB/decade using a least-squares fit. The value of $f_T$ in our device was also verified by Gummel’s approach (inset),9 yielding $f_T = 371$ GHz. This is the highest $f_T$ ever reported in any III-V MOSFET on any material system. In addition, it should be noted that the short-circuit current gain ($|h_{21}|^2$) keeps increasing with a $-20$ dB/decade slope as frequency decreases even with the positive gate bias of 0.6 V, unlike conventional HEMTs with Schottky gate. This is due to the
dramatic reduction of $I_G$ by using the Al$_2$O$_3$ dielectric layer, as shown in the inset of Fig. 2(b).

In order to assess the significance of our work, we have benchmarked our device against reported III-V MOSFETs. From a logic operation standpoint, what matters in the end is how to maximize current driving capability at low $V_{DS}$ while minimizing OFF-state current. As a result, both the transconductance ($g_m$) and subthreshold-swing ($S$) are of great importance, as proposed in Ref. 10. Figure 4 plots $g_{m,\text{max}}$ as a function of $S$, for the devices in this work, as well as reported III-V MOSFETs with planar architectures.$^{3,6,7,11-13}$ The subthreshold-swing that we have obtained in this work is among the best reported III-V MOSFET technologies, while our $g_{m,\text{max}}$ stands out against all of them.

Table I summarizes key device parameters for our devices in contrast with previously demonstrated $L_g = 75$ nm InGaAs MOSFET.$^3$ Our recessed In$_{0.7}$Ga$_{0.3}$As MOSFETs combine an outstanding $g_m$ and $R_{ON}$, together with excellent high-frequency response and short-channel effects down to $L_g = 60$ nm. This is mainly attributed to the triple-recess process that yields a very tight side-recess spacing ($L_{\text{side}} = 5$ nm) plus aggressive EOT scaling (EOT = 1.2 nm). This in turn suggests a very small interface density ($D_{it}$) below the conduction band edge, revealing that a composite dielectric stack of ALD grown Al$_2$O$_3$ and MBE-grown InP is very promising for future III-V MOSFET.

In conclusion, we have demonstrated $L_g = 60$ nm recessed In$_{0.7}$Ga$_{0.3}$As quantum-well MOSFETs with EOT = 1.2 nm. The devices exhibit excellent logic characteristics, such as $S = 110$ mV/dec and DIBL = 200 mV/V with E-mode operation. More significantly, our devices feature record performance for any III-V MOSFET technology in terms of $g_{m,\text{max}}$ and $f_T$. The outstanding performance that we demonstrate stems from the triple-recess fabrication process that yields a very tight side recess spacing, coupled with aggressive EOT scaling. Our work strongly reveals that with further device optimization in the form of self-aligned ohmic contacts, the proposed InGaAs MOSFETs with Al$_2$O$_3$ insulator could well become the technology of choice for sub-10 nm CMOS logic and THz applications.
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<th>$f_{max}$ [GHz]</th>
<th>$S$ [mV/dec.]</th>
<th>DIBL [mV/V]</th>
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