$L_{g} = 60\text{nm}$ recessed $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ metal-oxide-semiconductor field-effect transistors with $\text{Al}_{2}\text{O}_{3}$ insulator.

Citation

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The increasing difficulty in shrinking Si complementary-metal-oxide-semiconductor (CMOS) transistor footprint while managing power consumption and extracting improved performance threatens to bring Moore’s law to a halt. At its heart, the problem is the need to reduce operating voltage and the difficulty of obtaining sufficient drain current drive. A solution to this problem appears in the use of certain III-V compound semiconductors, which are endowed with very high electron mobilities and thermal velocities (Ref. 1 and references therein). Transistors with record high frequency characteristics have been demonstrated.2 Recently, these materials have also shown great promise for a next-generation ultra-low power and high density III-V CMOS logic technology. 

In this Letter, we report on sub-100 nm recessed In0.7Ga0.3As metal-oxide-semiconductor field-effect transistors (MOSFETs) with outstanding logic and high-frequency performance. The device features ex-situ atomic-layer-deposition (ALD) 2-nm Al2O3 layer on a molecular-beam-epitaxy (MBE) 1-nm InP layer and is fabricated through a triple-recess process. An $L_g = 60$ nm MOSFET exhibits on-resistance ($R_{ON}$) = 220 $\Omega \cdot \mu$m, subthreshold-swing ($S$) = 100 mV/decade, and drain-induced-barrier-lowering (DIBL) = 200 mV/V at $V_{DS} = 0.5$ V, together with enhancement-mode operation. More importantly, this device displays record maximum transconductance ($g_{m,max}$) = 2000 $\mu$S/($\mu$m and current-gain cutoff frequency ($f_T$) = 370 GHz at $V_{DS} = 0.5$ V, in any III-V MOSFET technology. © 2012 American Institute of Physics. [http://dx.doi.org/10.1063/1.4769230]
and 150 nm. The devices exhibit excellent pinch-off characteristics up to $V_{DS} = 0.5$ V, and a fairly small value of ON-resistance ($R_{ON} = 220 \Omega \cdot \mu m$) at $V_{GS} = 0.8$ V for the device with $L_g = 60$ nm. This is mainly the consequence of combining the proposed triple-recess process and the epi layer design with a multi-layer cap, which provides a tight control of the side-recess spacing ($L_{side} = 5$ nm) on each side of the gate as can be observed in the TEM image of Fig. 1(c).

From transmission line method (TLM) measurements after S/D ohmic, we obtain a contact resistance ($R_c$) to the heavily doped cap of $15 \Omega \cdot \mu m$ and a sheet resistance ($R_{sh}$) of $50 \Omega/sq$. This outstanding value of $R_{ON}$ yields a maximum transconductance ($g_{m, max}$) of $2000 \mu A/\mu m$ at $V_{DS} = 0.5$ V, which is the highest $g_{m}$ reported in any III-V MOSFET.

Figure 2(b) shows subthreshold characteristics at $V_{DS}$ of 0.5 V, for $L_g = 60, 100$ and 150 nm devices. Using a definition for $V_T$ as the value of $V_{GS}$ that yields $I_{D}$ = 1 mA/mm, the 60 nm device exhibits enhancement-mode operation with $V_T = 0.02$ V at $V_{DS} = 0.5$ V. More importantly, the device exhibits excellent short-channel effects as manifested by a subthreshold-swing (S) of 110 mV/dec and drain-induced-barrier-lowering (DIBL) of 200 mV/V at $V_{DS} = 0.5$ V. These numbers are comparable to the device in Ref. 3, which had $S = 100$ mV/dec and DIBL = 130 mV/V for $L_g = 75$ nm. In addition, we find that the gate leakage current ($I_{G}$) is lower than 0.1 nA/µm at all the measured bias conditions, and that our device delivers $I_{ON} = 0.27$ mA/µm at an $I_{OFF} = 100$ nA/µm with $V_{DS} = 0.5$ V. In other words, an $I_{ON}/I_{OFF}$ ratio is easily in excess of $10^3$ in our devices, even with supply voltage of 0.5 V.

Microwave performance was characterized using a precision-network-analyzer (PNA) system with an off-wafer standard line-reflection-reflection-match (LRRM) calibration from 1 GHz to 50 GHz. We used on-wafer open and short structures to subtract pad capacitances and inductances from the measured device S-parameters. Figure 3 plots $|h_{21}|^2$, maximum-available-gain (MAG) and Mason’s unilateral-gain ($U_g$) against frequency from 1 to 50 GHz for a 60 nm gate length device with $W_G = 2 \times 20 \mu m$ at $V_{GS} = 0.6$ V and $V_{DS} = 0.5$ V. In this particular measurement, values of $f_T = 370$ GHz and $f_{max} = 280$ GHz were, respectively, obtained by extrapolating $|h_{21}|^2$ and $U_g$ with a slope of −20 dB/decade using a least-squares fit. The value of $f_T$ in our device was also verified by Gummel’s approach (inset), yielding $f_T = 371$ GHz. This is the highest $f_T$ ever reported in any III-V MOSFET on any material system. In addition, it should be noted that the short-circuit current gain ($|h_{21}|^2$) keeps increasing with a −20 dB/decade slope as frequency decreases even with the positive gate bias of 0.6 V, unlike conventional HEMTs with Schottky gate. This is due to the
dramatic reduction of $I_G$ by using the Al$_2$O$_3$ dielectric layer, as shown in the inset of Fig. 2(b).

In order to assess the significance of our work, we have benchmarked our device against reported III-V MOSFETs. From a logic operation standpoint, what matters in the end is how to maximize current driving capability at low $V_{DS}$ while minimizing OFF-state current. As a result, both the transconductance ($g_m$) and subthreshold-swing ($S$) are of great importance, as proposed in Ref. 10. Figure 4 plots $g_{m,\text{max}}$ as a function of $S$, for the devices in this work, as well as reported III-V MOSFETs with planar architectures.\textsuperscript{3,6,7,11–13} The subthreshold-swing that we have obtained in this work is among the best reported III-V MOSFET technologies, while our $g_{m,\text{max}}$ stands out against all of them.

Table I summarizes key device parameters for our devices in contrast with previously demonstrated $L_g = 75$ nm InGaAs MOSFET.\textsuperscript{3} Our recessed In$_{0.7}$Ga$_{0.3}$As MOSFETs combine an outstanding $g_m$ and $R_{ON}$, together with excellent high-frequency response and short-channel effects down to $L_g = 60$ nm. This is mainly attributed to the triple-recess process that yields a very tight side-recess spacing ($L_{\text{side}} = 5$ nm) plus aggressive EOT scaling (EOT = 1.2 nm). This in turn suggests a very small interface density ($D_{it}$) below the conduction band edge, revealing that a composite dielectric stack of ALD grown Al$_2$O$_3$ and MBE-grown InP is very promising for future III-V MOSFET.

In conclusion, we have demonstrated $L_g = 60$ nm recessed In$_{0.7}$Ga$_{0.3}$As quantum-well MOSFETs with EOT = 1.2 nm. The devices exhibit excellent logic characteristics, such as $S = 110$ mV/dec and DIBL = 200 mV/V with E-mode operation. More significantly, our devices feature record performance for any III-V MOSFET technology in terms of $g_{m,\text{max}}$ and $f_T$. The outstanding performance that we demonstrate stems from the triple-recess fabrication process that yields a very tight side recess spacing, coupled with aggressive EOT scaling. Our work strongly reveals that with further device optimization in the form of self-aligned ohmic contacts, the proposed InGaAs MOSFETs with Al$_2$O$_3$ insulator could well become the technology of choice for sub-10 nm CMOS logic and THz applications.
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<th>Lg [nm]</th>
<th>EOT [nm]</th>
<th>R_DON [Ω·μm]</th>
<th>f_m_max [μs/μm]</th>
<th>f_T [GHz]</th>
<th>S [mV/dec.]</th>
<th>DIBL [mV/V]</th>
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<tr>
<td>InGaAs MOSFET (This work)</td>
<td>60</td>
<td>1.2</td>
<td>220</td>
<td>2000</td>
<td>370</td>
<td>110</td>
<td>200</td>
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<tr>
<td>InGaAs MOSFET (Ref. 3)</td>
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<td>2.2</td>
<td>440</td>
<td>1750</td>
<td>N/A</td>
<td>100</td>
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