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<td>Nature Publishing Group</td>
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Electronic transport and device prospects of monolayer molybdenum disulphide grown by chemical vapor deposition

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Layered transition metal dichalcogenides display a wide range of attractive physical and chemical properties and are potentially important for various device applications. Here we report the electronic transport and device properties of monolayer molybdenum disulphide (MoS2) grown by chemical vapor deposition (CVD). We show that these devices have the potential to suppress short channel effects and have high critical breakdown electric field. However, our study reveals that the electronic properties of these devices are at present, severely limited by the presence of a significant amount of band tail trapping states. Through capacitance and ac conductance measurements, we systematically quantify the density-of-states and response time of these states. Due to the large amount of trapped charges, the measured effective mobility also leads to a large underestimation of the true band mobility and the potential of the material. Continual engineering efforts on improving the sample quality are needed for its potential applications.

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Introduction

Two-dimensional materials are attracting considerable attention due to their unique electronic, optical, and mechanical properties\(^1\). Following the success of graphene, a group of 2D materials known as the transition metal dichalcogenides (TMD) has begun to garner attention. Among them, molybdenum disulfide (MoS\(_2\)) is probably one of the most explored TMDs\(^2,3\). The sizeable (1.8 eV) direct bandgap of monolayer MoS\(_2\)\(^4\) makes it a potential material for not only digital electronics, but numerous photonic applications such as light emitters\(^5\), photodetectors\(^6,7\), and solar cells\(^8\). Excellent mechanical flexibility of MoS\(_2\) also makes it a compelling semiconducting material for flexible electronics\(^9,10\).

Most existing studies and device demonstrations were performed on exfoliated MoS\(_2\) flakes\(^11-19\). In particular, field-effect-transistors based on monolayer MoS\(_2\) was found to exhibit high on/off ratios of ~10\(^8\), steep subthreshold swing of ~70 mV/dec\(^18,20\), with reported electron effective mobility ranging from 1 cm\(^2\)/Vs to 480 cm\(^2\)/Vs\(^14,17,20-26\) depending on the device structures, dielectric environment and processing\(^21,27\). These encouraging early reports coupled with continual engineering efforts\(^28\), present a compelling case for monolayer MoS\(_2\) as an alternative to traditional organic material or amorphous silicon for low-end applications with basic requirement of an effective mobility of > 30 cm\(^2\)/Vs\(^20\) e.g. high resolution displays and photodetection\(^6,7\).

Recently, the advent of mass production technologies has enabled scalable growth of polycrystalline monolayer MoS\(_2\) by chemical vapor deposition (CVD)\(^29-32\), hence providing a commercially viable path towards MoS\(_2\) electronics at low cost\(^33\). However, the mobility of CVD MoS\(_2\) is typically much lower than its exfoliated counterpart, with
reported values in the range of 5 to 22 cm$^2$/Vs \(^{34-36}\). The physical origin of the differences between CVD and exfoliated MoS$_2$ are not clear at present, however, structural defects \(^{37}\) such as vacancies, dislocations, grain boundaries as well as charged interfacial states due to the dielectrics in contact \(^{14}\) can be responsible for the degradation in mobility. Although this problem has presented a major hurdle to the realization of wafer-scale MoS$_2$ electronics and photonics, systematic studies of it are very few\(^ {35}\). Very recently, the MoS$_2$ community realized that there technical difficulties to accurate mobility extraction, due to the role of contacts and fringing capacitive contributions \(^{38}\). Four-terminal Hall effect measurements are more accurate, but have only been demonstrated at very high carrier densities using a electrolyte gating scheme \(^{26}\), or at very low temperatures \(^{17}\). These Hall measurements were all performed on exfoliated MoS$_2$, and will be more challenging to perform in CVD samples due to significantly larger amount of localized states, as will be discussed in this manuscript.

In this paper, we present a systematic methodology for characterizing electronic properties of scalable CVD MoS$_2$, reporting also the presence of significant amounts of band tail states and their profound impact on the electrical device performance. The density distribution and dynamics of these trap states of CVD MoS$_2$ are characterized through systematic capacitance and ac conductance measurements. Extraction of basic electronic transport quantities like the mobility edge and effective mobility are performed using four-probe current measurements. Complementary modeling allows us to draw insights into relevant device quantities such as the fractional occupation of band and trap states, band mobility and the anomalous sub-threshold slope. Lastly, high field electrical
behavior such as drain-induced barrier lowering and critical breakdown fields are examined.

**Results**

**Characterization of monolayer CVD MoS$_2$**

Monolayer MoS$_2$ were synthesized by CVD, using solid sulfur (S) and molybdenum oxide (MoO$_3$) as the precursors and perylene-3,4,9,10-tetracarboxylic acid tetra-potassium salt (PTAS) $^{39}$ as the seed for the CVD growth (see Methods for details). Hall-bar devices were fabricated on these CVD MoS$_2$ mono-layers. Fig. 1a illustrated the schematic of the device. The top gate dielectrics are 2nm aluminum deposited by e-beam evaporation and re-oxidized as a seed layer, followed by 30nm HfO$_2$ deposited by atomic layer deposition (ALD). The details of the device process are discussed in Methods. The atomic force microscopy (AFM) image and the step height profile at the boundary of a MoS$_2$ triangular area are shown in Fig. 1b and the inset of Fig. 1b, respectively. The thickness of the MoS$_2$ layer is measured to be about 0.8 nm, confirming its monolayer character. The Raman spectrum of the CVD MoS$_2$ is shown in supplementary Fig. S1. The E$_{2g}$ and A$_{1g}$ modes are at around 383 and 403 cm$^{-1}$, respectively. Comparing the peak position to the spectrum obtained from the exfoliated monolayer MoS$_2$ $^{40}$, we further verify that the MoS$_2$ film is monolayer.

**Density and dynamics of band tail states**

At present, the reported values of the electron mobility in CVD-grown MoS$_2$ devices $^{34-36}$ are at least two orders of magnitude smaller than the intrinsic limit $^{41}$, suggesting a high degree of disorder and scattering. An inhomogeneous potential distribution in a
semiconductor leads to the smearing of the band-edge and the formation of a tail of band-gap state \(^{42}\). For example, this inhomogeneity could be the result of a random distribution of trapped charges in sulfur vacancies in MoS\(_2\) itself \(^{43}\), or at MoS\(_2\)–dielectric (SiO\(_2\) or high-k dielectric) interfaces \(^{14}\). Structural defects \(^{37}\), e.g. simple vacancies \(^{43}\), dislocations and grain boundaries would also lead to localized gap states.

The electronic states in the band tail can be characterized using standard capacitance and ac conductance measurement commonly used in the study of semiconductor devices \(^{44}\). Here, these localized states respond like traps with different time constants \(\tau_{\text{it}}\), and are electrically equivalent to an additional capacitance and resistance in parallel to the semiconductor capacitance. The gate-to-channel capacitance and resistance were measured on the Hall-bars, with high terminal on the top gate and low terminal on the source, drain and all four voltage probing leads simultaneously, as shown in supplementary Fig. S2. The measured capacitance as a function of frequency is shown in Fig. 2a. The observed double hump feature indicates at least two types of traps with different time constants at a given gate voltage. Herein, we denote these traps by the labels “M” and “B”, for reasons which will be made apparent below. The equivalent circuit model of the device is shown in Fig. 2b with total impedance given by:

\[
Z = (Y_{\text{itB}} + Y_{\text{itM}} + i\omega C_s + i\omega C_j)^{-1} + (i\omega C_{\text{ox}})^{-1} + r_s + \omega Y_{\text{itB}} + 1/(i\omega C_{\text{itB}}))^{-1}
\]

where \(\omega\) is the angular frequency, \(C_s\) is the quantum capacitance of the MoS\(_2\), \(C_j\) is the parasitic capacitance, \(C_{\text{ox}}\) is the oxide capacitance, \(r_s\) is the series resistance, \(Y_{\text{itM}}\) and \(Y_{\text{itB}}\) are the traps’ admittance. Here \(Y_{\text{itB}} = [\tau_{\text{itB}}/C_{\text{itB}} + 1/(i\omega C_{\text{itB}})]^{-1}\), where \(C_{\text{itB}}\) and \(\tau_{\text{itB}}\) are the capacitance and time constant of trap B. The trap capacitance \(C_{\text{itB}}\) is related to the trap
density $D_{ab}$ via: $C_{ab} = eD_{ab}$, where $e$ is the elementary electric charge. Similar expressions apply to trap M. The measured capacitance in series mode $C_{ms}$ is related to the imaginary part of the total impedance $Z$ by:

$$ C_{ms} = -\frac{1}{\omega \text{Im}[Z]} \tag{2} $$

The lines in Fig. 2a are the fits using this model. We can see that the model provides an excellent fit to the experimental data. From the fitting, we can extract the density of traps and their time constant as a function of gate voltage, shown in Fig. 2c. Here, we observe that traps “M” and “B” are populated predominately within the “mid-gap” and “band-edge” regions, respectively.

Alternatively, the density and time constant of the traps can be extracted from the ac conductance $G_p$. The ac conductance is obtained from the measured capacitance and resistance. The measured resistances as a function of gate voltage at various frequencies are shown in supplementary Fig. S3. The extraction method of ac conductance are described in more detail in the Supplementary Note 1. The extracted ac conductance over angular frequency $G_p/\omega$ is plotted as function of the driving frequencies $f$ in Fig. 2d. Since the density-of-states of type B traps is several orders of magnitude larger than that of type M in this gate bias range, we expect the former to dominate the ac conductance.

The relation between $G_p(\omega)$ and the trap density $D_{ab}$ is given as:

$$ \frac{G_p(\omega)}{\omega} = \frac{eD_{ab}}{2\omega\tau_{ab}} \ln[1 + (\omega\tau_{ab})^2] \tag{3} $$
from which one can deduce the $D_{iB}$ and the respective time constant $\tau_{iB}$ from the following simple relations \(^{44}\):

$$D_{iB} = \frac{2.5}{e} \left( \frac{G_p}{\omega} \right)_{\text{peak}}$$

$$\tau_{iB} = \frac{1.98}{2 \times 3.14 \times f_0}$$

Here, $(G_p/\omega)_{\text{peak}}$ is the maximum $G_p(\omega)/\omega$ value, and $f_0$ is the frequency at which this maximum is obtained. Repeating the above procedure for different top gate voltages $V_{TG}$, allows us to extract $D_{iB}(V_{TG})$ and $\tau_{iB}(V_{TG})$ as shown in Fig. 2c. From Fig. 2c, we see that the density-of-states and time constant of B type traps extracted based on the capacitance and ac conductance are in good agreement.

Below, we present parameterized models for the electronic density-of-states and their time constants fitted to the experiments. We describe the electronic density-of-states of the measured distributed trap states at the band-edge (i.e. type B) and the extended states with two piece-wise functions as follows:

$$D_{n}(E) = \begin{cases} 
\alpha D_0 \exp \left[ \frac{E - E_D}{\varphi} \right] + D_{iM}, & E_D - \frac{1}{2} E_G < E < E_D \\
D_0 - (1-\alpha) D_0 \exp \left[ \frac{-E - E_D}{\varphi'} \right] + D_{iM}, & E > E_D 
\end{cases}$$

and illustrate them in Fig. 2c and 2e. Here, $D_0$ is the 2D density-of-states for perfect crystalline MoS\(_2\), taken to be $3.3 \times 10^{14}$ eV\(^{-1}\)cm\(^{-2}\), consistent with an effective mass of $0.4 \, m_0$ at the conduction band minimum at the K valley for monolayer MoS\(_2\) \(^{45}\). Here we ignored contribution from the satellite valley along ΓK with energy 200meV higher than
the conduction band minimum \(^{41,46}\), because the carrier population is insignificant at these energies at our biasing range. Furthermore, our MoS\(_2\) devices are typically n-type doped. \(\varphi\) is the characteristic energy width of the band tail. In the limit of \(\varphi = 0\), \(D_n(E)\) becomes a step function as required for perfect 2D crystals with the conduction band edge situated at \(E_D\). \(\varphi\) is chosen so that the two piece-wise functions have continuous gradients at \(E_D\). Solving the electrostatics problem, to be described below, a best-fit to the experimentally extracted density-of-states yields the parameter set: \(\alpha = 0.33\) and \(\varphi = 100\,meV\). The comparison between the model \(D_n(V_{TG})\) and the measured band tail states \(D_{ab}(V_{TG})\) is shown in Fig. 2c, and the mid-gap states \(D_{ab}(V_{TG})\) is described by an error function instead. The traps’ response time are fitted to an exponential model,

\[
\tau = \tau_0 \exp\left[ -\frac{E - E_{mid}}{\Phi_{\tau}} \right]
\]  

(7)

and the comparison with experimental data is shown in Fig. 2c.

With the parameterized density-of-states model, we can calculate the ac capacitance and compare against experiments. The Poisson equation describing the electrostatics of the problem can be expressed as:

\[
Q_n + Q_0 = \varepsilon_{ox} \left( \frac{V_{TG} + E_D / e}{t_{top}} \right)
\]

(8)

where \(t_{top}\) is the "effective-oxide-thickness" for the top gate dielectric, \(\varepsilon_{ox}\) is the dielectric constant of silicon oxide, \(Q_0\) is a constant which includes contributions from the fixed
charges and doping in as-prepared MoS₂ etc, and \( Q_n \) is the electronic charges in the smeared out conduction band and can be computed from
\[
Q_n = e \int D_n(E) f_n(E, E_F) dE
\]
where \( f_n \) is the Fermi Dirac function. In solving for the self-consistent electrostatics described by Eq. 8, the Fermi energy \( E_F \) is taken to be the reference i.e. \( E_F = 0 \). Once the electrostatics is determined, the admittance associated with each of the traps can then be computed via,
\[
Y_t = e^2 \int D_n \frac{f_\omega + \omega^2 \tau_n \partial f_n}{1 + (\tau_n \omega)^2} \partial E dE
\]
and the total capacitance can be computed employing the equivalent circuit model in Fig. 2b, and using equation (1) and (2). Reasonable agreement with the measured ac capacitance is obtained as shown in Fig. 2f.

To summarize, the electronic density-of-states model described above is well-calibrated to the experimentally measured density and dynamics of the band tail states. It follows an exponentially decaying behavior, with a significantly large energy width of \( \varphi = 100 \text{meV} \), suggesting a high degree of potential disorder and scattering. This model will be employed in the subsequent discussion to obtain other quantities of interest, such as the band mobility.

**Mobility edge**

The concept of a "mobility edge" has greatly facilitated our understanding of electronic transport in a disordered system \(^{47}\). The mobility edge is a boundary located in the band tail, in which states above it are extended states with band transport, while those below it
are localized states that conduct via thermally assisted mechanisms such as Mott variable range hopping (VRH) or an Arrhenius-type activated behavior. Four point variable temperature measurements were performed on our devices from 4.4 to 400 K as shown in Fig. 3a. We found that neither the VRH nor the Arrhenius model can individually describe the data satisfactorily over the whole temperature range. It is very likely that a combination of both transport mechanisms might be operating here. For example, the VRH usually dominates for localized states deep in the band tail, while the Arrhenius-type activated behavior is more likely for shallow localized states.

The conductance versus the inverse of temperature \( (1/T) \) is shown in Fig. 3b, showing the exponential decrease with \( 1/T \) over the intermediate temperature range, where the conductance \( G \) can be described by:

\[
G = G_0 e^{-E_a/k_B T}
\]

(10)

where \( E_a \) is the activation energy, \( k_B \) is the Boltzmann constant and \( G_0 \) is a fitting parameter. This allows us to extract the activation energy \( E_a = E_M - E_F \). The measured \( E_a \) (versus \( V_{TG} \)) is compared to the model (see Fig 3b inset), which allows us to determine the location of the mobility edge \( E_M \) in the energy band picture. We found that in our devices \( E_M \) is \( \approx 0.01 eV \) above \( E_D \), as illustrated in Fig. 2e. We also noticed a departure from activated behavior at lower temperature or bias, indicating the possible onset of an additional transport mechanism such as VRH. The extracted activation energy in the inset of Fig. 3b suggests that in most of our gate biases, the Fermi level does not exceed the mobility edge energy. However, at large \( V_{TG} \) i.e. \( V_{TG} > 2V \), the Fermi energy
is within tens of meV from the mobility edge. Hence, one can expect an appreciable fraction of extended states occupation due to thermal smearing. The calculated band carrier density as a function of gate voltage at various temperatures are shown in Fig. 3c.

**Transport coefficients**

The “effective mobility”, or sometimes referred to as the “drift mobility”, is a commonly used transport coefficient in semiconductors. It is defined as the ratio of the measured conductivity to the total charge density i.e. \( \mu_{\text{eff}} = \sigma / Q_{\text{total}} \). The total charge density \( Q_{\text{total}} \) is typically estimated from \( C_{\text{ox}} (V_g - V_T) \), where \( C_{\text{ox}} \) is the oxide capacitance, \( V_g \) is the gate voltage, and \( V_T \) is the threshold voltage. We extract \( C_{\text{ox}} \) from the measured capacitance at strong accumulation. Fig. 4a shows the effective mobility as a function of gate voltage at different temperatures. The effective mobility is <10 cm²/V-s over the range of temperature and applied bias in our experiments. Contact resistance is eliminated in our measurement which employs a four-probe scheme. The measured effective mobility is significantly lower than the phonon-limited intrinsic mobility in monolayer MoS₂, predicted to be over 400 cm²/V-s, and the highest measured mobility of ~200 cm²/V-s in exfoliated MoS₂ devices. However, it is consistent with results on similar CVD-grown MoS₂ devices which report mobilities in the range of 5 to 25 cm²/V-s. The significantly lower mobility for CVD-grown MoS₂ is, to a large part, due to the presence of traps.

The total charge density includes both the free and trapped charges: \( Q_{\text{total}} = e \left( n_{\text{loc}} + n_{\text{band}} \right) \) where \( n_{\text{loc}} \) and \( n_{\text{band}} \) refer to the density of occupied states below and above the mobility edge, respectively. Another commonly used transport coefficient in a disordered system
is the "band mobility" \(^{53,54}\). It is defined as the ratio of the measured conductivity to the density of occupied states above the mobility edge (i.e. extended states):

\[
\mu_{\text{band}} = \frac{\sigma}{en_{\text{band}}} = \mu_{\text{eff}} \frac{n_{\text{loc}} + n_{\text{band}}}{n_{\text{band}}}
\]

(11)

In general, the density of the extended states is difficult to measure, since the large amount of localized states would result in large noise-to-signal ratio the in the Hall measurement. Up to now, the Hall effect has only been observed in exfoliated MoS\(_2\) with very high carrier density induced by an electrolyte gating scheme \(^{26}\) or at very low temperatures \(^{17}\).

Previously, we obtained \(D_n(E)\) in conjunction with \(E_M\) in the energy band picture. Solving the electrostatics in conjunction with the above information would allow us to estimate the fraction of localized and extended states. Fig. 3c plots the computed \(n_{\text{band}}(V_{TG})\) at different temperatures. The result indicates that \(n_{\text{band}}\) only accounts for less than 25% of \(n_{\text{total}}\). Only at high temperature or bias, \(n_{\text{band}}\) can exceed 25% i.e. \(T > 300K\) and \(V_{TG} > 2V\). The comparison between the extracted band mobility and measured effective mobility is shown in Fig. 4b. The band mobility is several times higher than the effective mobility, but still significantly lower than the phonon-limited mobility as predicted in Ref. \(^{41}\). This mobility degradation may involve many sources of scattering. For example, structural defects in CVD MoS\(_2\) layer and grain boundaries can induce short-range scattering. Surface polar phonon either in the high-k dielectrics (HfO\(_2\) and AlO\(_x\)) or in the SiO\(_2\) substrate underneath can also play a role. However, the significant trap population measured here suggests that Coulomb scattering due to trapped charges is
the likely limiting factor for the electron mobility. Due to the parabolic band-structure of MoS$_2$, the energy averaged scattering time due to Coulomb scattering should increase proportionally to temperature $\mu \propto k_B T$. This is also consistent with the observed trend in Fig. 4b for temperature below 300K. Above this temperature phonon scattering takes over.

**Sub-threshold swing**

In an ideal semiconductor, the sub-threshold swing is given by $S = k_B T \ln(10)(1 + C_D / C_{ox})$, where $C_D$ is the depletion capacitance. The sub-threshold swing increases linearly with temperature, since the carrier density increases exponentially with temperature $n \propto \exp\left(\frac{E_F - E_i}{k_B T}\right)$. In our device, we observed that the sub-threshold swing is $\approx 200$ mV/dec and nearly independent of temperature, as shown in Fig. 3a. Similar observations were made on MoS$_2$ flakes. This departure from the ideal behavior can be understood by recalling that the band tail is distributed in energy, i.e. $\exp\left[\frac{E - E_D}{\phi}\right]$, with an energy width that is significantly larger than the thermal energy i.e. $\phi \gg k_B T$. Indeed, the calculated sub-threshold behavior confirms that temperature does not have a significant effect, as shown in Fig. 3c. Hence, the observed temperature independent sub-threshold swing reinforced our earlier conclusions on the existence of band tail states.

**Drain-induced-barrier-lowering**
The electrostatic integrity of an electronic device upon downscaling is often quantified by evaluating the amount of drain-induced-barrier-lowering (DIBL) \(^{56}\). This measures the reduction in threshold voltage due to the applied drain bias. A common approach used to suppress DIBL involves reducing the channel thickness, since the minimum channel length needed to preserve the long channel behavior is typically \(~4\text{-}5\) times the electrostatic scaling length \(\lambda = \sqrt{\varepsilon_s t_s / \varepsilon_{ox}}\) for a planar device structure\(^{57,58}\), where \(\varepsilon_s\) and \(\varepsilon_{ox}\) are the dielectric constants of the semiconductor and the gate oxide and \(t_s\) and \(t_{ox}\) are the thicknesses of the semiconductor and gate oxide, respectively. In this regard, thinner silicon has been pursued by using SOI (silicon-on-insulator) and ETSOI (extremely thin silicon-on-insulator). However, the mobility degrades dramatically as the thickness is scaled down due to surface roughness \(^{59,60}\). Atomically thin 2D semiconducting material such as MoS\(_2\) and WSe\(_2\) are promising candidates in this regard. The typical DC performances of MoS\(_2\) MOSFETs with various channel lengths are shown in Supplemental Figure S4. Fig. 5a shows the DIBL of CVD MoS\(_2\) MOSFET with variable channel lengths from 4\(\mu\)m to 32nm. Despite the thick dielectric used in our MOSFETs, \((~34\text{nm HfO}_2/ \text{AlO}_x\) stack for the long channel devices, \(~60\text{nm HfO}_2/ \text{AlO}_x\) for the short channel devices, limited by the bulging of gate dielectrics on the source/drain side wall), a clear upturn of DIBL is only observed at a channel length of 32nm. Extrapolating to a device with a 3nm HfO\(_2\) gate insulator would predict a limiting channel length feature of \(~7\text{nm}\). Theoretically, for a MOSFET with monolayer MoS\(_2\) (channel thickness: \(~0.8\text{nm},\) dielectric constant: \(6.8\text{-}7.1 \varepsilon_0\), where \(\varepsilon_0\) is the vacuum permittivity \(^{61}\)) and 1nm equivalent oxide thickness (EOT), the electrostatic scaling length \(\lambda\) is only about 1.2nm.
These considerations suggest that MoS₂ could be a very promising material for scaled, high-density electronics.

**Breakdown electric fields**

The large band gap of MoS₂ implies the possibility of device operation at higher voltages or electric fields. Fig. 5b shows the critical breakdown fields of graphene and CVD MoS₂ MOSFETs devices. The measurement setup is shown on the upper-left inset of Fig. 5b. The channel-length dependence of breakdown voltage of MoS₂ MOSFETs is shown in the lower-right inset of Fig. 5b. The critical field can be extracted from the slope of the breakdown voltage vs channel length. Here we extracted the breakdown field from MoS₂ transistors with channel lengths of 80nm and 285nm. (More details about the breakdown test results of MoS₂ transistors and graphene transistors are shown in the Supplementary Figure S5 and S6, and Supplementary Note 2 and 3) The measured breakdown field of CVD MoS₂ is about 5 times larger than that of graphene, and significantly larger than that of SOI with 100nm silicon thickness ⁶². In this regard, MoS₂ can also be a very promising platform for power devices.

**Discussion**

We have systematically studied the electronic transport properties of CVD MoS₂ devices. We report the observation of a significant amount of electronic trap states through capacitance and ac conductance measurements and their impact on the low-field electronic properties of MoS₂ devices. In particular, the measured effective mobility significantly underestimates the band mobility. An anomalous sub-threshold behavior,
with distinctive temperature insensitivity, is also accounted for by the presence of these band tail states. We also studied the high-field electronic properties of MoS$_2$ devices and demonstrated the possibility to aggressively scale them down and their high breakdown electric fields. These attractive device attributes present a compelling case for wafer-scale monolayer MoS$_2$ as alternative to organic and other thin film materials for flexible electronics and photonics, including high resolution displays, photo-detection, logic electronics, power devices with solar energy harvesting etc. From the fundamental material standpoint, understanding of the microscopic origin of these band tail states is critical for further improvement of the material's electronic properties.

**Methods:**

**Fabrication**

Large-scale monolayer MoS$_2$ was synthesized at 650 °C by APCVD using perylene-3,4,9,10-tetracarboxylic acid tetra-potassium salt (PTAS) as the seed on SiO$_2$/Si substrate. Sulfur powder and molybdenum oxide (MoO$_3$) were used as the precursors for the synthesis. The SiO$_2$ thickness was 300 nm. In the Hall-bar and transistor devices, the source/drain contact metal stack consisted of Ti/Au/Ti (5/15/5 nm). The MoS$_2$ channel was patterned using electron beam lithography and oxygen plasma etching. The top gate dielectric was comprised of an AlO$_x$/HfO$_2$ stack. The AlO$_x$ was formed by electron beam evaporation of 2 nm of aluminum metal followed by its natural oxidization in air for a few hours. The 30 nm thick HfO$_2$ layer was formed using atomic layer deposition (ALD) at 170 degrees. The top gate electrode was Ti/Au (5/40 nm).
Characterization

The capacitances were measured using Agilent B1500 Semiconductor Device Analyzer produced by Agilent technology. The temperature dependence of conductance was measured using cryogenic probestation produced in Lake Shore Cryotronics, Inc. The Raman spectrum was taken using Labram Aramis produced by Horiba Jobin Yvon. Scanning electron microscopy was measured using Leo 1560 produced by Carl Zeiss.

Acknowledgement:

We would like to thank Bruce Ek, Jim Bucchignano and Simon Dawes for their contributions to device fabrication. We would also like to thank Jin Cai and Vasili Perebeinos in IBM, Xiao Sun and Prof. Tso-Ping Ma at Yale University, and Prof. Mingfu Li at Fudan University for valuable discussions.

Author contributions:

W.Z. and F.X. initiated the project. Y-H.L. and J.K. carried out CVD MoS$_2$ growth. W.Z., F.X. and H.W. contributed to device design and fabrication. W.Z. performed the electrical characterization. W.Z., T.L, and F.X. analyzed the data. T.L. performed the modeling. D.B.F. grew the ALD gate dielectric. Y-H.L. carried out Atomic force spectroscopy (AFM). W.Z. performed Scanning electron spectroscopy (SEM) and Raman spectrum measurement. W.Z. designed, fabricated and measured the graphene devices. P.A. supervised this project. All authors participated in writing of the paper.

Competing financial interests: The authors declare no competing financial interests.
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Figure legends:

Figure 1. Chemical vapor deposition (CVD) molybdenum disulphide (MoS2) physical properties and device structure. (a) Schematic of MOSFET with monolayer CVD grown MoS2. (b) AFM image of CVD grown MoS2 on SiO2/Si substrate. The scale bar in the AFM image is 10μm. The inset shows the step height profile of MoS2 in the AFM image.

Figure 2. Characterization and modeling of the density and dynamics of band tail states. (a) Capacitance as a function of frequency measured at various gate voltages. The device width is 4μm and length is 44μm. The symbols are the experimental results and the lines are fittings using the device model shown in (b). (b) The equivalent circuit model of the device, simplified parallel model and the measurement model in series mode. (c) Density and time constant of trap states as a function of gate voltages. The symbols are experimental results extracted from the capacitance $C_{mns}$ and ac conductance $G_p$. The lines are models, see text. (d) Extracted ac conductance over angular frequency $G_p/\omega$ as a function of frequency $f$ at various gate voltages. (e). Parameterized model, $D_n(E)$, describing the electronic density-of-states of both the extended and localized states. The valence density-of-state is also included in the illustration using the mirror image of conduction density-of-state. The inset illustrates the band diagram of MoS2 MOSFET. (f) Multi-frequency capacitance of MoS2 Hall-bar as a function of gate voltage. The symbols are experimental results and the lines are the modeling results.
Figure 3. **Temperature dependence of conductance and activation energy.** (a) Four point conductance as a function of gate voltage measured at various temperatures from 4.4K to 400K on a MoS$_2$ Hall-bar. (b) Conductance as a function of reverse of temperature $1/T$ at various gate voltages. The inset shows the activation energy at various gate voltages fitted to the Arrhenius activated energy model. The symbols are experimental results extracted from the conductance, the solid line gives the modeling results. (c) The calculated band carriers as a function of gate voltage at various temperatures.

Figure 4. **Effective mobility and band mobility.** (a) Effective mobility as a function of gate voltage measured at various temperatures in MoS$_2$ Hall-bar. (b) Effective mobility and the corresponding band mobility as a function of temperature at $V_{TG} = 4V$. The mobility limited by MoS$_2$ phonons scattering based on theoretical calculations$^{41}$ are also plotted for comparison.

Figure 5. **Device properties at high electrical fields.** (a) Drain-induced-barrier-lowering (DIBL) of MOSFET with CVD MoS$_2$ at various channel lengths. The inset shows the SEM image of the 32nm and 80nm channel length devices. (b) Critical electric field of CVD MoS$_2$ and graphene. The upper inset shows the measurement configuration. The lower inset shows the lateral breakdown voltage as a function of channel length for MOSFET with CVD MoS$_2$. 

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Figure-1 (Zhu)
Figure 3 (Zhu)

(a) Conductance ($\mu$S) vs. Gate Voltage $V_{TG}$ (V) for temperatures $T=4.4K$ to $400K$.

(b) Conductance ($\mu$S) vs. $1/T$ ($K^{-1}$) for a range of Gate Voltages $V_{TG}$.

(c) Band density ($n_{band}$) vs. Gate Voltage $V_{TG}$ for temperatures $50K$ to $400K$. 

- Conductance scales: $1E^{-4}$ to $1E^{-1}$.
- Gate Voltage $V_{TG}$ scales: $200mV/dec$.
- Temperature range: $T=4.4K$ to $400K$. 

Inset in (b) shows $E_M - E_F$ vs. $V_{TG}$.
Figure-4 (Zhu)
Figure-5 (Zhu)