A 249Mpixel/s HEVC video-decoder chip for Quad Full HD applications

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9.5 A 249Mpixel/s HEVC Video-Decoder Chip for Quad Full HD Applications

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The latest video coding standard High Efficiency Video Coding (HEVC) [1] provides 50% improvement in coding efficiency compared to H.264/AVC, to meet the rising demand for video streaming, better video quality and higher resolutions. The coding gain is achieved using more complex tools such as larger and variable-size coding units (CU) in a hierarchical structure, larger transforms and longer interpolation filters. This paper presents the first integrated circuit which supports Quad Full HD (QFHD, 3840x2160) video decoding for HEVC draft standard. It addresses new design challenges for HEVC ("H.265") with three primary contributions: 1) a system pipelining scheme which adapts to the variable-size largest coding unit (LCU) and provides a two-stage sub-pipeline for memory optimization; 2) unified processing engines to address hierarchical coding structure and many prediction and transform block sizes in area-efficient ways; 3) a motion compensation (MC) cache which maintains an average hit rate of 61% despite the large LCU sizes. In addition, we propose a two-stage 2-D tiling in the DRAM to increase horizontal separation between two DRAM rows for a given bank. This reduces the probability of changing rows in a bank to save bandwidth wasted on precharge/activate (ACT) cycles. Compared to a raster scan of 8x4 cache lines, 70% DRAM ACT bandwidth is saved. When benchmarked against sharing fetched pixels in only one sub-PBP, our cache design saves 67% DRAM bandwidth for MC.

The chip specifications are summarized in Figure 9.5.5. The core size is 1.77mm² in 40nm CMOS, which consists of 715K logic gates and 124KB on-chip SRAM. It is compliant to HEVC Test Model (HM) 4.0, and the supported decoding tools in HEVC Working Draft (WD) [4] [1] are also listed. This chip achieves 249Mpixels/s decoding throughput for QFHD videos at 200MHz with the target DDR3 SDRAM operating at 400MHz. The core power is 219mW (modeled by [5]) for QFHD decoding at 30fps, for which the much larger for LCU 64x64 and [3-4] do not have line buffers. The DRAM power is 219mW (modeled by [5]) for QFHD decoding at 30fps, for which the proposed MC cache saves 122mW. Despite the increased complexity, this work demonstrates the lowest normalized system power, which facilitates the use of HEVC on low-power portable devices for QFHD applications.

Figure 9.5.6 shows the comparison with state-of-the-art video decoders [2-4]. This work supports HEVC draft standard which is the successor of H.264/AVC and has higher complexity and larger CUs for 2x compression capability. More SRAM is used than [2-4] because the pipeline buffers and cache SRAM are much larger for LCU 64x64 and [3-4] do not have line buffers. The DRAM power is 219mW (modeled by [5]) for QFHD decoding at 30fps, for which the proposed MC cache saves 122mW. Despite the increased complexity, this work demonstrates the lowest normalized system power, which facilitates the use of HEVC on low-power portable devices for QFHD applications.

Acknowledgements:
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References:
Figure 9.5.1: System block diagram and pipelining scheme in variable-size pipeline block (VPB).

Figure 9.5.2: Unified prediction engine and memory-efficient two-stage sub-pipeline in PPB and sub-PPB.

Figure 9.5.3: Unified 2-D inverse transform engine with variable-size partial transform for all square/non-square TUs with 4 to 32-pt IDCT and 4-pt IDST.

Figure 9.5.4: Four-parallel high throughput MC cache and twisted 2-D DRAM mapping.

Figure 9.5.5: Chip specifications and measurement results.

Figure 9.5.6: Comparison with state-of-the-art video decoders.