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A 0.6V 2.9μW Mixed-Signal Front-End for ECG Monitoring

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Abstract

This paper presents a mixed-signal ECG front-end that uses aggressive voltage scaling to maximize power-efficiency and facilitate integration with low-voltage DSPs. 50/60Hz interference is canceled using mixed-signal feedback, enabling ultralow-voltage operation by reducing dynamic range requirements. Analog circuits are optimized for ultra-low-voltage, and a SAR ADC with a dual-DAC architecture eliminates the need for a power-hungry ADC buffer. Oversampling and $\Delta\Sigma$-modulation leveraging near-$V_T$ digital processing are used to achieve ultralow-power operation without sacrificing noise performance and dynamic range. The fully-integrated front-end is implemented in a 0.18μm CMOS process and consumes 2.9μW from 0.6V.

Introduction

Symptoms of cardiovascular disease are often very intermittent, necessitating ultra-low-power wearable ECG monitors with long lifetimes. In order to minimize system power, digital signal processing (DSP) can accomplish feature extraction and data compression which reduces the power burden of data transmission or storage. Recent biomedical DSPs leverage voltage scaling (down to 0.5V) to improve energy-efficiency [1]. Additional size and power benefits can be obtained by integrating the analog front-end (AFE) with the DSP back-end [2]. However, current AFEs rely on high supply voltages [3, 4] to perform signal conditioning and accommodate aggressors like electrode offset (EO) and power-line interference (PLI), limiting their compatibility with low-voltage DSPs. Therefore, this paper presents a mixed-signal front-end (MSFE) that leverages a highly-digital architecture in order to operate from a 0.6V supply which improves power-efficiency through voltage scaling, and facilitates integration with low-voltage DSPs. This work focuses on the design of ultra-low-voltage front-end analog circuits aided by configurable and energy-efficient digital processing at near-$V_T$ operation. A highly-integrated solution is presented to demonstrate feasibility of a 0.6V system.

System Description

Supply voltage scaling is an effective way to achieve linear and quadratic power reduction in analog and digital circuits respectively. However, for ECG acquisition, PLI can be a limiting factor for voltage scaling. For example, 5mV$_{p-p}$ of PLI with 40dB of front-end gain could easily saturate a sub-1V system before digitization by the ADC. Therefore, the system architecture in this work is based on [4], but uses $\Delta\Sigma$-modulation to simultaneously achieve a larger PLI cancellation range and low-noise performance as a key enabler for ultra-low-voltage operation. The burden of signal processing is shifted to the digital domain which is suitable for low-voltage systems. Compared to [4], this work reduces the supply voltage from 1.5V to 0.6V and optimizes analog circuits for ultra-low-voltage operation.

Shown in Fig. 1, a low-noise amplifier (LNA) gains the input by 34.5dB, and ac-coupling achieves greater than ±300mV of EO rejection as required [5]. A sinc anti-aliasing filter (SAAF) provides an integrate-and-dump function at a sampling frequency of $f_S=10$kHz, resulting in a sinc frequency response with notches placed at multiples of $f_S$ which are precisely in the center of the aliasing bands. At the end of each integration period, the signal is digitized by a 9b dual-DAC SAR ADC.

Any PLI in the signal is captured by a programmable digital band-pass filter (BPF) and fed back to the input with an 8b charge-redistribution DAC, cancelling PLI right at the input to enable low-voltage operation. Moreover, this mixed-signal topology creates an extremely sharp and tunable notch without large passives required in purely analog systems. Since the frequency content of ECGs is well below 100Hz, $\Delta\Sigma$-modulation and oversampling at 10kS/s are exploited to achieve greater than 12mV$_{p-p}$ of PLI cancellation without introducing significant quantization noise with an 8b DAC. A decimation filter removes out-of-band noise and reduces the data rate down to 312.5S/s, providing up to 10.8 ENOB at the output. All reference voltages are generated by 2b R-string DACs whose reference comes from a 400mV supply-independent reference, and an on-chip oscillator and clock generator produce all clock phases.

Low-Voltage Mixed-Signal Circuit Design

The LNA is fully-differential to maximize signal range, and uses passive feedback to accurately set gain and ensure good linearity at 0.6V. Although the CMRR is limited to 70dB by using passive feedback, the CMRR requirements are relaxed since the mixed-signal notch in this system filters out PLI. Switched-capacitor common-mode feedback (SC-CMFB) is used to avoid distortion from the CMFB loop with large signal swing at low voltage. Although SC-CMFB introduces spikes at the switching frequency of 10kHz, the SAF in this system also acts as a spike reduction filter.

In addition to anti-aliasing and spike reduction, the SAF shown in Fig. 2 also provides a gain of $G_S = G_M/(2f_S C_{INT})$ which is digitally tunable through $G_M$ and $C_{INT}$. The SAF uses negative feedback to implement a linear transconductor and avoids cascading in order to operate at 0.6V. $C_{INT}$ is the sum of a 4b switched-capacitor $C_D$, and the sampling capacitance $C_S$, of the SAR ADC whose block diagram is shown in
A noise includes contributions from LN A, SAAF, ADC, and decimation filter.

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