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Ultrafast phase-change logic device driven by melting processes

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The ultra-high demand for faster computers is currently tackled by traditional methods such as size scaling (for increasing the number of devices), but this is rapidly becoming almost impossible, due to physical and lithographic limitations. To boost the speed of computers without increasing the number of logic devices, one of the most feasible solutions is to increase the number of operations performed by a device, which is largely impossible to achieve using current silicon-based logic devices. Multiple operations in phase-change-based logic devices have been achieved using crystallization; however, crystallization is a slow process and this approach can achieve mostly speeds of several hundreds of nanoseconds. A difficulty arises from the trade-off between increasing the speed of crystallization and, at the same time, extending the long-term (non-volatile) stability of the initialized glassy state to avoid spontaneous crystallization causing corruption of the initial logic state.

Here we instead control the processes on melting via premelting disordering phenomena, while maintaining the superior advantage of the phase-change-based logic devices over silicon-based logic devices, as well as avoiding the stability drawbacks in previous crystallization-based logic devices by using a stable crystalline phase, rather than the thermally vulnerable amorphous phase, as the initial logic state. Ultrafast melting speeds were achieved, as well as multiple Boolean algebraic operations. Ab initio molecular-dynamics (AIMD) simulations and in situ electrical characterization revealed the microscopic origin and transient kinetics of melting through premelting disordering phenomena, respectively, which were observed to be key to increasing the melting speeds.

We find that Ge–Sb–Te alloys (e.g., Ge2Sb2Te5 or GST), which are technologically important for phase-change nonvolatile information storage, provide a nearly ideal system for achieving the cell itself. Multiple operations in phase-change–based logic devices have been achieved using crystallization; however, crystallization is a slow process and this approach can achieve mostly speeds of several hundreds of nanoseconds (10, 11). A difficulty arises from the trade-off between increasing the speed of crystallization and, at the same time, extending the long-term (non-volatile) stability of the initialized glassy state to avoid spontaneous crystallization causing corruption of the initial logic state (12).

The extremely high and ever-increasing demand for faster computers is currently addressed by traditional methods, such as miniaturization (to increase the number of devices), but this is rapidly becoming almost impossible, due to physical and lithographic constraints (1–4). The speed of computers is known to be determined almost solely by the performance of logic devices, i.e., their speed and number, which control most computations (or processes) in computers (5). Logic devices are mostly required to operate around 1 ns for achieving fast computations, and to transfer information between alternate devices, such as random-access memories, without delays (5). To increase the speed of computers without increasing the number of logic devices, one of the most feasible methods is to increase the number of operations performed by a device, which is largely unachievable using current silicon-based logic devices (6, 7).

Multiple operations in a logic device are currently best achieved using devices comprised of phase-change nonvolatile memory materials—based on the reversible and multilevel switching of a phase-change material (PCM) between crystalline and glassy states having a contrast in physical properties, e.g., electrical resistivity (8, 9)—which can perform more than three times the number of operations than can silicon-based logic devices (10, 11). They also have the advantage of in-memory operation: the logical state is stored in a nonvolatile manner in the cell itself. Multiple operations in phase-change–based logic devices have been achieved using crystallization; however, crystallization is a slow process and this approach can achieve mostly speeds of several hundreds of nanoseconds (10, 11). A difficulty arises from the trade-off between increasing the speed of crystallization and, at the same time, extending the long-term (non-volatile) stability of the initialized glassy state to avoid spontaneous crystallization causing corruption of the initial logic state (12).

Significance

The ever-increasing demand for faster computers is tackled by reducing the size of devices, but this is becoming almost impossible to continue. To improve the speed of computers, a solution is to increase the number of operations performed per device. Numerous operations in phase-change–based “in-memory” logic devices have previously been achieved using crystallization, but they show slow speeds, mostly due to a trade-off between the crystallization speed and stability of the initialized-glassy states. Here, we instead control melting processes to perform logic operations. Ultrafast melting speeds and diverse operations were achieved. Computer simulations and electrical measurements show the origin and kinetics of melting. These advances open the doorway for developing computers that can perform calculations at well beyond current processing rates.


The authors declare no conflict of interest.

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Boolean algebraic operations, and for tracking the transient behavior of melting or solid-to-liquid (s-to-l) transitions. This allows for the precise and systematic control of disorder in a crystalline solid via the use of a weak electric field/electrical priming pulse, which is applied to a test cell, comprising a 90-nm-wide cylinder of GST sandwiched between two TiW electrodes (Methods and SI Appendix, Fig. S1). Such priming effects are largely difficult to detect through conventional material characterization, for instance electron diffraction of the gradual changes in the structure of GST caused by multiple electrical pulses (13), but are evidenced in this study via a simple approach comprising in situ electrical–conductivity measurements of both pronounced and fast variations in the GST structure upon applying a single electrical pulse. Such high electrical sensitivity is the key to revealing the microscopic origin of an s-to-l transition in this material.

We have shown that a GST cell shows multiple Boolean algebraic operations via control of the switching from crystalline to glassy states. By applying a double-pulse priming/switching–excitation scheme, a single cell can exhibit two combinations of electrical-resistance levels: (i) an L–H–H–H resistance combination resulting from LO–LO, LO–HI, HI–LO, and HI–HI pulses with no separation (Fig. 1A); and (ii) an L–L–L–L–H resistance combination resulting from the same set of pulses, but with a separation of \( t = 100 \text{ ns} \) (Fig. 1B). \( L \) and \( H \) refer to low- and high-resistance levels, which are below and above a reference resistance level, here taken to be \( R = 0.7 \text{ M}\Omega \), and LO and HI denote low- and high-voltage pulses, respectively (Fig. 1C and D). By representing the \( L \) and \( H \) resistance levels, and the causative HI and LO pulses, as the binary numbers 1 and 0, \( \neg(x\lor y) \)/NOR and \( \neg(x\land y) \)/NAND operations are demonstrated, respectively (Fig. 1C and D). It should be noted that this is also twice the number of operations observed in the nonpriming excitation scheme (using only HI pulses), which can only show NAND operation both with and without a separation (SI Appendix, Fig. S18). Furthermore, single LO/HI pulses and their corresponding resulting \( L- \) and \( H- \)resistance levels can be used to generate a \( \neg x \) NOT operation (Fig. 1E). Such control is derived from a dependence of the cell resistance on the voltage, length, and separation of the electrical pulses (SI Appendix, Figs. S14–S16).

Ultimately, a modular expansion of such a method can facilitate even greater control of the resistance levels, as new material/device structures are developed with a higher number of resistance levels and resistance-level combinations (11, 14).

The GST cells have been shown to exhibit ultrafast Boolean algebraic operations via boosting the energy delivered by electrical-pulse excitation. Generally, a fast crystal-to-glass transition is realized through applying a high input energy, which promotes rapid structural disordering in GST (15–17). As predicted, the GST cell exhibits faster switching from the crystalline to glassy states for both NOR and NOT operations as the amplitudes of the LO/HI electrical pulses are increased from 1.55/1.70 to 4.6/5.0 V (Fig. 1F). Remarkably, such operations can be achieved with electrical pulses as short as \( t = 400/500 \text{ ps} \) or a total pulse length of 900 ps (Fig. 1F)—which is two orders of magnitude shorter than those needed to manipulate the alternative crystallization excitation schemes previously used for Boolean algebraic operations.

![Fig. 1](image-url) Examples of the use of s-to-l transitions for achieving fast and multiple Boolean algebraic (logic) operations in the GST cell. Waveforms for the double electrical-pulse sequence (A) without and (B) with a time separation between the pulses. The dependence of the electrical resistance on the double-pulse excitation scheme applied to the cells used to demonstrate (C) \( \neg(x\lor y) \)/NOR and (D) \( \neg(x\land y) \)/NAND operations, without and with \( t \) a separation between the pulses, respectively. (E) Correlation between the electrical-resistance level and the single-pulse excitation used to achieve the \( \neg x \) NOT operation. HI and LO refer to high- and low-voltage pulses with amplitudes of \( V = 1.70 \) and 1.55 V, respectively. The length of the pulses was kept constant at 15 ns, and the time separation between them, where required, was maintained to be the same at 100 ns. The reference resistance levels, \( R_{\text{ref}} \), for the NOR and NAND, and NOT operations were chosen to be \( R = 0.7 \) and 0.3 M\( \Omega \), respectively. Truth tables for the Boolean algebraic operations are demonstrated (C–E, Right). The HI and LO electrical pulses represent the binary numbers 1 and 0 for both inputs \( x \) and \( y \) of the Boolean algebraic operations, and the cell resistances below and above the \( R_{\text{ref}} \) values define the binary numbers 1 and 0 for the output of such operations, respectively. The error bars show the range of values obtained from experiments performed on three different cells. (F) Plots showing the switching times achievable with different pulse voltages. (Right) The tables show the electrical-resistance values of the cells measured after applying picosecond-range pulses to perform NOR (Upper) and NOT (Lower) operations with a time separation between the pulses. The \( R_{\text{ref}} \) values for the NOR and NOT operations were chosen to be \( R = 0.8 \) and 0.3 M\( \Omega \), respectively. The cells were switched between the low- and high-resistance levels of \( R = 0.05 \) and 1.00 M\( \Omega \), respectively.
operations in GST (10, 11). It should be noted that this is also as short/shorter than those obtained for the cells in the nonpriming excitation scheme [of 5.0 V and (minimum) 1 ns] (SI Appendix, Figs. S18 and S17). In addition, the energy density needed to perform Boolean algebraic operations can be estimated by a simple calculation of the area under the pulse waveforms used (i.e., the sum of their amplitude–length products). In the worst case scenario, to perform Boolean algebraic operations with two high-voltage (input) pulses, the energy density needed for the priming excitation scheme is given by $2 \times (5.0 \times 0.5 \times 10^{-9}) = 5 \text{ nJ/A}$, which is 139 times lower than the crystallization excitation scheme [that is given by $2 \times (2.4 \times 70 \times 10^{-9} + 1.5 \times 120 \times 10^{-9}) = 696 \text{ nJ/A}$] (10). This is also two times lower than for the nonpriming excitation scheme (which is given by $2 \times 5.0 \times 1.0 \times 10^{-9} = 10 \text{ nJ/A}$). This demonstrates the potential for exploiting crystal-to-glass kinetics for ultrafast logic applications, although the device performance and (Boolean algebraic) implementation of a GST cell, such as the power consumption, temporal resistance drift, and sequential operation, can be enhanced/optimized further (SI Appendix).

We investigated the transient characteristics of an s-to-l transition occurring during the Boolean algebraic operations by evaluating the in situ electrical conductance of a GST cell upon electrical-pulse excitation. The cell, initially in the crystalline state, was excited with an onset voltage, e.g., $V_{on} \sim 1.5 \text{ V}$ (similar to the amplitudes of the low-voltage pulses that were key to achieving the Boolean algebraic operations in Fig. 1 C and D), which induces the onset of an s-to-l transition by locally heating the material above its melting temperature, $T_m$, via Joule heating (18); the $V_{on}$ value was determined via the dependence of the current flow on the constant voltage applied to the cell (Fig. 2A, Top Right). In general, most metals or materials exhibit a transition from the solid to a liquid/melt state that yields an increase in the electrical conductivity (19, 20). By applying an electrical pulse with an amplitude of around $V_{on}$ (e.g., $V = 1.47$ or $1.50 \text{ V}$), we find that the GST cell exhibits a similar transition (as manifested by a pronounced rise in the current flow or electrical conductivity), which is mostly discontinuouslike—it does not occur instantly, but rather at longer time scales ($t = 1.3 \text{ or } 1.8 \mu s$; Fig. 2A, Left). In addition, such a delay or growth of disorder before an s-to-l transition is not observed when either a low- or high-voltage pulse is applied (e.g., $V = 1.10$ or $1.90 \text{ V}$), i.e., the transition has not occurred or has taken place almost immediately, respectively, meaning that such phenomena occur only around $T_m$.

To investigate the origin of the growth of disorder, the structural disordering of a crystalline GST model at varying temperatures was examined. Recently, we have investigated such disordering essentially at and after an s-to-l transition in GST using AIMD simulations, which have provided new structural and functional insights into the microscopic processes involved (17). We illustrate the power of this approach by examining the structural changes before an s-to-l transition in a GST model, comprising 22 Ge, 22 Sb, and 55 Te atoms, heated between $T = 800$ and 900 K (Methods); these parameters were chosen based on a correlation between the temperature, size, and time scale of the simulational studies (SI Appendix). Generally, during an s-to-l transition, a sharp decrease would occur in the number of ordered structural units, viz. fourfold rings (which are a structural motif of the metastable rock-salt crystal structure of GST), due to the high level of structural disordering characteristic of the liquid/melt phase (20) (Fig. 2B, Right). Indeed, the time evolution of the decay in the number of fourfold rings in the GST models at intermediate temperatures (e.g., $T = 825$ and 850 K) exhibits such transitional characteristics, but only after a (growth of disorder) time of around $t = 50 \mu s$ (Fig. 2B, Left), similar to those observed.

![Fig. 2](https://example.com/f2.png)
experimentally, although the time scale is shorter due to the small GST model used (Fig. 2A, SI Appendix). Moreover, pronounced fluctuations in the number of fourfold rings are observed during the growth of disorder, suggesting the emergence of a premonitory structural disordering.

During the growth of disorder, we found that the GST model exhibits a repeated stretching or “buckling” of the bonds within clusters of atoms, viz. the formation and annihilation of fourfold rings (Fig. 2C), while preserving the essence of crystalline order, which is largely independent of the model size, structural definition, and starting configuration used (SI Appendix). We thus refer to this process as premelting disordering (PD). Such disordering seems to be enabled by the intrinsic ability of the constituent atoms to occupy lower-coordinated sites in the liquid/melt phase than in the solid phase (21, 22) (SI Appendix). It should be noted that the PD phenomenon can be affected by the intrinsic disorder generated by thermal excitations, e.g., vibrational modes and point defects, or grain boundaries; although they should yield similar changes in the material properties that accelerate the approach to an s-to-l transition, regardless of the crystalline structure that remains until the transition itself (23, 24).

The PD phenomenon allows for the precise control of an s-to-l transition in a GST model/cell. In the simulations, the preheated GST model shows a much faster onset of such a transition (t ~10 ps) than a nonpreheated GST model when melted at T = 875 K (t ~40 ps); the former is preheated at T = 825 K for ~35 ps before the melting at T = 875 K, and the latter is melted solely at T = 875 K (Fig. 3A). In addition, including the preheating time, the preheated model requires an overall time of t ~40 ps to complete an s-to-l transition, which is almost identical to that required by the nonpreheated model, meaning that a similar transitional behavior (or outcome) can be achieved via two different excitation schemes (Fig. 3A, Top Right)—this not only allows the Boolean algebraic operations, but also saves energy (during preheating). The same phenomena are observed experimentally for the electrically prewarmed and nonprimed GST cells—they exhibit switching from the crystal to glass states using electrical pulses with lengths of t = 22 (7) ns including (excluding) the priming pulse and t = 25 ns, respectively (Fig. 3B). That is, the switching speed of the cells can be altered, which confirms that such schemes could be applied to practical device operations. In addition, Fig. 3A and B shows that, by preheating the models/cells using a simple priming method, the melting times can be reduced by more than 3.5 times compared with not preheating the models/cells. Furthermore, the switching voltage (in the range V = 3.00 to 1.55 V) and time (in the range t = 25 to 5 ns) decrease with an increase in the amplitude (V = 1.35 to 1.75 V) and length (t = 5 to 20 ns) of a priming pulse (Fig. 3 C and D). This indicates that the degree of PD can be controlled and tuned for achieving multiple Boolean algebraic operations, and possibly even completely new applications.

Both experimental and simulation results suggest that fast, multiple, and low-power Boolean algebraic operations may stem from the cooperative movement of atoms during growth of disorder/priming, leading to a rapid, tunable, and low-energy formation of different glassy structures. At intermediate (high) temperatures, a large (much larger) buckling of bonds of clusters of atoms, evident from the AIMD simulations, will promote atomic diffusion, which is required for structural disordering. This phenomenon would explain both the observed fast switching, and also the multiple electrical-resistance levels and low power consumption seen in the GST cells.

The priming scheme can provide an excellent approach for performing Boolean algebraic operations. The priming scheme can avoid spontaneous crystallization of the initial logic state.

![Control and tuning of the s-to-l transition via the PD phenomenon in GST. (A) Computer simulation of the PD phenomenon in a GST model. (Left) Time evolution of the number of fourfold rings in the preheated and nonpreheated GST models melted at T = 875 K. The preheated model was heated at T = 825 K for two different times of t = 30 and 40 ps before the melting at T = 875 K, and the latter model was melted solely at T = 875 K from two different starting configurations. (Upper Right) Overall melting process, including the evolution of rings during the initial thermal treatment of the preheated models (at T = 825 K for the two different times). (Lower Right) Schematics of the heating profiles used in the simulations. (B) Electrical characterization of the PD phenomenon in a GST cell. (Left) Dependence of the electrical-resistance level of the primed and nonprimed GST cells on the length of a switching pulse at V = 1.70 V. (Upper Right) Complete switching scheme, including the initial electrical stimulation applied to the primed cells with an electrical pulse of V = 1.55 V and t = 15 ns. (Lower Right) Schematics of the electrical pulse waveforms used. Dependence of the pulse amplitude Vp and length t, required to switch the cells on: (C) the amplitude Vp, and (D) the length t, of a priming pulse. Vp and Vp were kept constant at 1.55 and 1.70 V, respectively, when the voltage dependence was not being investigated, and t and t were both maintained to be the same at t = 15 ns when not being used as a variable. The error bars show the range of values obtained from the experiments performed on three different cells.

Loke et al. PNAS. September 16, 2014 vol. 111 no. 37 13275
Before performing the logic operations using the crystallization scheme, the cell needs to be initialized to the amorphous state, and after the logic operations, the cell mostly needs to be reinitialized back to the amorphous state to stand by for the next logic operation (10, 11). In contrast, before/after performing the logic operation using the priming scheme, the cell needs to be initialized/reinitialized back to the crystalline state, and thus, the priming scheme can perform logic operations using stable initial crystallization states, and therefore does not suffer from the unavoidable problem of spontaneous transformation (crystallization) of the initial state plaguing the crystallization logic scheme.

In addition, another advantage of the priming scheme concerns resistance drift in the amorphous state (SI Appendix). Because the initialized state is always the crystalline state, this will not suffer from resistance drift and hence time-dependent corruption of the initial state, in marked contrast to the case of the previous crystallization scheme (10, 11), especially if the reference resistance level of assigning the logical state is used. The fact that the final amorphous state could suffer from eventual resistance drift with time should not be too much of a problem as long as the logic state is always read out immediately after switching.

Furthermore, the priming scheme can allow a much simpler way of reading out the logic outputs than the crystallization scheme. In the crystallization scheme, the logical state is mostly read out by using a final confirm pulse (10). In contrast, in the priming scheme, the logical state can be read out by just using a reference level (which is much simpler) (24) and Quickly. The priming scheme can also perform all logic operations using just one cell, rather than the two cells used by the crystallization scheme (11).

In general, apart from the input energy, the melting kinetics of a solid depend strongly on the strength of bonds between the atoms (25), and thus one interesting avenue for future investigation might be to examine the transient behavior during an s-to-l transition of alternative solid-state or phase-change materials with different structural characteristics, which could display varying PD phenomena. Indeed, it may be fruitful to study the glassesy forms of a phase-change material, where local structural variability, particularly in the strength of bonds, could yield a less-pronounced $T_m$. These future studies would facilitate the use of various types of materials/device structures, in isolation and in combination, to open up new opportunities for optimizing the performance of phase-change–based, in-memory logic devices.

**Methods**

**Cell Structure.** SI Appendix, Fig. S1 shows the structure of a test cell in the lateral or cross-sectional plane, wherein the cell is deposited on an SiO$_2$-on-Si substrate. The cell has a porelike structure comprising a 35-nm-thick phase-change (PC) material layer (Ge$_2$Sb$_2$Te$_5$), which is sandwiched between the top and bottom electrodes (TiW) with thickness of 200 nm. The phase-change material is confined in a 90-nm-wide via formed by an insulating layer (SiO$_2$) with a thickness of 35 nm. The electrodes are used to connect the cell to the external circuitry for the electrical measurements, and the insulating layer provides the electrical and thermal insulation.

**Device Fabrication.** The cells were fabricated using an integrative conventional lithography and nanopatterning technique. Each patterning step was accomplished using 365-nm photolithography (Cannon) or electron-beam lithography (JEOL), followed by the material-deposition and lift-off procedures. All of the materials were deposited using composite targets in a DC magnetron sputtering system (Balzers Cube). A 4-inch Si wafer with a 1-μm-thick SiO$_2$ layer was used as the starting structure, on which a 200-nm-thick TiW bottom electrode was deposited and patterned. An insulating layer, comprising a 35-nm-thick SiO$_2$ layer, was deposited and etched to form vias with diameters of 90 nm. The vias were filled with 35-nm-thick GST to form the active phase-change region. Finally, a 200-nm-thick TiW top electrode was deposited to complete the structure.

**Electrical Characterization.** The electrical performance of the cells was investigated using an in-house built PC device-testing system comprising a picosecond (Picosecond Pulse Labs) or nanosecond- (Tektronix) pulse generator, a digital oscilloscope (Agilent Technologies), and a probe station, as shown in SI Appendix, Figs. S2 and S15. The AIMD simulations were performed using the Cambridge High-Performance Computing Facility. We thank the Data Storage Institute, Agency for Science, Technology and Research, for providing the necessary computational facilities.
Loke et al.