Lecture 9 - MOSFET (I)

MOSFET I-V Characteristics

March 6, 2003

Contents:

1. MOSFET: cross-section, layout, symbols
2. Qualitative operation
3. I-V characteristics

Reading assignment:

Howe and Sodini, Ch. 4, §§4.1-4.3

Announcements: Quiz #1, March 12, 7:30-9:30 PM, Walker Memorial; covers Lectures #1-9; open book; must have calculator.
Key questions

- How can carrier inversion be exploited to make a transistor?
- How does a MOSFET work?
- How does one construct a simple first-order model for the current-voltage characteristics of a MOSFET?
1. **MOSFET**: layout, cross-section, symbols

Key elements:

- inversion layer under *gate* (depending on gate voltage)
- heavily-doped regions reach underneath gate ⇒ inversion layer electrically connects *source* and *drain*
- 4-terminal device: *body* voltage important
Circuit symbols

Two complementary devices:

- n-channel device (n-MOSFET) on p-Si substrate (uses electron inversion layer)
- p-channel device (p-MOSFET) on n-Si substrate (uses hole inversion layer)
2. Qualitative operation

Water analogy of MOSFET:

- **Source**: water reservoir
- **Drain**: water reservoir
- **Gate**: gate between source and drain reservoirs

Want to understand MOSFET operation as a function of:

- gate-to-source voltage (gate height over source water level)
- drain-to-source voltage (water level difference between reservoirs)

Initially consider source tied up to body (substrate or back).
Three regimes of operation:

- **Cut-off regime:**

  - MOSFET: $V_{GS} < V_T$, $V_{GD} < V_T$ with $V_{DS} > 0$.
  - Water analogy: gate closed; no water can flow regardless of relative height of source and drain reservoirs.

\[ I_D = 0 \]
□ **Linear or Triode regime:**

- **MOSFET:** $V_{GS} > V_T$, $V_{GD} > V_T$, with $V_{DS} > 0$.

- **Water analogy:** gate open but small difference in height between source and drain; water flows.

Electrons drift from source to drain $\Rightarrow$ electrical current!

- $V_{GS} \uparrow \rightarrow |Q_n| \uparrow \rightarrow I_D \uparrow$

- $V_{DS} \uparrow \rightarrow E_y \uparrow \rightarrow I_D \uparrow$
**Saturation regime:**

- **MOSFET:** \( V_{GS} > V_T, V_{GD} < V_T \) \((V_{DS} > 0)\).

- Water analogy: gate open; water flows from source to drain, but free-drop on drain side \(\Rightarrow\) total flow independent of relative reservoir height!

\[ I_D \text{ independent of } V_{DS}: I_D = I_{D_{sat}} \]
3. I-V characteristics

Geometry of problem:

\[ V_{BS} = 0 \]
\[ V_{GS} > V_T \]
\[ V_{DS} \]
\[ I_D \]

\[ J_y = Q_n(y)v_y(y) \]

Total channel current:

\[ I_y = WQ_n(y)v_y(y) \]

Drain terminal current is equal to \textit{minus} channel current:

\[ I_D = -WQ_n(y)v_y(y) \]
\begin{equation}
I_D = -WQ_n(y)v_y(y)
\end{equation}

Rewrite in terms of voltage at channel location \( y \), \( V_c(y) \):

- If electric field is not too big:

\[
v_y(y) \simeq -\mu_n E_y(y) = \mu_n \frac{dV_c(y)}{dy}
\]

- For \( Q_n(y) \) use charge-control relation at location \( y \):

\[
Q_n(y) = -C_{ox}[V_{GS} - V_c(y) - V_T]
\]

for \( V_{GS} - V_c(y) \geq V_T \).

All together:

\[
I_D = W\mu_n C_{ox}(V_{GS} - V_c(y) - V_T)\frac{dV_c(y)}{dy}
\]

Simple linear first-order differential equation with one unknown, the channel voltage \( V_c(y) \).
Solve by separating variables:

\[ I_D dy = W \mu_n C_{ox} (V_{GS} - V_c - V_T) dV_c \]

Integrate along the channel in the linear regime:

- for \( y = 0 \), \( V_c(0) = 0 \)
- for \( y = L \), \( V_c(L) = V_{DS} \) (linear regime)

Then:

\[ I_D \int_0^L dy = W \mu_n C_{ox} \int_0^{V_{DS}} (V_{GS} - V_c - V_T) dV_c \]

or:

\[ I_D = \frac{W}{L} \mu_n C_{ox} (V_{GS} - \frac{V_{DS}}{2} - V_T) V_{DS} \]
For small $V_{DS}$:

$$I_D \approx \frac{W}{L} \mu_n C_{ox} (V_{GS} - V_T)V_{DS}$$

Key dependencies:

- $V_{DS} \uparrow \rightarrow I_D \uparrow$ (higher lateral electric field)
- $V_{GS} \uparrow \rightarrow I_D \uparrow$ (higher electron concentration)
- $L \uparrow \rightarrow I_D \downarrow$ (lower lateral electric field)
- $W \uparrow \rightarrow I_D \uparrow$ (wider conduction channel)

This is the *linear* or *triode* regime.
In general,

\[ I_D = \frac{W}{L} \mu_n C_{ox} (V_{GS} - \frac{V_{DS}}{2} - V_T) V_{DS} \]

Equation valid if \( V_{GS} - V_c(y) \geq V_T \) at every \( y \).

Worst point is \( y = L \), where \( V_c(y) = V_{DS} \), hence, equation valid if \( V_{GS} - V_{DS} \geq V_T \), or:

\[ V_{DS} \leq V_{GS} - V_T \]

term responsible for bend over of \( I_D \): \( -\frac{V_{DS}}{2} \)
To understand why $I_D$ bends over, must understand first channel debiasing:

Along channel from source to drain:

$$y \uparrow \rightarrow V_c(y) \uparrow \rightarrow |Q_n(y)| \downarrow \rightarrow |E_y(y)| \uparrow$$

Local ”channel overdrive” reduced closer to drain.
Impact of $V_{DS}$:

As $V_{DS} \uparrow$, channel debiasing more prominent
$\Rightarrow I_D$ rises more slowly with $V_{DS}$
1.5 × 46.5 NMOSFET

Output characteristics ($V_{GS} = 0 - 3 \, V$, $\Delta V_{GS} = 0.5 \, V$):

Zoom close to origin:
Transfer characteristics ($V_{DS} = 0.1\ V$):
Key conclusions

• The MOSFET is a field-effect transistor:
  – the amount of charge in the inversion layer is controlled by the field-effect action of the gate
  – the charge in the inversion layer is mobile ⇒ conduction possible between source and drain

• In the linear regime:
  – $V_{GS}$ ↑⇒ $I_D$ ↑: more electrons in the channel
  – $V_{DS}$ ↑⇒ $I_D$ ↑: stronger field pulling electrons out of the source

• Channel debiasing: inversion layer ”thins down” from source to drain ⇒ current saturation as $V_{DS}$ approaches:

$$V_{DS_{sat}} = V_{GS} - V_T$$