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A 58nW ECG ASIC with Motion-tolerant Heartbeat Timing Extraction for Wearable Cardiovascular Monitoring

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***Abstract*—An ASIC for wearable cardiovascular monitoring is implemented using a topology that takes advantage of the electrocardiogram's (ECG) waveform to replace the traditional ECG instrumentation amplifier, ADC, and signal processor with a single chip solution. The ASIC can extract heartbeat timings in the presence of baseline drift, muscle artifact, and signal clipping. The circuit can operate with ECGs ranging from the chest location to remote locations where the ECG magnitude is as low as $30\mu V$. Besides heartbeat detection, a midpoint estimation method can accurately extract the ECG R-wave timing, enabling the calculations of heart rate variability. With $58nW$ of power consumption at $0.8V$ supply voltage and $0.76mm^2$ of active die area in standard $0.18\mu m$ CMOS technology, the ECG ASIC is sufficiently low power and compact to be suitable for long term and wearable cardiovascular monitoring applications under stringent battery and size constraints.**

***Index Terms*—Electrocardiogram, heart rate, motion artifacts, cardiovascular monitoring, wearable sensor.**

I. Introduction

CARDIOVASCULAR disease (CVD) affects 37% of the United States population and is the leading cause of death in the U.S. [1]. One type of CVD is cardiac arrhythmia, which is characterized by irregular heartbeat intervals. The most common form of cardiac arrhythmia is atrial fibrillation (AF) [2]. AF occurs when the atrium exhibits rapid and irregular contractions. AF is often undiagnosed, but increases the risk of stroke and heart failure by up to nine times [2]. Another example of arrhythmia is premature ventricular contraction (PVC). PVC's can be the symptom of an underlying CVD such as cardiomyopathy. Both AF and PVC can be identified using continuous heartbeat timing monitoring [3].

The electrocardiogram (ECG) is a non-invasive surface measurement of the heart's electrical potentials and is a primary tool for the assessment of cardiac health. Traditionally, the topology for an ECG heartbeat detection circuit consists of a low noise instrumentation amplifier (IA), an anti-alias filter, an ADC, and a digital processor [4] [5] [6]. This topology is shown in Fig. 1(a) along with a labeled ECG in Fig. 1(c).

In this conventional topology, the IA amplifies the differential ECG signal with low noise op amps. The gain of the IA is set so that the amplified output is not saturated. After the anti-alias filter, the ADC uniformly quantizes the ECG signal, treating small features such as the ECG's P-wave and large features such as the ECG's R-wave with equal resolution. The ADC is usually implemented with a medium resolution SAR architecture to minimize power consumption. Finally, to detect heartbeats, the digitized ECG is processed using an algorithm to detect R-waves. Depending on the computational power available, such an algorithm ranges from simple thresholding to wavelet transforms. Even with a deep subthreshold digital processor such as in [6], the digital R-wave detection algorithm can consume three times higher power than the analog front end.

The traditional topology is necessary for clinical ECG measurements, where multi-lead ECG signals are acquired with high fidelity in order to diagnose arrhythmias. These recordings are usually quantized with at least 12 bits to preserve P-wave details [7]. The American Heart Association recommends a sampling frequency of at least $150Sa/s$ to capture all features, while stating that a bandwidth of $1Hz$ to $30Hz$ generally produces a stable ECG without artifacts [8].

However, as mentioned, common arrhythmias can be detected with heartbeat timing monitoring where only the R-wave timing is needed. To take advantage of this fact, a new topology is presented that removes the need for the ADC and the signal processor to decrease the overall circuit's complexity, power, and area. The demonstrated ASIC receives the ECG signal as an analog input and outputs a digital heartbeat signal, while being tolerant to signal interferers such as motion artifacts.

This paper is organized into the following sections. Section II explains how the proposed topology operates. Section III discusses each circuit block in detail. In Section IV, measured results from both testbench and human subject tests are presented. Furthermore, a method to accurately extract R-wave timings from the ASIC output is validated using clinical data.

II. Proposed Circuit Topology

The proposed topology is based on the fact that heartbeat detection relies on the ECG's QRS complex, which has a higher frequency content and a greater magnitude than the adjacent ECG features. This circuit topology is shown in Fig. 1(b).

In Fig. 1(b), the differential ECG signal is first amplified by a low noise programmable gain amplifier (PGA). The PGA's output signal is split into two paths. The first path goes through the "QRS Amp," which has a bandwidth that

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preserves the QRS complex. The second path goes through the "Baseline Amp," which has an equal gain but a lower bandwidth to preserve only the low frequency baseline drift caused by motion artifacts. Then, a positive inline DC offset V_{DC} is added to $V_{Baseline}$ to create an adaptive threshold $V_{Baseline+DC}$. A QRS complex (or heartbeat) occurs whenever $V_{QRS} > V_{Baseline+DC}$. This comparison is performed by a comparator, which consequently pulses a high D_{OUT} when a heartbeat is detected.

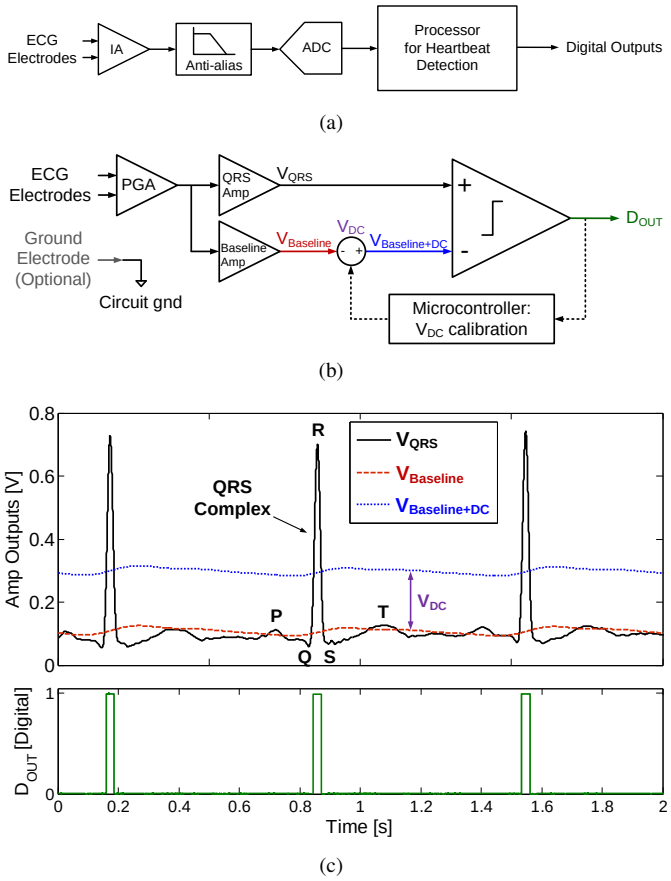

Fig. 1. a) The traditional topology for ECG heartbeat detection, b) the proposed topology with voltage nodes labeled, and c) an ECG waveform illustrating the QRS complex, baseline, baseline with V_{DC} offset, and digital output.

To correctly set V_{DC}, it is incremented until the period between D_{OUT} pulses is regular and is in the range of human beat-to-beat interval. As shown in Fig. 1(c), there is a wide range of valid V_{DC} values since V_{DC} can be set at any level between the R-wave and the next highest amplitude feature (usually the T-wave). Because respiration causes slight baseline modulation of the ECG, we use four respiratory cycles to complete the V_{DC} calibration routine, which takes 20 seconds on average. This calibration is performed at the beginning of measurement by an external microcontroller that consumes $5\mu A$ at a clock frequency of $4kHz$, which is powered off afterwards.

During measurement, V_{DC} may need to be recalibrated if the measurement condition changes significantly due to motion artifacts or muscle noise. The need to recalibrate V_{DC} can be detected in real time when D_{OUT} exceeds the human heart rate range or when D_{OUT} becomes irregularly spaced. Once detected, the initial calibration routine can be rerun to update V_{DC}. If the irregular D_{OUT} is caused by actual irregular R-waves, then the recalibration will be unable to complete, in which case arrhythmia can be implied.

There are several advantages to this topology in terms of circuit design. First, no signal processor or ADC is required, which significantly reduces the device's power and area. Second, a low voltage supply is possible because a clipped R-wave that exceeds the amplifier's output range still possesses heartbeat information. Third, any comparator offset is automatically compensated due to the V_{DC} calibration. Fourth, amplifier linearity is unimportant because the signal path is highly nonlinear. In terms of practical usage, this topology is tolerant to motion artifacts because the signal is differentially compared against its own baseline. Furthermore, no predefined subject-dependent parameters are needed.

III. Circuit Design

A. Programmable Gain Amplifier

The PGA's function is to amplify the ECG directly from the electrodes with minimal circuit noise and power while having a range of gain to adapt to various ECG amplitudes. Fig. 2 shows the schematic of the PGA, which consists of an op amp in the difference configuration.

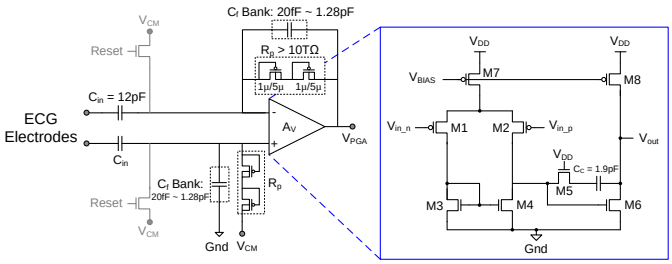

Fig. 2. The PGA schematic.

Sensing a biopotential such as the ECG creates several circuit requirements. First, because the ECG amplitudes vary between different body locations and different subjects by up to two orders of magnitude, an adjustable gain is required. The gain of the PGA is set by C_{in}/C_f, where $C_{in} = 12pF$ and C_f is implemented as a 6-bit binary weighted capacitor bank of $20fF$ to $1.28pF$ to adjust the PGA gain from $19dB$ to $56dB$.

Second, the AgCl electrode's half-cell potential generates approximately $200mV$ of near-DC electrode offset voltage (EOV) which would saturate the amplifier if not removed. To filter this EOV, PMOS pseudo-resistors (R_p) are used [9]. The R_p's are greater than $10T\Omega$ but only occupy $10\mu m^2$, thus enabling on-die sub-Hz high pass filters and effectively removing the EOV. The large R_p also allows the DC biasing of the amplifier inputs while maintaining a high input impedance, which is needed due to the capacitive C_{in}. Furthermore, because the input impedance is significantly larger than $R_{elec} \approx 300k\Omega$, any differential voltage caused by unequal and varying R_{elec} (such as during motion) is negligible.

It should be noted that the high impedance at the PGA input nodes leads to long start-up settling times. As a solution, reset switches shown in Fig. 2 are added to the PGA inputs to immediately shunt the input nodes to their final common-mode DC voltage V_{CM} during start-up.

The PGA's op amp is a two-stage Miller-compensated op amp. This topology is chosen because of its compatibility with low voltage supply, wide output swing, and self-biasing. Due to the low frequency and bandwidth requirements of ECG signals ($1Hz - 25Hz$), the PGA can operate in deep subthreshold with $90nA$ of bias current. The low g_m leads to a greater thermal noise spectral density, but the thermal noise contribution is limited because of the PGA's low bandwidth.

At this frequency, the dominant noise source is $1/f$ noise. Chopper modulation at the PGA inputs is a possible method to eliminate $1/f$ noise. However, chopper switches introduce a current path between the PGA inputs. If there is any input offset voltage, then an offset current would exist that can saturate the PGA through the high resistance feedback R_p. A solution is to use a $G_M - C$ servo-loop to provide a current path, but it consumes additional current [10]. Without chopping, the input $1/f$ noise can be designed to be within $1\mu V_{rms}$ ($0.5Hz - 50Hz$) by appropriate transistor sizing, which is acceptable for ECG signals that are typically at $1mV$. For these reasons, chopper modulation is not used.

The input-referred $1/f$ noise spectral density for this op amp is shown in Equation (1), where $(g_{m3}/g_{m1})^2 = 1$ when in subthreshold [11]:

$$\frac{v_{ifsub}^2}{\Delta f} = \frac{2 \cdot K_1}{W_1 L_1 C_{ox}^2 f} + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \cdot \frac{2 \cdot K_3}{W_3 L_3 C_{ox}^2 f} \quad (1)$$

According to Equation (1), several design choices are made to minimize $1/f$ noise. First, PMOS input transistors are used because they offer lower noise coefficients than NMOS transistors: $K_1 = K_p < K_n$. Second, increasing W_1 and L_1 will reduce the noise contribution of the input transistors. However, excessive input transistor area will introduce significant parasitic capacitance at the drain of M2. This decreases the frequency of the second pole and lowers the phase margin. A dimension of $864\mu m/1.5\mu m$ (96 fingers of $9\mu m/1.5\mu m$) is chosen so that M1 and M2's $1/f$ noise contributes to 40% of total input noise. Third, increasing W_3 and L_3 will reduce the noise contribution of the mirror transistors. However, signal swing places an upper limit on W_3 and process technology places an upper limit on L_3. A dimension of $100\mu m/20\mu m$ (8 fingers of $12.5\mu m/20\mu m$) is chosen so that M3 and M4's $1/f$ noise contributes to 20% of total input noise.

B. QRS and Baseline Amplifiers

The PGA's output is connected to the inputs of the QRS and Baseline Amps. The function of the QRS Amp is to amplify the ECG signal with a bandwidth that passes the QRS complex. Meanwhile, the Baseline Amp has the same gain but has a lower bandwidth that only passes the baseline signal.

In Fig. 3, both amplifiers use identical two-stage Miller-compensated op amps in the non-inverting configuration. The only difference is in the compensation capacitors (C_C). The Miller multiplied C_C and a $0.5nA$ bias current create very low corner frequencies while being area-efficient. For the QRS Amp, $C_C = 560fF$ sets the low pass corner frequency at $25Hz$, which passes the QRS complex. For the Baseline Amp, $C_C = 15pF$ sets the low pass corner frequency at $1Hz$, which only passes the baseline drift. Pseudo-resistors are used to bias the inverting node.

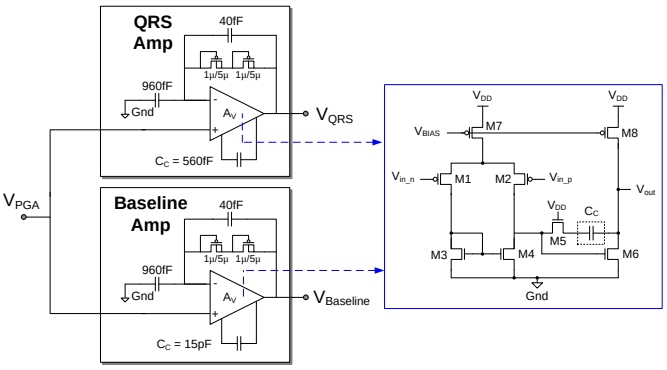

Fig. 3. The QRS Amp and the Baseline Amp schematic.

Both QRS and Baseline Amps have a fixed gain of $960fF/40fF = 28dB$, thus resulting in an overall gain range of $47dB$ to $84dB$. At this overall gain range and with $V_{DD} = 0.8V$, the full dynamic range can be used to measure ECG signals at various wearable locations on the body where the ECG ranges from approximately $30\mu V_{pp}$ to $3mV_{pp}$.

C. V_{DC} Generator

The V_{DC} generator's function is to add V_{DC} to $V_{Baseline}$ to produce an adaptive threshold $V_{Baseline+DC}$. The V_{DC} generator schematic is shown in Fig. 4.

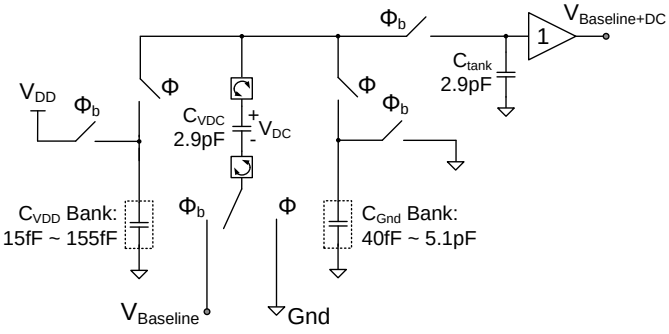

Fig. 4. The V_{DC} generator schematic.

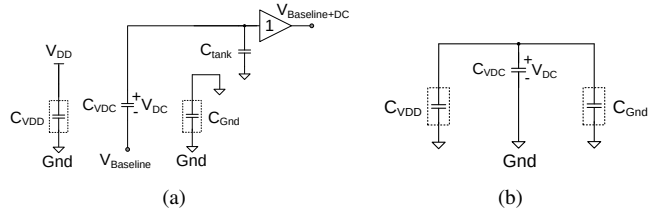

Fig. 5. The V_{DC} generator in a) clock phase Φ_b and b) clock phase Φ.

C_{VDD} is a 4-bit binary weighted capacitor bank of $15fF$ to $155fF$, and C_{Gnd} is a 7-bit binary weighted capacitor bank of $40fF$ to $5.1pF$. C_{VDD} and C_{Gnd} values are selected during the initial V_{DC} calibration by the microcontroller.

Non-overlapping clock phases Φ and Φ_b are generated on-chip at $2.0kHz$ by a clock generator. The clock frequency is chosen as a compromise between low power (favors lower frequency) and low charge leakage (favors higher frequency).

During clock phase Φ_b (Fig. 5(a)), C_{VDD} and C_{Gnd} are respectively reset to V_{DD} and ground. During the following clock phase Φ (Fig. 5(b)), C_{VDC} is charged to a final voltage of $V_{DC} = V_{DD}C_{VDD}/(C_{VDD}+C_{Gnd})$. During the following clock phase Φ_b, V_{DC} is added to $V_{Baseline}$ to produce $V_{Baseline+DC}$, while C_{VDD} and C_{Gnd} are again reset. C_{tank} is present to reduce voltage ripples. With the selectable ranges of C_{VDD} and C_{Gnd}, V_{DC} can be adjusted from 0% to 80% of V_{DD}. This range covers most situations where the interferer or noise occupies up to 80% of V_{DD} while having a lower amplitude than the R-wave.

In consideration for long term at-home usage where the ECG electrodes are applied by the wearer, the V_{DC} generator has the ability to generate negative V_{DC} if the user accidentally reverses the electrodes. This is symbolized by the two digital blocks in Fig. 4 that can flip C_{VDC} during phase Φ_b. In the case that the ECG is reversed and C_{VDC} is flipped, then the heartbeat occurs when $D_{OUT} = 0$ instead of $D_{OUT} = 1$. These digital blocks are expanded in Fig. 6(a).

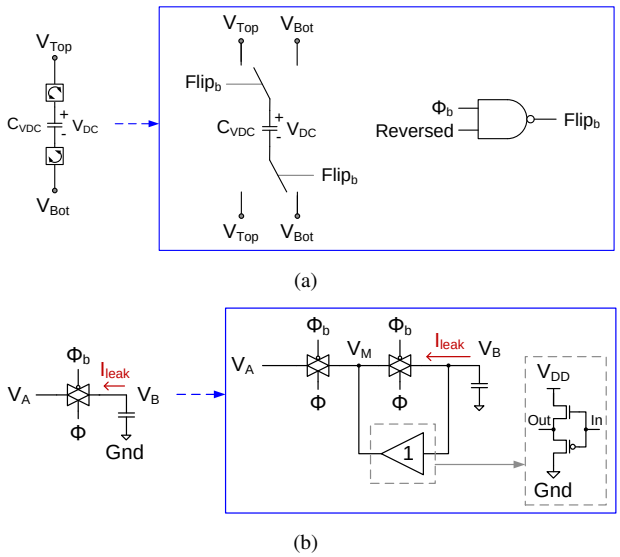

Fig. 6. The V_{DC} generator's internal circuit blocks: a) C_{VDC} can be flipped during phase Φ_b in the case of reversed electrodes, and b) the low leakage switch implementation to prevent capacitor discharge [12].

Because the switching frequency is only $2.0kHz$ and $C_{VDC} = 2.9pF$, a leakage current of only $5.8pA$ can reduce V_{DC} by $1mV$ between clock cycles. To reduce switch leakage, stacked switches with a push-pull buffer are implemented based on [12]. The switch schematic is shown in Fig. 6(b) and is used for all switches in Fig. 4. The two stacked switches in Fig. 6(b) exponentially reduce the subthreshold I_{leak} by decreasing the $|V_{GS}|$ of the two switches. The push-pull buffer drives V_M to the same voltage as V_B, thus further decreasing I_{leak} by reducing the $|V_{DS}|$ of the switch closest to the capacitor. All switch and buffer transistors are minimally sized (PMOS: $400nm/180nm$, NMOS: $220nm/180nm$) to reduce the effect of charge injection.

D. Comparator

The comparator's role is to output a digital pulse when a QRS complex has occurred, which is when $V_{QRS} > V_{Baseline+DC}$. A dynamic latched comparator based on [13] is used (Fig. 7). The dynamic topology is chosen because it consumes power only when latching. This topology offers the additional benefit of only using a single clock signal Φ, thus placing no requirements on Φ_b timing.

M11 and M12 are added to reduce short circuit currents through M13-M16 when V_L and V_R are transitioning. This is important because short circuit currents of several nano-amps can be a significant portion of the overall power. $V_{Baseline+DC}$ contains switching transients from the V_{DC} generator. However, these transients are designed to occur with Φ_b, which do not affect comparator accuracy because comparator latching occurs with Φ.

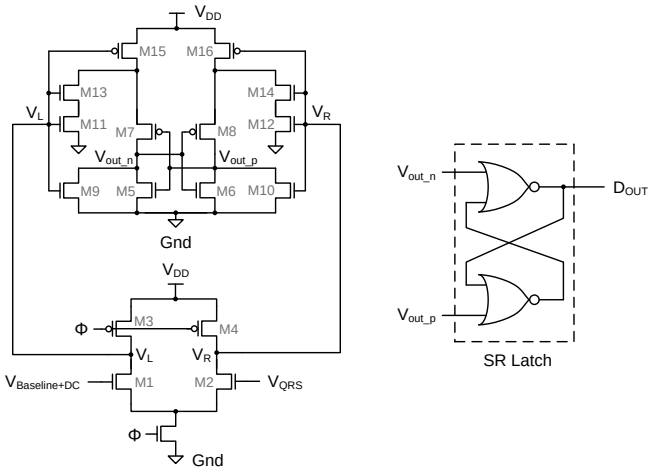

Fig. 7. The dynamic latched comparator with SR latch. The comparator is based on [13].

M1-M4 gate lengths are set at $1\mu m$ to reduce geometry mismatch. A Monte Carlo mismatch simulation of 100 runs produces an input-referred comparator offset range of $-13mV$ to $16mV$. However, as mentioned in Section II, no comparator offset compensation is needed due to the V_{DC} calibration routine. The final output of the SR latch, D_{OUT}, is a digital signal that pulses when a heartbeat is detected.

E. Peripheral Circuits

All peripheral circuits and passive components are implemented on-chip. These circuits include a fast startup current reference for the amplifiers based on [14], a diode ladder voltage reference to generate the common-mode voltage for the PGA, and a clock generator that provides the $2.0kHz$ non-overlapping clock signals for the V_{DC} generator and the comparator.

IV. Measurement Results

The ASIC is fabricated using a standard TSMC $0.18\mu m$ 1P6M CMOS technology. The die area is $1.8mm \times 1.8mm$ with an active area of $0.76mm^2$ as shown in Fig. 8.

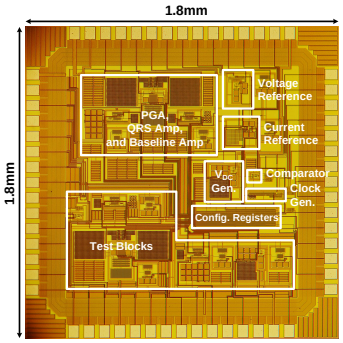

Fig. 8. Die micrograph of the ECG ASIC with the circuit blocks labeled.

A. Testbench Measurements

The ECG's amplification path goes through the PGA and then the QRS Amp. Fig. 9 shows the gain response and input-referred noise response at the highest gain setting. In the gain response, the plot shows the sub-Hz high pass corner enabled by the PGA and QRS Amp's pseudo-resistors, the low pass corner implemented by the QRS Amp's low g_m and large C_c, and the $40dB/dec$ falloff at higher frequencies due to the two poles from the PGA and the QRS Amp. In terms of noise response, the circuit exhibits a $1/f$ characteristic below $10Hz$ (or $1/\sqrt{f}$ when plotted as $V/\sqrt{Hz}$).

TABLE I
Simulated vs. measured results from the PGA-QRS Amp signal path.

Parameter	Simulated	Measured
Programmable gain range	47 dB – 84 dB	47 dB – 88 dB
Passband	0.52 Hz – 51 Hz	0.50 Hz – 22 Hz
Unity-gain bandwidth	6.4 kHz	2.9 kHz
Input-referred noise (in band)	0.99 μV_{rms}	2.7 μV_{rms}
CMRR	78 dB	66 dB
PSRR	53 dB	61 dB
Current consumption (at 0.8 V)	92 nA	64 nA

Table I compares the simulated and measured results from the PGA-QRS Amp signal path. Increasing the transistor bias currents did not appreciably decrease the input-referred noise, which indicates that the in-band noise is $1/f$ dominated as Fig. 9 indicates. Because of this, the actual PGA's bias current is lowered compared to simulation, and the reduced low pass frequency of $22Hz$ remains sufficient to preserve the ECG's QRS complex. The measured input-referred noise is greater than the simulated noise by 2.7 times, which is likely attributed to differences between the transistor model's and the actual transistor's $1/f$ characteristics. The measured level of noise is compatible with sensing the ECG, where the QRS amplitude is typically $1mV_{pp}$.

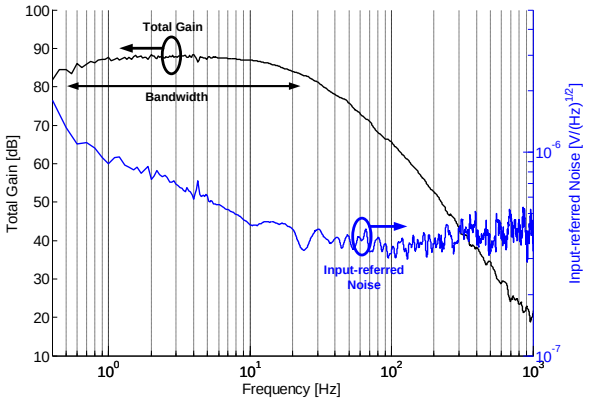

Fig. 9. The measured PGA-QRS Amp signal path's gain response and noise response.

Table II lists the power consumption of each circuit block at $V_{DD} = 0.8V$. 87% of the total power is allocated to the PGA due to bandwidth and thermal noise considerations. The peripheral circuits consume 8.6% of the total power. The ECG ASIC's elimination of the ADC and the signal processor enables it to reduce power consumption. Another portion of the power saving is contributed by the PGA's low bandwidth. A further source of power saving is the ECG ASIC's low V_{DD}, which is enabled by its tolerance to signal clipping.

TABLE II
Simulated vs. measured power consumption of each circuit block at $V_{DD} = 0.8V$.

Circuit block	Simulated Power (nW)	Measured Power (nW)
PGA	72.8	50.4
QRS Amp	0.5	0.7
Baseline Amp	0.5	0.7
V_{DC} generator	1.6	0.8
Comparator	0.3	0.4
Current reference	2.2	1.8
Voltage reference	2.2	1.0
Clock generator	2.0	2.2
Total	82.0	58.0

B. ECG Measurements

Fig. 10(a) to 10(d) show measured ECG and digital outputs from various wearable ECG scenarios to demonstrate the ASIC's robustness in the presence of baseline drift, muscle artifacts, and attenuated signal.

In Fig. 10(a), the at-rest chest ECG offers $1.8mV_{pp}$ of stable signal. Here, V_{DC} is set to $0.3V$ so that $V_{Baseline+DC}$ is approximately half of the V_{QRS} amplitude. However, any V_{DC} setting between $0.1V$ and $0.65V$ would produce the correct digital QRS output at D_{OUT}.

In Fig. 10(b), the chest ECG contains significant baseline drift due to motion. Despite the baseline drift, the same V_{DC} setting as in Fig. 10(a) results in a correct D_{OUT}. In fact, any V_{DC} setting between $0.1V - 0.5V$ would be valid. This demonstrates the ASIC's tolerance to motion artifacts because its adaptive threshold $V_{Baseline+DC}$ tracks the baseline drift.

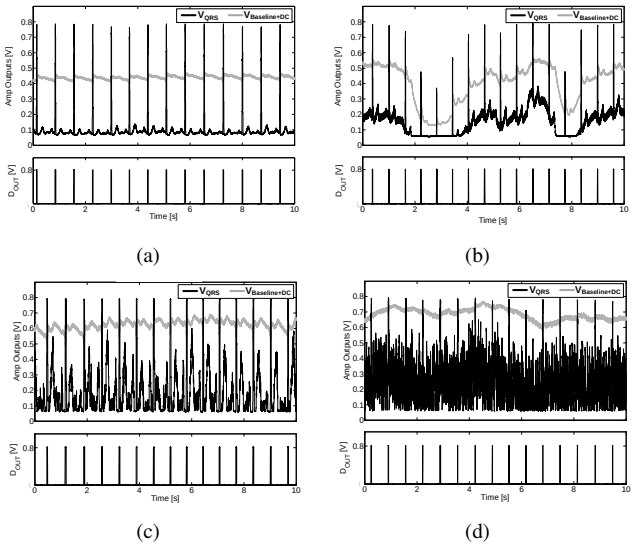

Fig. 10. a) Measured chest ECG at rest ($gain = 52dB$), b) measured chest ECG with baseline drift due to motion artifacts ($gain = 52dB$), c) measured chest ECG with muscle noise and signal clipping ($gain = 64dB$), and d) measured head ECG with high gain due to attenuated signal ($gain = 84dB$).

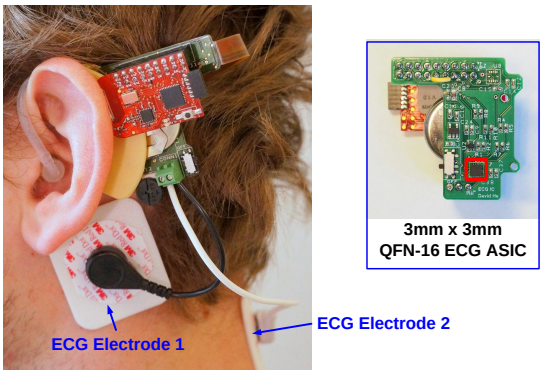

Fig. 11. The wearable ASIC board at the head with wireless data transmission to a computer.

In Fig. 10(c), pectoral muscle artifacts are present from a rapid horizontal 90° arm movement. Also, an intentional high gain of $64dB$ increases the amplified ECG to $2.8V_{pp}$, which is beyond $V_{DD} = 0.8V$ and is clipped. To produce the correct D_{OUT}, V_{DC} needs to be increased to $0.5V$ so that $V_{Baseline+DC}$ rises above V_{QRS}'s muscle artifacts and amplified T-waves. The QRS complex's clipping does not matter because the beat information is still present. This scenario is an example of a significant change of measurement condition leading to a new V_{DC} setting.

To test the ASIC in the presence of an attenuated ECG signal, we mount it at the head so that the ECG is measured across the ear and the middle upper neck as shown in Fig. 11. The ECG at this location is in the range of $30\mu V_{pp} - 40\mu V_{pp}$, which is two orders of magnitude smaller than the standard chest ECG. This attenuation is due to the pattern of the ECG field lines at the head, which yield a very small potential difference when projected onto the lead. Because of this attenuation, the head ECG has a poor signal-to-noise ratio and only R-waves are immediately visible [15].

Due to the attenuation, the gain is increased to $84dB$ to sense the $30\mu V_{pp}$ of ear ECG. At this high gain, a significant portion of the amplified output is noise and R-wave clipping is present, leading to an SNR of only $2.7dB$. However, with the identical V_{DC} setting as in Fig. 10(a) and 10(b), $V_{Baseline+DC}$ is able to rise above the noise and correctly capture the heartbeats as shown by D_{OUT} in Fig. 10(d).

C. Recovering the ECG R-wave Timing from D_{OUT}

While D_{OUT} provides an approximate timing of the ECG R-wave, an accurate ECG R-wave timing is necessary for several cardiovascular monitoring applications such as the calculation of heart rate variability for disease prediction.

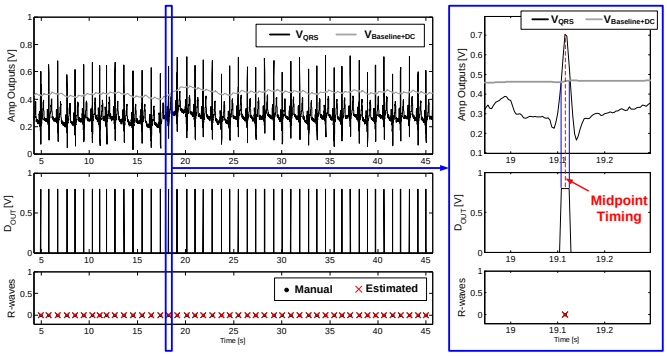

Fig. 12. Estimation of the R-wave timing using the midpoint timing of D_{OUT}.

Although the R-wave's peak is clipped in D_{OUT}, the original R-wave timing can still be recovered with minimal error. As shown by Fig. 12, the R-wave timing can be estimated from the midpoint timing of D_{OUT} pulses. This method is tested on normal chest ECG records from ten subjects totaling 2,304 heartbeats from the MIT-BIH PhysioNet database and from our MIT clinical test (MIT IRB approval #1104004449). Midpoint estimated R-wave timings are compared with manually annotated timings, the results of which are summarized in Table III.

TABLE III
COMPARISON BETWEEN MIDPOINT-ESTIMATED R-WAVE TIMINGS AND MANUALLY ANNOTATED R-WAVE TIMINGS FROM TEN SUBJECTS.

Subject	Number of Beats	Mean R-wave Timing Error [ms]	Stdev. R-wave Timing Error [ms]	Sampling Freq. [Hz]
1	250	0.91	1.6	250
2	183	0.91	1.6	250
3	63	0.97	2.2	250
4	123	-1.70	1.6	250
5	73	-2.40	1.8	250
6	467	-1.50	0.71	500
7	363	-1.00	0.71	500
8	357	-2.80	0.72	500
9	226	-0.88	0.72	500
10	199	-0.29	0.84	500
Overall	**2,304**	**-0.70**	**1.25**	-

In all ten subjects, the standard deviation of R-wave timing error is less than the sampling period. This demonstrates that the R-wave midpoint estimation method can accurately recover the ECG peak timing information from D_{OUT}. This enables the use of the ECG ASIC for applications beyond heartbeat detection, such as heart rate variability analysis, where accurate R-wave timing is necessary.

V. Conclusion

An ECG ASIC for wearable heart monitoring is presented that takes advantage of the ECG's characteristics to extract heartbeat timings in the presence of motion artifacts, muscle noise, signal clipping, and attenuated ECG signals as low as $30\mu V$. Besides heartbeat detection, the R-wave timing is extracted using a midpoint estimation method. R-wave timings can be used for the calculation of predictive cardiovascular parameters such as heart rate variability.

Implemented using a standard $0.18\mu m$ 1P6M CMOS technology, the ASIC consumes $58nW$ of power at $0.8V$ supply and occupies $0.76mm^2$ of active die area. The ECG ASIC has sufficiently low energy consumption for one year of continuous operation from a $0.7mAh$ thin-film battery, making it ideal for miniaturized and long term heartbeat monitoring in extremely battery constrained applications such as implantable pacemakers and defibrillators. Furthermore, the ECG ASIC's power consumption is in range of energy harvesting power sources, thus making batteryless heartbeat monitoring a possibility.

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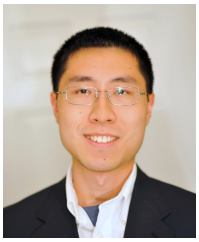

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