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Citation: Lee, Kwang Hong, Yew Heng Tan, Adam Jandl, Eugene A. Fitzgerald, and Chuan Seng Tan. "Comparative Studies of the Growth and Characterization of Germanium Epitaxial Film on Silicon (001) with 0° and 6° Offcut." Journal of Electronic Materials 42, no. 6 (March 26, 2013): 1133–1139.

As Published: http://dx.doi.org/10.1007/s11664-013-2538-7

Publisher: Springer US

Persistent URL: http://hdl.handle.net/1721.1/105856

Version: Author's final manuscript: final author's manuscript post peer review, without publisher's formatting or copy editing

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Massachusetts Institute of Technology

Journal of ELECTRONIC MATERIALS, Vol. 42, No. 6, 2013
DOI: 10.1007/s11664-013-2538-7
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Comparative Studies of the Growth and Characterization of Germanium Epitaxial Film on Silicon (001) with 0° and 6° Offcut

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The quality of germanium (Ge) epitaxial films grown directly on silicon (Si) (001) with 0° and 6° offcut orientation using a reduced-pressure chemical vapor deposition system is studied and compared. Ge film grown on Si (001) with 6° offcut presents ~65% higher threading dislocation density and higher root-mean-square (RMS) surface roughness (1.92 nm versus 0.98 nm) than Ge film grown on Si (001) with 0° offcut. Plan-view transmission electron microscopy also reveals that threading dislocations are more severe (in terms of contrast and density) for the 6° offcut. In addition, both high-resolution x-ray diffraction and Raman spectroscopy analyses show that the Ge epilayer on 6° offcut wafer presents higher tensile strain. The poorer quality of the Ge film on Si (001) with 6° offcut is a result of an imbalance in Burgers vectors that favors dislocation nucleation over annihilation.

Key words: Germanium, offcut, heteroepitaxy, reduced-pressure chemical vapor deposition

INTRODUCTION

For the past few decades, rigorous scaling methods have been driving silicon (Si) complementary metal–oxide–semiconductor (CMOS) technology to maintain device performance, decrease power consumption, and reduce cost per transistor.[1,2] As the device size approaches the scaling limit, a paradigm shift has occurred in the industry from dimensional scaling alone to materials innovation. One such example is the compound III–V materials, which have unique properties for future high-speed and low-power computation applications.[3–9] Most of the III–V materials show 20× to 70× higher electron mobility and ~20× higher conductivity compared with Si. In addition, the feasibility of bandgap engineering in III–V materials enables fabrication of devices suitable for communications and optoelectronics applications. However, III–V materials are not able to replace Si completely because the substrates are expensive and smaller in size due to brittleness (wafer diameters are typically less than 200 mm). Therefore, III–V materials have to be integrated onto a Si substrate in order to be compatible with mainstream CMOS manufacturing. To realize III–V materials integration on low-cost, mechanically stronger Si substrates, a number of research groups have investigated III–V growth on Si for optoelectronic and microelectronic applications.[10,11]

The main challenges of producing high-quality III–V materials on Si are: (i) the large lattice mismatch between the two materials [in the case of gallium arsenide (GaAs), the mismatch is 4.1%], and (ii) the formation of antiphase domains (APDs) due to the polar compound semiconductor growth on

(Received August 31, 2012; accepted February 7, 2013; published online March 26, 2013)

a nonpolar elemental structure. In an attempt to resolve challenge (i), germanium (Ge), which has a lattice constant perfectly matched to GaAs (0.07% at 300 K) and superior electron and hole mobility compared with Si, can be grown on Si to provide a buffer layer for integration and fabrication of GaAs-based devices on a Si substrate.[12–15] Since Ge and GaAs have diamond and zincblende structure, respectively, two possible sublattice allocations are possible for the GaAs layer, although they have exactly the same crystal structure. In one allocation, Ga atoms occupy the face-centered cubic (FCC) sublattice containing the cubic corners, whereas in the other allocation, As atoms occupy this FCC sublattice. Each allocation is rotated by 90° with respect to the other, corresponding to a switching of the cation and anion sublattices. These distinct domains of each sublattice are usually called antiphase domains (APDs). An APD is separated by a plane of incorrect nearest-neighbor bonds (e.g., Ga–Ga or As–As) termed an antiphase boundary (APB), which may propagate into the GaAs epilayer. To resolve this, a high offcut angle (usually 4° to 6°) is used to reduce the step spacing and possibly shrink the sizes of APDs.[16–18]

Prior to the growth of III–V on Ge, a Ge layer with high quality needs to be grown on Si. Hartman et al. grew a thick ($\sim$2.5 μm) Ge epilayer on both 0° and 6° offcut wafers and reported similar Ge qualities [in terms of surface roughness, threading dislocation density (TDD), and strain state].[19] It is well known that the quality of the Ge film improves with increasing film thickness.[20,21] For a thinner Ge film (e.g., $\sim$1 μm), one can expect different quality of the Ge epilayer when grown on 0° and 6° offcut wafers. Recently, an epitaxial Ge film ($\sim$1 μm) grown directly on Si (001) with 0° offcut was reported by Tan et al.[19] using a "three-step growth" approach in a reduced-pressure chemical vapor deposition (RPCVD) system with TDD level of $\sim 10^7$ cm^{-2} and RMS surface roughness of $\sim$0.9 nm.[22] In this manuscript, the qualities of Ge film (with thickness of 1 μm) grown directly on two different Si substrates, namely Si (001) with 0° offcut and Si (001) with 6° offcut toward [110], using the same growth method are studied and compared.

EXPERIMENTAL PROCEDURES

In this experiment, silicon (001) wafers (diameter 150 mm, p-type, resistivity 0.018 Ω cm to 0.025 Ω cm) with 0° and 6° offcut toward [110] direction were cleaned using RCA solutions followed by drying the wafers using an isopropanol (IPA) dryer. The clean wafers were loaded into the N_2-purged loadlock of an ASM Epsilon 2000 RPCVD reactor. To initiate growth, each wafer was transferred to the growth chamber and baked in hydrogen (H_2) at 1000°C for 2 min to desorb the thin surface oxide that is detrimental to the epitaxy process. The precursor for Ge was 10% diluted germane (GeH_4) in H_2 balance. A three-step Ge growth was introduced with target thickness of 1 μm.[19] The three steps in the growth sequence were: (i) low-temperature growth at 400°C to obtain a relatively smooth and continuous Ge seed layer, (ii) low- to high-temperature ramping from 400°C to 600°C at rate of 6.5°C/min, and (iii) high-temperature growth at 600°C. This approach has been described in detail in a previous publication.[22] Thermal cycling was introduced immediately after step (iii) to enhance the surface mobility of the Ge atoms in order to control the surface roughness and reduce the TDD. Thermal cycling was performed by H_2 annealing between 680°C to 825°C for a repetition of 8× with 10 min annealing at 825°C.

The qualities of the Ge epitaxial film grown on both types of substrate were characterized by various techniques. The Ge surface topography and its thickness were examined by scanning electron microscopy (SEM) using a Zeiss Leo model 1550. The Ge RMS roughness was determined by atomic force microscopy (AFM) using a Veeco/Digital Instrument Dimension 3000 in tapping mode. Transmission electron microscopy (TEM, Philips CM200) with operating voltage of 200 kV was used to study the dislocations along the Ge/Si interface. x-Ray diffraction (XRD, Bruker D8 Discover) analysis was used to determine the crystallinity and strain of the Ge epilayer. The Si (004) reflection was used for the XRD rocking curves. To further confirm the strain and quality of the Ge film, Raman spectra were collected using a WITec alpha 300 confocal Raman microscope. An excitation laser wavelength of 532 nm was used with focal length and objective lens magnification of 80 cm and 100×, respectively. Dynamic secondary-ion mass spectroscopy (D-SIMS) profiles were measured using a Cameca IMS 6f. The primary beam and energy used were Cs^+ and 10 kV. The beam raster size was 200 μm × 200 μm, and the analysis area was 60 μm in diameter. The electrical properties of the Ge films were characterized by capacitance–voltage (C–V) measurements of metal–oxide–semiconductor (MOS) structure on a Cascade/Suss Microtec PM8PS probe station, using a Keithley 4200-SCS semiconductor characterization system.

RESULTS AND DISCUSSION

The SEM images in Fig. 1 show plan and cross-sectional views of the 0° and 6° offcut Ge/Si samples after thermal cycling. From the cross-sectional SEM images, the thickness of the Ge film on 0° and 6° offcut samples is 978 nm and 969 nm, respectively. These values closely match the target value of 1 μm. The RMS surface roughness of the 0° and 6° offcut samples is 0.98 nm and 1.92 nm, respectively, as estimated from the AFM images shown in Fig. 2. The surface roughness is doubled when the Ge is grown on the 6° offcut substrate. In Fig. 2a, a clear cross-hatch pattern is seen on the 0° sample. The threading dislocation density (TDD) can be

determined from the plan-view TEM image by estimating the dislocations in a given area at a number of locations across the samples, as shown in Fig. 3. The TDD is more prominent in terms of visual contrast and density in the 6° offcut sample. The estimated TDD is $3.95 \pm 0.663 \times 10^7$ cm^{-2} and $6.53 \pm 0.931 \times 10^7$ cm^{-2} for 0° and 6° offcut samples, respectively. The TDD value was estimated based on an average number of 40 plan-view TEM images for accuracy.

The cross-sectional bright-field TEM images in Fig. 4 show that the thickness of the Ge epitaxial film is ~970 nm and ~985 nm, respectively, for 0° and 6° offcut samples. These values are in good agreement with earlier estimations from the cross-sectional SEM images shown in Fig. 1. The cross-sectional TEM images also show that, for both cases, the misfit dislocations are mostly confined along the Ge/Si interface. It is evident that a larger number of misfit dislocations are concentrated at the Ge/Si interface of the 6° offcut sample. In addition, within the first ~400 nm (beginning from the Ge/Si interface), a larger number of threading dislocations are propagated into the film in the 6° offcut sample compared with the 0° offcut sample. As a result, the 6° offcut sample presents a higher TDD on the top surface. The apparent discrepancy in the TDD count in both samples can be explained from the point of view of the effect of surface orientation on the dislocation Burgers vectors. On the Si (001) with 0° offcut, an even balance of Burgers vectors are nucleated when misfit dislocations form to relieve the misfit strain. Therefore, the annihilation process has a more balanced probability of locating the opposite Burgers vectors. When the Si (001) surface is 6° offcut, it is speculated that certain Burgers vectors are preferred at nucleation and this results in an imbalance in the Burgers vectors.[23–25] When the possible annihilation events are completed under the processing conditions used in this experiment, more misfit dislocations remain at the Ge/Si interface for the sample with 6° offcut that eventually thread to the top surface, hence giving rise to a higher net TDD.

Since the strain state of the final Ge epilayer heavily influences its electrical and optical properties, XRD study was performed to estimate the strain level of the Ge epilayer. The XRD analysis in Fig. 5 shows that the Ge epilayer on the 0° offcut sample has better crystal quality than the 6° offcut sample, as the Ge signal curve is sharper and the peak intensity is much higher. In addition, the difference in intensity of the Ge peak on 0° and 6° offcut samples may be due to the slight misalignment of the 6° offcut sample. The Ge signal from the 6° offcut sample has a broader distribution, possibly due to the presence of Ge clusters with different strain levels. Both of the Ge signal curves are asymmetric and show a clear shoulder at the side towards higher incidence angle. This is due to Ge/Si intermixing at the interface during thermal processing that perturbs the abrupt interface, resulting in an intermediate $Si_{1-x}Ge_x$ layer. The Ge peaks are shifted to the right with respect to the Ge bulk substrate as a result of tensile strain. The tensile strain is thermally induced in the Ge epilayer during cooling from high-temperature processing steps to room temperature, as Ge (5.8 ppm/°C) and Si

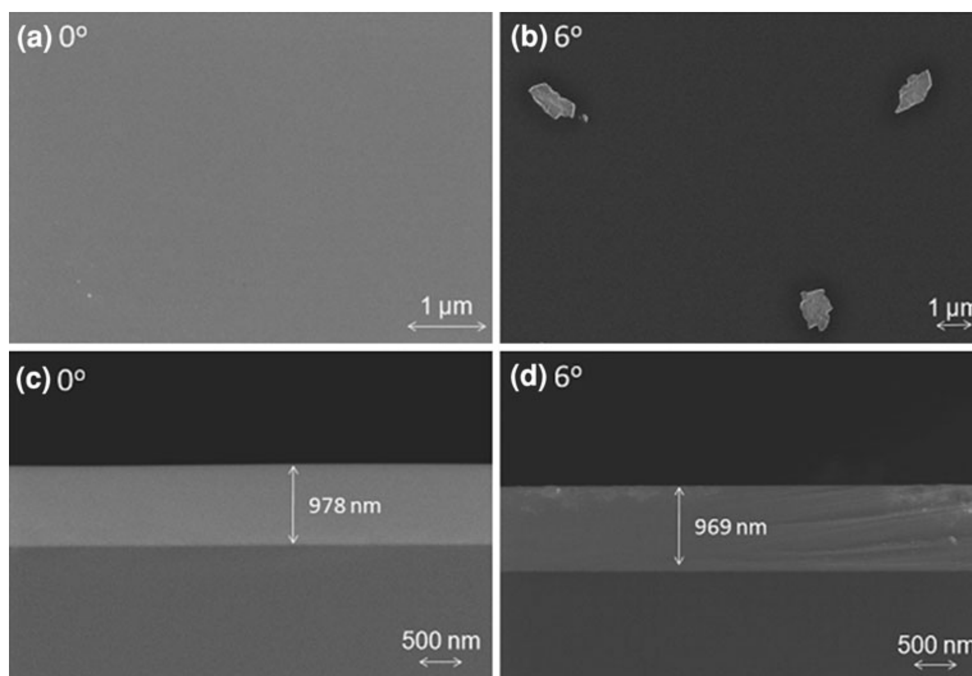

Fig. 1. SEM images of epitaxial Ge on Si substrate with (a, c) 0° offcut, (b, d) 6° offcut; (a, b) plan view, (c, d) cross-sectional view.

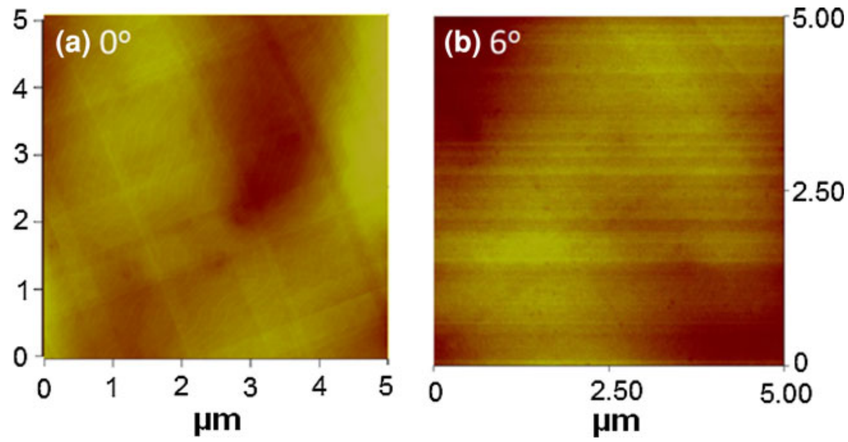

Fig. 2. Two-dimensional (2-D) AFM scans (dimensions 5 μm × 5 μm) showing the RMS roughness of the as-grown Ge epilayer on Si substrate with (a) 0° offcut and (b) 6° offcut.

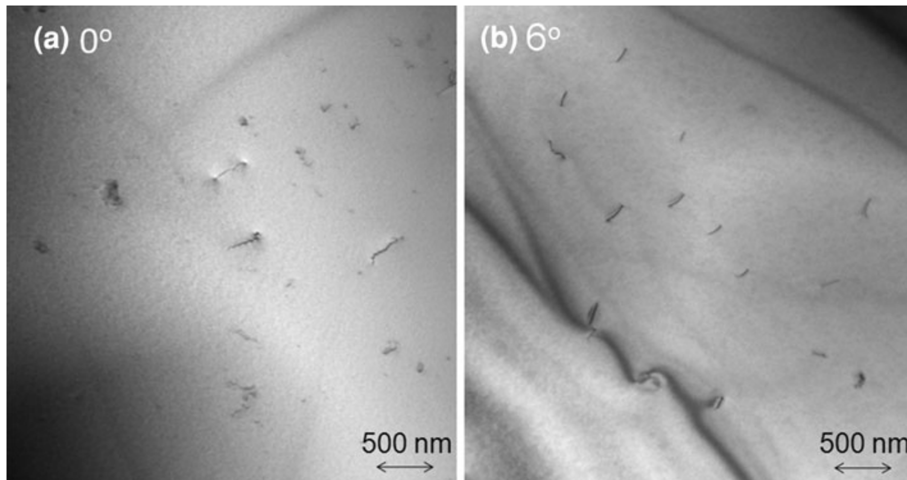

Fig. 3. Plan-view TEM images showing the threading dislocations on the Ge surface for (a) 0° offcut sample and (b) 6° offcut sample.

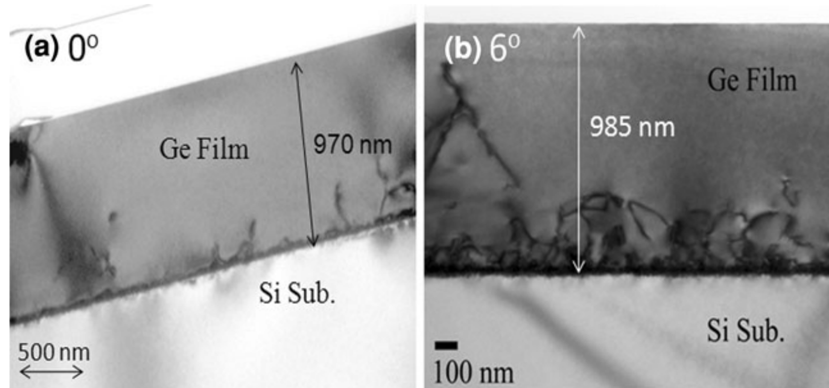

Fig. 4. Cross-sectional TEM bright-field images showing the Ge epitaxial film for (a) 0° offcut sample and (b) 6° offcut sample. In both cases, the misfit dislocations are confined along the Ge/Si interface and threading dislocations are propagated through the film.

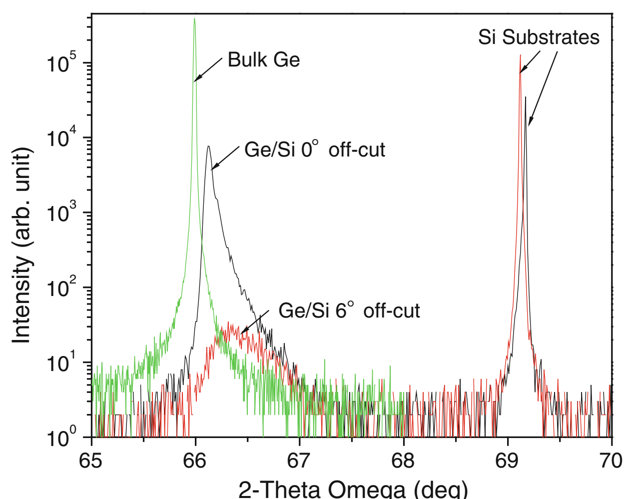

Fig. 5. High-resolution x-ray diffraction (HRXRD) profile illustrating the crystallinity and strain state of the Ge epitaxial films with respect to bulk Ge.

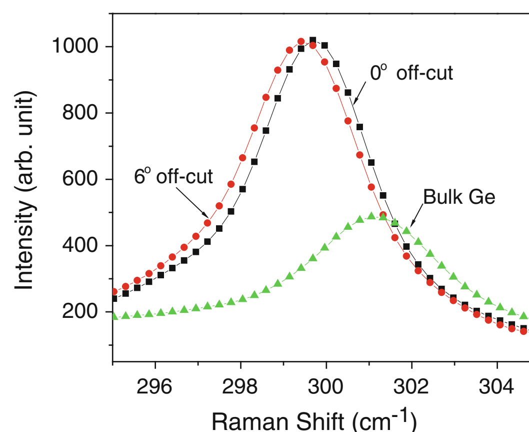

Fig. 6. Raman spectroscopy illustrating the alloy composition and strain of the Ge epilayers with respect to bulk Ge.

(2.6 ppm/°C) have different linear coefficient of thermal expansion (CTE).[26]

The perpendicular lattice constant ($a^{\perp}$) of the Ge epilayer in the growth direction can be calculated from the XRD diffraction peak using Bragg's law as follows:

$$a^{\perp} = \frac{2\lambda}{\sin(\frac{\omega_{\mathrm{Ge}}}{2})}, \tag{1}$$

where λ is the incident radiation wavelength (Cu $K_{\alpha 1}$ line, λ = 1.5406 Å) and ω_{Ge} is the angular position of the Ge peak from the HRXRD of Si (004). Using Eq. 1, the $a^{\perp}$ of the Ge on Si 0° and 6° offcut samples can be estimated as 5.6482 Å and 5.6433 Å, respectively. The in-plane lattice constant, $a^{||}$ of the Ge epilayer can be calculated using Eq. 2 by taking the elastic modulus of Ge, υ = 0.271, and the unstrained Ge lattice constant, a_{Ge} = 5.6576 Å:

$$a^{||} = \left(\frac{1+\upsilon}{2v}\right)\left[a_{\mathrm{Ge}} - a^{\perp}\left(\frac{1-\upsilon}{1+v}\right)\right]. \tag{2}$$

Therefore, the estimated $a^{||}$ of Ge on Si 0° and 6° offcut samples is 5.6708 Å and 5.6744 Å, respectively. The residual strain of the Ge epilayer can be calculated by Eq. 3 as

$$\varepsilon = \frac{a_{\mathrm{Ge}}^{||} - a_{\mathrm{Ge}}}{a_{\mathrm{Ge}}}. \tag{3}$$

Positive and negative values of ε for the Ge epilayer indicate either tensile or compressive strain. From the calculation, the Ge epilayers on both Si 0° and 6° offcut substrates exhibit tensile strain. The Ge layer on the 6° offcut substrate has higher average tensile strain of 0.6%, compared with the Ge on the 0° offcut substrate that has 0.2% tensile strain. This discrepancy is not fully understood and is most likely due to the complex interactions of the larger amount of threading dislocations in the Ge layer on the 6° offcut substrate.

Raman spectroscopy was used to determine the quality and properties of the Ge/Si epitaxial film by measuring the alloy composition and strain. In Fig. 6, a redshift of the Ge–Ge vibration peak position is clearly observed in the Ge/Si samples relative to the bulk Ge reference (peak at 301.3 cm^{-1}). The Ge–Ge peak is located at wavenumber of 300.1 cm^{-1} and 299.45 cm^{-1}, respectively, for the 0° and 6° offcut samples. In both samples, there is only one observable signal peak associated with the Ge–Ge vibration mode, with no other signal originating from Si–Ge or Si–Si vibration modes. This is expected due to the strong absorption property of the Ge layer. The full-width at half-maximum (FWHM) of the Ge–Ge vibration peak for bulk Ge, and the 0° and 6° offcut samples is 2.50 cm^{-1}, 2.17 cm^{-1}, and 2.22 cm^{-1}, respectively. Hence, the quality of the Ge/Si samples is comparable to that of bulk Ge. Both samples show a Ge–Ge peak that is shifted to lower wavenumber (with respect to the Ge bulk), indicating that they are under tensile strain. This observation agrees with the earlier XRD findings. In addition, the Ge–Ge peak from the 6° offcut sample is shifted to a wavenumber smaller than that of the 0° offcut sample, signifying higher tensile strain in the Ge epilayer grown on the 6° offcut sample.

The SIMS depth profiles are summarized in Fig. 7. The 6° offcut sample presents higher carbon (^{12}C) and oxygen (^{16}O) content in the Ge epilayer, possibly due to poor wafer handling. When the growth sequences are completed, samples are unloaded from the loadlock and exposed to ambient prior to SIMS analysis. There was a longer time lag prior to SIMS analysis for this 6° offcut sample, resulting in more significant surface oxidation and contamination. Based on the SIMS profile, a distinct level of the Ge signal in the epitaxial film that

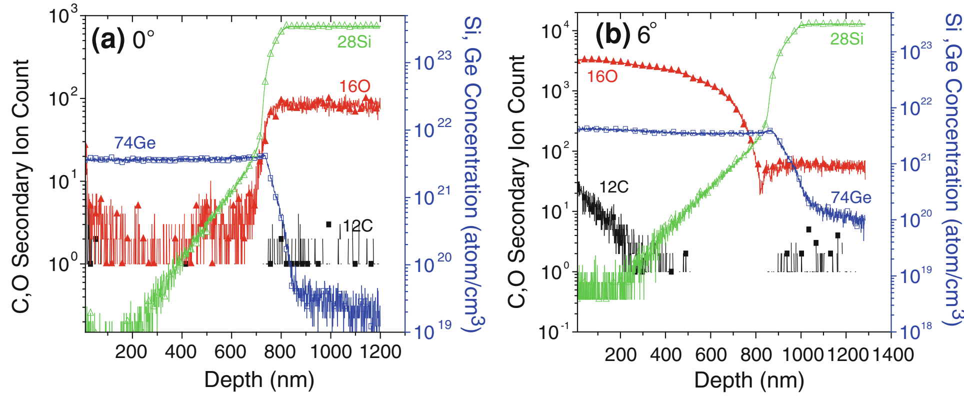

Fig. 7. SIMS analysis for elements of interest such as carbon (^{12}C), oxygen (^{16}O), silicon (^{28}Si), and germanium (^{74}Ge) for Ge epilayers grown directly on Si with (a) 0° and (b) 6° offcut.

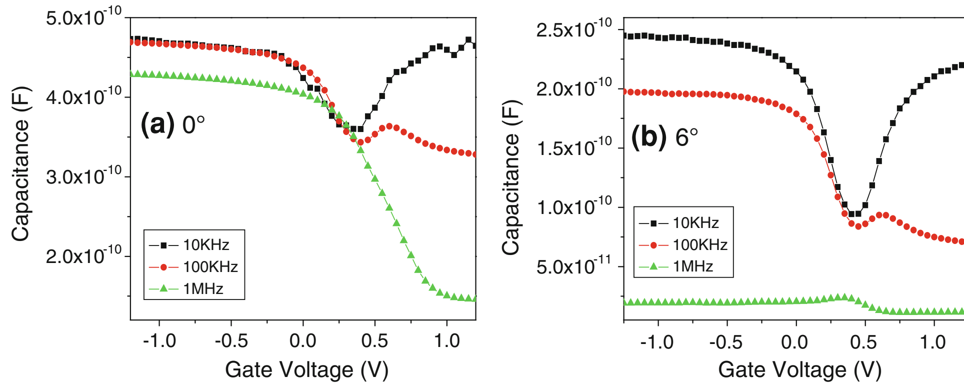

Fig. 8. *C–V* measurements at different frequencies on MOS structures fabricated on Ge epilayers: (a) 0° offcut sample and (b) 6° offcut sample.

Table I. Summary of the quality of Ge epitaxial film on Si (001) 0° and 6° offcut wafers

Characterization Method	Ge Epilayer on 0° Offcut Si	Ge Epilayer on 6° Offcut Si
XRD	0.2% tensile strain	0.6% tensile strain
Raman	Lower tensile strain	Higher tensile strain
AFM	RMS roughness 0.98 nm	RMS roughness 1.92 nm
TDD count from plan-view TEM	$3.95 \pm 0.663 \times 10^{7}$ cm^{-2}	$6.53 \pm 0.931 \times 10^{7}$ cm^{-2}
Cross-sectional TEM	Fewer threading dislocations are propagated within the first ~400 nm of film	More threading dislocations are propagated within the first ~400 nm of film
D_{it} from *C–V* measurements	4.7×10^{11} cm^{-2}/V	1.83×10^{12} cm^{-2}/V

tapers off rapidly in the Si substrate can be observed. Similarly, the Si signal decays rapidly as it crosses the Ge/Si interface into the Ge film. Therefore, Ge/Si intermixing is well controlled in both samples.

The Ge epitaxial film is undoped during the growth process. However, there is a possibility of background doping due to residual dopants from previous runs. This doping level is low and not reliably quantifiable. The conductivity in the Ge epilayer, despite its low dopant concentration, is attributed to the large offset between the valence bands of Ge and Si that forms a well that favors hole accumulation. This is confirmed by the *C–V* measurements on a 200 μm × 200 μm MOS structure fabricated on both of the undoped Ge layers, presented in Fig. 8. The gate electrode is TiN with thickness of ~150 nm, and the gate dielectric stack consists of Al_2O_3 (thickness ~10 nm) and interfacial GeO_xN_y (thickness ~2 nm). The interfacial quality

of both samples was estimated using the conductance method during C–V measurements. The calculated interface state density (D_{it}) for the 0° and 6° offcut samples is 4.7×10^{11} cm^{-2}/V and 1.83×10^{12} cm^{-2}/V, respectively. This is expected due to the higher TDD in the 6° offcut sample.

The properties and qualities of the Ge epitaxial film grown directly on Si (001) with 0° and 6° offcut are summarized in Table I. This study clearly shows that the starting Si substrate with 6° offcut orientation results in a poorer quality Ge layer. This is believed to be due to imbalanced Burgers vector nucleation during dislocation formation, leading to an unfavorable annihilation process. This study points to the need for additional investigation if direct Ge epitaxial growth on Si is to be attempted on substrates with nonzero offcut for III–V-on-Si integration.

CONCLUSIONS

Ge epitaxial film grown directly on Si substrate with 6° offcut presents higher TDD (~65% higher) and rougher surface (95% rougher) compared with a substrate with no offcut. The MOS structure fabricated on the 6° offcut sample also shows a higher D_{it} value (2.89 times higher). The poor quality of the Ge epilayer would be anticipated to degrade any subsequent III–V materials integration, and may also lead to device failure. The poorer quality of the Ge film on Si (001) with 6° offcut is attributed to the imbalance in Burgers vectors that favors dislocation nucleation over annihilation. Hence, additional attention is required if direct Ge (~1 μm) epitaxial growth on Si is to be attempted on substrates with nonzero offcut.

ACKNOWLEDGEMENTS

This research was supported by the National Research Foundation Singapore through the Singapore MIT Alliance for Research and Technology's "Low energy electronic systems (LEES) IRG" research. This work has also been carried out as part of the Nanyang Assistant Professorship supported by Nanyang Technological University (NTU). Authors are grateful for support provided by the management and technical staff in the Nanyang Nanofabrication Center at NTU.

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