Process-to-panel modeling of a-Si/c-Si heterojunction solar cells

Citation: Chavali, Raghu V. K., Eric C. Johlin, Jeffery L. Gray, Tonio Buonassisi, and Muhammad A. Alam. "Process-to-Panel Modeling of a-Si/c-Si Heterojunction Solar Cells." 2015 IEEE 42nd Photovoltaic Specialist Conference (PVSC) (June 2015).

As Published: http://dx.doi.org/10.1109/PVSC.2015.7356126

Publisher: Institute of Electrical and Electronics Engineers (IEEE)

Persistent URL: http://hdl.handle.net/1721.1/119177

Version: Author's final manuscript: final author's manuscript post peer review, without publisher's formatting or copy editing

Process-to-Panel Modeling of a-Si/c-Si Heterojunction Solar Cells

Raghu V. K. Chavali[1], Eric C. Johlin[2], Jeffery L. Gray[1], Tonio Buonassisi[2], Muhammad A. Alam[1]

[1]School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, USA

[2]Department of Mechanical Engineering, Massachusetts Institute of Technology, Cambridge, MA, USA

***Abstract* — The cell-to-panel efficiency gap observed in a-Si/c-Si heterojunction solar cells is one of the key challenges of this technology. To systematically address this issue, we describe an end-to-end modeling framework to explore the implications of process and device variation at the module level. First, a process model is developed to connect the a-Si deposition parameters to the device parameters. Next, a physics based device model is presented which captures the essential features of photo-current and diode injection current using the thermionic-diffusion theory. Using the process and device models, the effects of process conditions on cell performance are explored. Finally, the performance of the panel as a function of device and process parameters is explored to establish panel limits. The insights developed through this process-to-panel modeling framework will improve the understanding of the cell-to-panel efficiency gap of this commercially promising cell technology.**

I. Introduction

The a-Si/c-Si heterojunction (HJ) solar cell promises to capture a significant portion PV market [1] due to several advantages, such as, better temperature coefficient, possibility for bi-facial design, and lower processing temperature. However, the panel performance (and the prospect of large-scale deployment) is still very sensitive to process variations during a-Si deposition. These variations can alter the deposited a-Si film properties, such as, the band-gap, doping etc., which can significantly affect the cell performance, ultimately inducing cell-to-cell efficiency variations. This cell-to-cell variation is the main source of cell-to-panel efficiency gap, an important concern for this emerging technology.

It requires careful and self-consistent modeling and optimization at the process, device, and panel levels to reduce the cell-to-panel efficiency gap due to process variability. Hence, a multi-scale modeling framework is needed to explore the implications of process-device optimization on device-module optimization. The connection between the key process parameters, the device parameters and the module parameters can help establish the ultimate performance limit and commercial viability of a PV technology [2], [3].

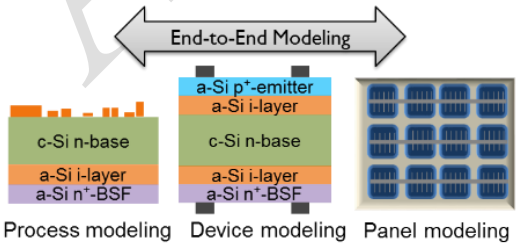

Fig. 1. The end-to-end modeling framework for a-Si/c-Si heterojunction cells.

Towards this goal, an end-to-end compact modeling framework to integrate the process, device and panel stages of the HIT cell technology (see Fig. 1) is presented. Here, we will study the sensitivities of process/device parameters at the module level and explore the optimization procedures essential for reducing the cell-to-panel efficiency gap. This study may also serve as an illustrative example for process-to-panel optimization flow for other PV technologies.

II. Amorphous Silicon Process Model

As discussed in section I, the deposition of a-Si on the c-Si wafer can introduce significant process variations which can ultimately impact the cell-to-panel efficiency gap. For example, a small change in deposition temperature/pressure can significantly affect the a-Si/c-Si band-offset (ΔE_V) (see Fig. 2 (a)) which in-turn reduces collection efficiency and the fill-factor (FF). Both the front and back a-Si layers can impact the performance of the cell, however, in good quality cells, the impact of front a-Si layer is dominant. Further, given the maturity of process-control of c-Si wafer to provide reproducible cell parameters (doping, bandgap, lifetime, etc.), this is not the dominant source of the cell-to-panel efficiency gap. Here, the a-Si process model which can predict the cell parameters (such as ΔE_V, emitter doping (N_A), etc.) based on the a-Si deposition conditions is presented.

A. Process Compact Model

An empirical model connecting the deposition parameters of plasma enhanced chemical vapor deposition (PECVD) of hydrogenated amorphous silicon (a-Si) to the material properties of the created films is developed. This model

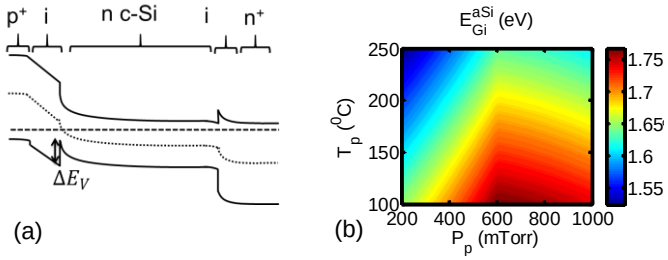

Fig. 2. (a) Schematic of energy band diagram indicating the process dependent a-Si/c-Si band offset ΔE_V. (b) The deposition temperature (T_P) and pressure (P_P) dependence on the a-Si bandgap (E_G^{aSi}).

This manuscript is the accepted copy. Please find the published version (© IEEE) through IEEE Xplore.
Link: http://dx.doi.org/10.1109/PVSC.2015.7356126

incorporates both measured relationships as well as those from the literature to predict film properties such as the material band gap [4]–[6], refractive index, optical constants, conductivity, hole mobility, density and stress, as well as the deposition rate [7] for given process conditions. The included conditions allow for variations in process pressure (P_P), power density, deposition time and temperature (T_P) [8], as well as dopant gas incorporation [9]. Relationships are extrapolated or estimated analytically to allow for an increased number of simulated conditions, or computed from a connected parameter, where appropriate (*e.g.* density and refractive index).

B. Influence of Process Parameters

Here, as an illustrative example, the dependence of the a-Si bandgap (E_G^{aSi}) as a function of deposition temperature (T_P) and pressure (P_P) is presented, see Fig. 2(b). Typical values of other process parameters discussed in section II A are used in this example. The material band gap is calculated by first starting with a standard baseline condition (200^0C, $400\ mTorr$, *etc.*), and the influence of the variance of the simulated deposition parameters (T_P and P_P) from this baseline condition are estimated to calculate the a-Si band gap. While T_P and P_P are the only process parameters considered here, this general procedure would allow one to calculate the influence of any combination of process parameters of the simulated material. *The experimental validation of the process model will be presented in the full paper.*

III. Heterojunction Device Model

In this section, we analyze the influence of process parameters on the efficiency of the HIT cell. As mentioned in section I, the properties of the a-Si/c-Si HJ cause several non-ideal effects in the even in good quality cells, thereby degrading their efficiencies. The non-ideal features in the experimental IV characteristics, such as, failure of superposition, injection limited transport in diode current (J_{Diode}) [10], occurrence of S-type curve in photo-current (J_{Pho}) [10], [11] are all attributed to the presence of large ΔE_V at the HJ and low N_A. These non-ideal features are well understood and modelled using numerical simulations (see Fig. 3(a-c)) [10], [11]. However, these models cannot be scaled to the panel level due to their inherent complexity. Hence, we need to develop a physics-based compact model to capture the distinctive features of I-V characteristics and relate it to the HJ properties such as ΔE_V, N_A etc. Using this compact model, along with the process model described in section II, we can explore the process sensitivity of cell-level performance parameters.

A. Device Compact Model

To capture the above mentioned features, J_{Pho}, J_{Diode} are modelled using diffusion-thermionic emission theory [12]. *The mathematical formulation will be discussed in the full paper*. Here we present the final expression for J_{Pho}, given by

$$J_{Pho} = qG_{Total}\left(\frac{v_d^{-1} + v_b^{-1}}{v_{fl}^{-1} + v_d^{-1} + v_b^{-1}}\right). \qquad (1)$$

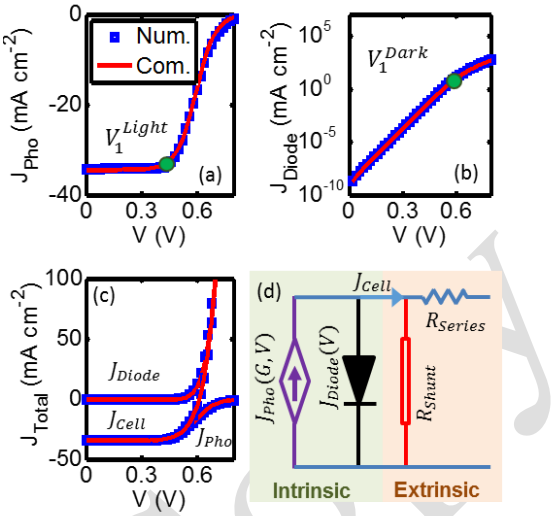

Fig. 3. The J_{Diode} obtained from numerical simulation (□) and compact model (−), indicating the current saturation at V_1^{Dark}. (b) The corresponding J_{Pho} also indicates the expected shift in S-type rollover at V_1^{Light}. (c) The corresponding J_{Cell} is plotted along with J_{Diode} and J_{Pho}. (d) The schematic of the compact model of the cell with the intrinsic and extrinsic components

Here, G_{Total} is the effective generation rate inside the absorber layer (assuming a uniform generation profile), v_b is the surface recombination velocity at the back interface, v_d is the diffusion velocity given by $v_d = D_h/W_c$, where D_h is the diffusion coefficient for holes and W_c is the thickness of the absorber region. The v_f is the emission velocity given by $v_{fl} = v_o e^{-(V-V_1^{Light})/k_bT}$, where v_0 is the diffusion velocity in the a-Si layer, and $V_1^{Light} = \phi_{Nl} - \Delta E_V = (\phi_N(V=0) - \beta_l V) - \Delta E_V$, β $(0<\beta<1)$ is the ratio of potential developed in absorber to the applied voltage (V), ΔE_V is the a-Si/c-Si valence band-offset and ϕ_{Nl} is the electrostatic potential in the absorber under illumination.

Similarly, the minority carrier current,J_{Diode}, is given by

$$J_{Diode} = q\frac{n_{ic}^2}{N_A}\left(\frac{1}{v_{fd}^{-1} + v_d^{-1}}\right)\left(e^{qV/k_BT} - 1\right). \qquad (2)$$

Here, n_{ic} is the intrinsic carrier concentration in the absorber layer, $v_{fd} = v_o e^{-(V-V_1^{Dark})/k_bT}$. Note that, at high bias, there can be an additional current component due to the majority carrier transport, *which will be discussed in the full paper*.

A close match between the numerical and the compact model is presented in the Fig. 3 (a-c). The compact model accurately captures the effect of current saturation of J_{Diode} above V_1^{Dark}, which is due to injection-limited transport in HJ (see Fig. 3(b)). Further, it also accounts for the S-type curve of J_{Pho} above V_1^{Light}, which is due to the HJ barrier for minority carrier collection (see Fig. 3(a)). *The experimental validation of the compact model will be presented in the full paper*.

B. Influence of Process Parameters

Based on the process dependence of E_G^{aSi} as described in Fig. 2(b), we explore the corresponding process dependence of *FF*

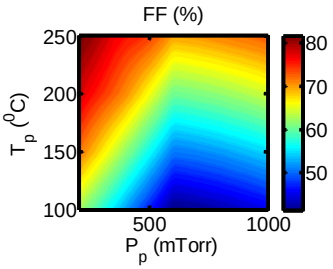

Fig. 4. The deposition temperature (T_P) and process pressure (P_P) dependence on the FF of the cell.

of the device in Fig. 4. Note that this difference in FF is due to the degree by which the ΔE_V effects the J_{Cell} through the S-type curve of J_{Pho}. The FF starts to drop-off rapidly for $T_P < 200^0C$. Above these values, the FF remains $> 70\%$, as the J_{Cell} is now limited by the J_{Diode}. *In the full paper, additional device level effects such as emitter doping (N_A), a-Si mobility (μ_h) will be discussed. The sensitivity of process parameters on cell efficiency will be explored.*

IV. Panel Performance

A. Module Compact Model

The compact model used to model each cell is shown in Fig. 3(d). The intrinsic components (J_{Photo} and J_{Diode}) are obtained from device model as discussed in section III A. The extrinsic components, which are R_{Shunt} and R_{Series} are added at the panel level to model the shunt and series resistance of the cells. The cells are connected in series configuration to form a panel of size 12x6. *In the full paper, we will the effects of distributed resistances and shunts for more accurate modeling.*

B. Influence of Process Parameters

In section III B, we discussed the influence of P_p *and* T_p on FF of the cell. Here, we will extend this discussion to understand the influence of process parameters at the panel level. P_P and T_P are assumed to vary around a mean values of $760mTorr$ and 200^0C with a *small* variance of $15mTorr$ and 10^0C respectively. The resulting variation in the normalized cell efficiency at the panel level is presented in Fig. 5. For the assumed process conditions, the optimal cell which has an efficiency of 21.4% (see Fig. 5 (a)), with mean at 20.9% and

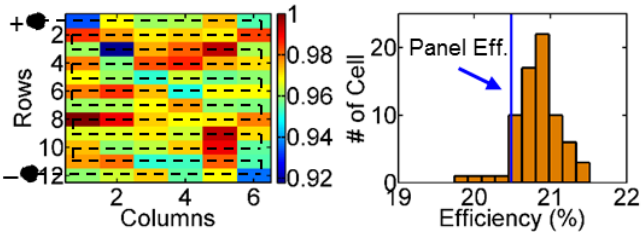

Fig. 5. (a) The panel simulation shows the normalized efficiency of the cells connected in series configuration obtained for (P_P, T_P) of (760mTorr, 200^0C) and a variance of ($15mTorr$, 10^0C). (b) The histogram indicates the cell-to-panel efficiency gap of about ~1%, even for excellent process control.

the overall panel efficiency is 20.5%. Even for such excellent process control, the cell-to-panel efficiency gap is significant (~1%). In practice, however, the process variations are much higher, resulting in a large cell-to-panel efficiency gap. *In the full paper, the effect of full process parameter variation space along with, log-normal shunt distributions, etc. on the cell-to-panel efficiency gap will be explored.*

V. Summary

A multi-scale end-to-end modeling framework integrating the process, device and panel stages of the a-Si/c-Si HJ technology is presented. The framework provides a unique opportunity to analyze the process parameter sensitivities at the cell and the panel level. Using this framework, the cell-to-panel efficiency gap, which is the key challenge to this technology, can be addressed. In particular, the influence of several process parameters (T_P, P_P) on the cell parameters (E_G^{aSi}) the FF of the device is presented as an illustrative example. The physics based device model is extended to the panel level. Then, the cell-to-panel efficiency gap is extracted for a sample process parameter set (T_P, P_P) to illustrate the usefulness of the method. *Using this end-to-end framework, the process parameter space will be further explored to understand the origin of the cell-to-panel efficiency gap in a-Si/c-Si HJ solar cells.*

This work is supported by the DOE-SERIIUS center and NSF- NEEDS center.

References

[1] G. Coletti, W. Sinke, and J. Bultman, "International Technology Roadmap for Photovoltaic (ITRPV) 2013 Results," no. March, pp. 1–37, 2014.

[2] M. A. Alam, B. Ray, M. R. Khan, and S. Dongaonkar, "The essence and efficiency limits of bulk-heterostructure organic solar cells: A polymer-to-panel perspective," *J. Mater. Res.*, vol. 28, no. 04, pp. 541–557, Feb. 2013.

[3] E. S. Mungan, Y. Wang, S. Dongaonkar, D. R. Ely, R. E. Garcia, and M. A. Alam, "From Process to Modules: End-to-End Modeling of CSS-Deposited CdTe Solar Cells," *IEEE J. Photovoltaics*, vol. 4, no. 3, pp. 954–961, May 2014.

[4] R. Platz, S. Wagner, C. Hof, A. Shah, S. Wieder, and B. Rech, "Influence of excitation frequency, temperature, and hydrogen dilution on the stability of plasma enhanced chemical vapor deposited a-Si:H," *J. Appl. Phys.*, vol. 84, no. 7, p. 3949, Oct. 1998.

[5] C. Koch, M. Ito, and M. Schubert, "Low-temperature deposition of amorphous silicon solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 68, no. 2, pp. 227–236, May 2001.

[6] B. Vet and M. Zeman, "Relation between the open-circuit voltage and the band gap of absorber and buffer layers in a-Si:H solar cells," *Thin Solid Films*, vol. 516, no. 20, pp. 6873–6876, Aug. 2008.

[7] J. Perrin, Y. Takeda, N. Hirano, Y. Takeuchi, and A. Matsuda, "Sticking and recombination of the SiH3 radical on hydrogenated amorphous silicon: The catalytic effect of diborane," *Surf. Sci.*, vol. 210, no. 1–2, pp. 114–128, Mar. 1989.

[8] M. Kunst and H.-C. Neitzert, "The influence of deposition temperature and annealing temperature on the optoelectronic properties of hydrogenated amorphous silicon films," *J. Appl. Phys.*, vol. 69, no. 12, p. 8320, Jun. 1991.

[9] W. E. Spear and P. G. Le Comber, "Substitutional doping of amorphous silicon," *Solid State Commun.*, vol. 17, no. 9, pp. 1193–1196, Nov. 1975.

[10] R. V. K. Chavali, J. R. Wilcox, B. Ray, J. L. Gray, and M. A. Alam, "Correlated Nonideal Effects of Dark and Light I--V Characteristics in a-Si/c-Si Heterojunction Solar Cells," *IEEE J. Photovoltaics*, vol. 4, no. 3, pp. 763 – 771, 2014.

[11] Z. Shu, U. Das, J. Allen, R. Birkmire, and S. Hegedus, "Experimental and simulated analysis of front versus all-back-contact silicon heterojunction solar cells: effect of interface and doped a-Si:H layer defects," *Prog. Photovoltaics Res. Appl.*, Jun. 2013.

[12] S. M. Sze and K. K. Ng, "Metal-Semiconductor Contacts," in *Physics of Semiconductor Devices*, John Wiley & Sons, Inc., 2006, pp. 134–196.