A High Dynamic Range Capacitive Displacement Sensor

by

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Abstract

This thesis covers many of the issues involved with the design of high dynamic range capacitive sensors. Several topologies for the drive electronics have been investigated. Specifically, a noise model has been developed for each of the topologies. The design of a displacement transducer system capable of Angstrom resolution over a 100 micron travel range is presented. The system includes a 20-bit A/D converter with a 1 kHz sampling rate.

An experimental prototype has been constructed and has demonstrated a very low noise output. With the variable capacitance located on the circuit board with the drive electronics, a noise floor of around 5 microvolts rms in a .1 to 300 Hz bandwidth has been demonstrated. With a 20 volt total output range, this gives a useful dynamic range of around 10^6:1. If the variable capacitance is located at the end of a cable, the broadband noise is relatively unchanged, but the low frequency drift is increased.

The complete displacement sensor system exhibits a nonlinearity of less than .5% of the full scale reading. Remaining issues that need to be addresses are: a large amount of line frequency noise is present in the output and a relatively large low frequency drift is present. The low frequency drift is believed to be related to variations in the cable used to connect the probe to the circuit board.

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1 Introduction

1.1 Overview

Capacitive sensors are a popular means of detecting displacements without making physical contact with the object being sensed [ADE 88]. These sensors operate on the principle that the capacitance between two conductors varies as their relative positions change. Some features that make capacitive sensing attractive are: no physical contact is required, the forces exerted on the device are electrostatic in nature and can be made very small, and finally extreme sensitivity may be realized. Systems have been constructed that give a full scale output for ±10 aF (10^{-18} F) deviations from the nominal capacitance value [Jones 88].

Capacitive sensors have been successfully used in a wide variety of applications including: medical instrumentation [Ramachandran 90], measuring machine spindle errors [Chapman 85], determining silicon wafer flatness [ADE 88], tiltmeters [Jones 88], and position control systems [Trumper 90].

1.2 Immediate Application

The system presented in this thesis will be used as the position sensing element in an Angstrom (Å) resolution motion control system being developed by Professor Trumper at the University of North Carolina, Charlotte (UNCC). The target specifications for the UNCC system include 1 Å control with a 100 μm range of travel. This 10^6:1 dynamic range places rather stringent requirements on the electronics. As the suspension system will ultimately be controlled with a digital controller, the position sensors need to provide a digital output. In order for the sensors to work with the proposed feedback loop, they must have a 1 millisecond. or less conversion time. Although the system needs to have a noise floor of less than 1 Å, an absolute accuracy of ± .5 Å is not required.

The system developed in this thesis is targeted for one specific application, however, the models presented should be of use in the design of other capacitance based instrumentation systems.

1.3 Project Goals and Target Specifications

The goal of this thesis is twofold. The first goal is to design and implement a very low noise capacitive displacement sensor. The second goal is to develop models that will predict the noise performance of a capacitive gauging system. Obtaining an accurate model will allow others to optimize a circuit for their specific application. In addition noise models will help the designer evaluate which approach is most suited to their application.

Target specifications for the system are listed in Figure 1.3-1. The dynamic range requirement is of primary concern as a comparable system is not commercially available. Additionally, the required A/D converter is faster than available 20-bit converters.

Specification	Goal
Dynamic Range	± 10 Volt output range ≤ 20 μVRMS noise (.1-100 Hz)
Bandwidth	> 100 Hz
Linearity	~1%
Digital Output	20-bits at a 1 kHz sample rate

Figure 1.3-1: Target Specifications

2 Probe Geometries

2.1 Basic Principle

Capacitive position sensors work on the principle that the capacitance between two conducting objects is a function of their relative positions. A parallel plate capacitor is shown below in Figure 2.1-1. In the case where the distance, d, between the conductors is small compared to the conductor dimensions, the fringing fields can be neglected and the capacitance is approximately given by

$$C \approx \frac{\varepsilon A}{d} \tag{2.1-1}$$

where ε is the permitivity of the dielectric, A is the plate area, and d is the distance between the plates.

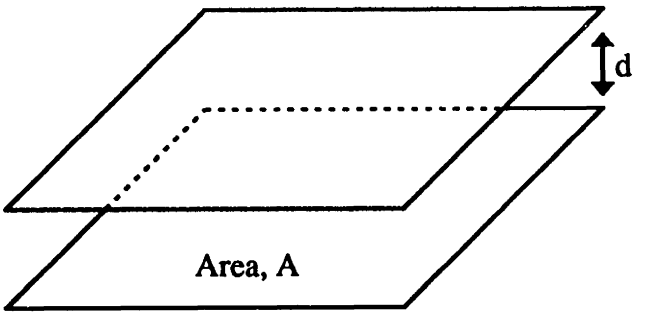

Figure 2.1-1: Parallel Plate Capacitor

It is evident from (2.1-1) that by measuring the capacitance between the two conductors, the displacement may be calculated if the area and permitivity are known. Alternatively, the overlapping area may be calculated from the capacitance if the displacement and the permitivity are known. While useful as a starting point, the simple parallel plate capacitor is usually not suitable for capacitive sensing without some modifications.

2.2 Guarding and Shielding

In the previous section, a parallel plate capacitor in free space was examined ignoring fringing fields. The uniform electric field lines that result when a voltage is applied to the sensor are shown in Figure 2.2-1.

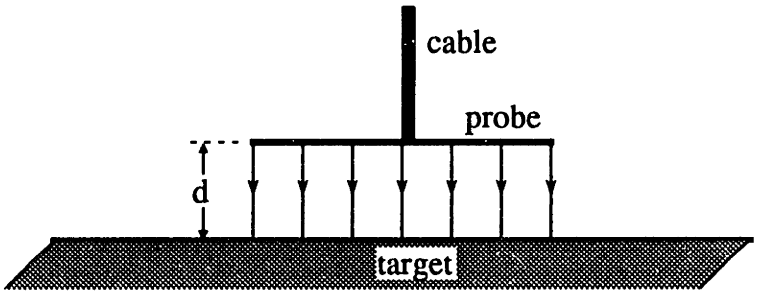

Figure 2.2-1: Probe With Uniform Electric Fields

When the metal probe housing and fringing fields are considered, the electric fields are more closely represented by Figure 2.2-2. As the distance between the plates becomes comparable to the dimensions of the plates, the fringing fields become significant. The presence of these fields causes $\frac{1}{C}$ to no longer be a linear function of distance.

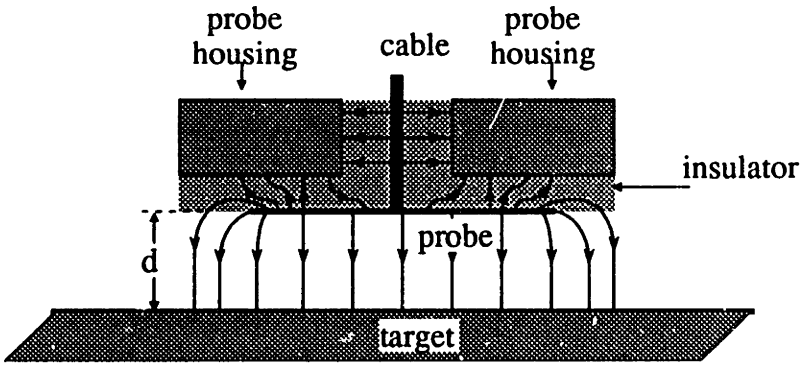

Figure 2.2-2: Probe With Fringing Fields

Another perhaps more significant feature of the sensor shown in Figure 2.2-2 is the sensitivity of the measured capacitance to the presence of any nearby conductors such as the probe housing. The effects of the additional fields are modeled by the circuit in Figure 2.2-3.

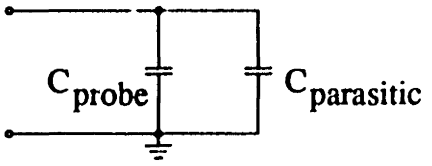

Figure 2.2-3: Circuit Model Showing Parasitic Capacitance

By surrounding the active probe and the wire that attaches to it by a guard which is driven with the same signal as the probe, the effects of nearby objects other than the target are ideally eliminated. In addition, the uniform field approximation for the probe is made better. A guarded probe and its associated electric fields are shown in Figure 2.2-4.

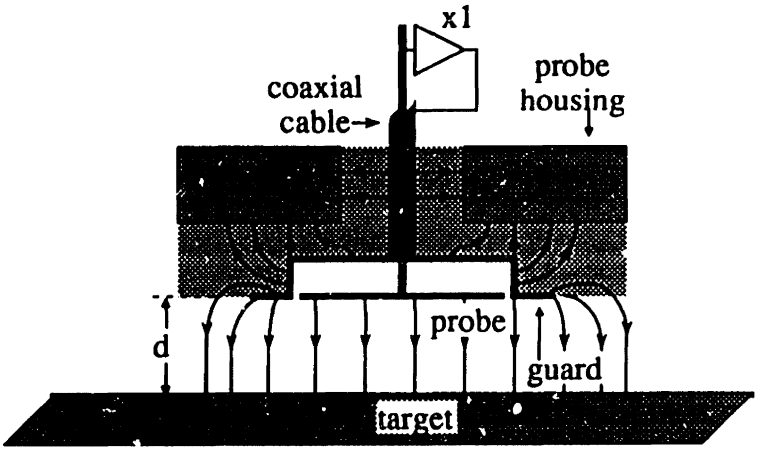

Figure 2.2-4: Guarded Probe

The circuit in Figure 2.2-5 illustrates the effect of adding the guard.

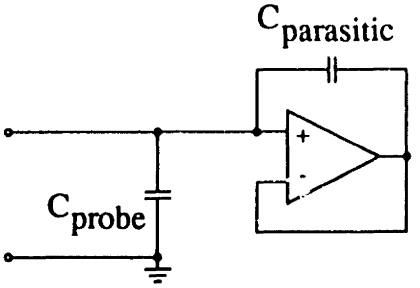

Figure 2.2-5: Guarded Probe Circuit Model

2.3 Practical Geometries

Many different probe geometries have been reported in the literature. A few of the more popular structures will be examined here. For a more detailed field analysis of various

structures, the reader is referred to [Bertone 90], [Fertner 88], [Klaassen 82], and [Kosel 81]. A detailed treatment of fringing fields is given by [Scott 39].

2.3.1 Linear Displacement Probes

A linear displacement probe that has enjoyed much commercial success is shown below in Figures 2.3.1-1 and 2.3.1-2. This probe is intended to measure changes in the distance from the active area to the grounded target.

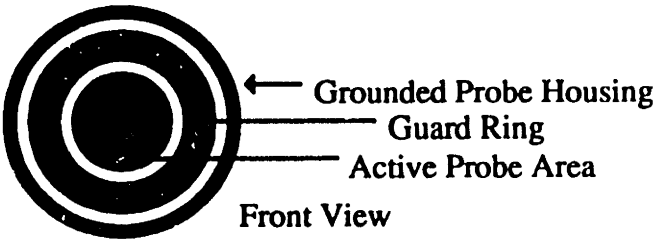

Figure 2.3.1-1: Linear Displacement Probe--Front View

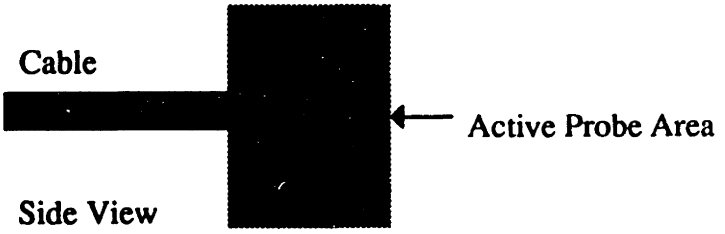

Figure 2.3.1-2: Linear Displacement Probe--Side View

A probe of this type is used as the transducer in this thesis.

Other geometries exist which are intended to respond to changes in the area of overlap between two conductors rather than changes in the distance between them. One such transducer is shown below in Figure 2.3.1-3.

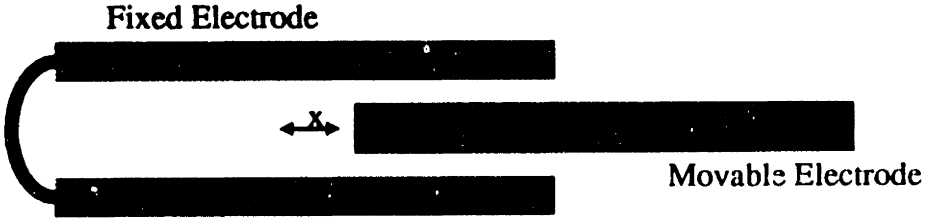

Figure 2.3.1-3: Sliding Probe

The two electrodes in the sliding probe may either be planar, or more typically, coaxial. Note that for a probe of this type, the displacement of interest gives rise to a change in the

area, A, in (2.1-1). The importance of this relation is that the capacitance is linearly related to the displacement as opposed to inversely related as is the case for the probe shown in Figure 2.3.1-1.

Another variation of the linear displacement probe is the periodic structure reported by [Klaassen 82] shown below in Figure 2.3.1-4. The fixed electrodes are driven by ground referenced ac voltage sources having the relative phase shifts indicated. By monitoring the phase of the voltage appearing between the moving probe and ground, the probe location may be determined. The output of the transducer as a function of displacement is periodic. If appropriate circuitry to keep track of how many periods the probe has moved through is included, very wide ranges of motion may be detected by simply adding more fixed electrodes.

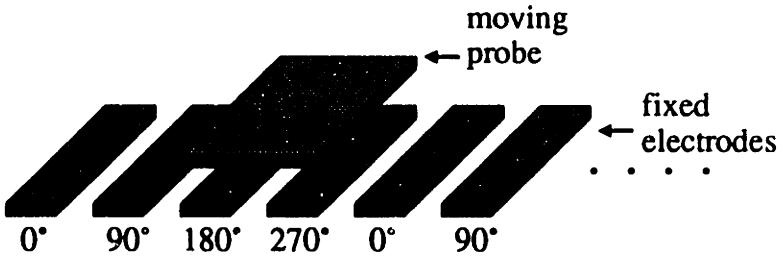

Figure 2.3.1-4: Periodic Probe Structure

2.3.2 Rotational Displacement Probes

In addition to detecting linear displacements, capacitive transducers may be used to measure rotational changes. One such transducer, known as a linear rotary differential capacitance transducer (LRDC) [Peters 92], is shown below in Figures 2.3.2-1 and 2.3.2-2. In this transducer, two probes like the one shown in Figure 2.3.2-1 are constructed. The probes are then mounted on opposing shafts as shown in Figure 2.3.2-2. The four conductors now form the capacitive bridge shown in Figure 2.3.2-3. By applying an ac voltage between the conductor on one of the probes and measuring the amplitude of the ac voltage appearing between the conductors of the other probe, the angle between the probes may be determined.

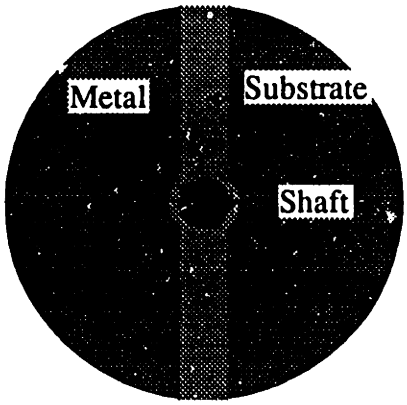

Figure 2.3.2-1: Rotational Capacitive Probe

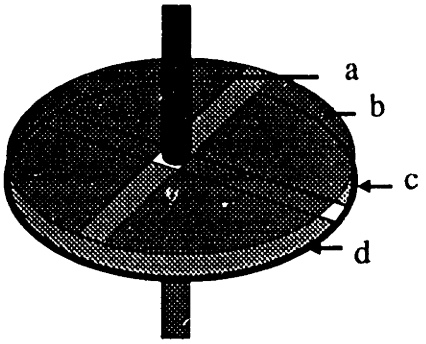

Figure 2.3.2-2: LRDC

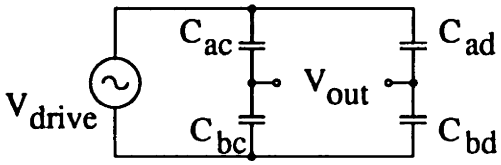

Figure 2.3.2-3: LRDC Bridge Circuit

2.4 Summary

Several probe structures have been briefly examined. Probes may be designed to yield a capacitance that is either linearly or inversely related to the displacement of interest. When designing a probe, it is important to provide a means of guarding against stray capacitances. The probe used in this thesis closely resembles the linear displacement probe shown in Figures 2.3.1-1 and 2.3.1-2.

3 Probe Drive Circuitry

3.1 Overview

A wide variety of drive circuits have been used with capacitive transducers. [Huang 88] gives a good overview of various approaches. It is often desirable to arrange the electronics in a way that allows one side of the probe capacitance to be grounded. Since a grounded target is required in this application, only those topologies which allow for that will be considered here.

3.2 Variable Frequency Drives

Various topologies that use the probe capacitance as the frequency determining element in an oscillator have been reported [Huang 88], [Cichocki 90], [Kudoh 91]. A frequency counter is then used to obtain a voltage output.

3.2.1 Relaxation Oscillator

One possible oscillator is the relaxation oscillator shown below in Figure 3.2.1-1 .

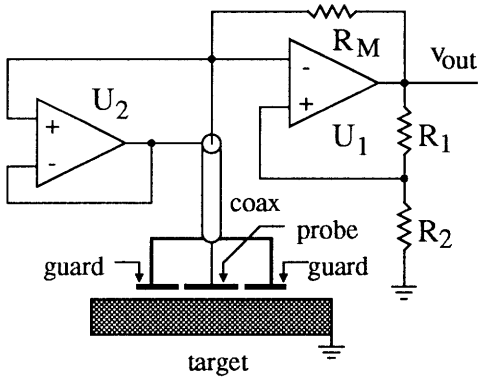

Figure 3.2.1-1: Relaxation Oscillator Drive

The cable capacitance and guard capacitance are effectively bootstrapped out by U_2. Comparator U_1 and resistors R_1 and R_2 form a Schmitt trigger. The output voltage, v_{out}, swings between the positive and negative supply voltages, $+V_S$ and $-V_S$. When v_{out} is at

$+V_S$, the probe capacitance charges through R_M until it reaches $+V_S \bullet \frac{R_2}{R_1 + R_2}$ volts. At this time, the output of the Schmitt trigger switches to $-V_S$. Now the probe capacitance discharges through R_M until it reaches $-V_S \bullet \frac{R_2}{R_1 + R_2}$ volts. At this point, the Schmitt trigger output returns to $+V_S$ and the cycle repeats. The period of oscillation, T, can be found from

$$\left(-V_s \frac{R_2}{R_1 + R_2}\right) e^{\frac{-T/2}{R_M C_M}} + V_s \left(1 - e^{\frac{-T/2}{R_M C_M}}\right) = V_s \frac{R_2}{R_1 + R_2} \tag{3.2.1-1}$$

Solving for T gives

$$T = 2R_M C_M \ln\left(1 + \frac{2R_2}{R_1}\right) \tag{3.2.1-2}$$

The frequency of oscillation is then given by

$$f_{out} = \frac{1}{2R_M C_M \ln\left(1 + \frac{2R_2}{R_1}\right)} \tag{3.2.1-3}$$

Assuming that R_1, R_2, R_M and the supply voltages are constant, the output frequency reduces to

$$f_{out} = \frac{k}{C_M} = \frac{kd}{\varepsilon A} = k'd \tag{3.2.1-4}$$

A frequency counter may now be used to obtain a linear response from displacement, d, to the output. This circuit has the advantage of being conceptually simple and easy to implement. In addition, the response to variations in displacement is linear.

Although this approach looks good on the surface, its potential for low noise instrumentation is limited. The period of oscillation depends strongly on the threshold levels of the Schmitt trigger. Unfortunately, the spectral density of the input voltage noise of a comparator is typically quite large. In addition the bandwidth is high. This combination leads to a large input noise voltage. To make matters worse, the positive feedback in the Schmitt trigger causes the comparator to respond to peaks in the noise voltage which may be 5-10 times as large as the RMS level of the noise. This leads to

significant variations of the actual comparator threshold from period to period which in turn leads to noise at the output of the system.

3.2.2 LC Oscillator

An alternative to the relaxation oscillator is an LC resonant oscillator. In this approach, the frequency of oscillation will be proportional to $\frac{1}{\sqrt{C}}$. One disadvantage of this type of approach is that the sensitivity of the frequency to changes capacitance is only $\frac{1}{2}$. This is shown by (3.2.2-1).

$$S = \left(\frac{\partial f}{\partial C}\right)\left(\frac{C}{f}\right) = \left(-\frac{1}{2}\frac{f}{C}\right)\left(\frac{C}{f}\right) = -\frac{1}{2} \qquad (3.2.2\text{-}1)$$

The result of this is that a 1% change in displacement (or capacitance) only results in a 0.5% change in the output. This leads to reduced resolution. Additionally, the output of the system does not vary linearly with the displacement.

3.3 Transformerless Charge Pump

The circuit shown below in Figure 3.3-1 can be used to generate a current or voltage that is proportional to the probe capacitance, C_M, [Roberge 93]. The drive voltage is a high frequency source that swings between 0 and V_S volts. By choosing the drive frequency to be much greater than $\frac{1}{\sqrt{LC}}$, the ac voltage across the probe is essentially the same as the drive voltage ignoring the diode drops. On each cycle, C_M is charged to $\frac{V_S}{2}$ through D_1 and subsequently discharged to $\frac{-V_S}{2}$ through D_2. The guard is driven through D_3 and D_4. The diodes are all located in the probe housing.

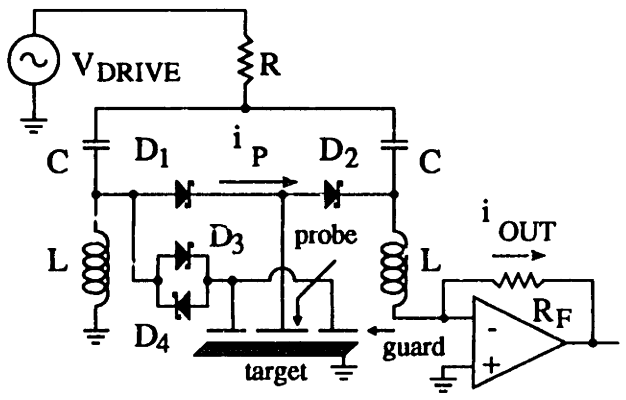

Figure 3.3-1: Transformerless Pump Circuit

The average current flowing through the diodes is simply the charge transferred each cycle multiplied by the drive frequency, f_S.

$$\langle i_P \rangle = f_s V_s C_M \tag{3.3-1}$$

Since a capacitor can have no net average current through it in the periodic steady state, the average current must flow through the right hand inductor and through R_F. This produces an output voltage proportional to the probe capacitance.

This circuit does not directly give an output that is linearly dependent on displacement, but rather one that is proportional to $\frac{1}{d}$. Several methods are available to produce the desired linear output. The simplest method is to ignore the nonlinearity and directly use the output. From the Taylor series expansion given by (3.3-2), it is evident that for small deviations from the nominal displacement, this method can give satisfactory results.

$$\frac{1}{d_{nom}+\tilde{d}} = \frac{1}{d_{nom}} + \tilde{d}\left(\frac{-1}{d_{nom}^2}\right) + \tilde{d}^2\left(\frac{2}{d_{nom}^3}\right) + \ldots \tag{3.3-2}$$

Another method is to send the output through a nonlinear network that approximates the $\frac{1}{x}$ function. This circuit may be based on translinear circuits or on a piecewise linear approximation. A third approach is to use a feedback loop that varies the drive voltage in such a way as to force the probe current to be equal to a reference current. Now the

amplitude of the drive voltage is taken as the output. In this case, the drive voltage amplitude will be given by

$$V_s = \frac{I_{REF}}{f_s C_M} \tag{3.3-3}$$

Yet another approach has been described by [Roberge 90]. This method involves a dual slope integrator in which a reference current is used during the up integration period and the probe current is used during the down integration. This approach is described in greater detail in section 4.2.3.

3.3.1 Circuit Averaging

The frequency response of the drive circuit must be examined for several reasons. The frequency response will determine how well the output will track a varying probe displacement. If a feedback loop is to be used to force a constant current, the dynamics of the system must be known in order to properly design the control loop. Finally, the noise performance of the circuit will be closely linked to its frequency response.

The analysis of the dynamic behavior of a linear time-invariant (LTI) circuit is a straightforward task. When presented with a circuit containing nonlinear elements such as a transistor, the usual approach is to linearize the nonlinear element about their operating points and consider small variations in the circuit variables. Once the small signal model is obtained, standard linear circuit analysis techniques may be applied. In the case of the charge pump, the analysis is not as straightforward. The nonlinear elements in the circuit, the diodes, are operated in a very nonlinear manner. In this circuit in fact, they behave as an open circuit part of the time and as a short circuit part of the time. Given this, it is clear that a straightforward linearization is not possible with this circuit. Nonetheless, a dynamic model is required.

In order to effectively analyze the circuit at hand, a few concepts must be reviewed. In section 3.3, it was shown that the average current flowing through the diodes in Figure 3.3-1 is equal to the product of the amplitude of the drive, the drive frequency, and the probe

capacitance. In the preceding analysis, the amplitude of the drive was assumed to be fixed and the average was taken over all time. If the drive frequency is much higher than $\frac{1}{\sqrt{LC}}$ in the circuit shown in Figure 3.3-1, then the output current is essentially the average diode current. A definition of a local average [Sanders 91] which will allow the investigation of the circuit dynamics is given here.

It is possible to represent a circuit variable over the interval (t-T,t] with a Fourier series representation of the form given in (3.3.1-1).

$$x(t-T+s)=\sum_{k=-\infty}^{\infty}\langle x\rangle_k(t)e^{jk\omega_s(t-T+s)} \tag{3.3.1-1}$$

Where ω_S is the angular frequency of the drive signal, T is the period of the drive signal and $s\in(0,T]$. The Fourier coefficients, $\langle x\rangle_k(t)$, are now functions of time and are given by (3.3.1-2). In the analysis presented here, we will only be concerned with the dc Fourier coefficient given in (3.3.1-3).

$$\langle x\rangle_k(t)=\frac{1}{T}\int_0^T x(t-T+s)e^{-jk\omega_s(t-T+s)}\,ds \tag{3.3.1-2}$$

$$\bar{x}(t)=\langle x\rangle_0(t)=\frac{1}{T}\int_{t-T}^{t}x(t)dt \tag{3.3.1-3}$$

An important property of the local average given by (3.3.1-3) is that the time derivative of an averaged variable is equal to the average of the derivative. The importance of this property is that when transforming a circuit to its averaged model, inductors remain inductors and capacitors remain capacitors. By choosing the interval T in (3.3.1-1) to be equal to the period of the drive voltage, the drive frequency components of the circuit variables are essentially eliminated.

As an example of circuit averaging, consider the circuit shown below in Figure 3.3.1-1. The diodes are considered to be ideal. The voltage sources, V_1 and V_2 are identical sinusoidal sources with slowly varying amplitudes.

$$V_1(t) = V_2(t) = v_a(t)\sin(2\pi f_s t) \tag{3.3.1-4}$$

The amplitude of V_1 and V_2, v_a, is assumed to always be positive.

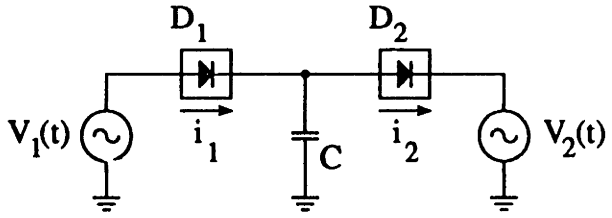

Figure 3.3.1-1: Circuit to Be Averaged

The current in the capacitor is given by

$$\begin{aligned} i_C(t) &= i_1(t) - i_2(t) \\ &= C\left(2\pi f_s v_a(t)\cos(2\pi f_s t) + \frac{dv_a(t)}{dt}\sin(2\pi f_s t)\right) \end{aligned} \tag{3.3.1-5}$$

The current i_1 is equal to i_c during half of the cycle and zero during the other half. Similarly, i2 is equal to ic during the other half cycle and zero during the first half. Assuming that v_a is varying slowly compared to f_s, then i_1 and i_2 appear to be identical with a 180 degree phase shift between them. In order to determine the local average of the diode currents, they must be integrated over 1 cycle.

$$\bar{i}_1 = \bar{i}_2 = \frac{1}{f}\int_{-\frac{1}{4f}}^{\frac{1}{4f}} i_C(t)dt \tag{3.3.1-6}$$

Since va is moving slowly, it may be considered a constant when evaluating the integral in (3.3.1-6). The result is

$$\bar{i}_1(t) = \bar{i}_2(t) = 2v_a(t)f_s C \tag{3.3.1-7}$$

An equivalent circuit may now be constructed which shows the relation between the averaged circuit variables. The averaged circuit is shown below in Figure 3.3.1-2. The voltage sources V_1 and V_2 have local averages of zero and hence have been replaced by ground. This particular example by itself isn't too exciting because the only remaining

element is a dependent current source. In the next section, however, this model will be expanded on.

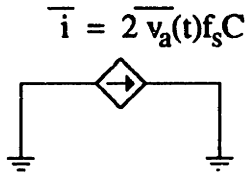

Figure 3.3.1-2: Averaged Circuit

3.3.2 Frequency Response

In the circuit shown below in Figure 3.3.2-1, the drive voltage, v_{DRIVE}, is given by (3.3.2-1). This section will find the frequency response from variations in $V_S(t)$ to variations in the local average of the output current.

$$v_{DRIVE}(t) = v_s(t)\frac{1+\sin(2\pi f_s t)}{2} \qquad (3.3.2\text{-}1)$$

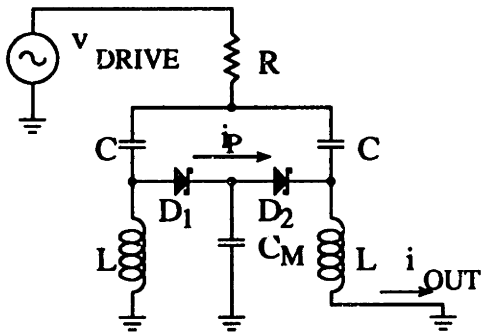

Figure 3.3.2-1: Pump Circuit

By applying the averaging method outlined in section 3.3.1, an averaged circuit model may be obtained. The impedance of the probe capacitance is assumed to be large compared to the impedance of the LC circuit at the drive frequency. As a first step, the dc output resistance of the circuit needs to be determined. Consider the effects of a non-zero voltage at the pump output as shown in Figure 3.3.2-2.

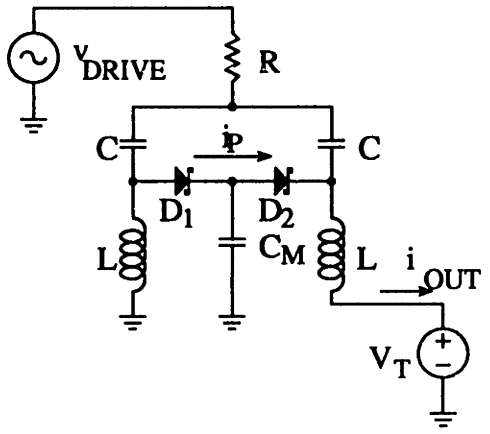

Figure 3.3.2-2: Circuit to Determine Output Resistance

The peak-to-peak voltage across the probe capacitance is decreased by an amount equal to V_T as shown in Figure 3.3.2-3.

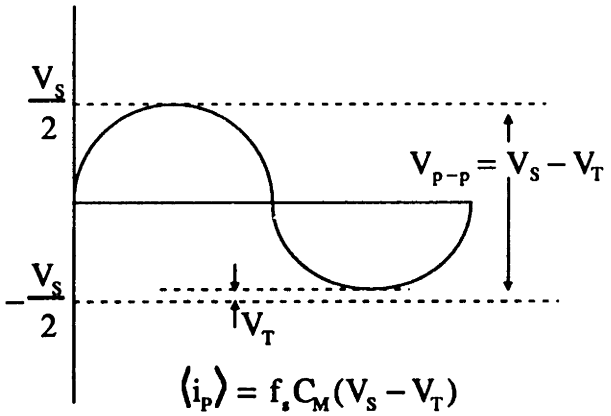

Figure 3.3.2-3: Probe Capacitance Voltage Waveform

The average current predicted by (3.3-1) becomes

$$\langle i_P \rangle = f_s C_M (V_s - V_T) \tag{3.3.2-1}$$

The dc output impedance, r_m, of the charge pump is then given by

$$r_m = \frac{1}{f_s C_M} \tag{3.3.2-2}$$

It is important to note that this model is only valid for frequencies much less than the drive frequency. Additionally, the voltage, V_T, at the probe output must be much less than a diode drop for the model to remain valid.

After averaging, the circuit shown in Figure 3.3.2-4 is obtained. The series resistances, R_S, of the inductors are shown explicitly. The replacement of the diodes and probe capacitance by an equivalent current source is a good approximation as long as the impedance seen looking back into the LC circuits is low compared to the impedance presented by the diodes and C_M at the excitation frequency. The response from perturbations in the drive voltage amplitude to the output current can be found from this averaged circuit.

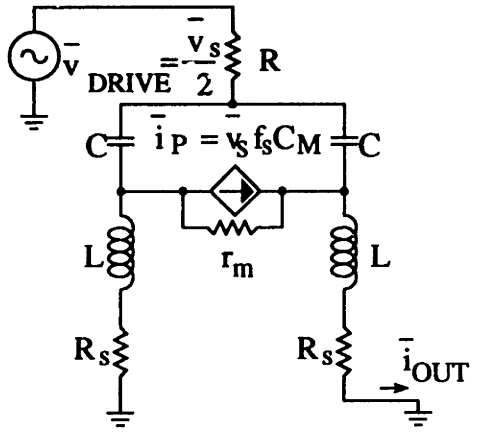

Figure 3.3.2-4: AC Analysis Circuit

The circuit may be broken down into differential and common mode circuits to simplify the analysis. The dependent current source presents a differential input. The transfer function from the dependent current source to output current is given by (3.3.2-1).

$$\frac{\bar{i}_{out}}{\bar{v}_s} = \left(\frac{1}{1+2f_sC_MR_s}\right)\left(\frac{f_sC_M}{\left(\frac{LC}{1+2f_sC_MR_s}\right)s^2+(R_sC+2f_sC_ML)s+1}\right) \qquad (3.3.2\text{-}1)$$

If the inductor series resistance, R_S, is small compared to the DC pump output resistance given in (3.3.2-2), then $\frac{\bar{i}_{out}}{\bar{v}_s}$ becomes

$$\frac{\bar{i}_{out}}{\bar{v}_s} = \left(\frac{f_sC_M}{LCs^2+(R_sC+2f_sC_ML)s+1}\right) \qquad (3.3.2\text{-}2)$$

The variations in the average value of the drive show up as signal that is common to both halves of the pump circuit. The common mode circuit used to determine the response due to variations in the average value of the drive is shown in Figure 3.3.2-5.

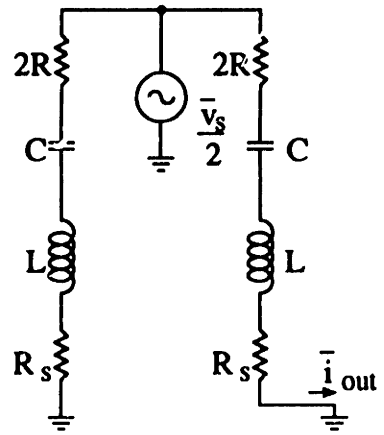

Figure 3.3.2-5: Common Mode Circuit

$$\frac{\bar{i}_{out}}{\bar{v}_s} = \left(\frac{1}{2}\right)\left(\frac{Cs}{LCs^2 + (2R + R_s)Cs + 1}\right) \tag{3.3.2-3}$$

The total response of the average output current to variations in the drive voltage is the sum of (3.3.2-2) and (3.3.2-3) and is given by

$$\frac{\bar{i}_{out}}{\bar{v}_s} = f_s C_M \frac{\frac{C}{2f_s C_M}LCs^3 + \left(2LC + \frac{C}{2f_s C_M}R_s C\right)s^2 + \left(2RC + R_s C + \frac{C}{2f_s C_M}\right)s + 1}{\left(LCs^2 + (R_s C + 2f_s C_M L)s + 1\right)\left(LCs^2 + (2R + R_s)Cs + 1\right)} \tag{3.3.2-4}$$

if $\frac{C}{2f_S C_M} >> 2(RC\text{-}f_S C_M L)$, then

$$\frac{\bar{i}_{out}}{\bar{v}_s} \approx f_s C_M \frac{\frac{C}{2f_s C_M}s + 1}{LCs^2 + (2R + R_s)C + 1} \tag{3.3.2-5}$$

If the diode polarities are reversed, the gain given by (3.3.2-1) becomes negative. This sign reversal causes the zero in (3.3.2-5) to move into the right half plane. If the circuit is to be used in a constant voltage drive system, having a right half vs. left half plane zero is of little

consequence. However, if a current control loop is to be implemented, the presence of the right half plane zero will severely limit the maximum obtainable crossover frequency.

3.3.3 Noise Analysis

In order to determine the feasibility of a given topology for high dynamic range measurements, an appropriate noise model must be developed. In this section a noise model for the circuit shown in Figure 3.3-1 is presented. The circuit shown below in Figure 3.3.3-1 can be used to determine the noise performance.

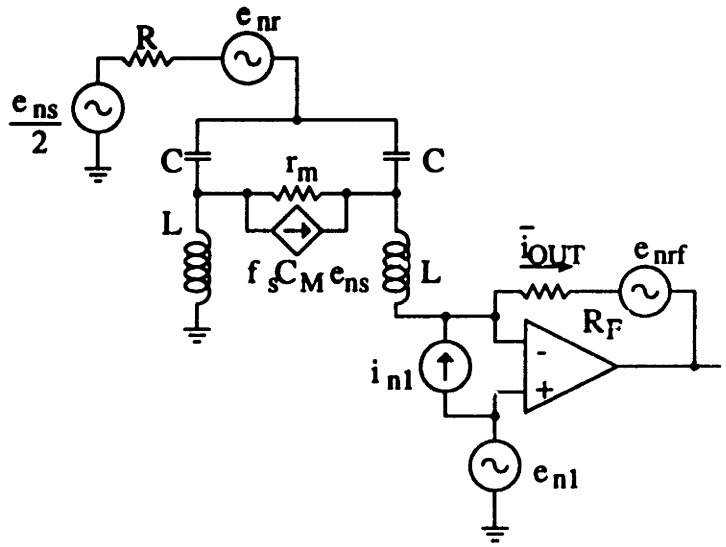

Figure 3.3.3-1: Transformerless Charge Pump Noise Model

The noise sources associated with the resistors, e_{nr} and e_{nrf}, are due to thermal noise [Gray 84] and have spectral densities given by (3.3.3-1) and (3.3.3-2).

$$S_{enr} = 4KTR \tag{3.3.3-1}$$

$$S_{enrf} = 4KTR_f \tag{3.3.3-2}$$

The noise performance of the operational amplifier can be modeled as a noiseless amplifier with an equivalent input noise voltage source, e_{n1}, and an equivalent input noise current source, i_{n1} [Gray 84]. Values for these equivalent input noise generators are given in the manufacturers data book. The spectral densities of the noise generators of the op-amp

contain a white noise component and a $\frac{1}{f}$ component. The compete spectral density is then given by

$$S_{e_n} = e_{n0}^2\left(\frac{f_{nc}}{f}+1\right) \tag{3.3.3-3}$$

Where f_{nc} is know as the $\frac{1}{f}$ noise corner frequency. A good low noise op-amp, such as the OP-27, may have input noises as low as 3 $nV/\sqrt{Hz}$ and .3 $pA/\sqrt{Hz}$ with $\frac{1}{f}$ corner frequencies around 3 Hz [Analog Devices 92].

This model ignores any contribution to the noise from shot noise in the diode. As an attempt at including diode shot noise in the model, a noise current generator was added in parallel with r_m in Figure 3.3.3-1. The spectral density of the shot noise was taken to be

$$S_{ind} = 2q\langle i_P\rangle \tag{3.3.3-4}$$

where <ip> is the average probe current. This model for diode shot noise, however, predicts a noise level that is several times larger than that observed experimentally.

Using the model presented above, the total noise present at the output of the system may now be determined. For any LTI system with a frequency response H(f), the noise at the output due to an input noise source with spectral density, S_n, can be found using (3.3.3-5). The integration limits are determined by the frequency range of interest.

$$v_{n-output}^2 = \int_{f_1}^{f_h} S_n(f)|H(f)|^2 df \tag{3.3.3-5}$$

When multiple noise sources are present, the total output noise is the RMS sum of the noise due to each source provided the noise sources are uncorrelated. All that remains now is to determine the gain from each noise source in Figure 3.3.3-1 to the output of the system. The transfer functions are listed below.

$$\frac{v_{out}}{e_{ns}} \approx R_F f_s C_M \frac{\frac{C}{2f_s C_M}s+1}{LCs^2+(2R+R_s)C+1} \tag{3.3.3-6}$$

$$\frac{v_{out}}{e_{nr}} = \left(\frac{R_F Cs}{LCs^2 + (2R + R_s)Cs + 1} \right) \tag{3.3.3-7}$$

$$\frac{v_{out}}{i_{n1}} = R_F \tag{3.3.3-8}$$

$$\frac{v_{out}}{e_{nrf}} = 1 \tag{3.3.3-9}$$

$$\frac{v_{out}}{e_{n1}} = \frac{LCs^2 + (R_T + R_F)Cs + 1}{LCs^2 + R_T Cs + 1} \tag{3.3.3-10}$$

where $R_T = R_S + R||R_S$.

The inductor series resistances are ideally very small. This leads to a very large peak in the noise around the resonant frequency of the LC circuit. Additionally, the zero in (3.3.3-6) can result in very large noise gains that are within the frequency range of interest. Given these possible difficulties, a different charge pump topology that does not exhibit the same peaking in the noise gain will be examined.

3.4 Transformer Coupled Charge Pump

An alternative to the transformerless charge pump is shown below in Figure 3.4-1. The inductance, L, represents the magnetizing inductance of the transformer. The basic operation of this circuit is that same as the one examined in Section 3.3. During the first half cycle, the probe capacitance, C_M, is charged to $\frac{V_S}{2}$ through D_1. During the second half of each cycle, C_M is discharged to $\frac{-V_S}{2}$ through D_2. The average current through the diodes is then given by (3.4-1). An auxiliary winding is used in conjunction with D_3 and D_4 to drive the guard.

$$\langle i_P \rangle = V_S f_s C_M \tag{3.4-1}$$

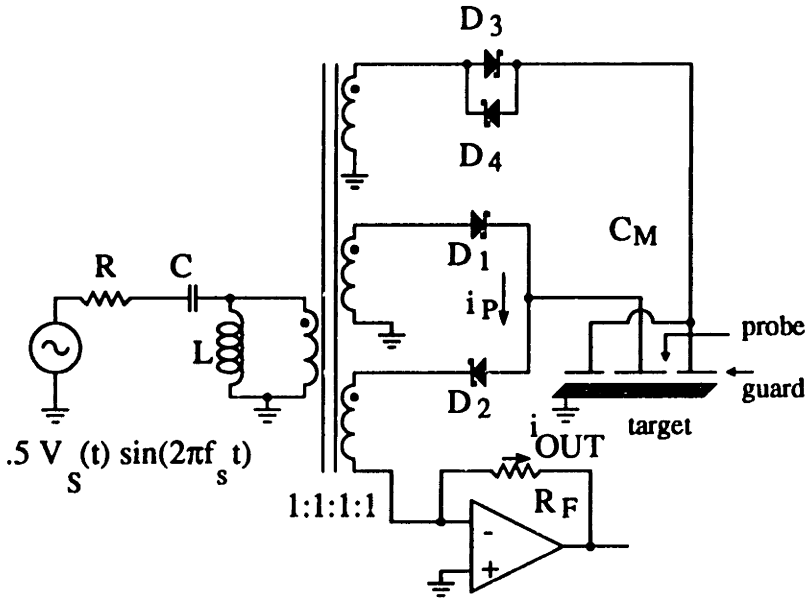

Figure 3.4-1: Transformer Coupled Charge Pump

The output resistance of the charge pump is identical to that of the transformerless charge pump given by (3.3.2-2). One feature of the transformer coupled charge pump that is of interest is that the impedance presented to the operational amplifier does not exhibit a sharp resonant dip. This feature is different from the transformerless pump examined in Section 3.3.

3.4.1 Frequency Response

An averaged model for the transformer coupled charge pump may be developed in a manner similar to the analysis in Section 3.3.2. The averaged model is shown below in Figure 3.4.1-1.

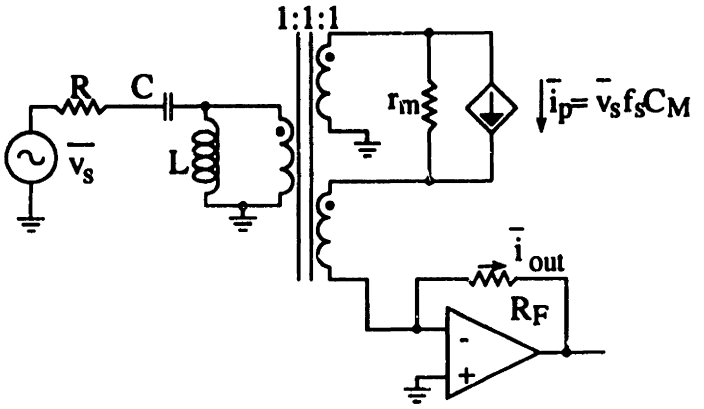

Figure 3.4.1-1: Averaged Model for a Transformer Coupled Charge Pump

The model shown in Figure 3.4.1-1 can be simplified to yield the model shown below in Figure 3.4.1-2.

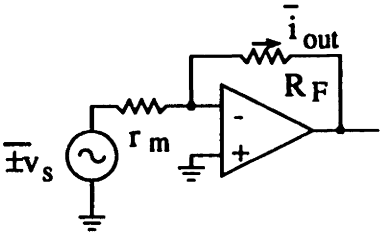

Figure 3.4.1-2: Simplified Averaged Circuit Model

The choice of polarity for the drive voltage in Figure 3.4.1-2 is determined by the orientation of the diodes in Figure 3.4-1.

3.4.2 Noise Analysis

The model shown in Figure 3.4.1-2 can be modified to include the various noise generators present in the circuit. The resulting model is shown below in Figure 3.4.2-1.

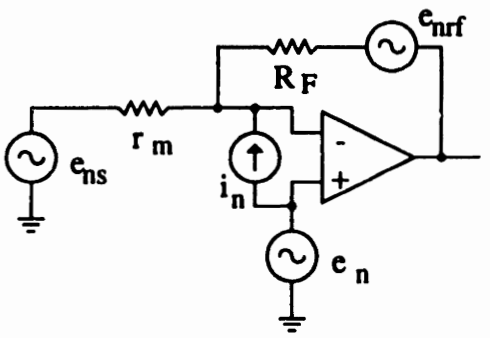

Figure 3.4.2-1: Transformer Coupled Charge Pump Noise Model

The operational amplifier noise is modeled by e_n and i_n, e_{nrf} is due to thermal noise in R_F, and e_{ns} is noise in the amplitude of the RF drive. The analysis of the model is now a simple task. The total output noise of this circuit is

$$e_{now}^2 = e_{ns}^2\left(\frac{R_F}{r_m}\right)^2 + i_n^2 R_F^2 + e_n^2\left(1+\frac{R_F}{r_m}\right)^2 + e_{nrf}^2 \qquad (3.4.2\text{-}1)$$

For small probe capacitances and/or low drive frequencies, the input current noise of the operational amplifier and thermal noise in the feedback resistor tend to dominate the noise. At higher drive frequencies and capacitances, the input voltage noise also is a significant contributor.

3.5 AC Bridge

The final type of measurement circuit to be examined is the ac bridge circuit. The ac bridge circuit consists of a sinusoidal drive signal, a circuit whose output amplitude varies as the probe capacitance varies, and a synchronous detector and low pass filter to measure the amplitude of the output.

3.5.1 Single Ended Bridge

The first of the bridge type circuits is shown below in Figure 3.5.1-1. By placing the probe capacitance in the feedback path of an operational amplifier and using a reference capacitor for the input path, the output may be made proportional to $\frac{1}{C_M}$ where C_M is the probe capacitance. This circuit was developed by the Wayne Kerr Company Limited [Richards 75]. It has been commercialized by ADE Corporation and some aspects of it may be covered by US Patent #4,918,376.

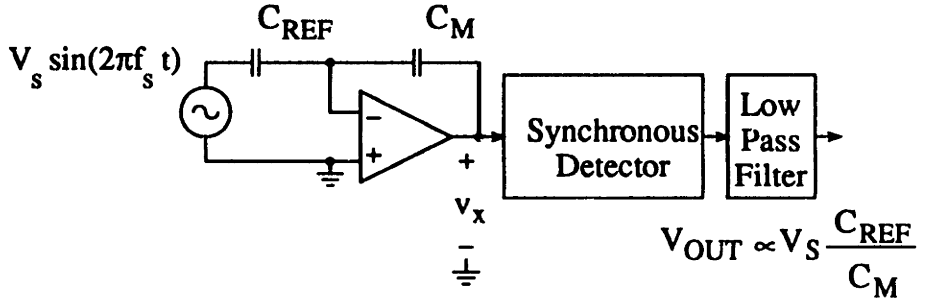

Figure 3.5.1-1: Single Ended Bridge

The input to the detector is

$$v_x(t) = V_S \sin(2\pi f_s t)\left(\frac{C_{REF}}{C_M}\right) \qquad (3.5.1\text{-}1)$$

The output of the lowpass filter is simply the amplitude of v_x.

Although the circuit as drawn doesn't allow for one side of the probe to be grounded, a simple modification shown in Figure 3.5.1-2 allows for that.

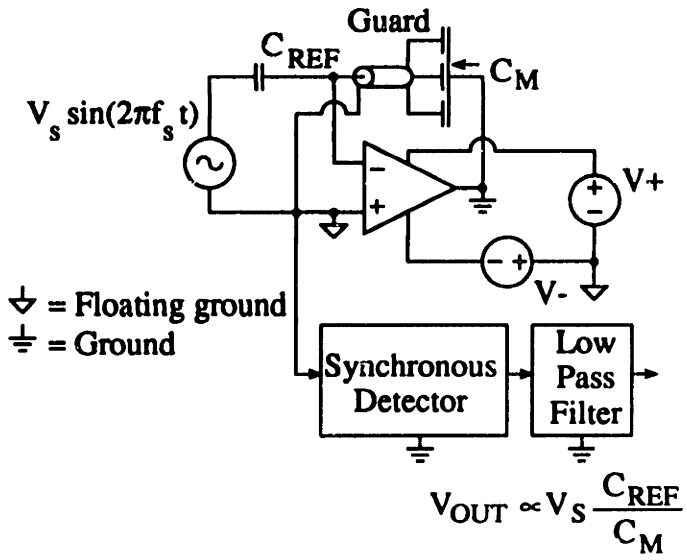

Figure 3.5.1-2: Single Ended Bridge with Grounded Probe

3.5.1.1 Frequency Response

The frequency response of the bridge circuit is largely determined by the characteristics of the low pass filter in Figure 3.5.1-1. The requirements on the low pass filter are bounded by two limits. The high frequency attenuation must be sufficient to reduce components at the excitation frequency and its harmonics to a level below the noise floor. The phase shifts at lower frequencies, however, must not be appreciable if the sensor is to be used inside of a feedback loop.

3.5.1.2 Noise Analysis

The noise appearing at the output of the circuit in the signal band results from two sources. The first source is noise near the excitation frequency (and possibly its harmonics) that is demodulated into the signal band by the detector. The second source of baseband noise is that generated in the detector and low pass filter.

Consider the operation of a demodulator in which the input signal contains noise, n(t), in addition to the desired signal.

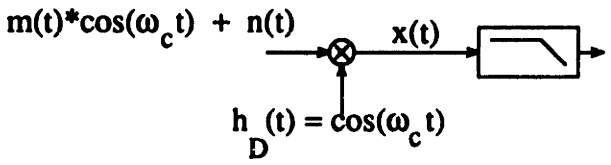

Figure 3.5.1.2-1: Synchronous Demodulator

If n(t) contains energy around the carrier frequency, the high frequency noise will be demodulated into the signal band. This is illustrated in Figure 3.5.1.2-2.

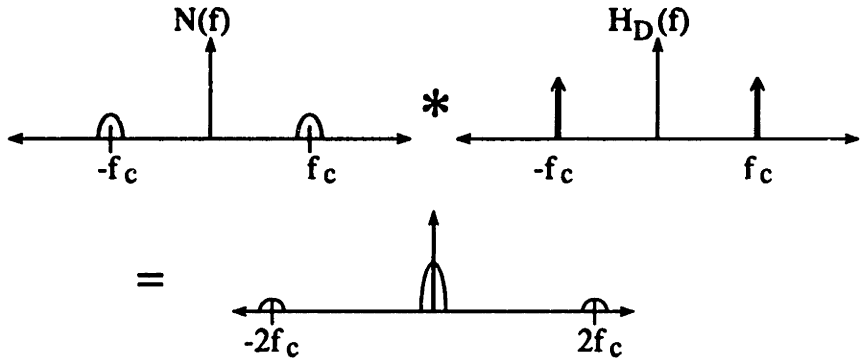

Figure 3.5.1.2-2: Demodulation of Noise

Many practical demodulators simply switch synchronously between an inverting and noninverting gain. This is equivalent to multiplying by a square wave. The implication of using a square wave demodulator is that in addition to demodulating noise around the carrier frequency, noise at its odd harmonics will also be demodulated. Since the amplitude of the harmonics fall off as $\frac{1}{n}$, their presence doesn't present a real problem as long as there are no peaks in the noise levels near the harmonics.

A noise model for the single ended bridge circuit is shown below in Figure 3.5.1.2-3. The capacitance of the cable going to the probe is represented by C_I. For the purposes of the analysis here, it is assumed that the detector contributes negligible amounts of noise.

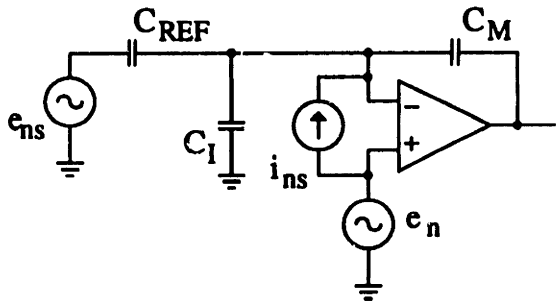

Figure 3.5.1.2-3: Single Ended Bridge Noise Model

$$e_{nout}^2 = \left(\frac{C_{REF}}{C_M}\right)^2 e_{ns}^2 + \left(1 + \frac{C_{REF} + C_I}{C_M}\right)^2 e_n^2 + \left(\frac{1}{2\pi f_s C_M}\right)^2 i_n^2 \qquad (3.5.1.2\text{-}1)$$

For probe capacitances that are small compared to the cable capacitance, the input voltage noise of the operational amplifier sees a large gain and tends to dominate the noise performance. For audio frequency drives, an op-amp with very low input current noise must be chosen as the impedance of C_M may be quite large. For sensitive instruments, great care must be taken in generating a very low amplitude noise drive voltage. The design of a suitable drive is a significant portion of the design of a system based on the ac bridge approach.

3.5.1.3 Other Issues

There are a few issues involved with the design of an ac bridge circuit that are worth mentioning. In order for the output to vary linearily with displacement as desired, the operational amplifier must have a large open loop gain at the drive frequency. This requirement places a limit on how high a drive frequency may be used. Additionally, the drive must have very low noise around the drive frequency. If a high frequency drive is used, a feedback loop may be used to stabilize the amplitude of the drive.

3.5.2 Transformer Ratio Arm Bridge

The final type of measurement circuit to be examined is the transformer ratio arm bridge shown in Figure 3.5.2-1. An alternative arrangement that allows the probe capacitance to be grounded is shown in Figure 3.5.2-2. The output impedance of the

transformer ratio bridge is simply that of the parallel combination of C_M and C_{REF}. A guarded cable is used to reduce any loading due to cable capacitance and other stray capacitances.

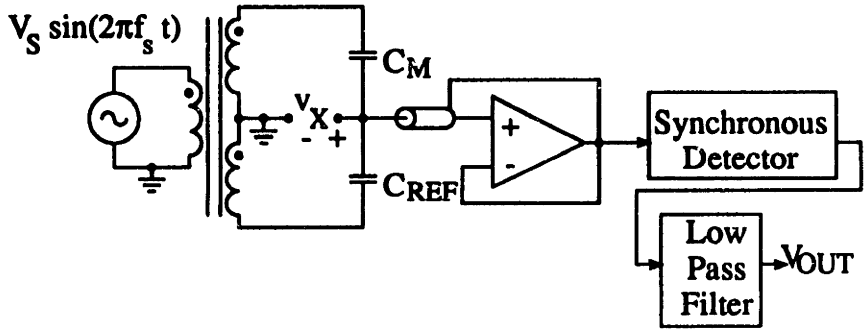

Figure 3.5.2-1: Transformer Ratio Arm Bridge

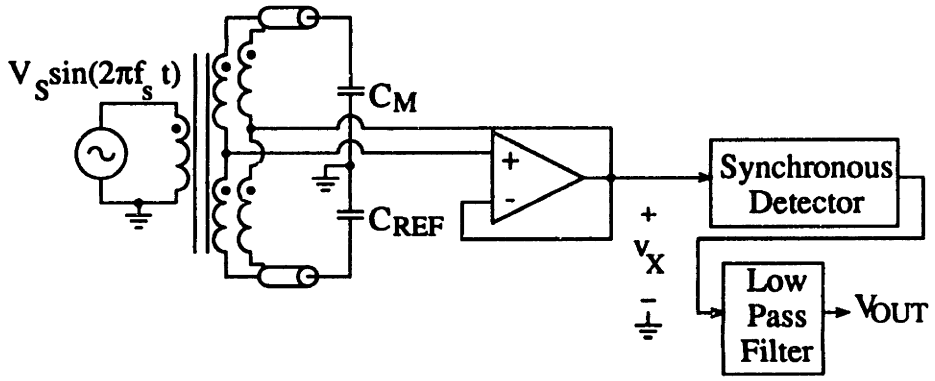

Figure 3.5.2-2: Alternate Transformer Ratio Arm Bridge

The output of the transformer ratio arm bridge is

$$v_X(t) = \left(\frac{C_M - C_{REF}}{C_M + C_{REF}}\right) V_S \sin(2\pi f_s t) \tag{3.5.2-1}$$

After demodulation and low pass filtering, the amplitude of (3.5.2-1) is recovered. If the probe is differential in nature, such as the sensor described by (3.5.2-2), then the output is linearly dependent on displacement as given by (3.5.2-3).

$$C_M = \frac{\varepsilon A}{D-d}, C_{REF} = \frac{\varepsilon A}{D+d} \tag{3.5.2-2}$$

$$\left(\frac{C_M - C_{REF}}{C_M + C_{REF}}\right) = \frac{d}{D} \tag{3.5.2-3}$$

If the probe is a single ended capacitance, then the output becomes a nonlinear function of displacement. In this case it may desirable to consider an alternative to the transformer ratio arm bridge which gives a linear response. One such alternative was examined in Section 3.5.1.

3.5.2.1 Frequency Response

The dynamics of the transformer ratio arm bridge are essentially the same as the single-ended bridge described in Section 3.5.1.1.

3.5.2.2 Noise Analysis

The noise performance of the transformer ratio arm bridge differs from that of the single-ended bridge only slightly. A noise model for the circuit is shown in Figure 3.5.2.2-1. The cable capacitance is represented by C_I.

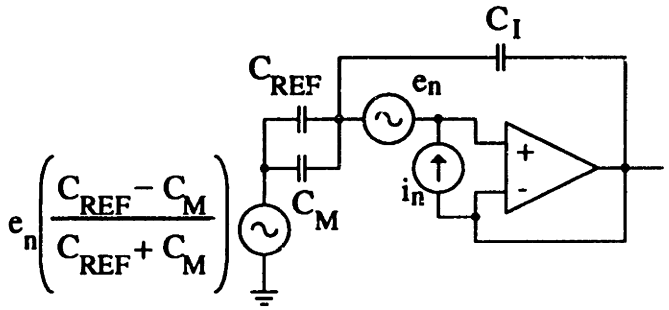

Figure 3.5.2.2-1: Transformer Ratio Arm Bridge Noise Model

The noise at the output of the bridge after demodulation is given by (3.5.2.2-1). As in section 3.5.1.2, the noise contribution of the demodulator and low pass filter have been ignored.

$$e_{nout}^2 = \left(\frac{C_M - C_{REF}}{C_M + C_{REF}}\right)^2 e_{ns}^2 + \left(\frac{1}{2\pi f_s (C_{REF} + C_M)}\right)^2 i_n^2 + \left(1 + \frac{C_I}{C_{REF} + C_M}\right)^2 e_n^2 \qquad (3.5.2.2\text{-}1)$$

The main feature of the noise performance of the transformer ratio arm bridge that differs from that of the single ended bridge is the effects of noise in the drive voltage. In the

transformer bridge, the effects of drive voltage noise are ideally zero when the bridge is balanced. This cancellation, however, only occurs for one particular location of the sensor.

3.6 Summary

Three general classes of probe drive circuits have been discussed. The transformer coupled charge pump and the single ended ac bridge circuit show the most promise for low noise measurement. Both approaches allow for an output which is linearly dependent on probe displacement. The charge pump allows for a higher frequency drive. This is true because the charge pump demodulates the probe current and uses a low frequency feedback loop to force a constant current. At the lower frequencies involved in the control loop, a large ammount of gain is possible. With the ac bridge, however, the constant current in the probe is being controlled by a feedback loop operating at the drive frequency. This places a limit on the maximum drive frequency. Using a higher probe current will generally allow for a lower noise measurement. Given this, the transformer coupled charge pump approach was chosen.

4 A/D Conversion

4.1 Overview

The sensors developed in this thesis are intended for use in a digitally controlled system. In order to achieve a 10^6:1 dynamic range, the digital output must be 20 bits. The control loop requires an output data rate of 1 kHz with an overall time delay of less than ~5 ms. The best commercially available A/D converters that are able to deliver 20 bits introduce severe time delays. The Crystal Semiconductor CS5323, for example, can deliver a 121 dB dynamic range with a 1 kHz sampling rate. The group delay, however, is 30 ms. This chapter will explore some techniques for A/D conversion which may meet the requirements at hand.

4.2 Dual Slope Integration

Dual slope integration is a popular technique for analog to digital conversion. A basic dual slope integrator is shown below in Figure 4.2-1.

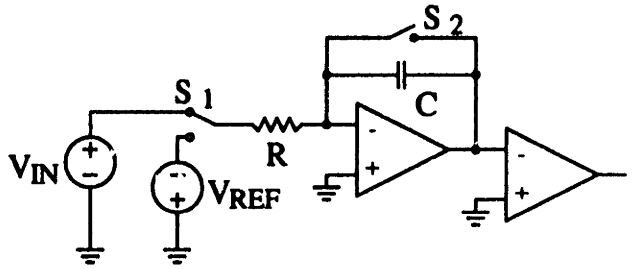

Figure 4.2-1: Dual Slope Integrator

The basic conversion cycle is as follows: Prior to the start of a conversion cycle, Switch S_1 is connected to the input, and S_2 is closed forcing the output of the integrator to be zero. S_2 is then opened and the input voltage is integrated for a fixed period of time, T_1. This portion of the cycle is known as up integration. At the end of up integration, S_1 is connected to a reference voltage. The reference is then integrated for a period of time, T_2,

until the integrator output returns to zero. The output of the integrator during a complete conversion cycle is shown below in Figure 4.2-2.

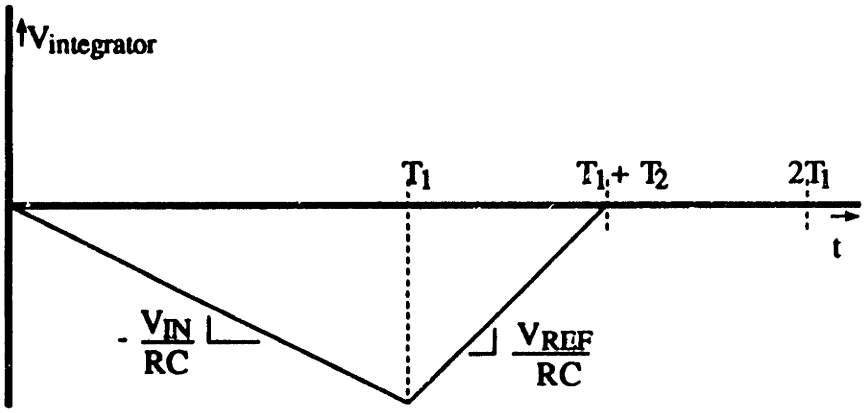

Figure 4.2-2: Integrator Voltage During Complete Conversion Cycle

The down integration time, T_2, is determined by

$$\int_0^{T_1} -\frac{V_{IN}}{RC}dt + \int_{T_1}^{T_1+T_2} \frac{V_{REF}}{RC}dt = 0 \qquad (4.2\text{-}1)$$

For a dc input, the ratio of down integration time to up integration time is given by

$$\frac{T_2}{T_1} = \frac{V_{IN}}{V_{REF}} \qquad (4.2\text{-}2)$$

A significant feature of this relation is that the specific values of R and C don't matter as long as they remain constant over the conversion cycle. In addition, the output is a ratio of two times. By using the same clock to measure T_1 and T_2, the ratio may be determined to a great degree of accuracy without requiring a very good absolute time reference. A final feature of dual slope integrators that makes them attractive is that the output depends on the average of the input over the up integration period as opposed to its instantaneous value. This decreases the sensitivity to noise on the input.

The main disadvantage of an integrating converter is the long conversion time. Assuming that T_1 and T_2 are measured with a digital clock and a counter, the conversion time is

$$T_{conversion} = \frac{2^{\#\,of\ bits+1}}{f_{CLK}} \qquad (4.2\text{-}3)$$

Using a 20 MHz clock, it would take 100 ms to obtain a 20-bit conversion. Given this, it is clear that a straight dual-slope converter is not adequate.

4.2.1 Frequency Response

The frequency response of the A/D converter is important for two reasons. In order to use the converter in a feedback loop, its dynamics must be fairly well behaved. In addition, the noise performance of a converter is somewhat dependent on its frequency response. The response of an integrating converter may be broken down into three parts as illustrated in Figure 4.2.1-1.

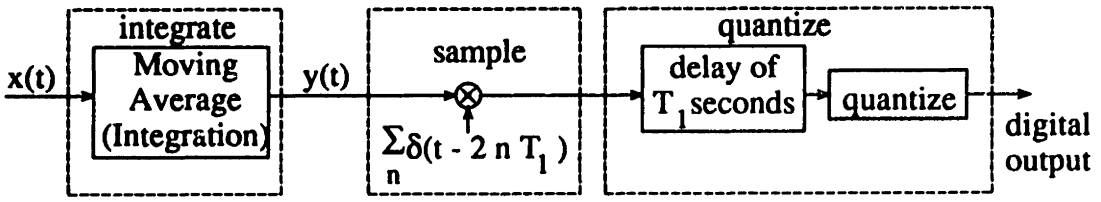

Figure 4.2.1-1: Converter Block Diagram

The first block models the up integration portion of the conversion cycle. Its operation is defined by

$$y(t) = \frac{1}{T_1} \int_{t-T_1}^{t} x(t)dt \qquad (4.2.1\text{-}1)$$

The integral in (4.2.1-1) can be viewed as the convolution of x(t) with the impulse response shown below in Figure 4.2.1-1. The frequency response is then given by (4.2.1-2).

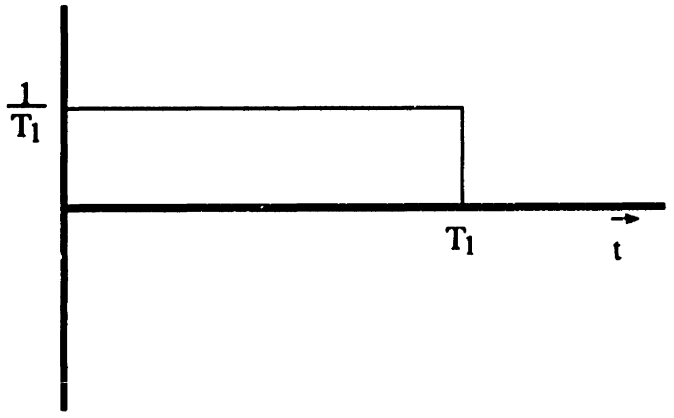

Figure 4.2.1-1: Integrator Impulse Response

$$H_1(s) = \frac{1}{T_1}\left(\frac{1}{s} - \frac{1}{s}e^{-sT_1}\right) \tag{4.2.1-2}$$

The second part of the frequency response is a pure time delay due to the down integration portion of the cycle. Assuming that the output of the converter is read $2T_1$ seconds after the start of the conversion, the down integration portion simply adds a delay of T_1 seconds. The final part of the transfer function is due to sampling and transforming from a continous time system to a discrete time system. Since this portion has little to do with the dynamics of the particular converter being analyzed, it will be omitted from the response. The complete transfer function is then

$$H_{tot}(s) = \frac{1}{T_1}\left(\frac{1-e^{-sT_1}}{s}\right)e^{-sT_1} \tag{4.2.1-3}$$

A little algebraic manipulation yields

$$H(j2\pi f) = \left(\frac{\sin(\pi T_1 f)}{\pi T_1 f}\right)\left(e^{-j3\pi T_1 f}\right) \tag{4.2.1-4}$$

4.2.2 Noise Analysis

When dealing with circuits that have white noise sources, it is often convenient to determine the noise bandwidth, f_n. The noise bandwidth, may be found using (4.2.2-1) [Gray 85].

$$f_N = \frac{1}{|H(j0)|^2}\int_0^{\infty}|H(jf)|^2\,df \tag{4.2.2-1}$$

Substituting (4.2.1-4) into the equation for noise bandwidth gives

$$f_N = \int_0^{\infty}\left(\frac{\sin(\pi T_1 f)}{\pi T_1 f}\right)^2 df = \frac{1}{2T_1} \tag{4.2.2-2}$$

Using the noise bandwidth given by (4.2.2-2), the total noise at the input of the comparator is

$$v_n^2 = \left(4kTR + S_{en} + S_{in}R^2\right)\left(\frac{T_1 + T_2}{RC}\right)^2\left(\frac{1}{2(T_1 + T_2)}\right) + S_{enref}\left(\frac{T_2}{RC}\right)^2\left(\frac{1}{2T_2}\right) + S_{encomp}f_{ncomp} \tag{4.2.2-3}$$

The operational amplifier noise is modeled by equivalent input generators, e_n and i_n, the noise in the reference is e_{nref}, and the comparator input noise is e_{ncomp}. The voltage noise at the input to the comparator translates into a time noise that is equal to the noise voltage divided by the slope of the voltage. The noise in the digital output is then given by (4.2.2-5).

$$T_n = RC\left(\frac{v_n}{V_{REF}}\right) \tag{4.2.2-4}$$

$$Noise = \frac{T_n}{T_{CLK}}\left(LSB \cdot s_{RMS}\right) \tag{4.2.2-5}$$

4.2.3 Application to Capacitance Probes

The dual slope integrator may be used in conjunction with one of the charge pump circuits examined in Chapter 3 to obtain a digital output that is directly proportional to probe displacement [Roberge 93]. Recall that the charge pumps produced a current that is proportional to the probe capacitance. If a reference current is integrated during the up integration portion of the cycle and the pump current is used during down integration, then the output is

$$\frac{T_2}{T_1} = \frac{I_{REF}}{V_{p-p}f_s C_M} \propto d \tag{4.2.3-1}$$

By using another pump circuit with a fixed reference capacitor to generate the reference current, an output which is simply the ratio of the reference capacitance to the probe capacitance is obtained.

4.3 Subranging Converter

The main disadvantage to the dual slope converter is the long conversion time. One approach to decreasing the conversion time is to use a subranging, also known as a dual rank, converter. The basic configuration is shown below in Figure 4.3-1.

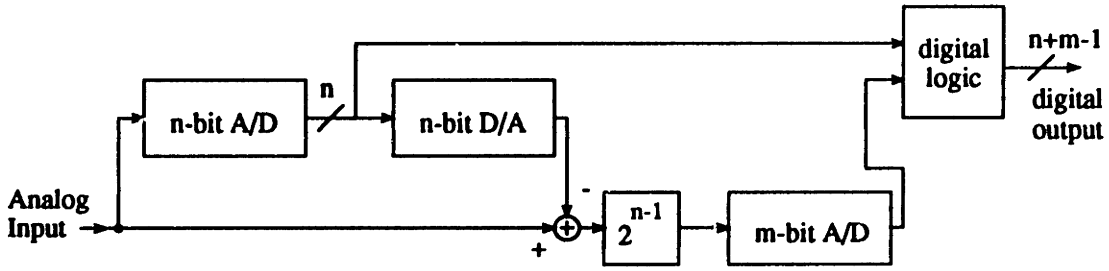

Figure 4.3-1: Dual Pass Converter

The basic operation is as follows: The analog input is converted to a n-bit digital representation. The initial approximation is subtracted from the input. The remainder is then amplified and converted to gain a additional resolution. Commercially available converters are able to provide a combination of high resolution and high sampling rate. The Burr-Brown ADC701, for example, delivers a 16-bit output at a 512 kHz sampling rate.

With a subranging converter, care must be taken to insure that the input doesn't change by more than 1 LSB of the initial A/D during a conversion cycle. If the input changes by more than an LSB, the amplifier will saturate and the second A/D input will be overdriven. If the input signal to the converter is arbitrary, then it is necessary to use a sample and hold (S/H) to hold the input constant during conversion. If, however, it is known that the input won't vary appreciably over 1 conversion cycle then the S/H may be omitted.

By getting 8 bits from an initial conversion and 12 bits from the second conversion, it may be possible to construct a satisfactory subranging converter. The probe displacement can be constrained to move less than 1 LSB at the 8 bit level during a conversion cycle. By including appropriate overload detection circuitry, a converter may be constructed which gives a coarser resolution for rapidly changing inputs.

4.4 Oversampled Converters

4.4.1 Quantization Noise

It can be shown that under certain conditions, the quantization error of an A/D converter may be modeled as an additive white noise [Candy 92a]. The exact derivation of the conditions under which this assumption is valid is beyond the scope of this thesis. An exhaustive development of the spectra of quantization noise is given in [Gray 90]. [Candy 92b] contains an excellent collection of articles covering oversampled data converters. The assumption that the quantization noise is white breaks down in a few important cases. The first case is for a dc input. The second case is for an input which changes by an integer number of least significant bits (LSB's) between samples. In both of these special cases, the quantization noise is a dc value. These two cases may be avoided by adding a dither signal to the input that is large enough to change the input by several LSB's. The dither has the effect of decorrelating the noise from the input. By using a dither signal which may be generated in both analog and digital form, it may be subtracted digitally from the result.

If the quantization error in each sample is assumed to be uniformly distributed between $\pm\frac{1}{2}$ LSB then the RMS value of the noise is simply

$$e_{RMS} = \sqrt{\frac{1}{1\ \text{LSB}} \int_{-\frac{1}{2}\text{LSB}}^{\frac{1}{2}\text{LSB}} e^2 de} = \frac{1\ \text{LSB}}{2\sqrt{3}} \tag{4.4.1-1}$$

If the input is sampled at a rate, f_S, then all of the noise power shows up in the 0 to $\frac{f_S}{2}$ frequency range. The spectral density of the quantization noise is then given by

$$S(f) = e_{RMS}^2 \frac{2}{f_s} \tag{4.4.1-2}$$

The total noise in the signal band is simply equal to e_{RMS}.

Consider the effect of sampling at a rate that is n times larger than f_S. The noise is now spread out over a wider frequency range. The resulting spectral density is

$$S(f) = e_{RMS}^2 \frac{2}{nf_s} \tag{4.4.1-3}$$

The total noise in the signal band ($0 \le f \le \frac{f_s}{2}$) is reduced to

$$e_n = \frac{e_{RMS}}{\sqrt{n}} \tag{4.4.1-4}$$

From (4.4.1-4) it is evident that for every doubling of the sampling rate, a 3 dB, or $\frac{1}{2}$ bit improvement in the noise floor is obtained. While useful for obtaining a few extra bits from a converter, straight oversampling is not practical as a means of significantly improving the resolution of a converter.

4.4.2 Noise Shaping

Noise shaping is an approach to data conversion that provides substantial improvement in the overall signal-to-noise ratio (SNR) of a low resolution converter using a modest amount of oversampling. A noise shaping loop is shown in Figure 4.4.2-1. The assumed white quantization noise is represented by e_n. H(f) is a low pass transfer function which typically includes one or more integrations. The closed loop transfer functions from the analog input and noise to output are given by (4.4.2-1) and (4.4.2-2).

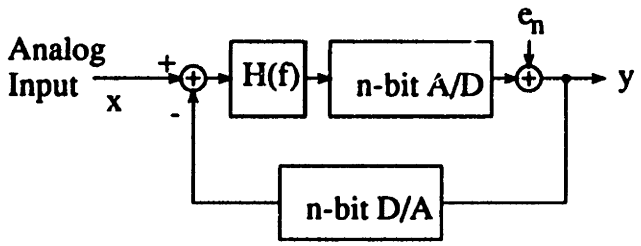

Figure 4.4.2-1: Noise Shaping Loop

$$\frac{Y}{X} = \frac{H(f)}{1 + H(f)} \tag{4.4.2-1}$$

$$\frac{Y}{e_n} = \frac{1}{1 + H(f)} \tag{4.4.2-2}$$

By recognizing that |H(f)| is very large at low frequencies, it is evident that the noise power at the output has now been shifted to higher frequencies. By using a digital low pass filter

to remove the high frequency noise, substantial improvements in SNR may be made with relatively low oversampling ratios. For example, straight oversampling with no noise shaping gives .5 bits improvement for every doubling of the sampling rate. A first order noise shaping loop will give 1.5 bits and a second order loop will give 2.5 bits for every doubling of the sampling rate. Higher order loops may provide even greater improvement. In practice, the A/D and D/A are typically 1-bit converters. The Crystal Semiconductor CS5349 uses 1-bit converters, a 4^{th} order noise shaping loop and 64x oversampling to achieve a 16-bit audio ADC.

Although oversampled A/D converters show great promise for relatively fast, high resolution data conversion, a suitable converter is not commercially available at this time.

4.5 Summary and Choice of A/D Approach

Three types of A/D converters have been examined. The dual slope integrator, while capable of very high resolution, is simply not fast enough for the application at hand. A subranging converter approach looks quite promising, but the design of such a converter is not realistic for this thesis effort. By using a 16-bit, 512 kHz A/D and averaging 512 samples, a resolution equivalent to 20.5 bits at a 1 kHz sample rate may be obtained.

5 Hardware Design

5.1 Overview

The final design is based on the transformer coupled charge pump drive examined in Section 3.4. In this design, the system is arranged in a constant probe current mode in order to obtain an output that is linearly dependant on the probe displacement. A simplified schematic for the system is shown below in Figure 5.1-1.

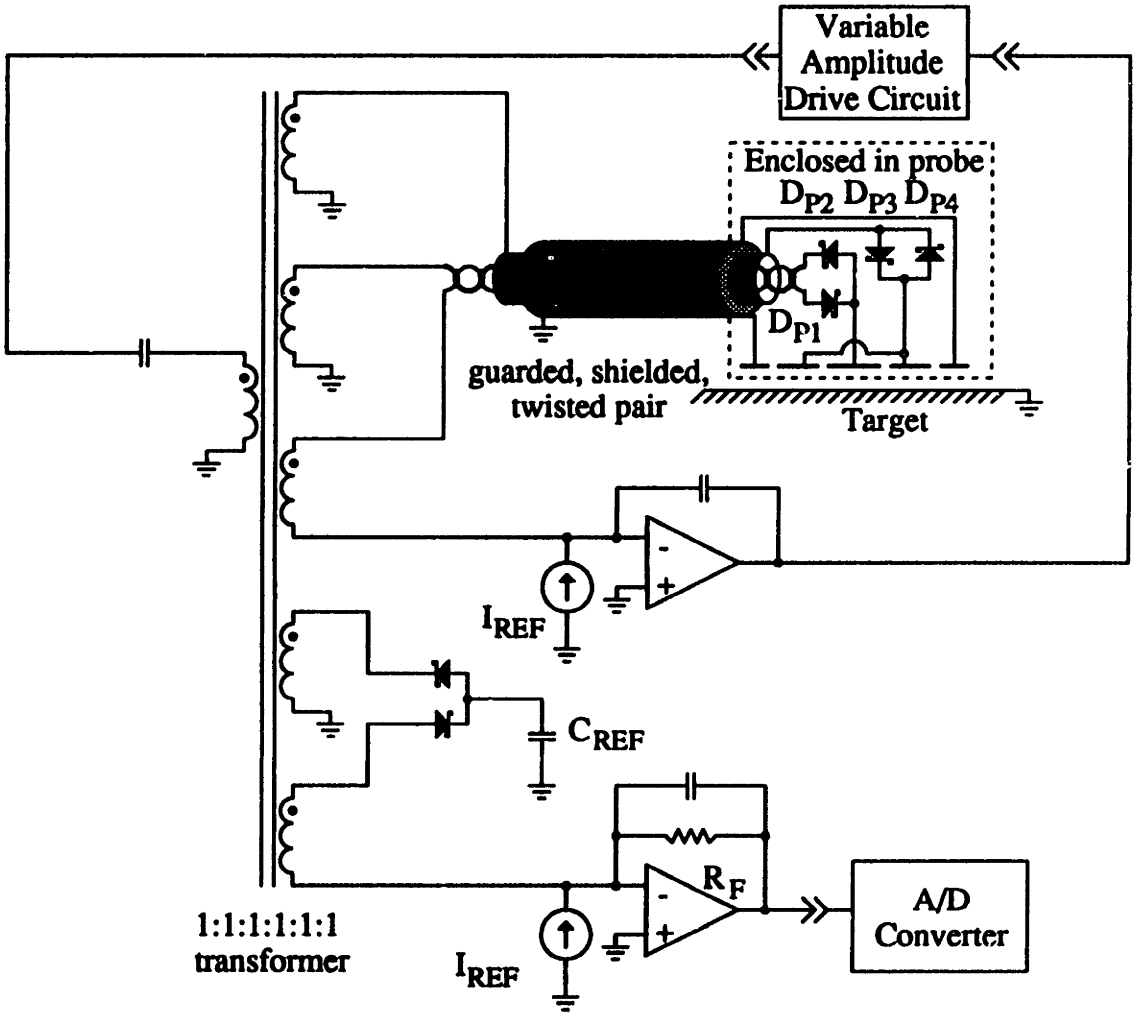

Figure 5.1-1: Simplified System

The feedback loop forces the average probe charge pump current to be equal to a reference current, I_{REF}. The peak-to-peak amplitude of the drive voltage is

$$V_{p-p} = \frac{I_{REF}}{f_s C_M} \tag{5.1-1}$$

where f_S is the drive frequency and C_M is the probe capacitance. The output current from the reference charge pump is

$$\langle i_{out} \rangle = V_{p-p} f_s C_{REF} = I_{REF}\left(\frac{C_{REF}}{C_M}\right) \tag{5.1-2}$$

The second reference current is used to give an output of zero when the probe is in its nominal position. The output voltage of the circuit is

$$V_{OUT} = R_F I_{REF}\left(\frac{C_{REF}}{C_M} - 1\right) = (R_F I_{REF})\left(\frac{1}{d_{nom}}\right)(d - d_{nom}) \tag{5.1-3}$$

5.2 Probe Circuit Details

5.2.1 Probe Details

The circuit is designed for a probe with a circular active area. The operating range is from 50 microns to 150 microns. The probe diameter in this design is chosen to be 12.5 mm. This gives a nominal probe capacitance of 11 pF at a 100 micron displacement. If a lower noise system is desired, a larger capacitance should be used. The larger capacitance may be achieved either by using a larger area probe or by filling the gap with a dielectric.

5.2.2 Probe and Reference Charge Pumps

The probe and reference charge pumps are shown below in Figure 5.2.2-1.

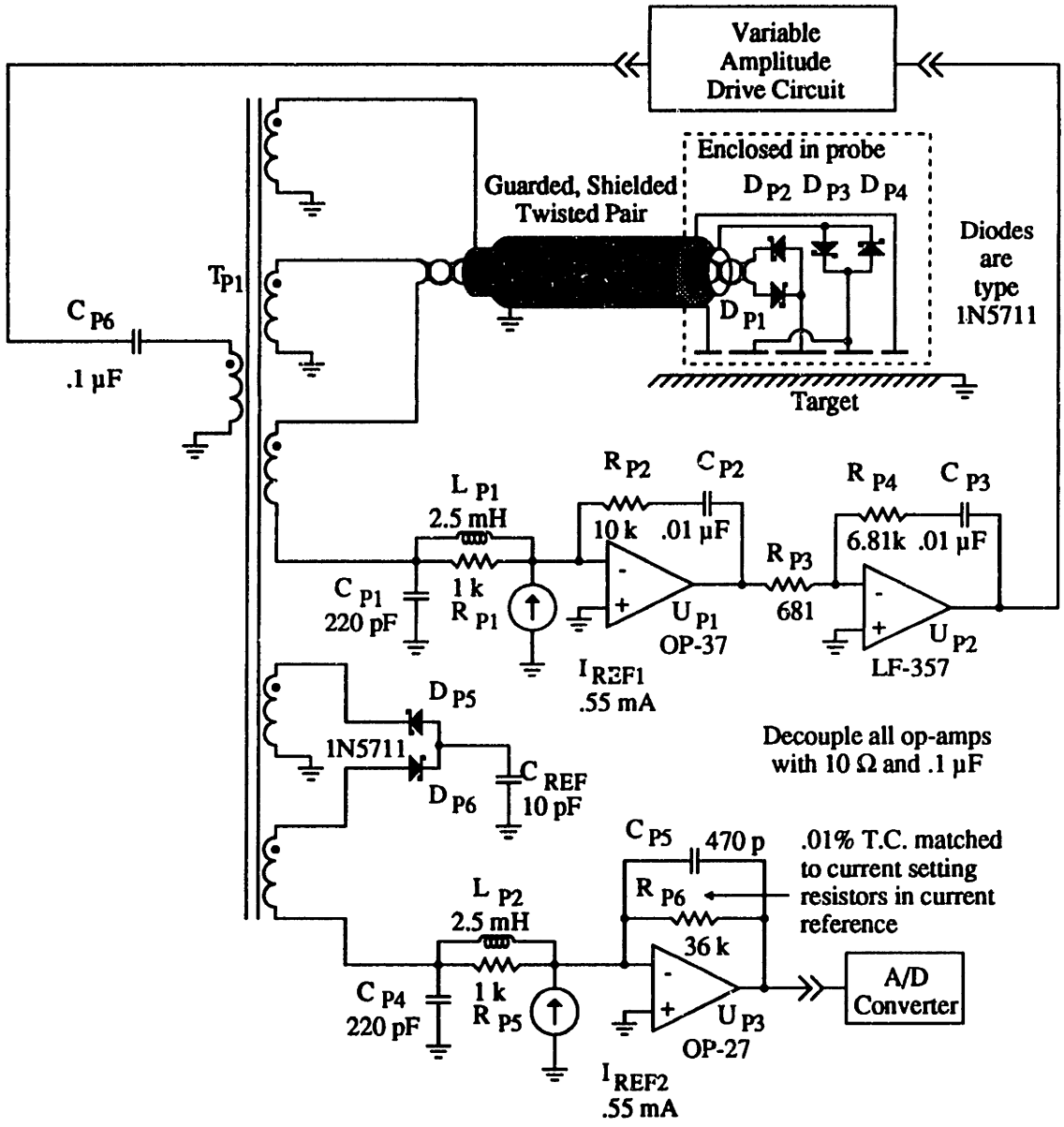

Figure 5.2.2-1: Probe and Reference Charge Pumps

The operation of the circuit is essentially the same as in the simplified system. A few important differences exist however. In the simplified circuit, the operational amplifier was assumed to be ideal. This assumption implies that the voltage at its inverting input is zero. In reality, however, the virtual ground at the inverting input to U_{P1} isn't very low impedance at the 5 MHz drive frequency. Having a nonzero voltage at that node can cause both of the charge pump diodes to conduct simultaneously. This condition will increase both measurement errors and the noise level. The filter network formed by C_{P1}, L_{P1},and R_{P1}

maintains a voltage at the bottom of the transformer winding that is close to zero. A similar network is included in the reference charge pump circuit. Including the filters in the circuit reduced the noise floor by almost 12 dB.

The transformer was wound on a FerroxCube 2213 size ungapped pot core. The core material is 4C4 which is a good high frequency ferrite. In order to assure tight coupling, the windings were wound together.

The feedback resistor, R_{P6}, in the reference charge pump circuit in conjunction with the reference current sets the gain of the system. In order to minimize thermal variations, the temperature coefficient of R_{P6} should be matched to that of the current setting resistors in the current reference.

5.2.3 Oscillator and Buffer

The oscillator and buffer are shown below in Figure 5.2.3-1. The oscillator is a Colpitts oscillator with output frequency determined by $\frac{1}{\sqrt{L_{O1}C_{O1}}}$. For the part values used, the drive frequency is ~5MHz. The oscillator output is buffered by a "diamond" follower. The buffer must be capable of driving the probe capacitance and any capacitance associated with the cable and guard.

The transfer function from the control voltage to peak-to-peak output amplitude can be modeled by the single pole low-pass system given by (5.2.3-1). See Appendix I for a detailed development of the oscillator dynamics.

$$\frac{v_{out(p-p)}(s)}{v_{control}(s)} = \left(\frac{R_{O2}}{R_{O1}+R_{O2}}\right)\frac{A\tau}{\tau s+1} \qquad (5.2.3\text{-}1)$$

where

$$A = \frac{V_{p-p}}{8V_T R_{OE} C_{O2}} \qquad (5.2.3\text{-}2)$$

and

$$\tau = (-4QZ_0C_2)\left(\frac{k}{k'}\right)\left(\frac{V_T}{V_{P-P}}\right) \qquad (5.2.3\text{-}3)$$

Q and Z_0 are the Q and characteristic impedance of the tank circuit, V_T is the thermal voltage, V_{P-P} is the peak-to-peak ouptut voltage at the operating point, and k and k′ are operating point dependant constants that may be determined from the plots in Figure A1.3-1 and Figure A1.3-2.

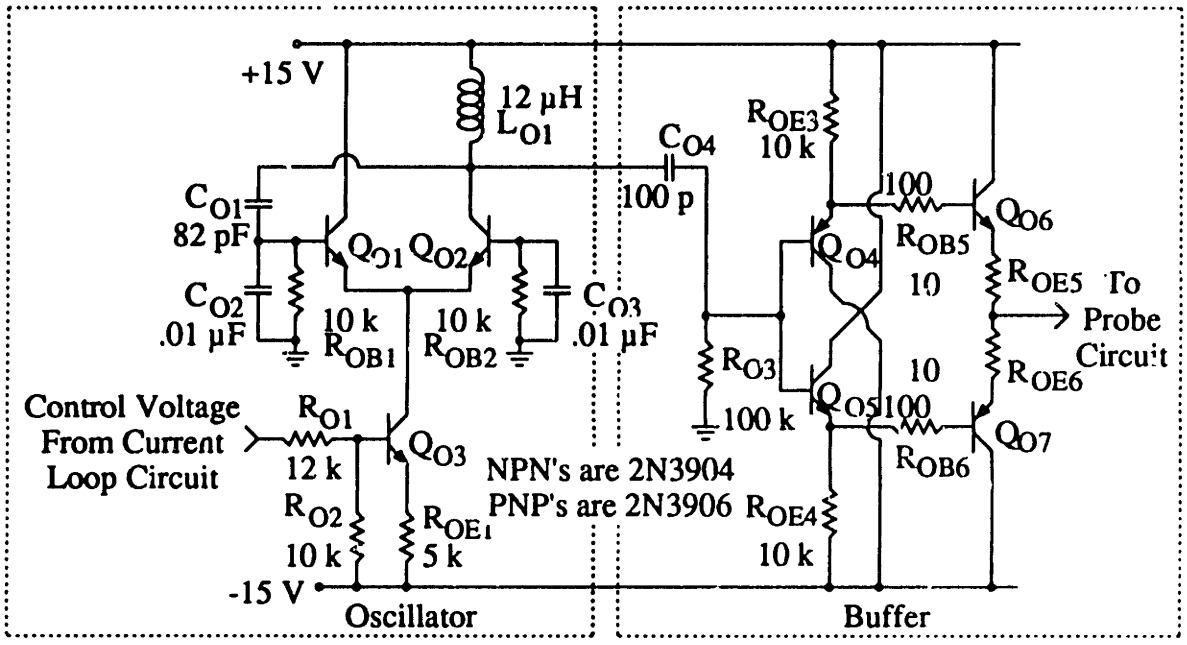

Figure 5.2.3-1: Oscillator and Buffer

For the part values used, the transfer function becomes

$$\frac{v_{out(p-p)}(s)}{v_{control}(s)} = \left(V_{P-P} \times 10^5\right)\left(\frac{\tau}{\tau s + 1}\right) \qquad (5.2.3\text{-}4)$$

The pole frequency is a nonlinear function of operating point and falls in the 5 kHz to 35 kHz range. If the system crossover frequency is well above 35 kHz, the exact location of the pole is relatively unimportant.

5.2.4 Voltage and Current References

The current references are derived from the low noise voltage reference shown below in Figure 5.2.4-1. The LM399 precision voltage reference has an internal temperature control loop which produces a very low drift reference. The effects of the relatively high level (~100 nV/$\sqrt{Hz}$) of white noise generated by the LM399 are greatly reduced by the low pass filter which limits the bandwidth to ~3 Hz. The filter also provides a slight gain to produce a 10 volt reference from the 6.95 volt LM399. A bootstrapped reference circuit of this type has two stable operating points. The first is the desired state with the Zener in reverse breakdown. The second occurs when the Zener is forward biased. Diode D_1 and resistors R_{R7} and R_{R8} forces the reference circuit into the proper state.

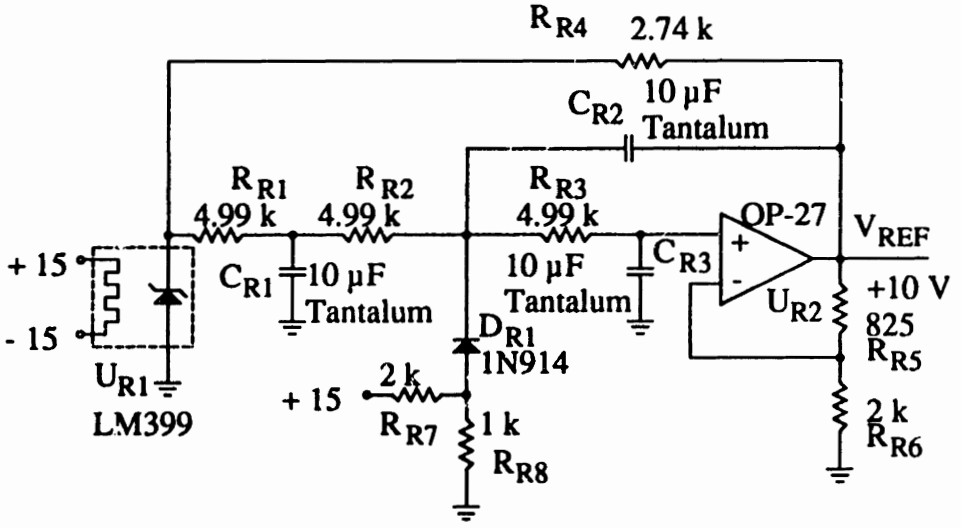

Figure 5.2.4-1: Voltage Reference

In order to maintain the low temperature coefficient provided by the LM399, the gain setting resistors, R_{R5} and R_{R6}, must have matched temperature coefficients. Tantalum capacitors are used in the filter network because of their high energy storage densities and low leakage currents. A low leakage current is important because the leakage current in an electrolytic capacitor tends to have a $\frac{1}{f}$ spectral density. The noise produced by a lower quality aluminum electrolytic can be several times larger than what is tolerable.

The voltage reference is used to create two precision current references as shown in Figure 5.2.4-2. The differential amplifier produces an output voltage that is V_{REF} volts below the positive supply. Operational amplifier U_{R4} forces the voltage across R_{R14} to be equal to V_{REF}. Since all of the current flowing through R_{R14} must flow through the JFET, the output current is simply equal to $\frac{V_{REF}}{R_{R14}}$. The second current reference is produced in an identical fashion.

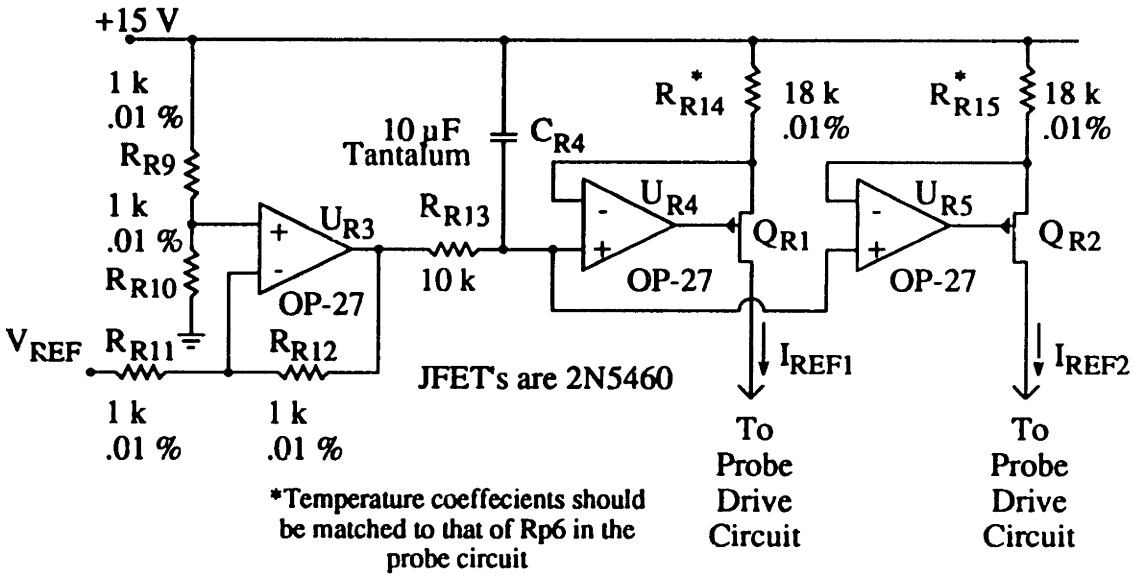

Figure 5.2.4-2: Current References

The power supply rejection ratio (PSRR) of the current reference is limited by the matching of the gain setting resistors in the differential amplifier. In order to be insensitive to power supply variations, the resistors must be well matched and have identical temperature coefficients (TC's).

The current setting resistors, R_{R14} and R_{R15}, should be selected to have matching TC's. In addition, the TC should be the same as that for the feedback resistance, R_{P6}, in the reference charge pump.

5.3 Current Loop Dynamics

The loop gain for the current loop is

$$L(s) = (f_s C_M)\left(\frac{\frac{L_{P1}}{R_{P1}}s+1}{L_{P1}C_{P1}s^2+\frac{L_{P1}}{R_{P1}}s+1}\right)\left(\frac{R_{P2}C_{P2}s+1}{C_{P2}}\right)\bullet$$
$$\left(\frac{R_{P4}}{R_{P3}}\right)\left(\frac{R_{P4}C_{P3}s+1}{R_{P4}C_{P3}s}\right)\left(H_{oscillator}(s)\right) \qquad (5.3\text{-}1)$$

The oscillator transfer function is derived in Appendix I and the result is repeated in Section 5.2.2 for convenience. One feature of interest is how the loop gain varies as the probe capacitance changes. The above expression predicts a gain that is proportional to C_M. However, the high frequency gain of the oscillator is proportional to the peak-to-peak drive voltage which in turn is inversely proportional to C_M. The net result is that if the crossover frequency is chosen to be above the highest possible pole frequency for the oscillator, the crossover frequency will be independent of the operating point. While not a requirement, it makes stabilizing the loop a little easier.

A Bode plot of the loop transfer function with the probe at its nominal displacement is shown below in Figure 5.3-1.

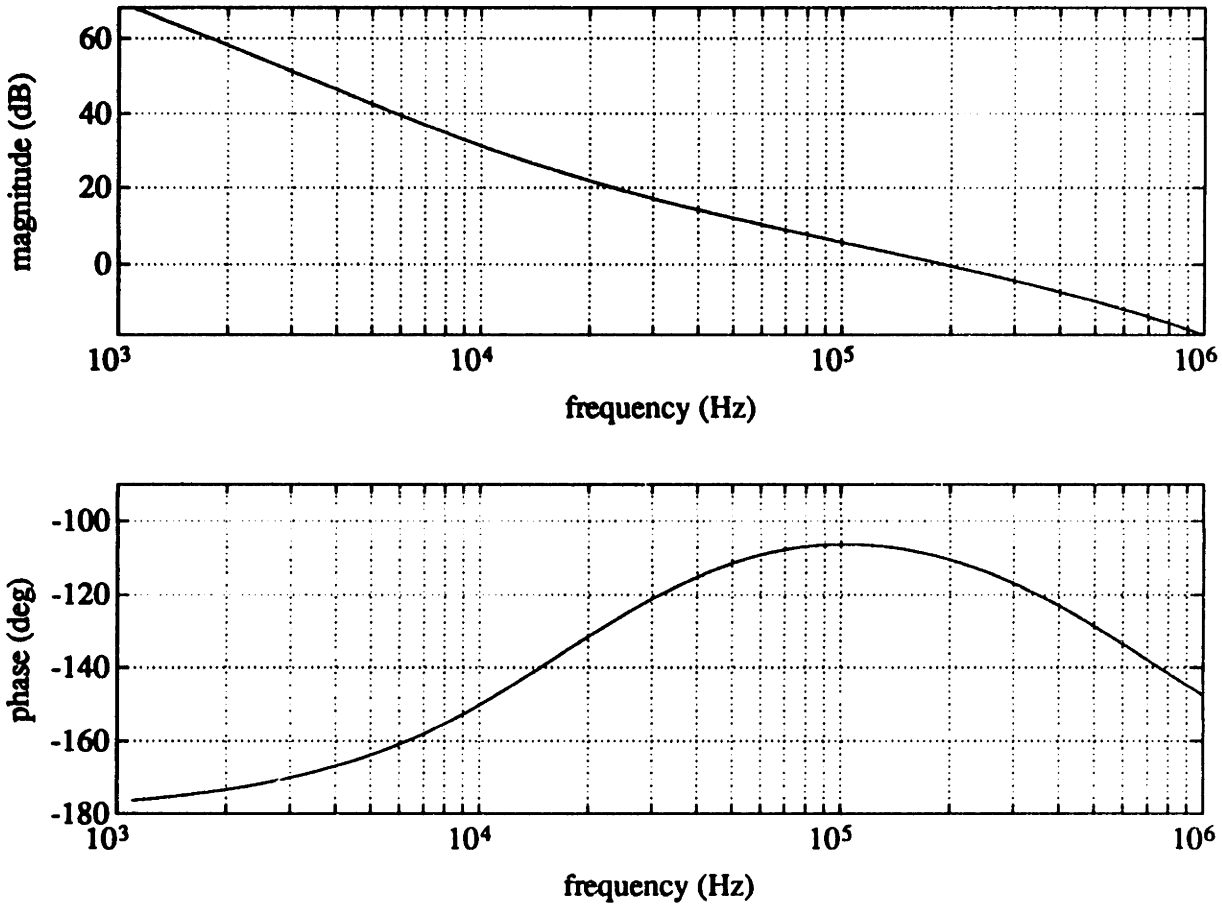

Figure 5.3-1: Current Control Loop Transfer Function

5.4 Noise Analysis

5.4.1 Current Reference Noise

A small signal noise model for the current reference is shown below in Figure 5.4.1-1. With the exception of its input referred noise sources, the op-amp is assumed to be ideal. In the frequency range of interest (< ~1 kHz), this approximation is quite good.

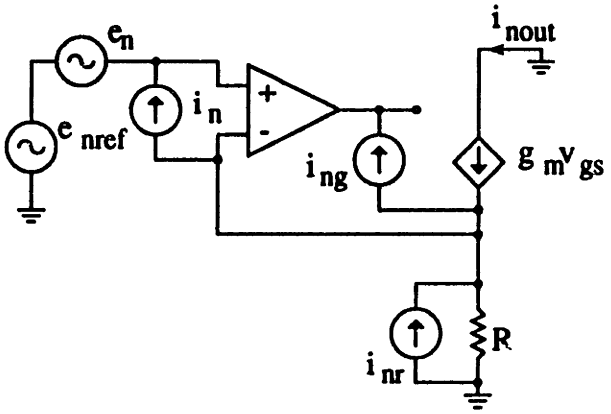

Figure 5.4.1-1: Current Reference Noise Model

The total noise in the output current is

$$i_{nout}^2 = \frac{e_{nref}^2 + e_n^2}{R^2} + i_n^2 + i_{ng}^2 + i_{nr}^2 \qquad (5.4.1\text{-}1)$$

The noise current due to the JFET is from the shot noise in the gate current and as a result is negligibly small. The relative contributions to the output noise current from each source is tabulated below.

Source	Contribution to Output Current Noise
i_n	9.5 pA
i_{nr}	30 pA
e_n	3.7 pA
i_{ng}	<< 1 pA
e_{nref}	90 pA

The noise from the voltage reference dominates the current reference noise. The noise is concentrated at frequencies below ~3 Hz due to the low pass filter used in the voltage reference.

5.4.2 Probe Circuit Noise

A model for the noise performance of the probe circuit is shown below in Figure 5.4.2-1. It is important to note that the noise associated with the two reference currents is highly correlated. The correlation is evident from the analysis of section 5.4.1. In order to account for this in the model, the noise in the current references is broken down into two sources. The first part, i_{nvref}, models the correlated noise due to noise in the voltage reference. The second part, i_{nr1} and i_{nr2}, models the uncorrelated reference current noise.

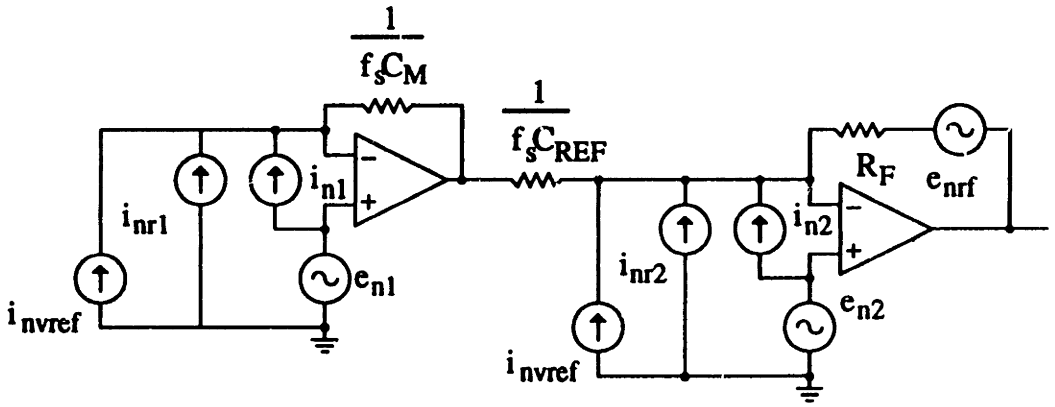

Figure 5.4.2-1: Probe Circuit Noise Model

The total noise at the output of the system is

$$\begin{aligned} e_{nout}^2 &= e_{n1}^2\left(f_s C_{REF} R_F\right)^2 + \left(i_{n1}^2 + i_{nr1}^2\right)\left(\frac{C_{REF}}{C_M}\right)^2 R_F^2 \\ &+ e_{n2}^2\left(1 + f_s C_{REF} R_F\right)^2 + \left(i_{n2}^2 + i_{nr2}^2\right)R_F^2 \\ &+ e_{nrf} + i_{nvref}^2\left(\left(\frac{C_{REF}}{C_M}\right) - 1\right)^2 R_F^2 \end{aligned} \qquad (5.4.2\text{-}1)$$

The spectral density of the output noise predicted by (5.4.2-1) is shown for three different probe displacements in Figure 5.4.2-2.

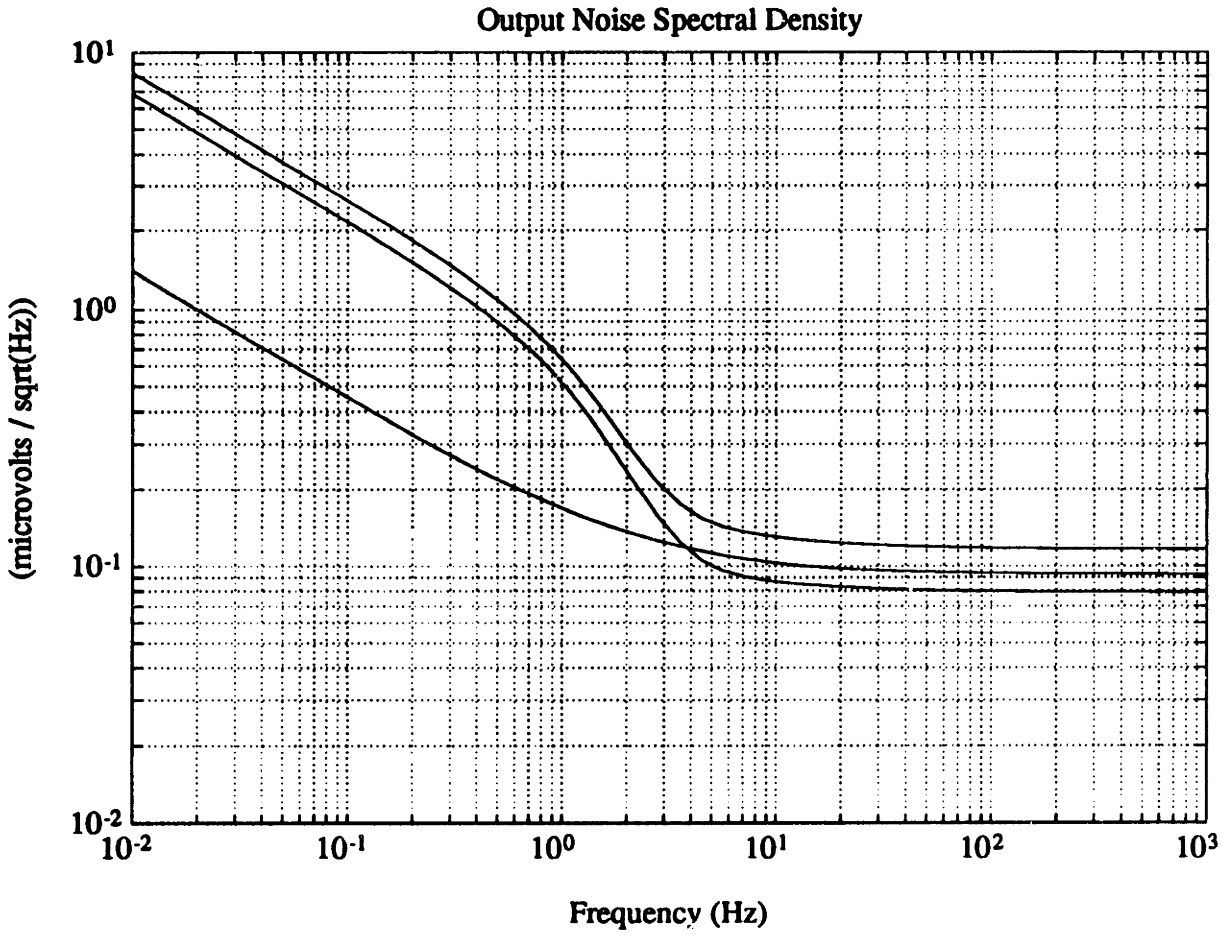

Figure 5.4.2-2: Output Noise Spectral Density

With the probe at its nominal displacement, the noise due to reference voltage noise is zero. This is evident in the lower trace. The other two traces are with the probe at either end of its range of travel. At low frequencies, the noise due to the voltage reference noise is dominant. In the 1 to 3 Hz range, the effect of the voltage reference low pass filter is evident. At higher frequencies, the noise is due to the operational amplifier input noise generators and thermal noise in the feedback resistance. The total integrated output noise as a function of the upper bandwidth limit is shown below in Figure 5.4.2-3.

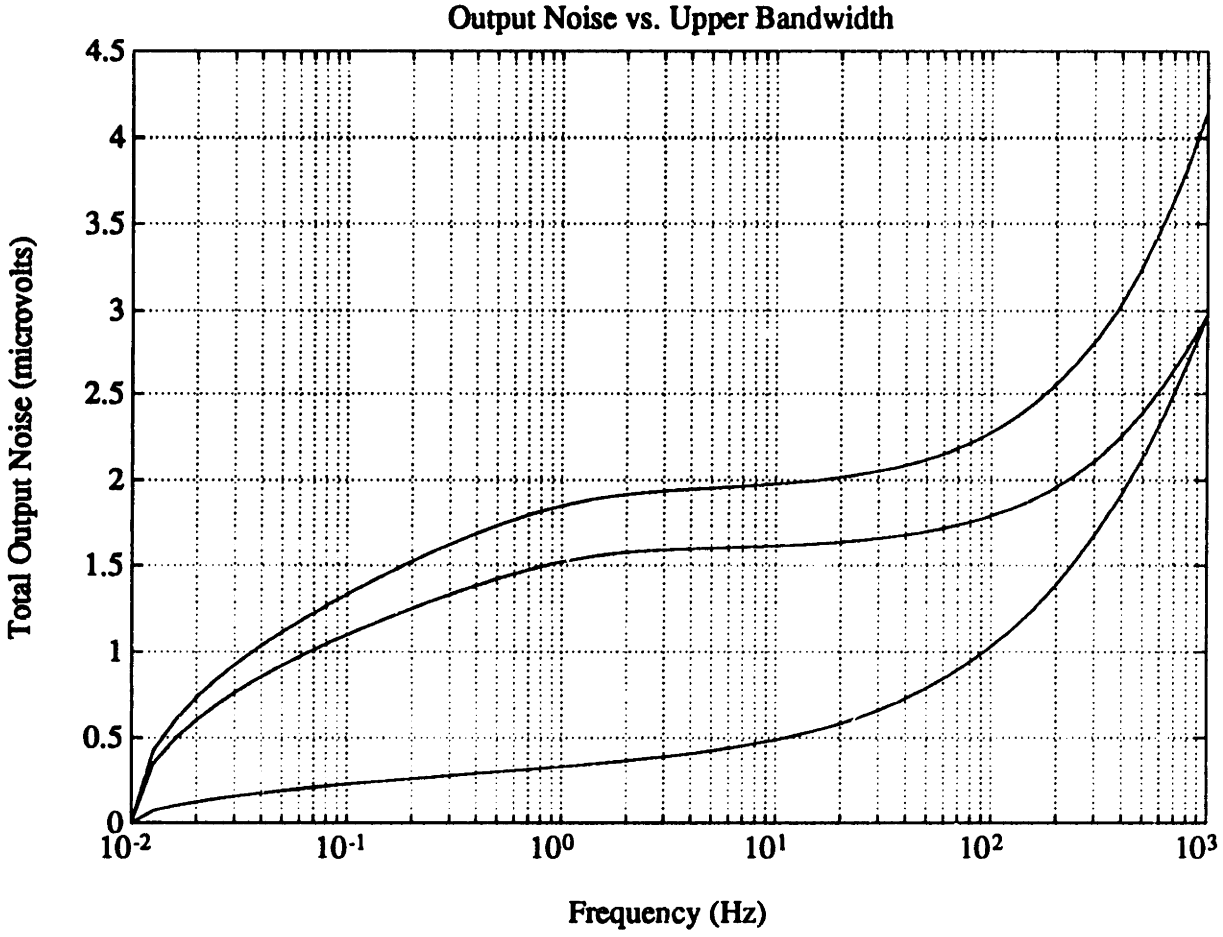

Figure 5.4.2-3: Total Integrated Output Noise

The noise is lowest when the probe is at its nominal displacement due to the cancellation of the voltage reference noise. The noise is highest at the largest displacement due to the gain seen by i_{n1}, i_{nr1}, and i_{nvref} when $C_{REF} > C_M$.

5.5 A/D Conversion Details

The A/D converter is an oversampled converter based on a fast 16-bit converter. The input is sampled at 512 kHz and convertered to a 16-bit digital output. The data is then sent into an accumulator circuit that adds up 512 successive samples and outputs the sum. The result is a converter that has a 25-bit output word and a 20-bit noise floor.

5.5.1 Analog Portion

The A/D converter is shown below in Figure 5.5.1-1. The filter formed with by U_{AD1}, $R_{AD1\text{-}4}$, and $C_{AD1\text{-}4}$ serves two purposes. By limiting the bandwidth of the analog signal, the total noise is reduced. The second purpose for the filter is anti-aliasing. Although the input is being sampled at 512 kHz, the final sampling rate at the output of the accumulator is only 1 kHz.

As discussed in Chapter 4, a dither signal may be used to decorrelate the quantization noise from the input and produce a quantization noise which is white. Due to time constraints, the dither circuit was not included in this design. A suitable dither may be produced in the following way: In the digital accumulator, a counter is used to keep track of how many samples have been added up. The output of this counter may be used as the input to a D/A converter. The output of the D/A is then attenuated with a resistive divider to a level equivalent to a few LSB's and summed with the A/D input signal. Since the averaging interval is precisely equal to an integer number of periods of the dither signal, the digital output due to the dither is zero.

Due to time constraints, an evaluation board for the A/D converter was used instead of putting the converter on the same board as the probe circuit. In the future it would be desireable to design a printed circuit board with a ground plane that would include the probe circuit and the A/D converter. When this is done, the A/D reference input should be

connected to the precision 10 volt reference used in the probe circuit. The output of the A/D converter is

$$output = \frac{V_{IN}}{V_{REF\ A/D}} \tag{5.5.1-1}$$

Recall that the output of the probe circuit is

$$V_{OUT} = V_{REF}\left(\frac{R_F}{R_C}\right)\left(\frac{C_{REF}}{C_M} - 1\right) \tag{5.5.1-2}$$

where V_{REF} is the probe reference voltage, R_C is the current setting resistor in the current reference, and R_F is the feedback resistor in the reference charge pump. By using the same reference voltage for the A/D and the probe circuit, the A/D output becomes

$$output = \left(\frac{R_F}{R_C}\right)\left(\frac{C_{REF}}{C_M} - 1\right) \tag{5.5.1-3}$$

From (5.5.1-3) it is evident that precise trimming of the voltatge reference isn't required. Additionally, $\frac{1}{f}$ noise and thermal drifts in the voltage reference will be cancelled out. It is required, however, that the current setting resistors in the current reference and the feedback resistor in the reference charge pump be well matched and track with temperature.

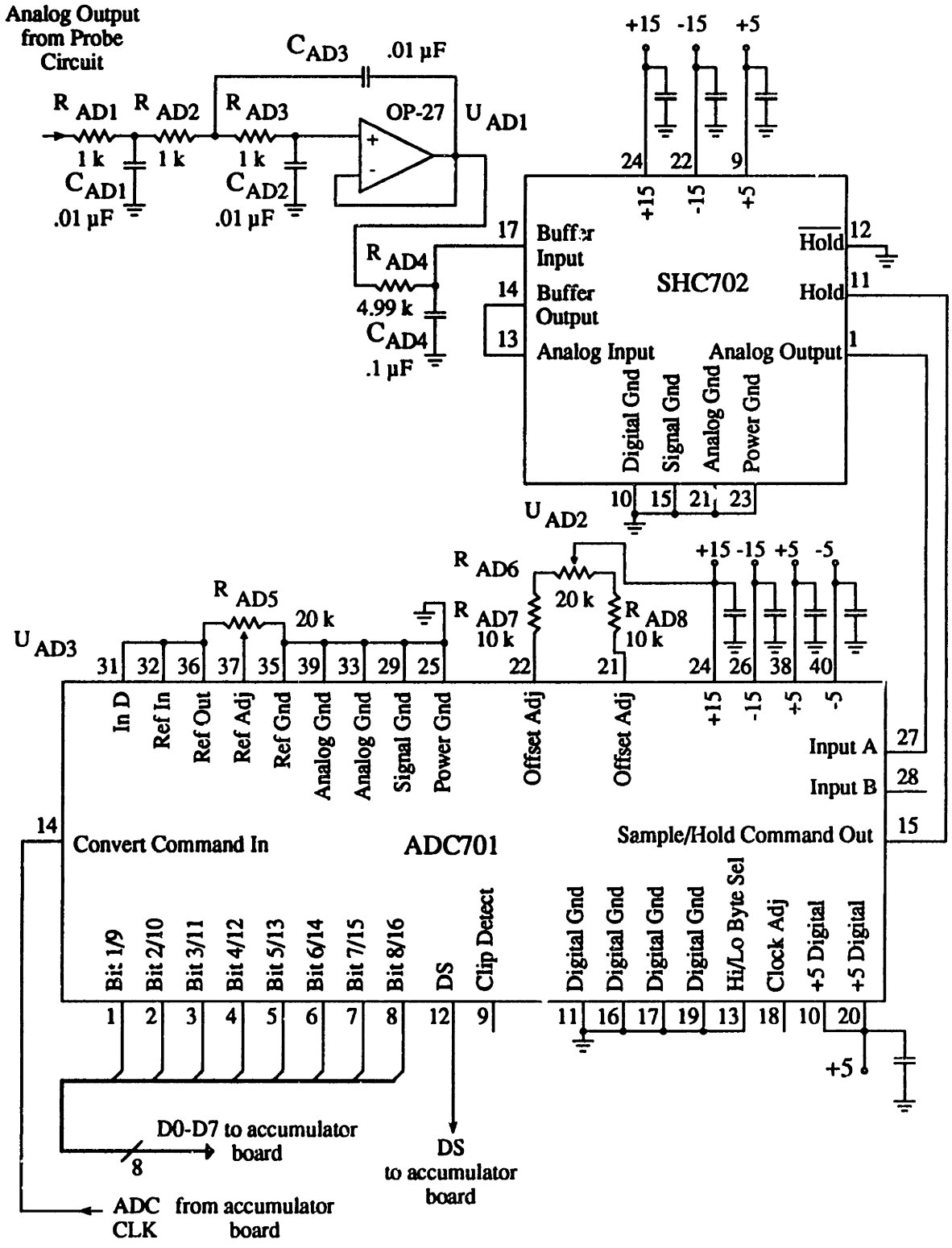

Figure 5.5.1-1: A/D Converter

5.5.2 Digital Portion

In order to obtain the required 20 bits from the A/D converter, 512 samples are averaged and then presented as the output. Since the A/D converter is sampling at 512 kHz and has a 16-bit output, the data rate is quite fast. Rather than trying to obtain a computer that is fast enough to handle the 512 kHz data, a digital accumulator circuit was constructed to perform the averaging. The resulting data is then sent serially into a computer.

A simplified block diagram of the accumulator is shown below in Figure 5.5.2-1. The accumulator is centered around a 28-bit adder and register. On each clock cycle the output of the adder is latched in the accumulator register. The adder output on the next clock cycle is then equal to the sum of the data input and the previous accumulator output. Every 512 clock cycles, the adder output is latched in the output register and the accumulator register is cleared. At the same time, the data available (DAV) flag is raised to notify the control circuit that valid data is available at the accumulator output.

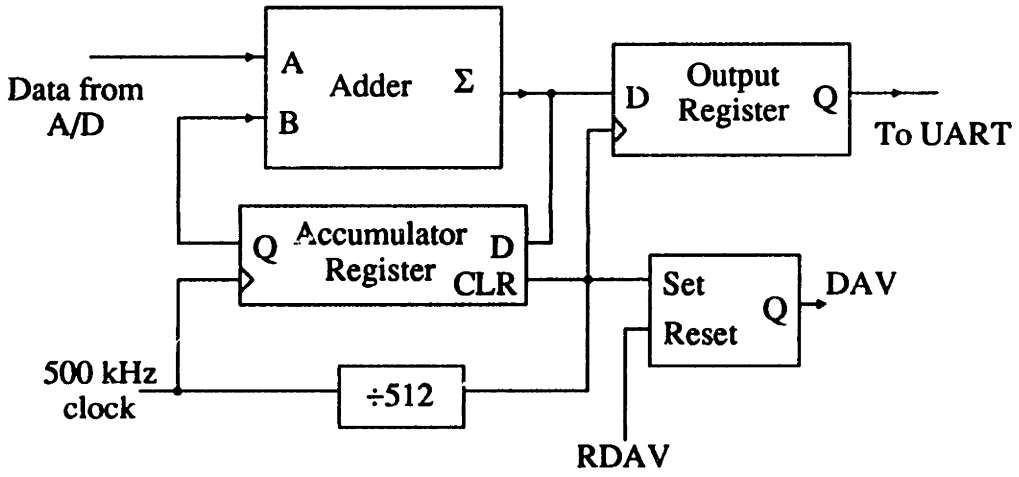

Figure 5.5.2-1: Accumulator Block Overview

The accumulator and the Universal Asynchronous Receiver/Transmitter (UART) used in the serial interface are controlled by a Motorola 68HC705K1 microcontroller. A simplified state diagram for the controller is shown below in Figure 5.5.2-2. Upon power up, the UART is initialized with the correct communications paramaters. After initializing the UART, the controller waits in state WaitMac for the host computer to signal that it is

ready for data. When the $\overline{MAC}$ line goes low, the DAV flag is reset and the controller waits for valid data to become available at the accumulator output. When DAV goes high, the data is clocked out through the serial port. Since 512 samp'es of 16-bit data have been added, the output data is 25-bits wide. The UART, however, only accepts 8-bits at a time. The 4-byte data is sent 1-byte at a time. Before sending each byte, the controller waits for the transmit buffer empty (TMBE) flag from the UART. When all of the data has been transmitted, the cycle repeats.

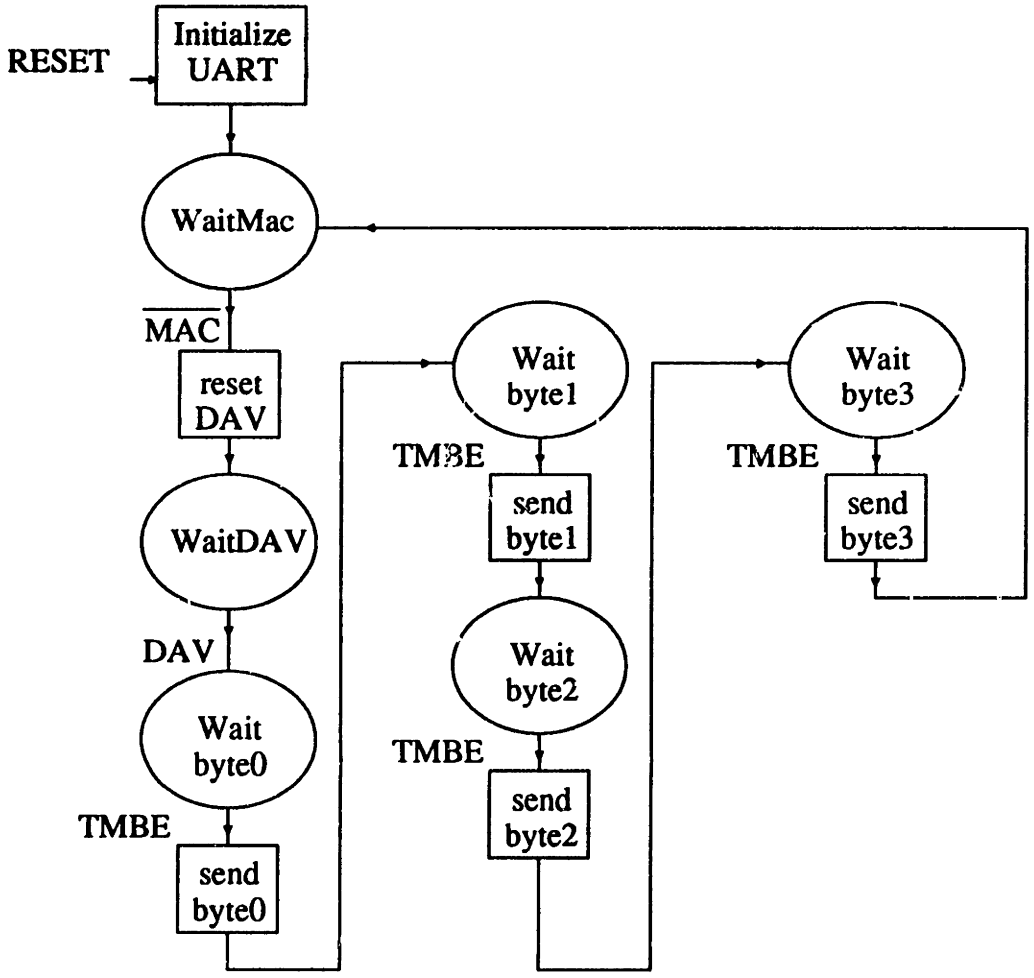

Figure 5.5.2-2: Accumulator Control Diagram

Complete schematics for the digital circuits are given in Appendix II. For the purposes of testing the circuit, a simple serial port driver program was written for the MacIntosh computer. The program prompts the user for a specified number of data points,

receives the data and saves it in a MATLAB compatible format The source code for the program is given in Appendix III.

6 Experimental Results

6.1 Analog Output

This section describes the tests performed on the probe system using the analog output. The analog output is taken from the output of the operational amplifier used as a low pass filter at the pump circuit output.

6.1.1 Noise Performance--Spectral Density Tests

The noise performance of the system was measured in several ways. First, a fixed capacitor was substituted for the probe capacitance. The fixed capacitor is less sensitive to mechanical vibrations and thermal variations. A HP3562A Dynamic Signal Analyzer was used to measure the spectral density of the output. The measured spectral density is shown below in Figure 6.1.1-1. The total output noise as a function of upper bandwidth is shown in Figure 6.1.1-2. For the plots in Figure 6.1.1-1 and Figure 6.1.1-2, the fixed capacitor is located on the probe circuit board.

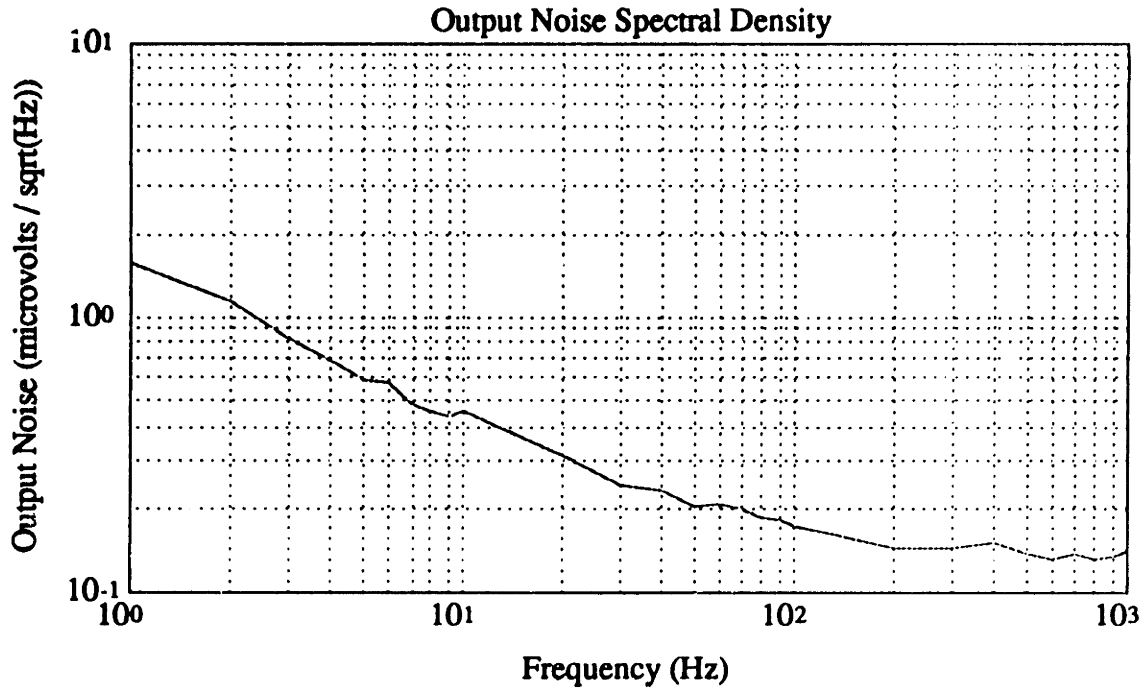

Figure 6.1.1-1: Output Noise Spectral Density with a Fixed Capacitor on Board

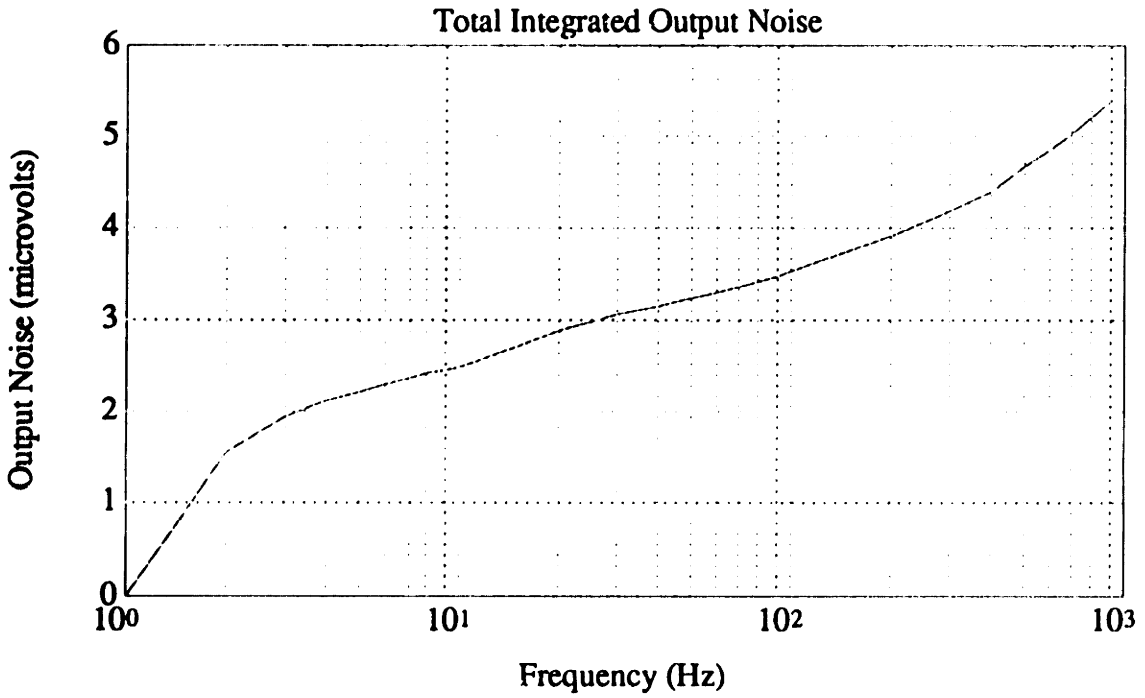

Figure 6.1.1-2: Total Output Noise vs. Upper Bandwidth with a Fixed Capacitor on Board

The next set of tests used a fixed capacitance at the end of a cable similar to the one used with the probe. The charge pump diodes are located at the capacitor end of the cable.

These experiments allow the noise effects of the cable to be determined. The same experiments as described above were performed. The measured output noise spectral density and the total integrated output noise are shown below in Figure 6.1.1-3 and Figure 6.1.1-4.

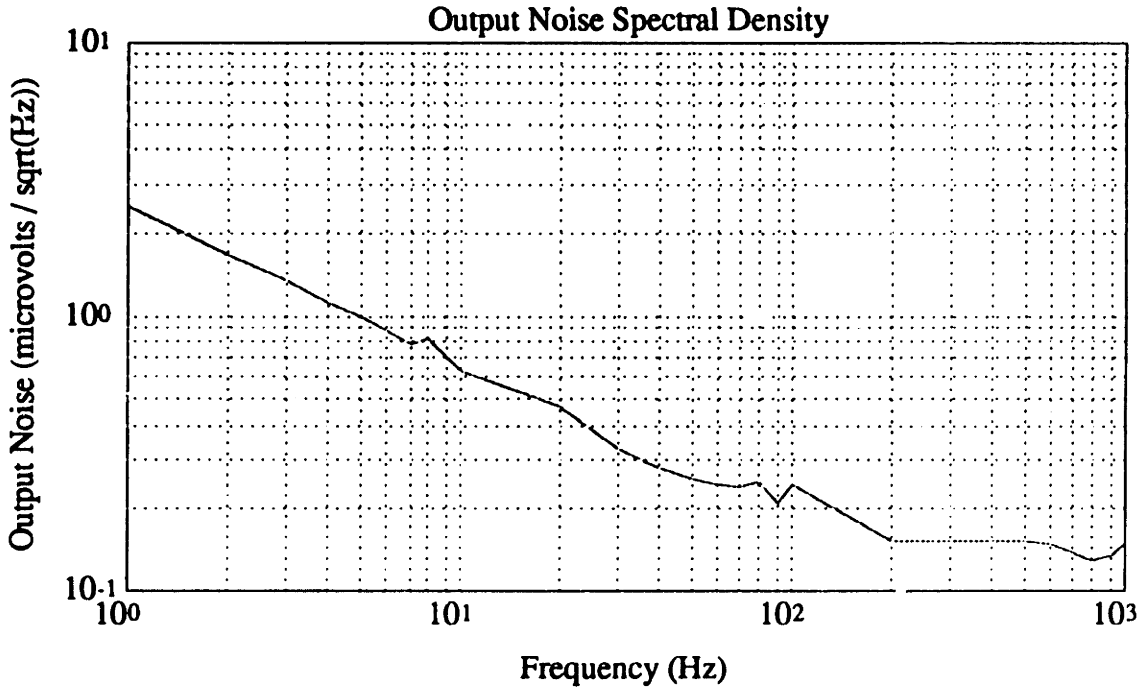

Figure 6.1.1-3: Output Noise Spectral Density with a Fixed Capacitor and Cable

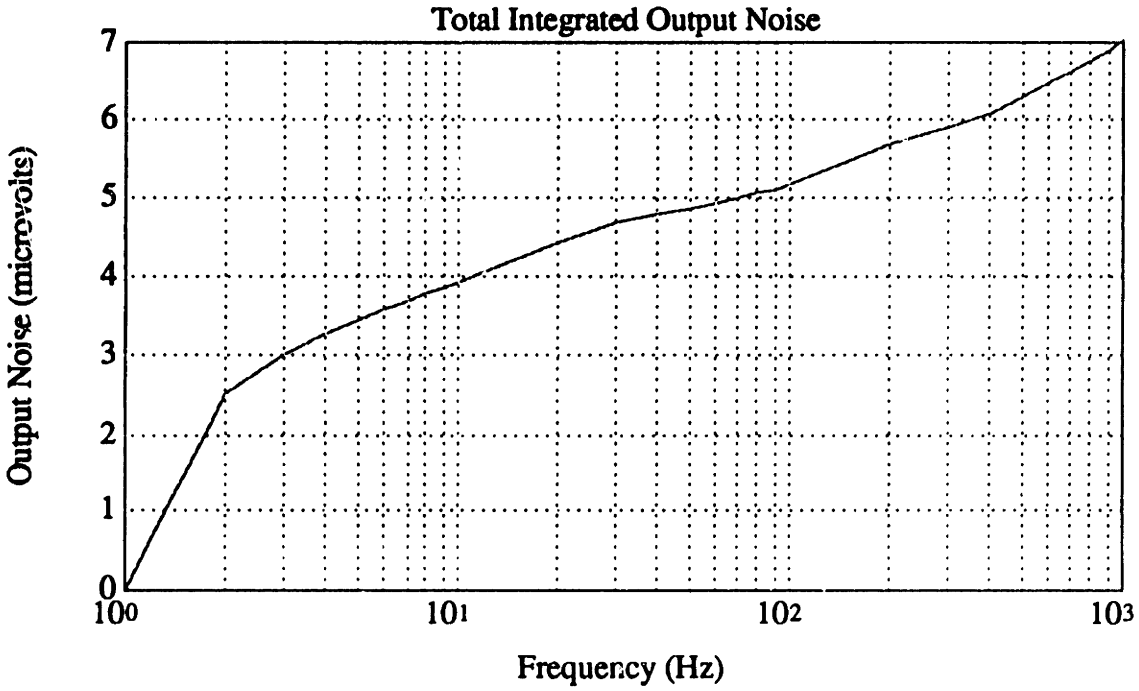

Figure 6.1.1-4: Total Output Noise vs. Upper Bandwidth with a Fixed Capacitor and Cable

It is interesting to note that the addition of the cable increase the low frequency noise. The noise at higher frequencies, however, is relatively unaffected. As will be seen later, the noise below 1 Hz is increased even more and is unacceptably large. At this time a definite explanation for this effect has not been determined. It is possible however, that the low frequency noise is due to thermal variations in the cable.

Finally, the same tests were performed on the system with the probe in a fixed location. One difficulty in reliably measuring the noise in the system with the probe is the effect thermal variations on the mechanical system. For the probe and fixture used, the temperature coefficient is roughly .1 micron/°C. This means that for a one degree temperature change, the output of the system will change by 20 mV.

Another difficulty encountered when measuring the noise present in a sensitive displacement sensor is the sensitivity to vibrations. Ideally, the probe would be perfectly rigid and it would be mounted in a perfectly rigid fixture. In this situation, any vibrations that are applied to the fixture will not cause a change in the displacement. However, if the fixture is not perfectly rigid, then applied vibrations will cause variations in the

displacement. Unfortunately, in a very sensitive sensor, the displacements due to vibrations may be quite significant. Since unwanted vibrations are abundantly available (trucks driving by, passing subway trains, fans in the other test equipment...), some means of attenuating their effect must be used.

The setup shown below in Figure 6.1.1-5 was used to reduce the effects of unwanted vibrations. The probe fixture is placed on a platform that is suspended from the ceiling by a length of elastic surgical tubing. Ignoring the effects of the cable and any parallel damping that is present in the surgical tubing, the transfer function from applied velocities in the ceiling to accelerations in the probe fixture is

$$\frac{a_{probe\ fixture}(s)}{v_{ceiling}(s)} = \frac{s}{C_T M_M s^2 + \frac{C_T}{R_M} s + 1} \qquad (6.1.1\text{-}1)$$

where R_M represents mechanical damping due to air resistance and series losses in the surgical tubing. The mass of the platform and probe fixture is M_M, and the compliance of the tubing is C_T. From (6.1.1-1) it is clear that the filter provides attenuation for frequencies that are greater than the resonant frequency of the system. For the tube and mass used here, the resonant frequency is somewhere around 1 Hz. At 10 Hz, the filter should provide a factor of almost 100 reduction in the mechanical noise.

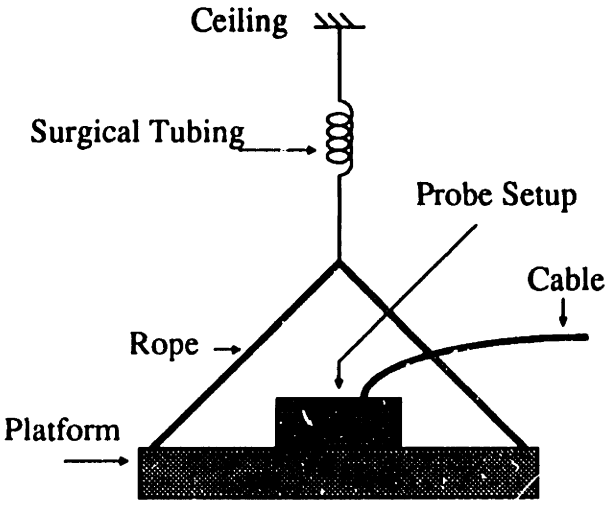

Figure 6.1.1-5: Mechanical Vibration Filter

The output noise spectral density was measured with the probe fixture on the platform. The resulting spectral density and integrated noise are shown below.

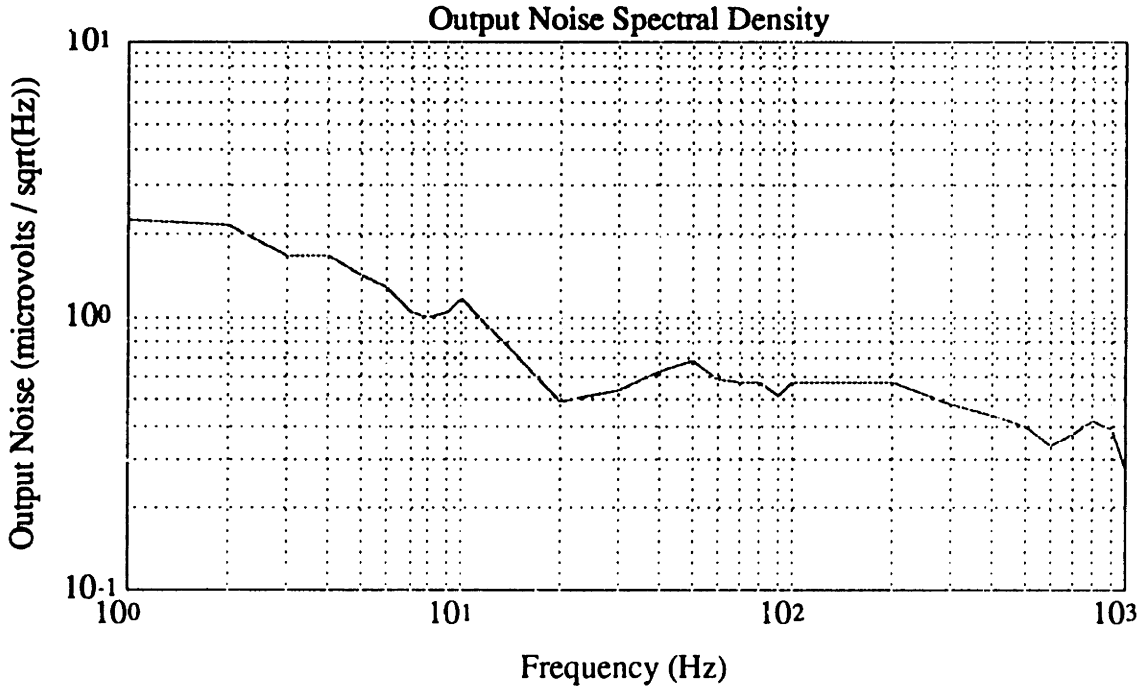

Figure 6.1.1-6: Measured Output Noise Spectral Density with Probe

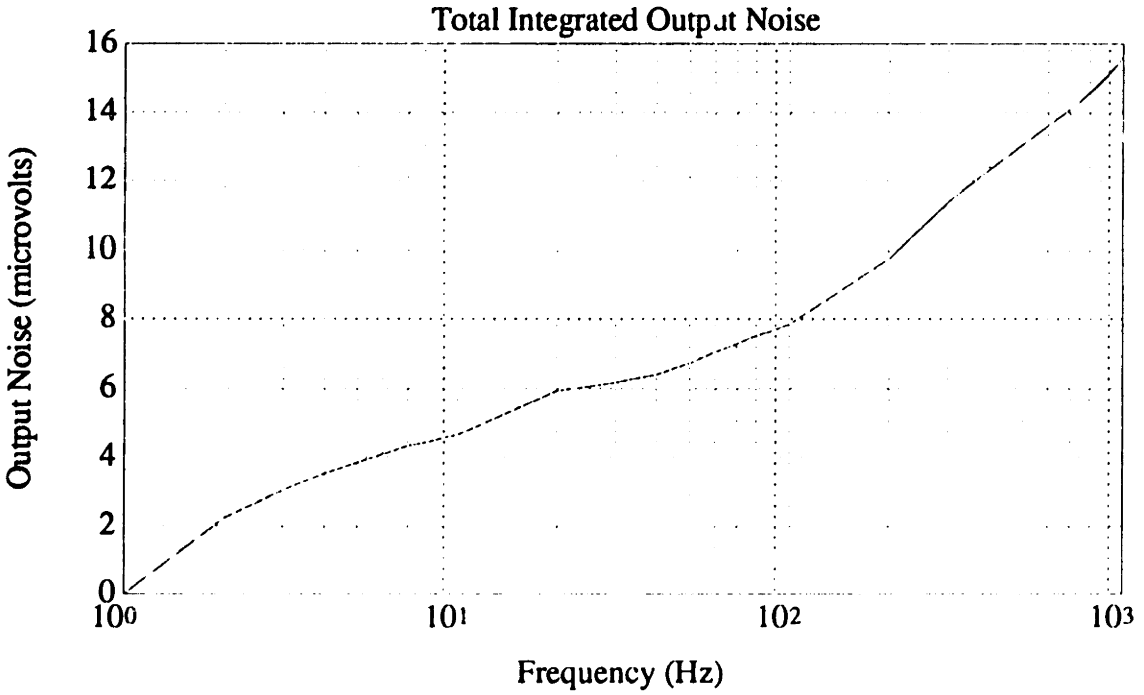

Figure 6.1.1-7: Total Output Noise vs. Upper Bandwidth with Probe

The measured noise performance of the circuit with a fixed capacitor on the circuit board and with a fixed capacitor at the end of a cable are quite similar and agree with the predictions. The exception is the increased low frequency noise when using the cable. When the probe is used, the noise increases substantially. It is likely that the increased noise is due to insufficient mechanical isolation of the probe and thermal variations in probe and fixture.

6.1.2 Noise Performance--Time Domain Tests

In order to provide another measure of the noise performance of the system, the output was measured using a Tektronix 7000 Series laboratory oscilloscope with a 7A22 differential amplifier plug-in. The 7A22 features a user selectable bandwidth and a maximum sensitivity of 10 μV/div. One difficulty encountered in measuring the noise was the presence of a large amount of 60 Hz (plus its harmonics) interference. In order to separate the line frequency components from the rest of the noise, the following experiment was performed. The 7A22 was used in conjunction with a Tektronix 7633 Storage Oscilloscope Mainframe. The trigger source was set to the ac line and the trigger mode was set to "NORM." The display was set to storage mode and it was allowed to run for 10 seconds. The 7A22 bandwidth was set from .1Hz to 300Hz. In order to accurately measure the low frequency components, the 7A22 input was set for dc coupling. To prevent overloading the input to the scope, the signal from the probe circuit was ac coupled with 2 μF and 1 MΩ. The capacitor used was a high quality paper capacitor. With a fixed capacitance located on the circuit board, the resulting waveform is shown below in Figure 6.1.2-1.

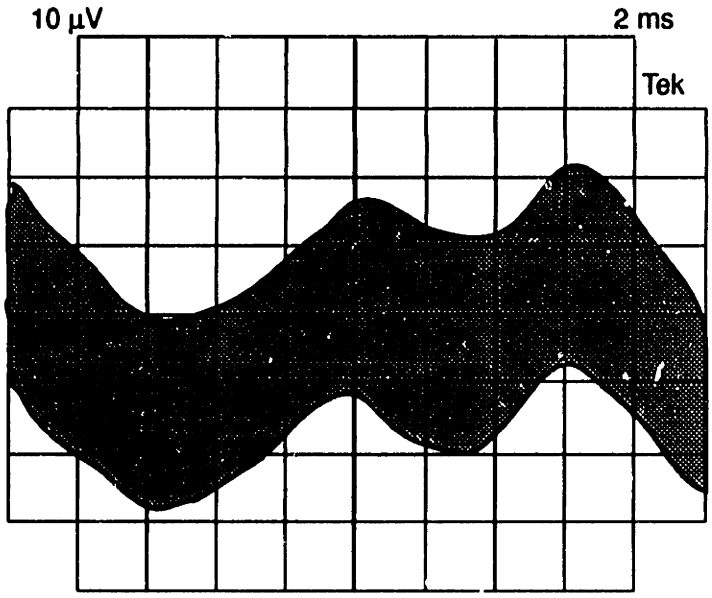

Figure 6.1.2-1: Time Domain Output Noise--Fixed Capacitor on Board

As seen from Figure 6.1.2-1, the total output noise in the .1 Hz to 300 Hz band, excluding the line frequency components, is on the order of 30 μV_{p-p} which corresponds to roughly 5 μV_{RMS}. This agrees with the frequency domain testing done in Section 6.1.1 and with the theoretical predictions from Chapter 5.

When the experiment is repeated with a fixed capacitor at the end of a cable, the waveform in Figure 6.1.2-2 results. The increase in the noise is almost entirely low frequency (below ~1 Hz) noise.

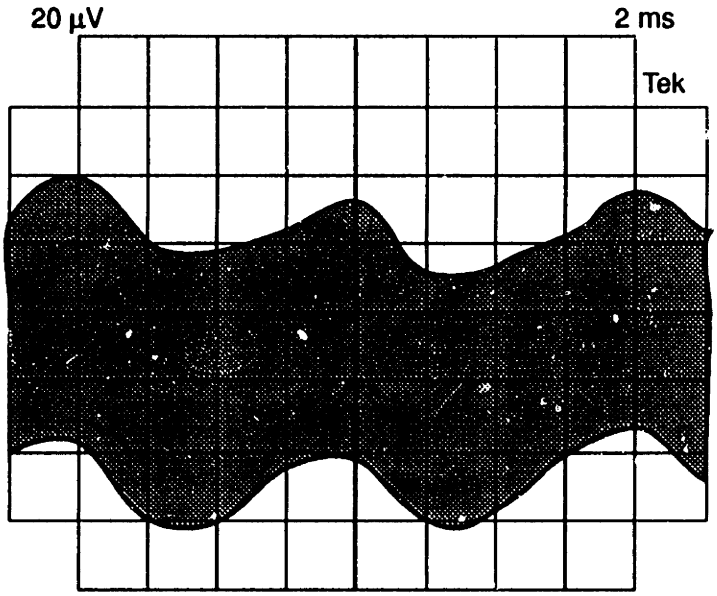

Figure 6.1.2-2: Time Domain Noise--Fixed Capacitor at End of Cable

The waveform shown below in Figure 6.1.2-3 results when the probe in a fixture is used. The noise contains the same large low frequency components seen in Figure 6.1.2-2. Additionally, a very large amount of line frequency interference noise has been introduced. It is clear that some means of reducing both the low frequency noise and the 60/120 cycle noise is required.

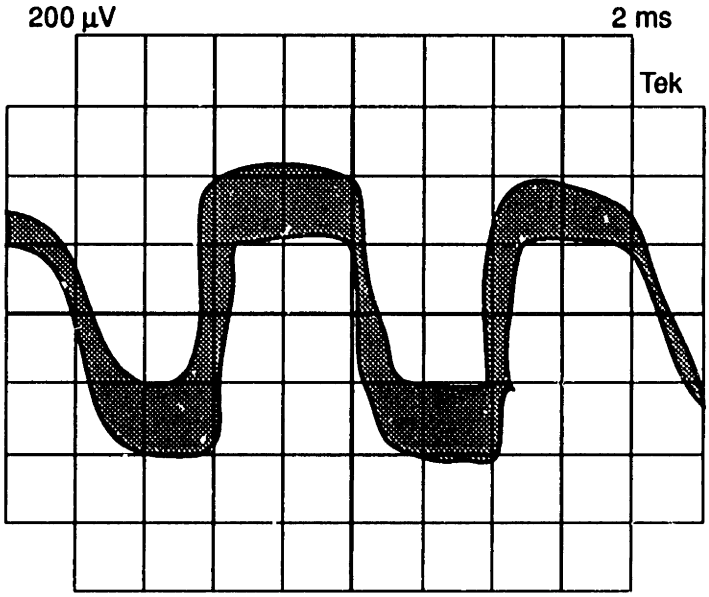

Figure 6.1.2-3: Time Domain Noise--System with Probe

6.2 A/D Converter

6.2.1 Noise

Tests on the A/D converter were performed in two ways. First, the output of the 16-bit converter was examined. Since a buffer to store the 16-bit / 500kHz data wasn't available, a cruder test was performed. The evaluation board used with the converter includes an analog reconstruction output. In addition, the digital signal may be multiplied by 32 before being sent to the DAC. By setting the digital multiplication to 32, shorting the A/D input to ground and monitoring the output of the DAC, a measure of the input noise to the A/D may be obtained. The output of the DAC under these conditions is shown below in Figure 6.2.1-1. The plot indicates that the converter is giving an output which is primarily switching between two adjacent values. Occasionally, the output is one more LSB away in either direction. This places the total input referred noise at somewhere around $\frac{1}{2}$ to 1 LSB_{RMS}.

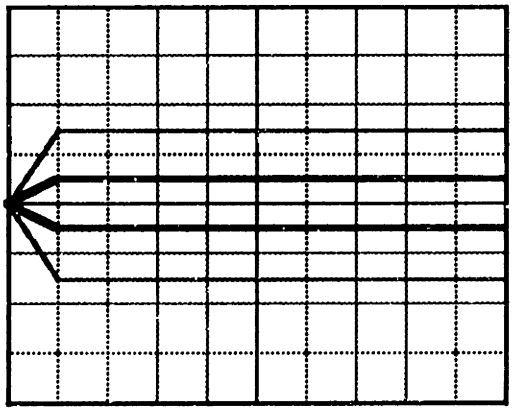

Figure 6.2.1-1: 16-Bit A/D Output Noise

The next level of testing includes the accumulator. For this test, the input to the A/D converter was shorted and 8192 samples were taken. A plot of the output with the dc portion removed is shown below in Figure 6.2.1-2. The amplitude scale is in least significant bits at the 20-bit level.

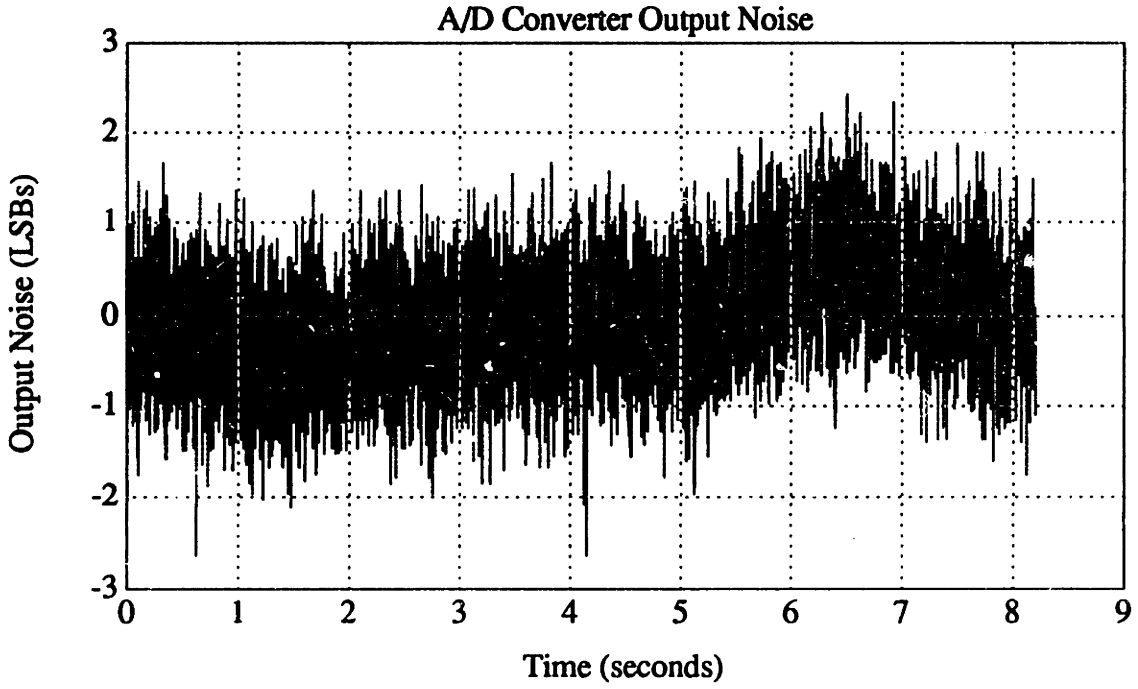

Figure 6.2.1-2: A/D Output with Grounded Input

From the plot in Figure 6.2.1-2, the A/D converter exhibits around 1 LSB of noise at the 20-bit level. An item of interest is the spectral content of the output noise. The `spectrum` command in MATLAB was used to obtain an estimate of the power spectral density. The Welch method of power spectrum estimation is used by `spectrum`. In order to obtain a smoother plot, 16 data records were collected and their spectrums were averaged. The result is shown below in Figure 6.2.1-3. Components at the line frequency and its harmonics are clearly present. Additionally, a component at around 220 Hz is present. Its origin is unknown at this time. With the exception of the components noted here, the noise is largely white.

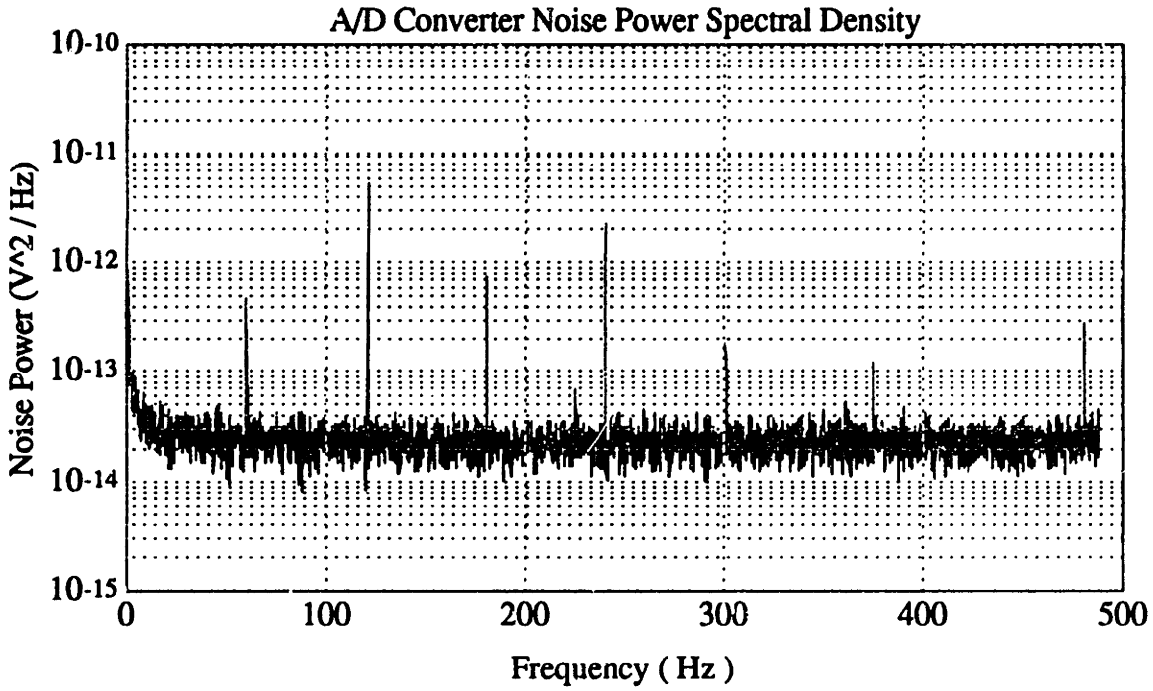

Figure 6.2.1-3: A/D Output Power Spectral Density with Grounded Input

At this time the source of the line frequency noise has not been determined. Two HP6291A dc supplies were used for the ±15 volt supplies for the A/D evaluation board. The +5 volt supply was obtained by regulating down the +15 volt supply with a LM350 3-terminal regulator. Similarly, the -5 volt supply was obtained from the -15 volt supply using a LM7905. The line frequency noise present in the A/D output may be either capacitively coupled into the system or due to ripple in the power supply.

6.2.2 Linearity

In order to determine the linearity of the A/D converter with any accuracy, a 6 or 7 digit voltmeter or a very high precision 6 or 7 digit adjustable voltage reference is required. Unfortunately, neither of these items were available. The ADC701 A/D converter and SHC702 sample and hold are both highly linear. Together, they have a total nonlinearity of ±.0015%. Given the lack of appropriate test equipment the A/D linearity wasn't measured.

6.3 Complete System

6.3.1 Noise Performance

As in section 6.1.1, the performance of the complete system (probe circuit and A/D) was measured with a fixed capacitor on the probe circuit board, with a fixed capacitor at the end of a cable, and with the probe fixture. The data collection program described in Appendix III was used to collect data records of 8192 samples each. The output of the system with a fixed capacitor on the probe circuit board is shown below in Figure 6.3.1-1 and Figure 6.3.1-2. The two plots represent the "best" looking data record and the "worst" looking record. The output of the probe circuit is directly coupled to the A/D board in these plots.

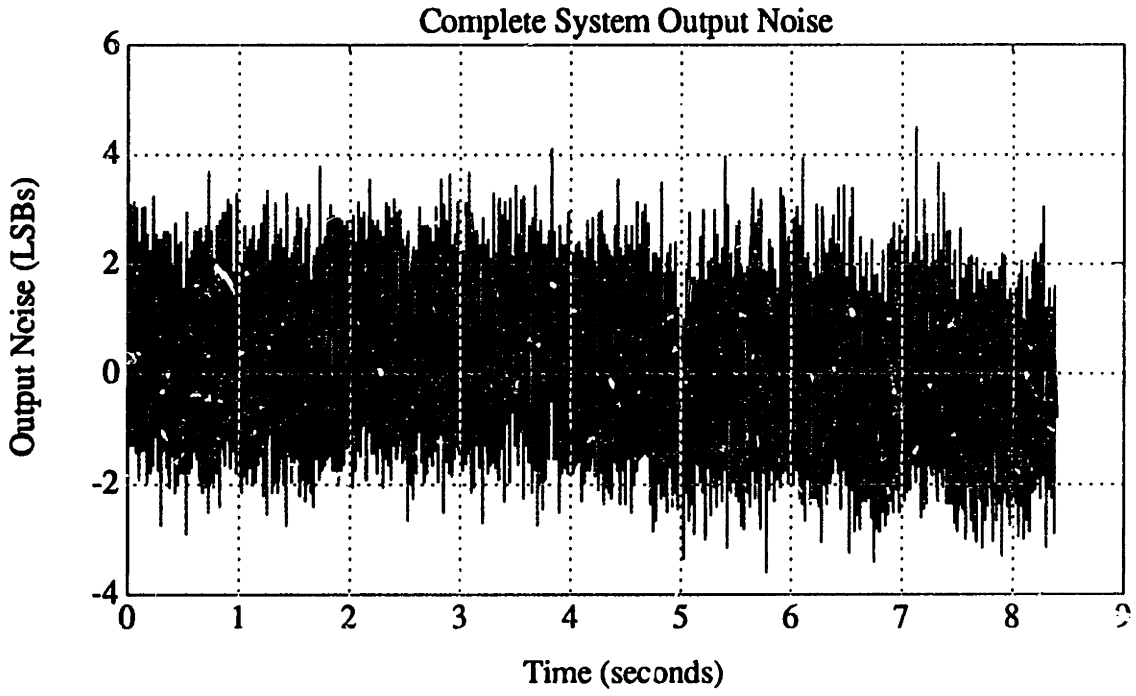

Figure 6.3.1-1: Complete System Output Noise--Best Plot

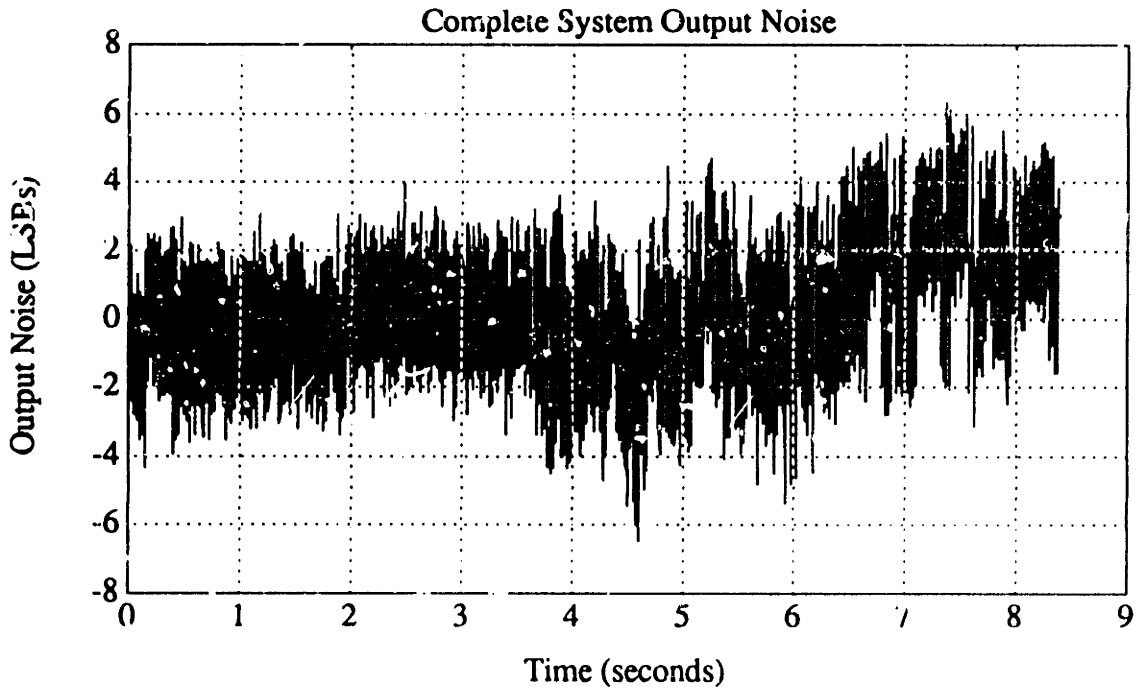

Figure 6.3.1-2: Complete System Output Noise--Worst Plot

The plots shown above show a noise level of around 4-5 LSB_{p-p}. The noise contains a large line frequency component. This is evident from the power spectral density shown below in Figure 6.3.1-3 or the time domain plot in Figure 6.3.1-4. The spectral density plot was obtain in the same manner described in Section 6.2.1.

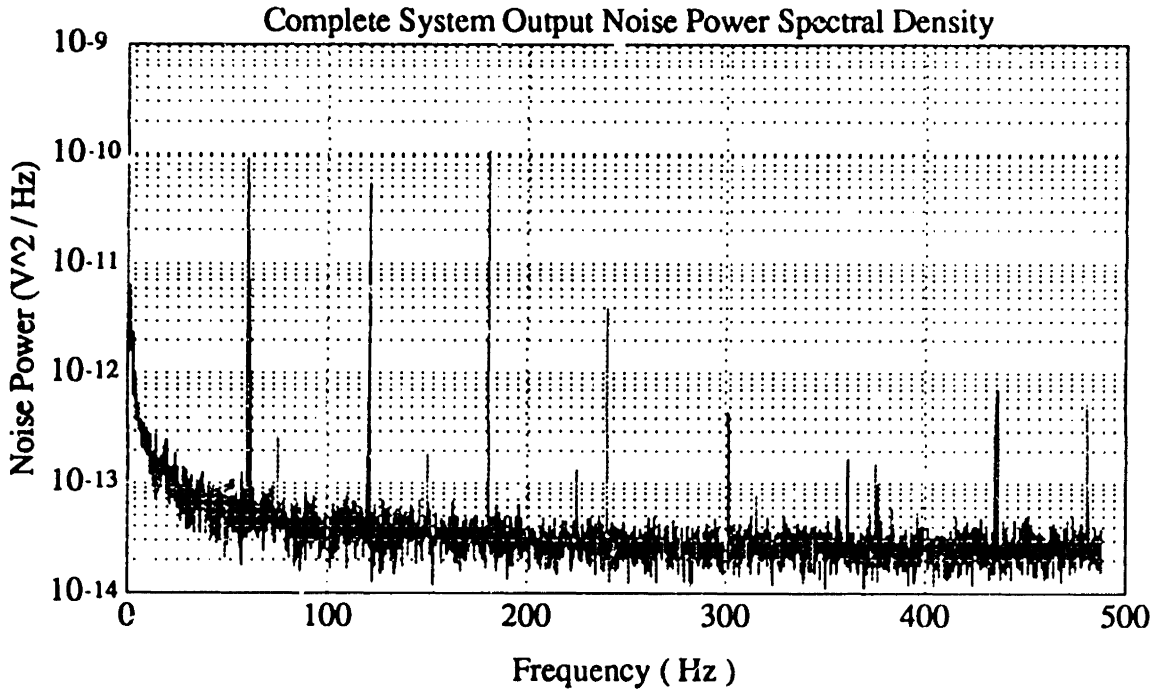

Figure 6.3.1-3: Complete System Output Noise Power Spectral Density

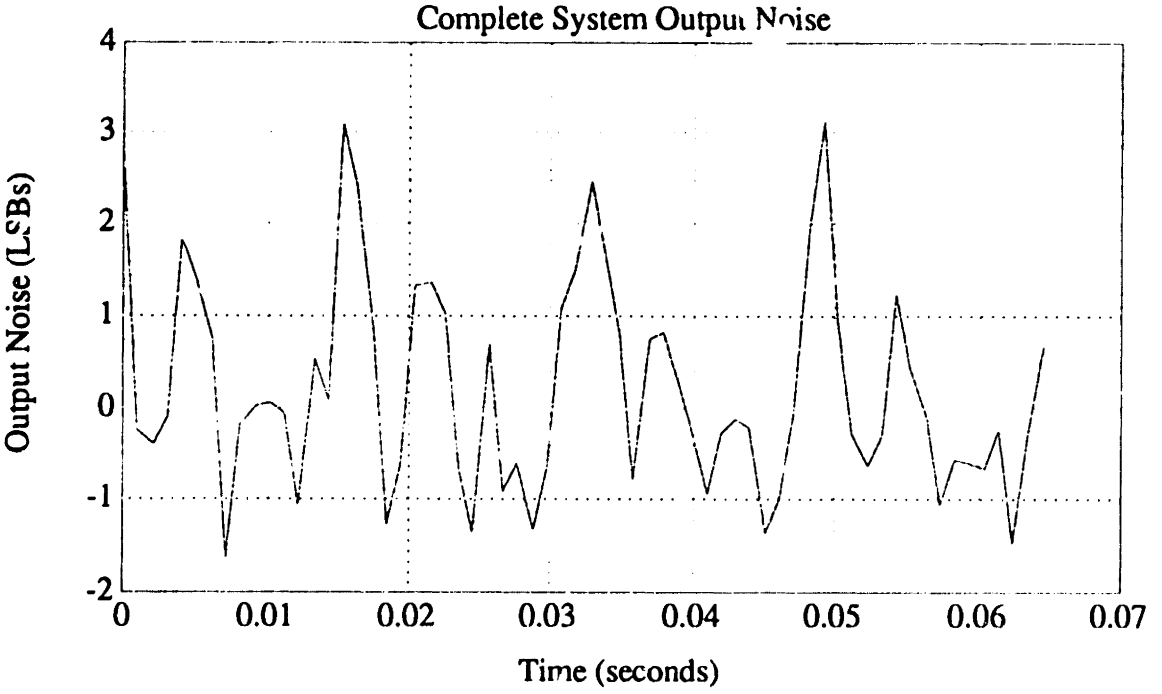

Figure 6.3.1-4: Complete System Output Noise

The tests presented above were repeated with the output of the probe circuit ac coupled to the A/D board. A .08 Hz lower corner frequency was used. The resulting time domain noise is shown in Figure 6.3.1-5 and Figure 6.3.1-6.

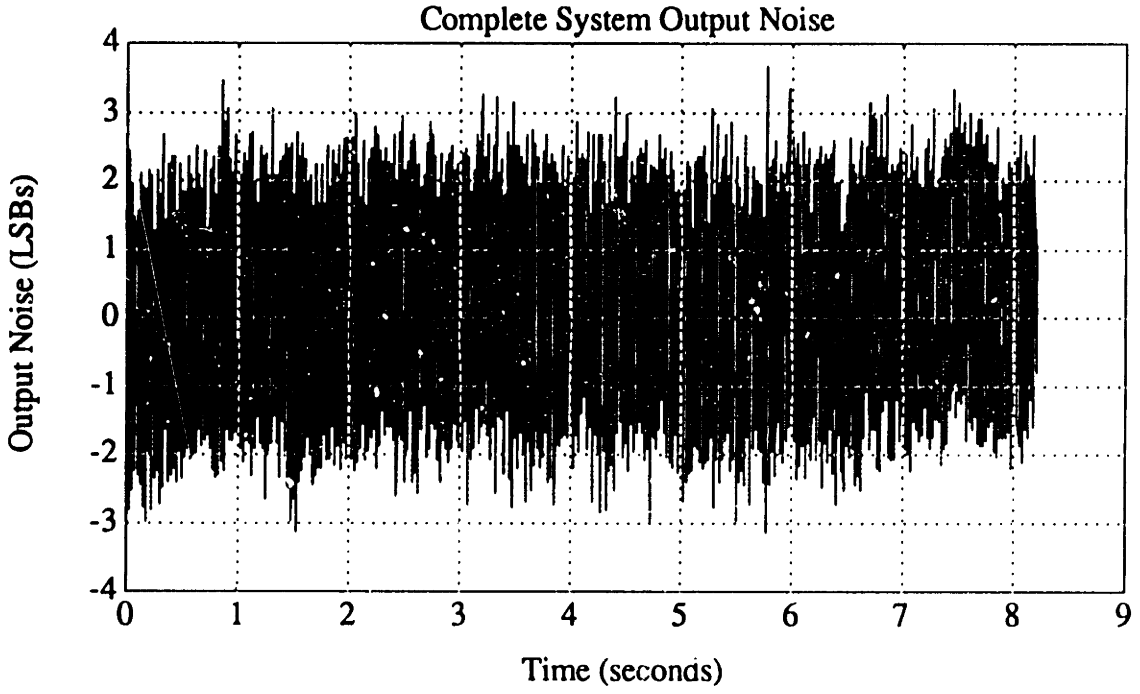

Figure 6.3.1-5: Complete System Output Noise--AC Coupled, Best Plot

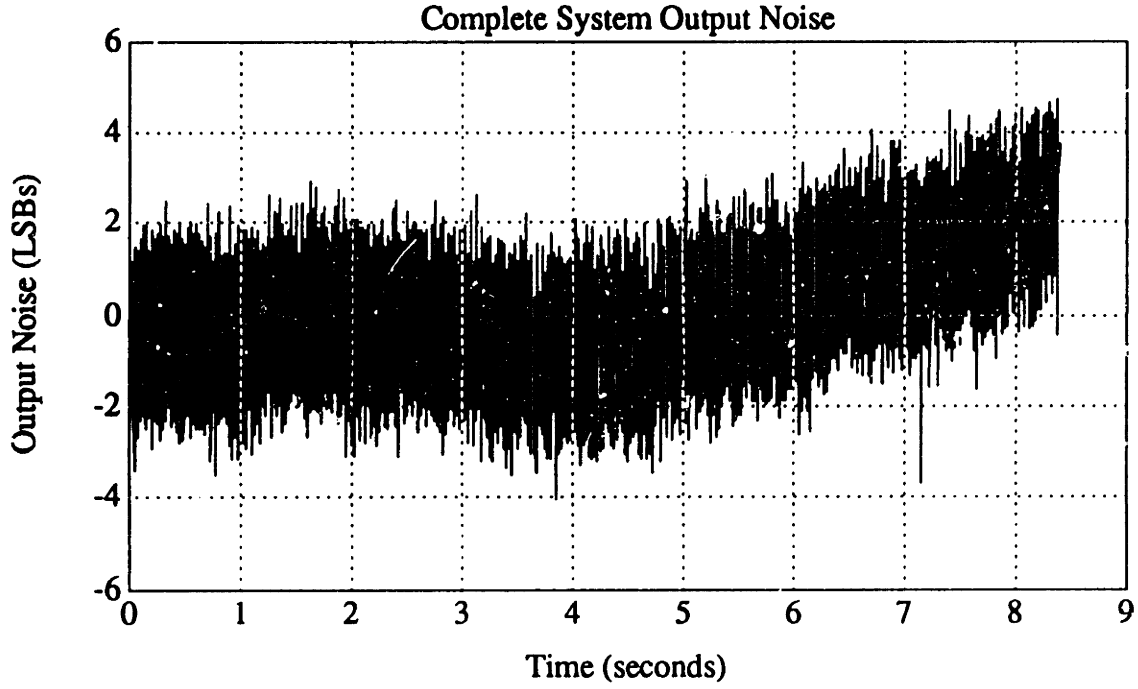

Figure 6.3.1-6: Complete System Output Noise--AC Coupled, Worst Plot

The estimated power spectral density of the output is shown below in Figure 6.3.1-7.

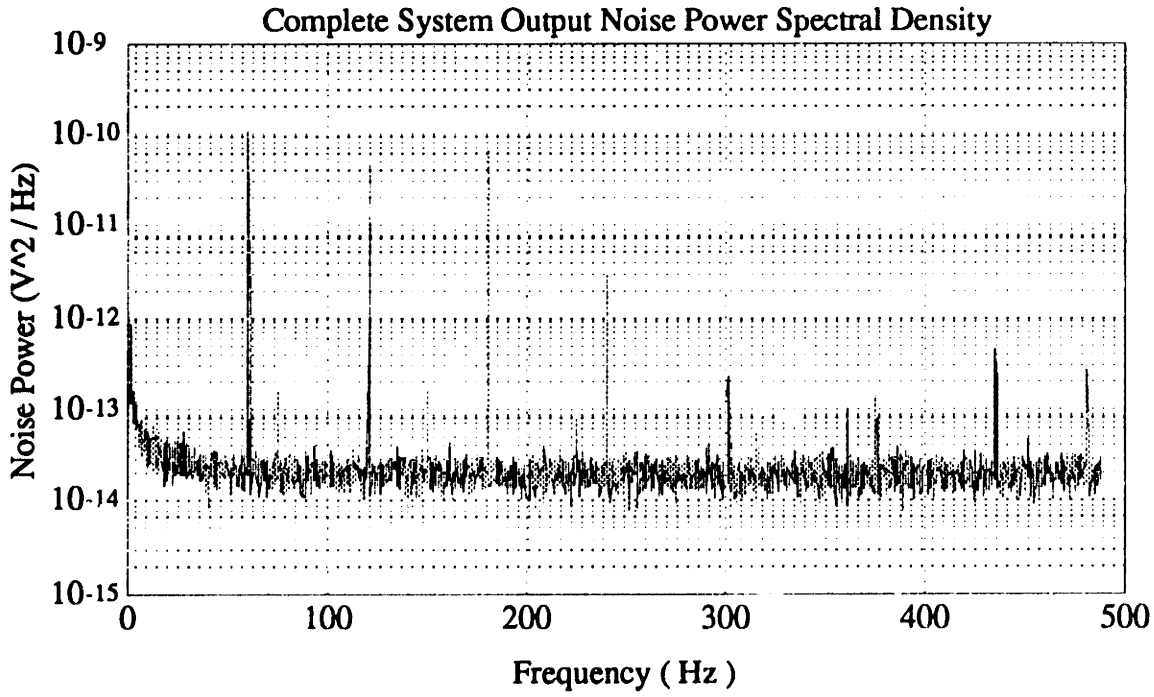

Figure 6.3.1-7: Complete System Output Noise Power Spectral Density--AC Coupled

The next test was to place the fixed capacitance at the end of a cable and repeat the test. The time domain waveform is shown below in Figure 6.3.1-8. As can be seen in this plot, a severe amount of low frequency noise has been introduced.

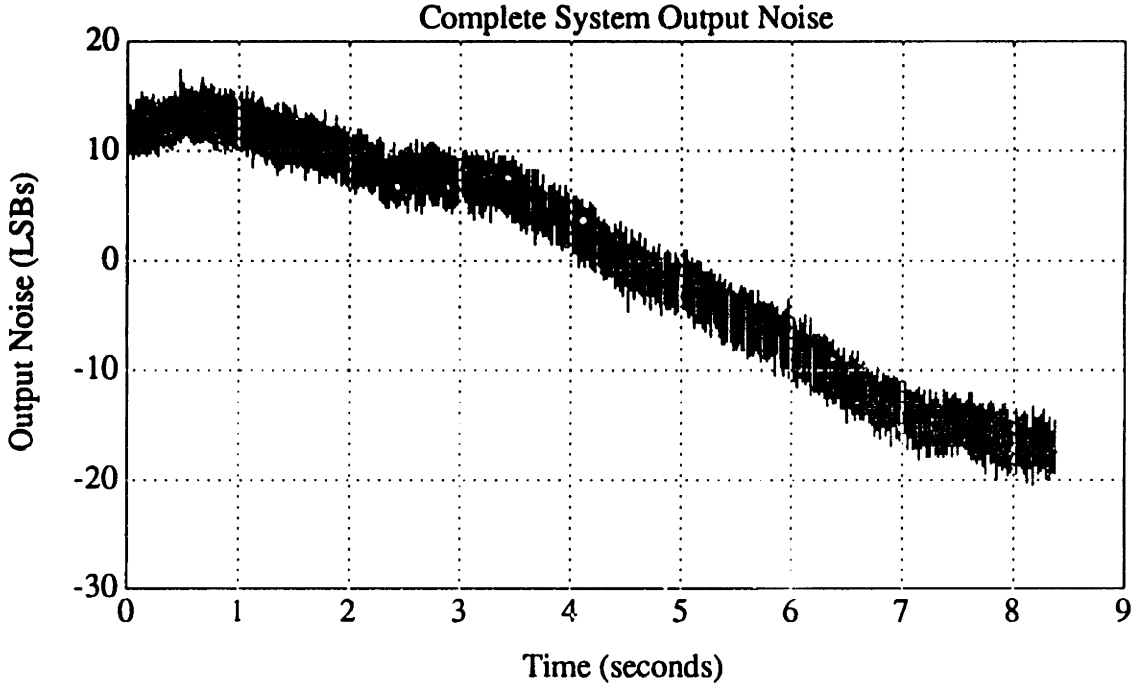

Figure 6.3.1-8: Complete System Output Noise--Fixed Capacitance at End of Cable

The power spectral density is shown in Figure 6.3.1-9.

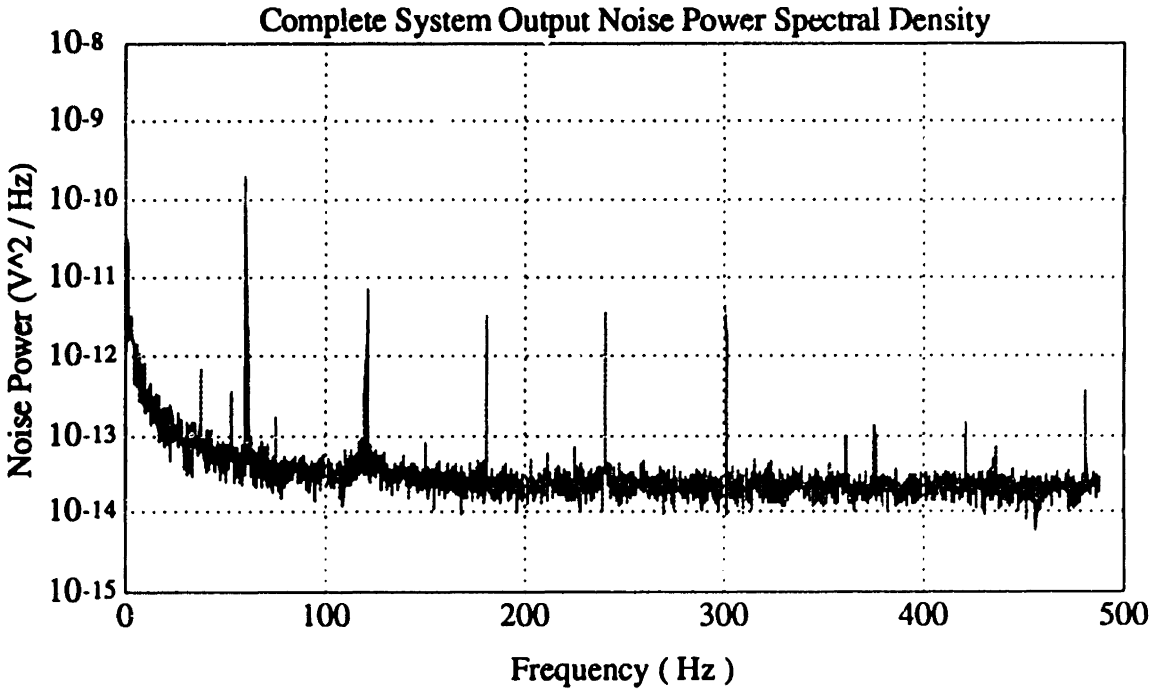

Figure 6.3.1-9: Complete System Output Noise PSD--Fixed Capacitance at End of Cable

From the power spectral density plot shown above, it is clear that the added noise is almost entirely low frequency in nature. As mentioned earlier, it is possible that the poor performance may be do to variations in the cable. Do to time constraints, it was not possible to verify this.

6.3.2 Linearity

In order to perform the linearity testing, the calibration fixture shown in Figure 6.3.2-1 was used. The fixture was provided by Dave Batchelder and John Murphy at UNCC. Initially, the probe mount is not attached to the micrometer shaft. To assemble the fixture, the micrometer is attached to the top piece of the fixture and the probe is bolted to the probe mount. Then, the micrometer is set for the reading that is to correspond to zero displacement. Finally, the probe mount is filled with epoxy and the micrometer assembly is bolted down on top. The Styrofoam applies pressure to the probe while the epoxy is drying to insure that it is parallel to the target surface. Additionally, the Styrofoam helps reduce the

mechanical backlash during testing. The micrometer used is made by Mitutoyo and has a 2.5 mm range of motion with a resolution of .1 micron.

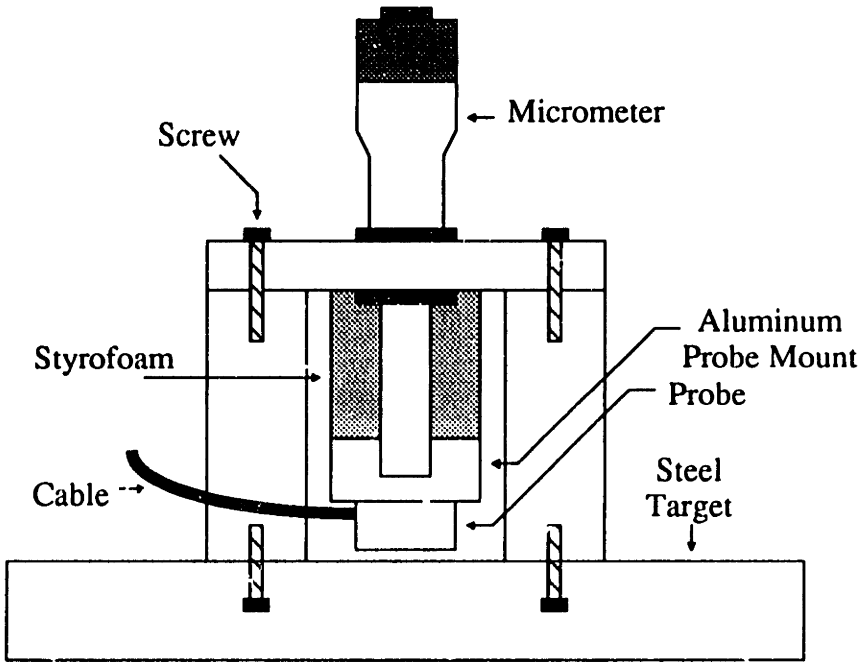

Figure 6.3.2-1: Calibration Fixture

The electronics were designed for use with a larger area (2x) probe than the probe that was eventually available. In liu of waiting for a larger area probe, the smaller one was operated in two different ranges. First, a reference capacitance of ~6 pF and a reference current of ~.25 mA were used to allow for a 100 micron range. Using the calibration fixture described above, the probe was stepped through its 100 micron range in increments of 1 micron. A plot of the output of the system as a function of the probe displacement is shown in Figure 6.3.2-2 Additionally, a best fit straight line is plotted on top of the actual data. Since the system is very linear, deviations from the ideal are not evident from this plot. In order to determine the linearity of the system, the straight line was subtracted from the actual data. The resulting error is shown in Figure 6.3.2-3. As seen in this plot, the deviations from a straight line correspond to roughly .1 micron which is the limit of the mechanical apparatus. This means that the linearity is at least ~.1%. If a more accurate number is desired, a more precise test fixture is required.

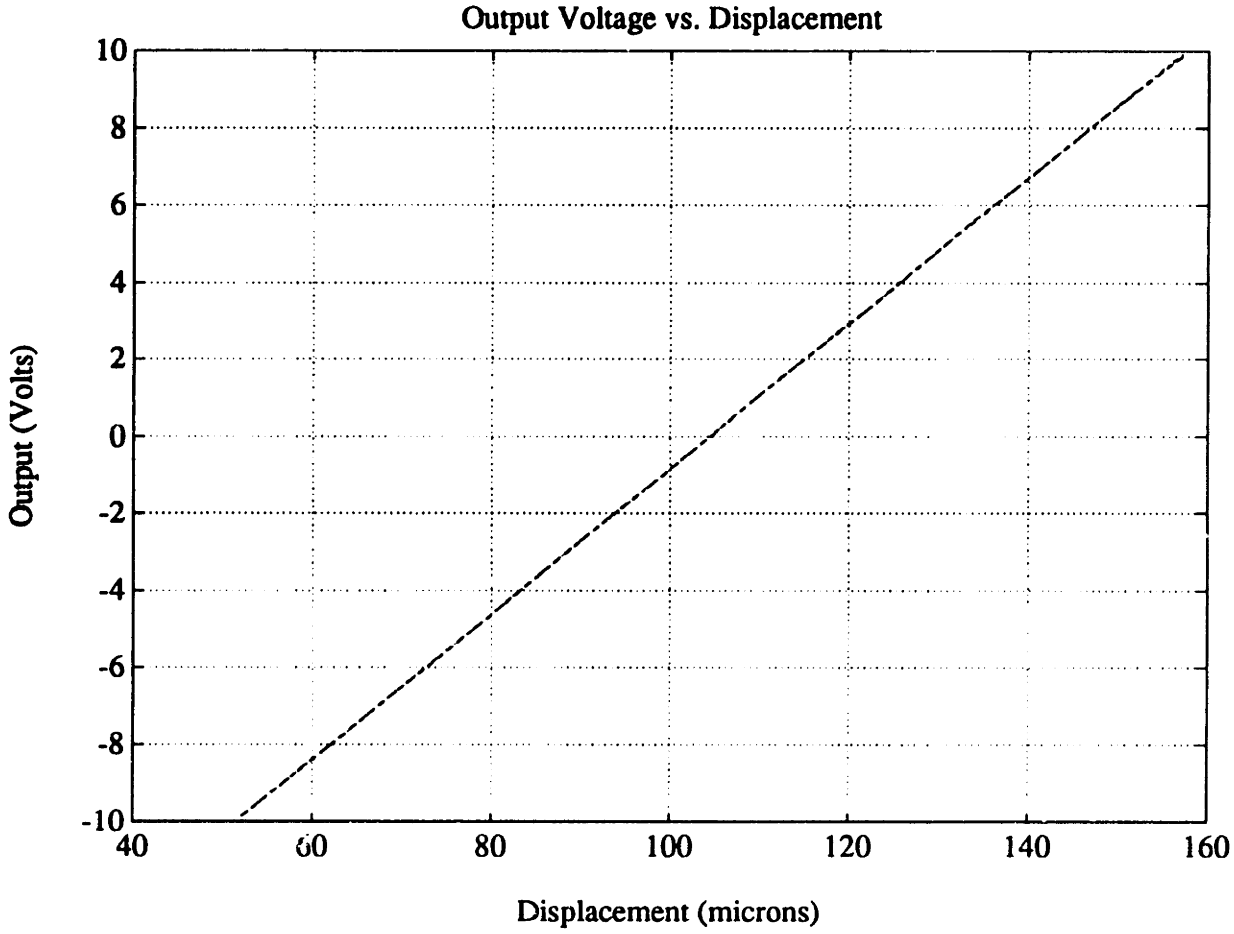

Figure 6.3.2-2: Output vs. Displacement--100 Micron Range

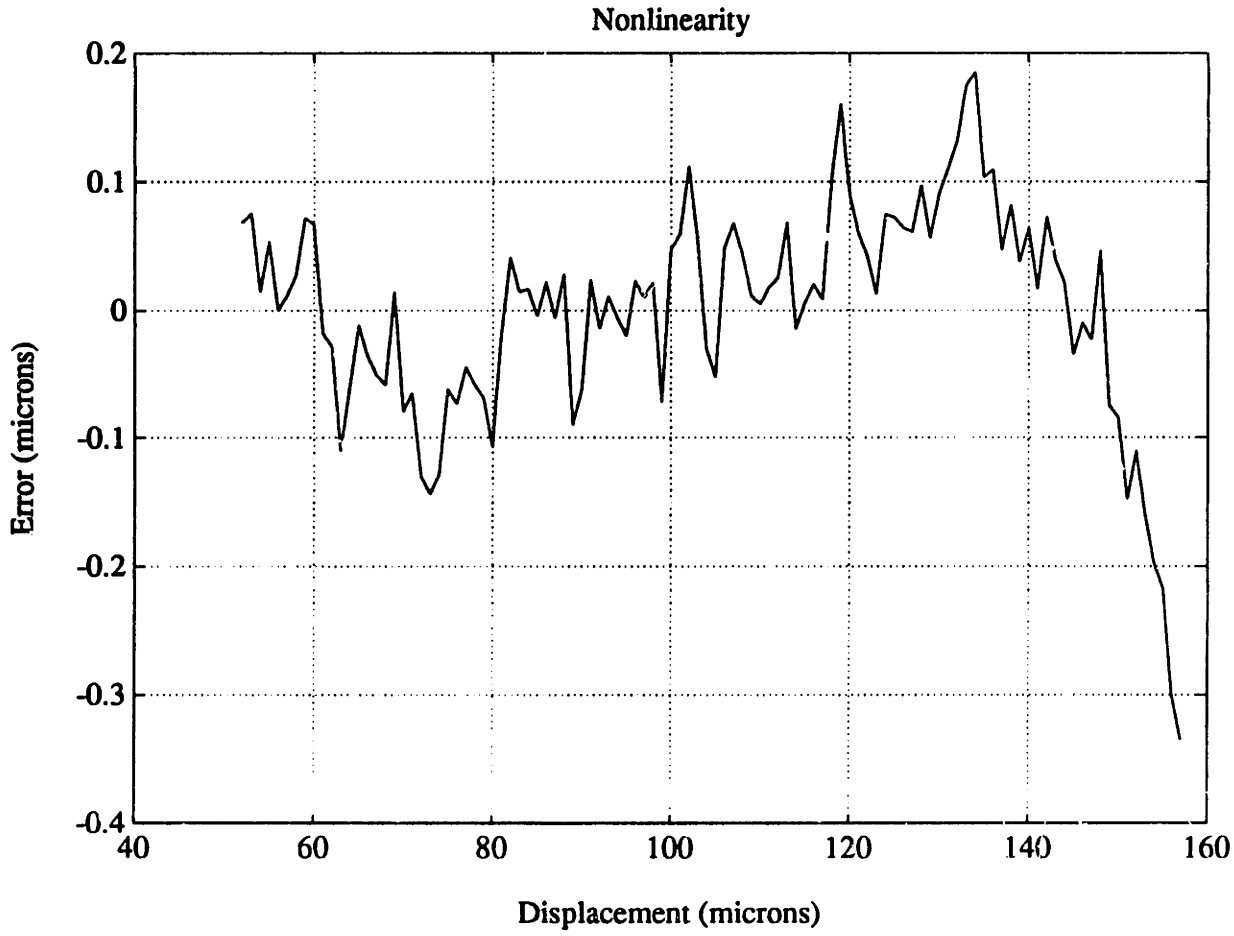

Figure 6.3.2-3: Nonlinearity--100 Micron Range

Since a larger probe area is desired, the linearity test was repeated with the probe operating in the 25 micron to 75 micron displacement range. In terms of the capacitance range, this is equivalent to a probe with twice the area being operated from 50 microns to 150 microns. The output as a function of displacement is shown in Figure 6.3.2-4. Once again, the data and a best fit straight line are shown. The residual error is shown in Figure 6.3.2-5. This time, a quadratic component to the error is clearly visible. The linearity is only about .4% as opposed to roughly .1% as in the case where the probe is operated from 50 microns to 150 microns.

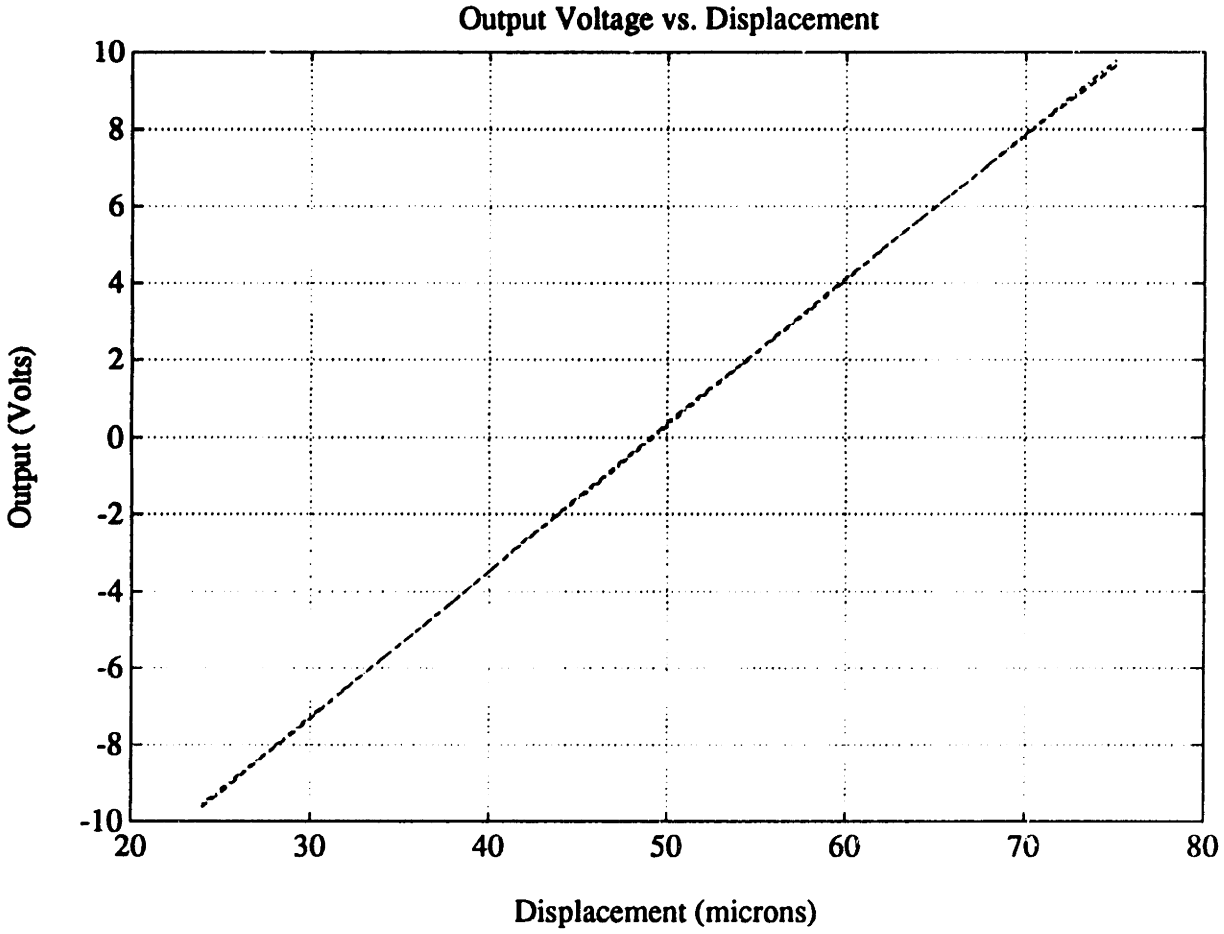

Figure 6.3.2-4: Output vs. Displacement--50 Micron Range

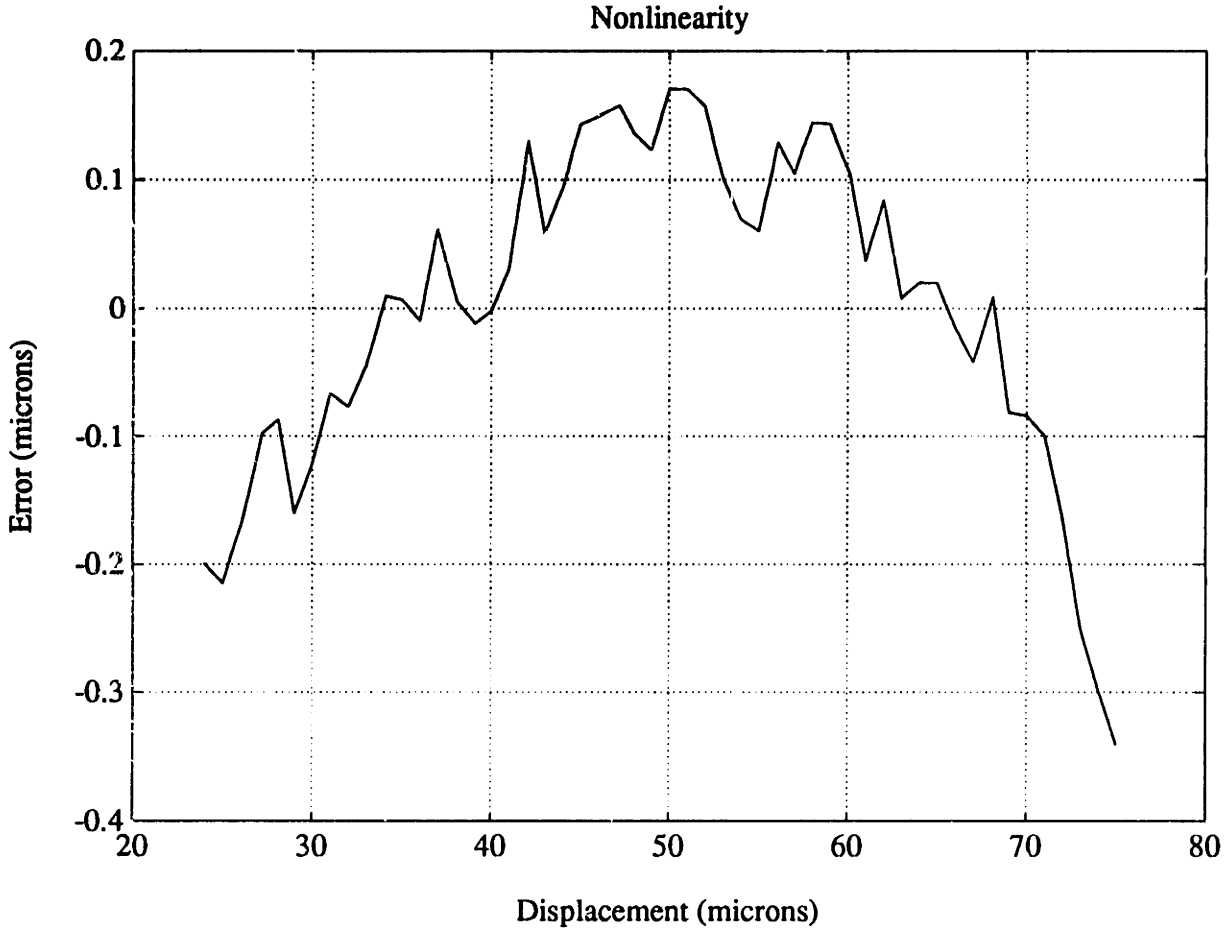

Figure 6.3.2-5: Nonlinearity--50 Micron Range

The nonlinearity observed in Figure 6.3.2-5 may be attributed to several sources. If the reference capacitor is not linear, then a nonlinearity will be introduced in the output. Since the two charge pumps are operating at different current levels, the errors caused by the diode forward drops will be different. Additionally, if the probe guard drive is not ideal, a nonlinearity will be introduced.

6.4 Summary

While still having a few bugs, the experimental prototype shows great promise for very low noise instrumentation. When the variable capacitance is located on the circuit board, the noise level is around 30 μVp-p in the .1 to 300 Hz frequency range. Unfortunately, a relatively large amount of drift is introduced when the variable capacitance

is moved to the end of a cable. Additionally, the line frequency interference become quite severe when the probe and fixture are connected to the circuit. Through careful shielding and grounding, this problem should eliminated.

The A/D converter displays an equivalent input noise of less than 1 LSB_{RMS} at the 20-bit level. The noise in the A/D has a strong line frequency component. Through the use of a better power supply and careful shielding, the interference noise should be eliminated. The linearity of the A/D was not tested due to lack of accurate enough test equipment.

The complete system exhibits a nonlinearity of less than .5% for large capacitances and less than .1% for smaller capacitances. The exact source of the nonlinearity is not known at this time. It is quite possible that the .5% nonlinearity observed with larger capacitances was due to nonlinearities in the reference capacitor.

7 Conclusions and Recommendations

7.1 Summary

Several approaches to the drive electronics for a capacitive based transducer have been examined. The approaches may be classified in to three broad categories. The oscillator class of circuit gives an output frequency that is a function of the unknown capacitance. The relaxation oscillator, while conceptually simple, is not well suited to low noise measurements. Resonant oscillators have the disadvantage of a reduced sensitivity to changes in capacitance. Two varieties of charge pumps have been considered. The charge pump circuits offer the advantage of being able to use an RF drive and hence produce a larger signal current. The main disadvantage of the diode based charge pumps is the thermal variations of the diodes. The final class of drive electronics considered is the ac bridge type circuit. This approach has the advantage eliminating the diodes. A major challenge in the design of an ac bridge circuit is the requirement for a very low noise excitation source. Additionally, the drive frequency is limited.

A noise model for each of the charge pumps and the bridge circuits has been developed. Using the model for the transformer coupled charge pump, a system with fairly predictable noise performance has been designed. When the variable capacitance is located on the probe drive circuit board, the noise level has been demonstrated to be around 5 μV_{RMS} with an output range of ± 10 volts. When the variable capacitance is moved to the end of a cable, the low frequency drift is increased to an unacceptable level. Although the exact reason for the increased drift has not yet been determined, it is likely a result of variations in the cable properties.

As part of the system, a 20-bit A/D converter with a delay of a few milliseconds has been designed. The A/D converter which is based on averaging 512 samples from a 16-bit

commercially available converter has demonstrated an equivalent input noise level of less than 1 LSB_{RMS} on the 20-bit level.

The overall system has demonstrated a linearity of better than .1% from displacement in to digital out when operated over a 50 to 150 micron range. When the system is operated over a 25 to 75 micron range, the linearity is reduced to ~.5%. The weak point in the system is a large amount of either thermal drifting or $\frac{1}{f}$ noise. If this issue can be corrected, then the system may be used for very high performance capacitive sensing.

7.2 Recommendations for Further Work

As a starting point for further research, the system presented in this thesis should be constructed on a printed circuit board with a ground plane. Care should be taken to isolate RF currents in the ground and power supplies from rest of the circuit. As part of this precaution, the air core inductor used in the oscillator circuit should be replaced with an inductor which confines the magnetic fields to its interior. This would involve using either a toroidal or pot core. When the circuit board is being laid out, the 10 volt reference used in the probe circuit should be connected to the reference input on the A/D converter. Additionally, a precision reference capacitor should be used. The reference capacitor should have a very low temperature coefficient as the drift of the circuit can be no better than that of the reference capacitance. Care should also be taken to select a reference capacitor with a low voltage coefficient to preserve the linearity of the system.

In addition to the layout, construction, and precision component issues mentioned above, the power supply should be improved. The supply presented in Appendix IV should be adequate if additional heatsinking is employed. The +5 and ±15 volt supplies for the digital accumulator should be separate from the main ±15 volt supply to avoid coupling noise through the power supply. The required digital supplies may be obtained by adding additional regulated outputs to the supply.

With the improved layout and power supplies, the equivalent input noise to the A/D converter should be reduced. At this point it will probably become necessary to add the dither circuit described in Chapter 5. This addition is needed to assure that the A/D input is always changing by a few LSB's to decorrelate the quantization noise from the input signal.

If further reductions in the noise level are required, the most promising approach is to increase the probe current. This may be done in a number of ways. First the probe capacitance may be increased by using a larger area probe or using a dielectric material in the gap. The other approach is to use a step up transformer at the output of the oscillator buffer. By using a larger drive voltage, a higher current will result. With the small gaps that are being used with this probe, care should be taken to not exceed the breakdown field of the dielectric. It appears that the low frequency drifting that was observed with a fixed capacitance at the end of a cable, may be due to thermal variations in the cable. If this is the case, then some cancellation may be possible by putting the reference capacitance and diodes inside of the probe. An additional benefit of this approach is that the diodes can be forced to be in close thermal contact. This would have the effect reducing thermal variations. Two disadvantages to putting the reference capacitance in the probe are the requirement for more conductors in the cable and the difficult involved with changing reference capacitances.

Some tests that should be performed on the system in addition to the ones presented here include: a more careful thermal characterization of the circuit, noise testing of the probe in a mechanically and thermally stable environment, and more accurate linearity testing using an interferometer.

A1 Oscillator Dynamics

A1.1 Circuit Overview

The oscillator circuit is a Colpitts oscillator and is shown below in Figure A1.1-1. The amplitude of the oscillations is determined by the control voltage, V_C, which sets the bias current in the differential pair.

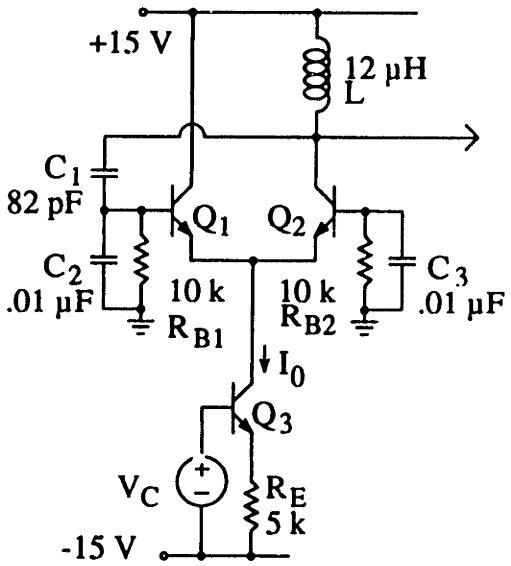

Figure A1.1-1: Colpitts Oscillator

A1.2 Linear Analysis

A small signal model for the Colpitts oscillator is shown below in Figure A1.2-1. The transistor differential pair has simply been replaced by an ideal transconductance. In the frequency range of interest, the r_π's of the transistors are large compared to the impedance of C_2 and hence have been omitted. Resistors R_S and R_P model all losses present in the circuit.

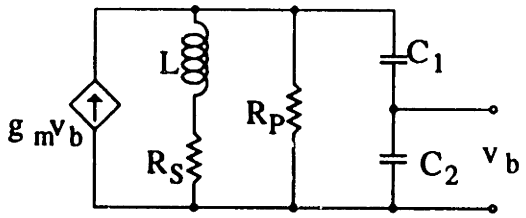

Figure A1.2-1: Oscillator Small Signal Model

Noting that the dependent current source is controlled by its own terminal voltage, it may be replaced by a resistance with value

$$r = -\left(\frac{C_1 + C_2}{C_1}\right)\left(\frac{1}{g_m}\right) \approx -\left(\frac{C_2}{C_1}\right)\left(\frac{1}{g_m}\right) \qquad \text{(A1.2-1)}$$

The transconductance, g_m, is that of the complete differential pair and is equal to one half the transconductance of each transistor. Note that the resistance is negative. The equivalent circuit is shown in Figure A1.2-2.

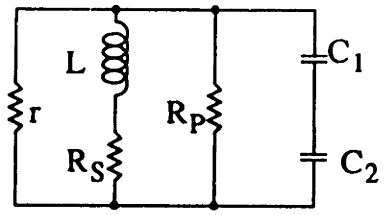

Figure A1.2-2: Simplified Small Signal Model

From the characteristic equation, (A1.2-2), it is evident that the poles may be placed precisely at $\frac{\pm j}{\sqrt{LC}}$ by varying the bias current through the differential pair. The capacitance, C, is the total capacitance of the circuit and is to a very good approximation equal to C_1.

$$LCs^2 + \left(R_S C + \frac{L}{R_P} + \frac{L}{r}\right)s + 1 \qquad \text{(A1.2-2)}$$

We are now in a position to determine the small signal transfer function from the control voltage to output amplitude for the circuit of Figure A1.1-1. Assume that g_m has been adjusted to place the poles precisely on the jω-axis. Now consider small variations in g_m around the nominal value.

$$g_m = G_M + \Delta g_M \qquad \text{(A1.2-3)}$$

The characteristic equation becomes

$$LCs^2 - \left(\Delta g_m \frac{C_1}{C_2} L\right)s + 1 \qquad \text{(A1.2-4)}$$

This places the poles of the system at

$$s = \frac{\Delta g_m}{2C_2} \pm \frac{j}{\sqrt{LC_1}} \qquad \text{(A1.2-5)}$$

Assume the system is oscillating with an initial amplitude, E_A. The form of the response is given by (A1.2-6).

$$E_A e^{\alpha t} \sin(\omega_o t) \qquad \text{(A1.2-6)}$$

where α is the real part of the poles given in (A1.2-5). Using a Taylor series expansion and disregarding the higher order terms, the envelope of the output signal is

$$E_A(1 + \alpha t) = E_A\left(1 + \frac{\Delta g_m}{2C_2} t\right) \qquad \text{(A1.2-7)}$$

Since the response to a step in the input, Δg_m, is a ramp in the output, the linearized transfer function is simply an integration and is given by (A1.2-8). V_A is the amplitude of the output oscillations.

$$\frac{V_A(s)}{\Delta g_m(s)} = \frac{E_A}{2C_2 s} \qquad \text{(A1.2-8)}$$

The transfer function given in (A1.2-8) can be rewritten in terms of the peak-to-peak amplitude as opposed to the peak amplitude. The result is

$$\frac{V_{out(p-p)}(s)}{\Delta g_m(s)} = \frac{V_{P-P}}{2C_2 s} \qquad \text{(A1.2-9)}$$

The complete transfer function from control voltage to peak-to-peak output amplitude is easily obtained by recognizing that the total circuit transconductance is $\frac{I_O}{4\,V_T}$ where V_T is the thermal voltage.

$$\frac{V_{out(p-p)}(s)}{v_c(s)} = \frac{V_{P-P}}{8V_T R_E C_2 s} \qquad \text{(A1.2-10)}$$

A1.3 Nonlinear Analysis

The linear analysis given in Section A1.2 predicts a transfer function from changes in the control voltage to output amplitude which is a pure integration. In reality, the nonlinearity of the transistors will cause the dc gain to be finite. At high frequencies, the linearized model is still valid. It is possible to predict the dc gain using describing function analysis. See [Roberge 75] for a treatment of describing functions.

The relationship between input voltage and output current of the differential transistor pair used is

$$I_C = \frac{I_0}{2}\left(1 + \tanh\left(\frac{V_{IN}}{2V_T}\right)\right) \qquad \text{(A1.3-1)}$$

The describing function transconductance is the ratio of the amplitude of the fundamental component of the output current to the amplitude of the input voltage for a sinusoidal input. The describing function transconductance is then

$$G_{MD}(E) = \frac{I_0}{\pi E}\int_0^{\pi} \sin(\theta)\tanh\left(\frac{E\sin(\theta)}{2V_T}\right)d\theta \qquad \text{(A1.3-2)}$$

E is the amplitude of the input voltage. It is useful to define a constant, k, which represents the change in the effective transconductance of the differential pair as a function of the input amplitude.

$$k\left(x = \frac{V_{IN}}{V_T}\right) = \frac{G_{MD}(V_{IN})}{G_{MD}(0)} = \frac{2}{\pi x}\int_0^{\pi} \sin(\theta)\tanh\left(\frac{x\sin(\theta)}{2}\right)d\theta \qquad \text{(A1.3-3)}$$

The effective transconductance of the circuit, g_{meff}, is simply k times the small signal transconductance. A plot of k versus input amplitude is shown below in Figure A1.3-1.

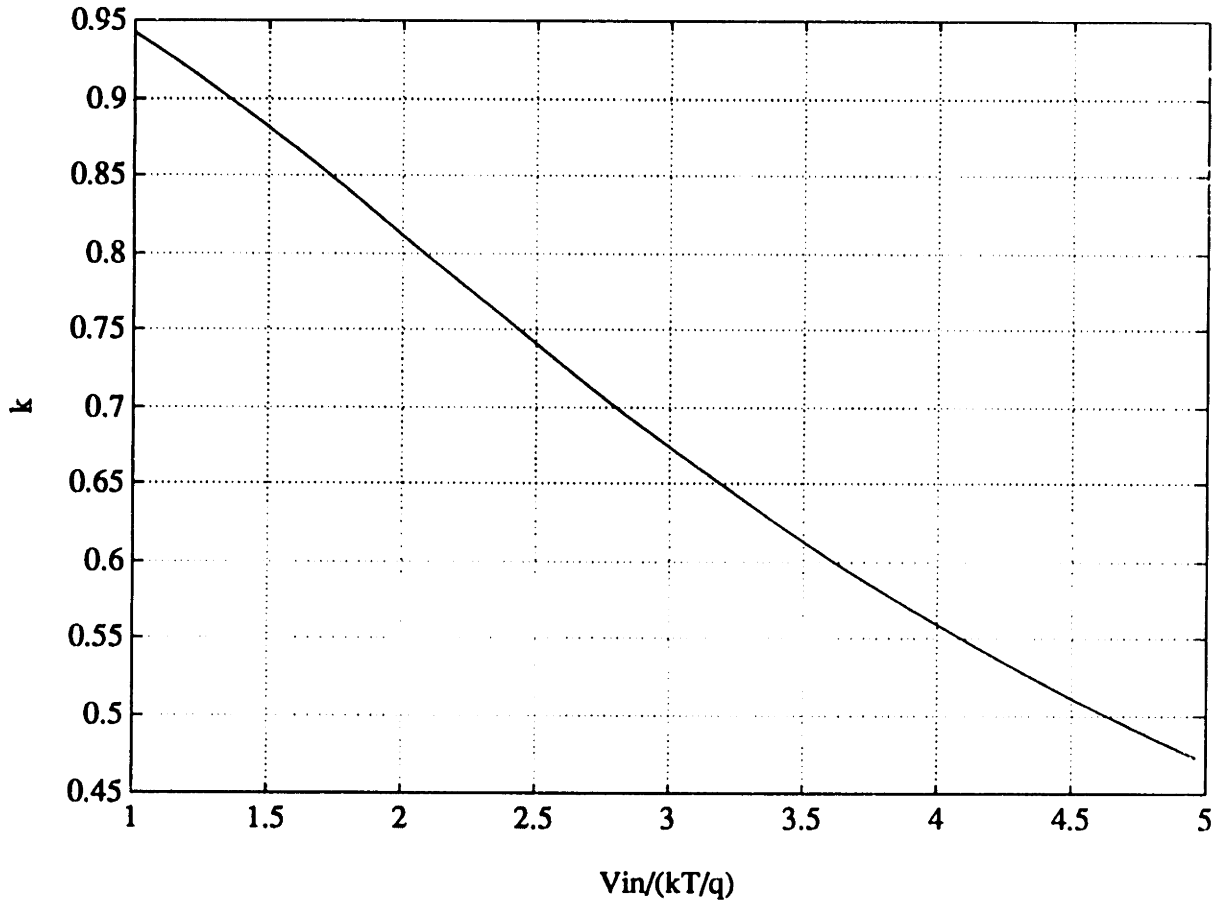

Figure A1.3-1: Normalized Describing Function Transconductance

The dc gain of the oscillator may be calculated in the following way. It is assumed that the Q of the tank circuit is independent of the operating point. Under that assumption, the effective transconductance should remain constant as the control voltage varies. This is stated mathematically by

$$\frac{\partial}{\partial V_C}\left(g_{meff} = k g_{m0}\right) = 0 \tag{A1.3-4}$$

Expanding (A1.3-4) gives

$$k\left(\frac{\partial g_{m0}}{\partial I_o}\right)\left(\frac{\partial I_o}{\partial V_C}\right) = -g_{m0}\left(\frac{\partial k}{\partial\left(\frac{V_{IN}}{V_T}\right)}\right)\left(\frac{\partial\left(\frac{V_{IN}}{V_T}\right)}{\partial V_C}\right) \tag{A1.3-5}$$

Where V_{IN} is the amplitude of the input to the differential pair. Defining the derivative of k as

$$k' = \frac{\partial k}{\partial\left(\frac{V_{IN}}{V_T}\right)} \qquad \text{(A1.3-6)}$$

and the dc gain as

$$dc\ \ gain = \frac{\partial V_{OUTp-p}}{\partial V_C} \qquad \text{(A1.3-7)}$$

the dc gain may be solved for. The result is given by (A1.3-8). The dc voltage across R_E in the circuit of Figure A1.1-1 is V_{RE}, V_T is the thermal voltage, and Q is the Q of the tank circuit.

$$dc\ \ Gain = (-2)\left(\frac{C_2}{C_1}\right)\left(\frac{k}{k'}\right)\left(\frac{V_T}{V_{RE}}\right) = \left(-\frac{1}{2}\right)\left(\frac{k}{k'}\right)\left(\frac{QZ_0}{R_E}\right) \qquad \text{(A1.3-8)}$$

A plot of $\frac{k}{k'}$ as a function of the input voltage to the differential pair is shown below in Figure A1.3-2.

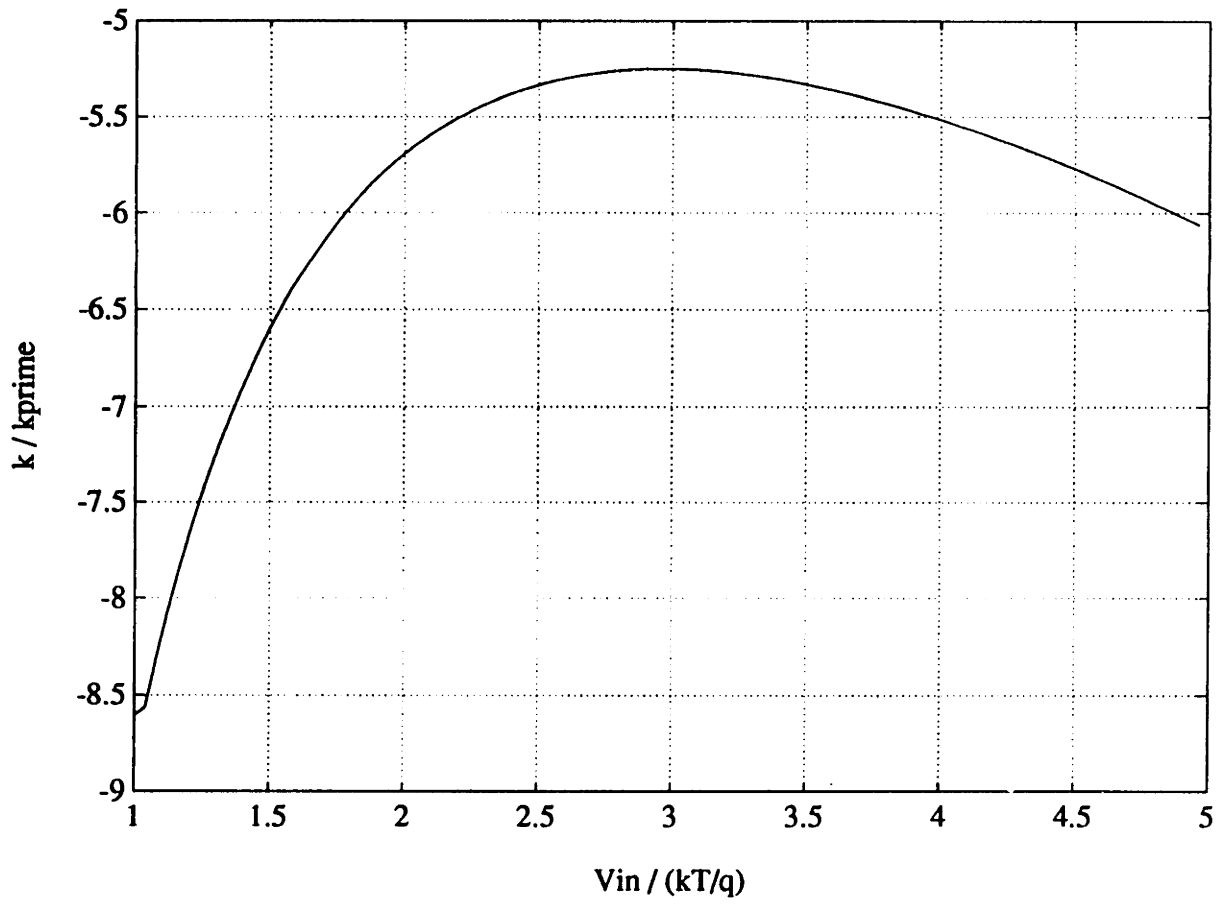

Figure A1.3-2: k/k' vs. Differential Pair Input Voltage

A1.4 Complete Dynamic Model

The results of the linear and nonlinear analyses presented here can be combined to obtain a good model for the response of the oscillator. A single pole transfer function whose dc gain is obtained via the describing function method and whose high frequency gain is determined from the linearized analysis will do a good job of predicting the oscillator behavior. The complete transfer function from control voltage to peak-to-peak output amplitude is

$$\frac{v_{out(p-p)}}{v_c} = \frac{A\tau}{\tau s + 1} \qquad \text{(A1.4-1)}$$

The constants, A and τ, are given by (A1.4-2) and (A1.4-3).

$$A = \frac{V_{P-P}}{8V_T R_E C_2} \tag{A1.4-2}$$

$$\tau = (-4QZ_0C_2)\left(\frac{k}{k'}\right)\left(\frac{V_T}{V_{P-P}}\right) \tag{A1.4-3}$$

Note that the dc gain is very dependent on the operating point. Figure A1.4-1 shows the variation for the part values shown in Figure A1.1-1.

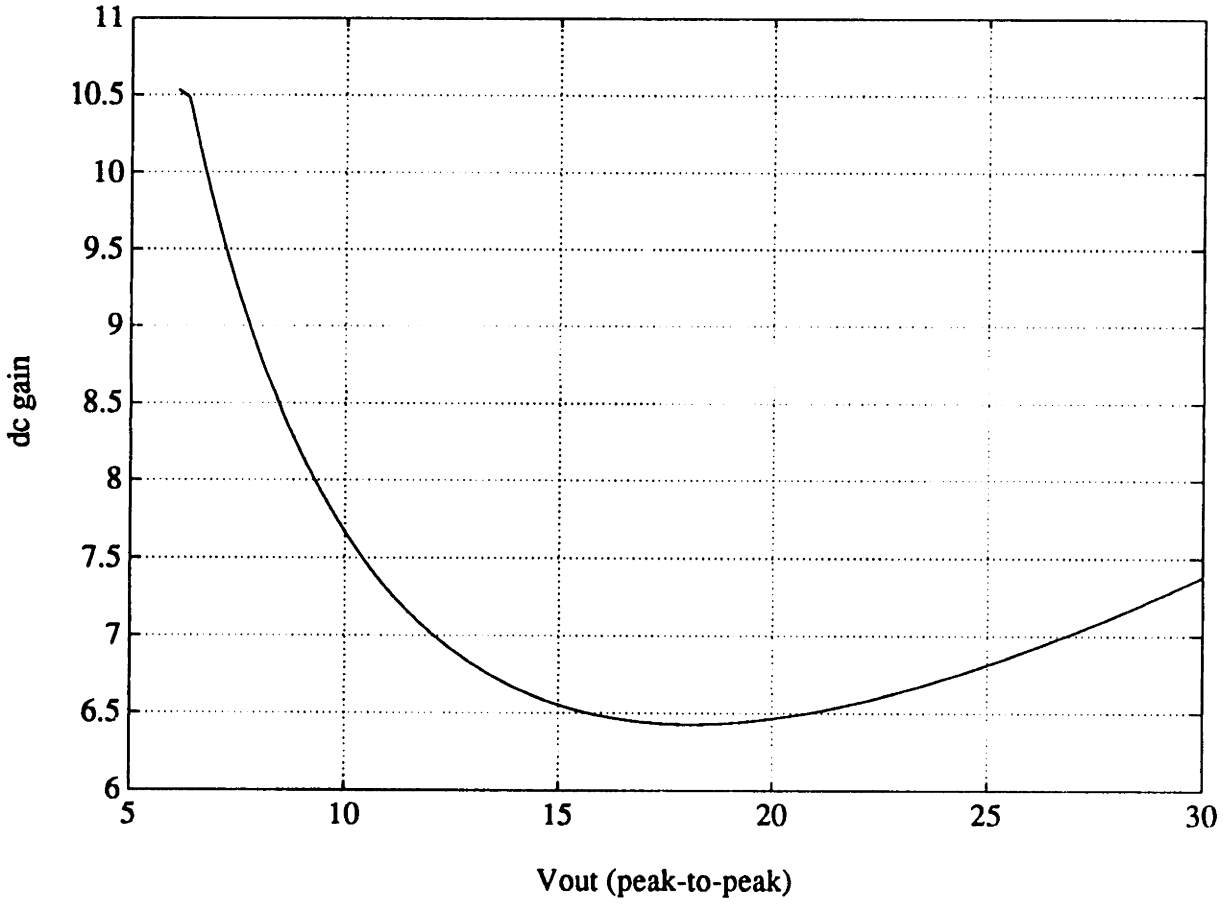

Figure A1.4-1: DC Gain vs. Peak-to-Peak Output Voltage

The pole frequency as a function of peak-to-peak output voltage is shown below in Figure A1.4-2.

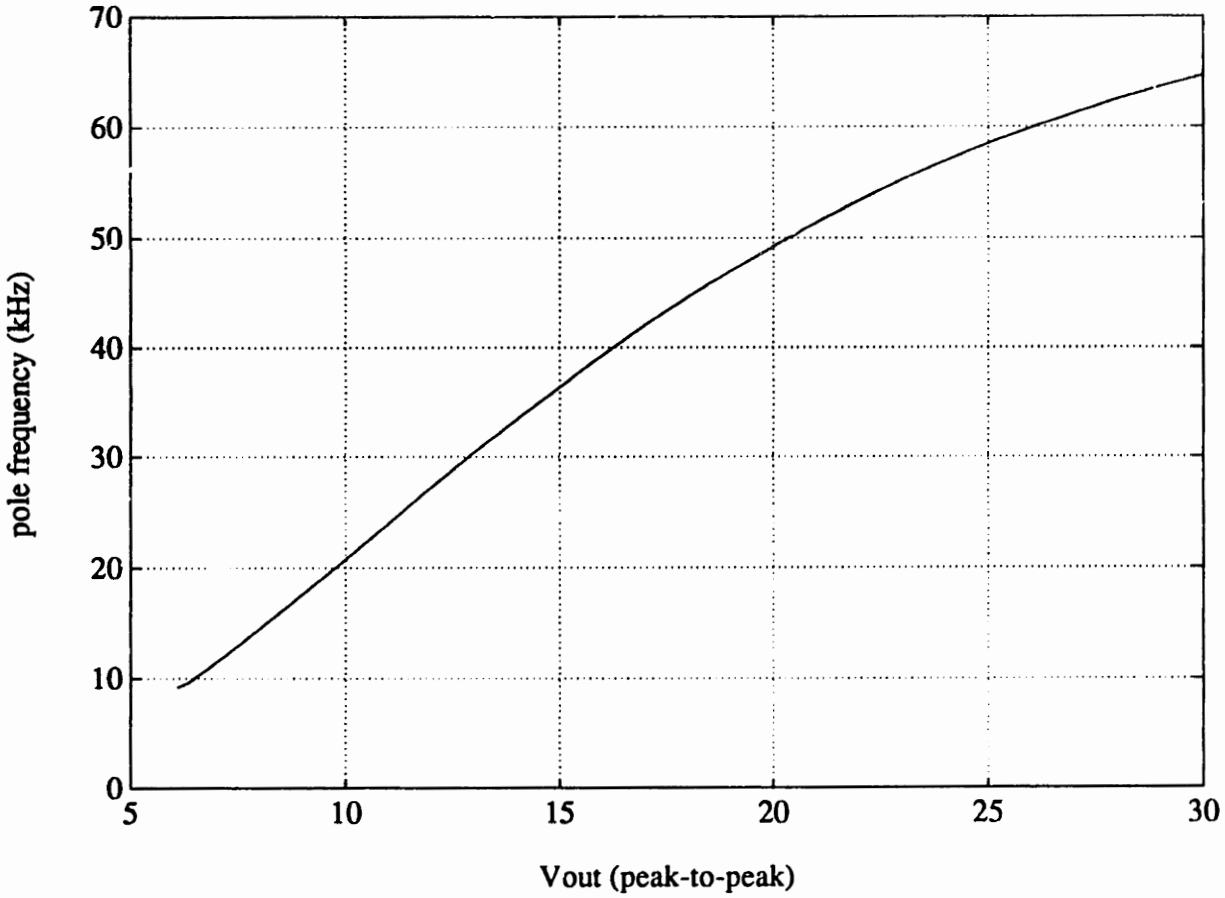

Figure A1.4-2: Pole Location vs. Peak-to-Peak Output Voltage

A2 Digital Accumulator

A2.1 Accumulator Schematics

Complete schematics for the digital accumulator are shown in Figures A2.1-1, A2.1-2, and A2.1-3. The assembly code for the 68HC705K1 microcontroller is given in section A2.2.

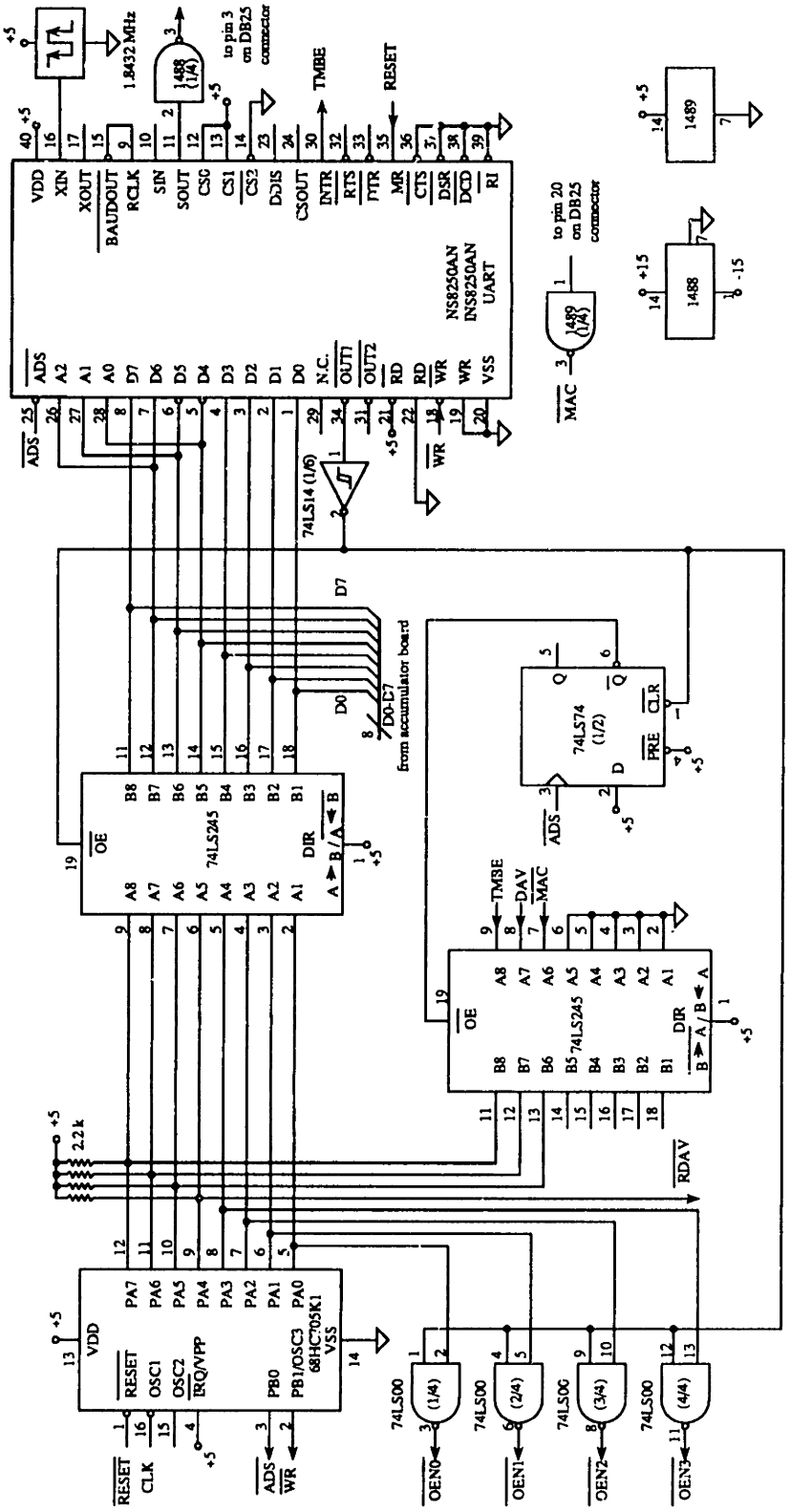

Figure A2.1-1: Accumulator Control Circuit

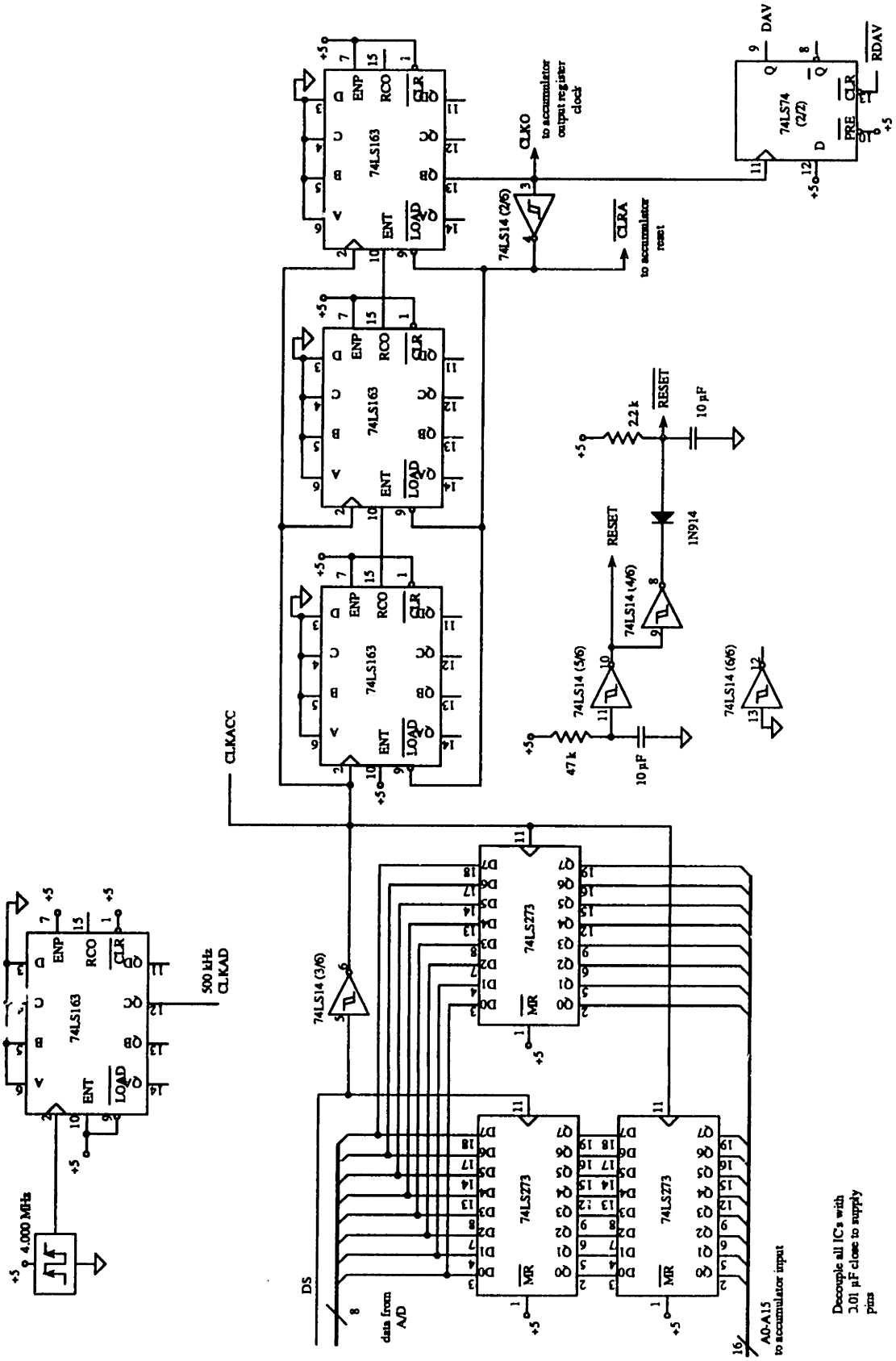

Figure A2.1-2: Accumulator Schematics--page 2

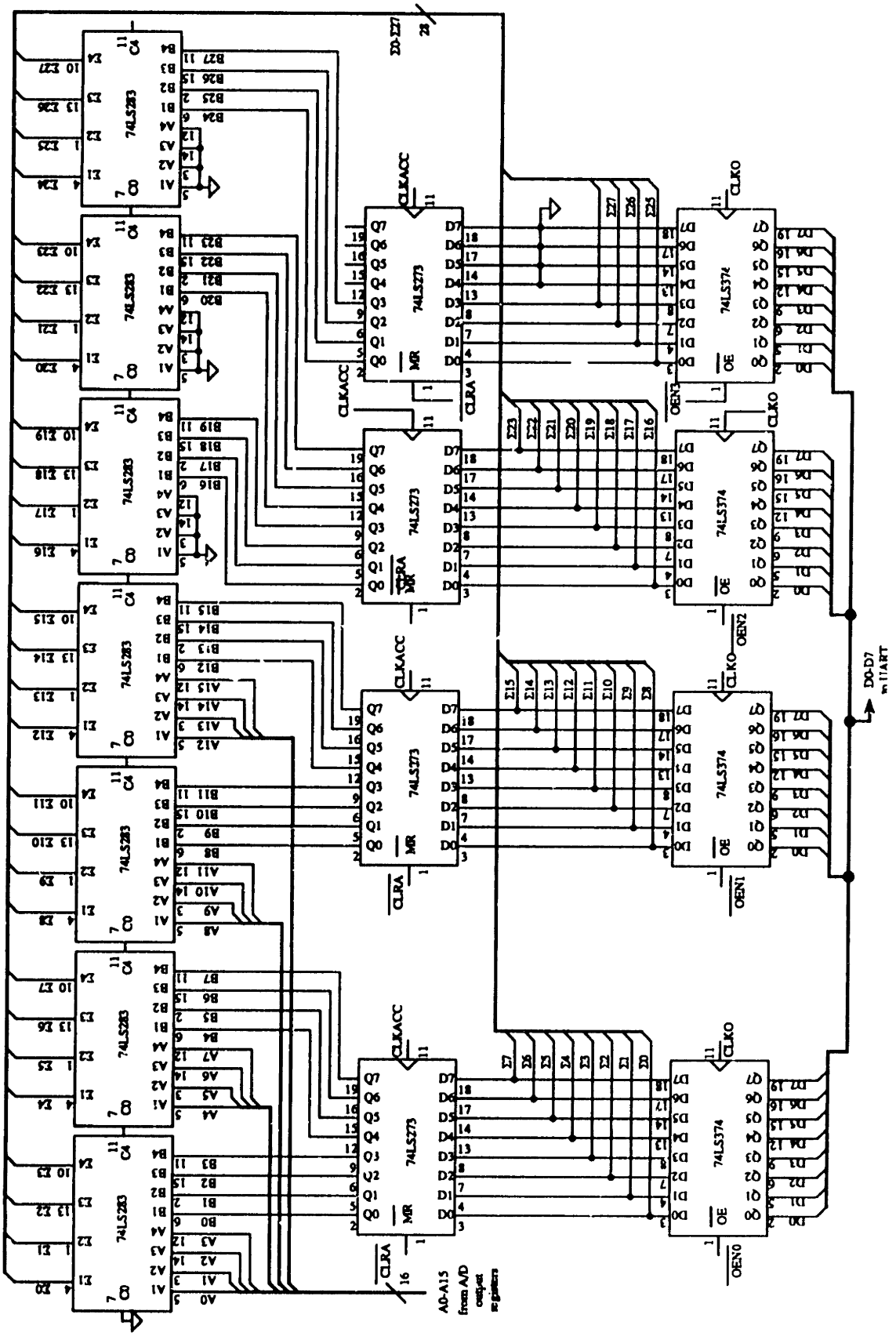

Figure A2.1-3: Accumulator

A2.2 68HC705K1 Assembly Program

```
DAN2.asm                Assembled with IASM   04/17/1993  21:02

                  1
0200              2                org   rom       ;program begins at location
                                                   $0200
                  3
                  4
0200 A6FF         5      init      lda   #$ff      ;set the port directions
0202 5F           6                clrx            ;clear the x register
0203 B704         7                sta   ddra      ;port a = all outputs
0205 B700         8                sta   porta     ;port a = all 1's
0207 BF01         9                stx   portb     ;set ADS=WR=0
0209 B705        10                sta   ddrb      ;portb=outputs
020B 1001        11                bset  0,portb   ;ADS=1
020D 1201        12                bset  1,portb   ;WR=1
                 13
                 14      initio
020F A630        15                lda   #$30      ;set up first UART address
0211 B700        16                sta   prta      ;
0213 1101        17                bclr  0,portb   ;strobe ADS to latch the UART
                                                   address
0215 1001        18                bset  0,portb   ;
0217 A683        19                lda   #$83      ;data to set UART parity,
                                                   data, and stop bits
0219 B700        20                sta   prta      ;
021B 1301        21                bclr  1,portb   ;clock data into UART
021D 1201        22                bset  1,portb   ;
                 23
021F 5F          24                clrx            ;address=00
0220 BF00        25                stx   prta      ;send out address
0222 1101        26                bclr  0,portb   ;strobe ADS=0
0224 1001        27                bset  0,portb   ;ADS=1
0226 A602        28                lda   #$02      ;set baud divisor=2 (57600
                                                   baud)
0228 B700        29                sta   prta      ;send LSB's of baud divisor
022A 1301        30                bclr  1,portb   ;strobe WR=0
022C 1201        31                bset  1,portb   ;WR=0
022E A610        32                lda   #$10      ;address = 01 (for MSB's of
                                                   baud divisor)
0230 B700        33                sta   prta      ;send address
0232 1101        34                bclr  0,portb   ;strobe ADS=0
0234 1001        35                bset  0,portb   ;ADS=1
0236 BF00        36                stx   prta      ;send out 0's to porta (the x
                                                   register still
                 37                               ;has zeros in it from above
0238 1301        38                bclr  1,portb   ;strobe WR=0
023A 1201        39                bset  1,portb   ;WR=1
023C A630        40                lda   #$30      ;address is 3
023E B700        41                sta   prta      ;send out address
0240 1101        42                bclr  0,portb   ;strobe ADS=0
0242 1001        43                bset  0,portb   ;ADS=1
0244 A603        44                lda   #$03;     restore DLAB=1 on UART
0246 B700        45                sta   prta      ;
0248 1301        46                bclr  1,portb   ;strobe WR=0
024A 1201        47                bset  1,portb   ;WR=1
                 48
024C A610        49                lda   #$10      ;address is 1 to set UART
                                                   interrupts
024E B700        50                sta   porta     ;
0250 1101        51                bclr  0,portb   ;strobe ADS=0
0252 1001        52                bset  0,portb   ;ADS=1
0254 A602        53                lda   #$02      ;TMBE interrupt enabled
```

```
0256 B700    54              sta   porta     ;
0258 1301    55              bclr  1,portb   ;strobe WR=0
025A 1201    56              bset  1,portb   ;WR=1
             57
025C A640    58              lda   #$40      ;address for Modem control
                                               register
025E B700    59              sta   porta     ;
0260 1101    60              bclr  0,portb   ;strobe ADS=0
0262 1001    61              bset  0,portb   ;ADS=1
0264 A604    62              lda   #$04      ;activate out1
0266 B700    63              sta   porta     ;
0268 1301    64              bclr  1,portb   ;strobe WR=0
026A 1201    65              bset  1,portb   ;WR=1
             66
026C A61F    67              lda   #$1F      ;set the porta data direction
026E B704    68              sta   ddra      ;
0270 A618    69              lda   #$18      ;select chip 4
0272 B700    70              sta   porta     ;
             71
0274 1101    72              bclr  0,portb   ;strobe ADS=0 to set the UART
                                               to send
0276 1001    73              bset  0,portb   ;ADS=1 and also enable U3
             74
             75
0278 0A00FD  76    waitmac   brset 5,porta,waitmac   ;wait for the MAC to
                                               go low
027B 1900    77    rdav      bclr  4,porta   ;reset DAV
027D 1800    78              bset  4,porta   ;
             79
027F 0D00FD  80    waitdav   brclr 6,porta,waitdav   ;wait for DAV to go
                                               high (data ready)
             81
0282 1000    82              bset  0,porta   ;enable byte0
             83
0284 0F00FD  84    waitb0    brclr 7,porta,waitb0    ;wait for TMBE to go
                                               high (UART ready)
             85
0287 1301    86              bclr  1,portb   ;strobe WR=0 to send byte0
0289 1201    87              bset  1,portb   ;WR=1
028B 1100    88              bclr  0,porta   ;disable byte0
028D 1200    89              bset  1,porta   ;enable byte1
             90
028F 0F00FD  91    waitb1    brclr 7,porta,waitb1    ;wait for TMBE to go
                                               high (UART ready)
0292 1301    92              bclr  1,portb   ;strobe WR=0 to send byte1
0294 1201    93              bset  1,portb   ;WR=1
0296 1300    94              bclr  1,porta   ;disable byte1
0298 1400    95              bset  2,porta   ;enable byte2
             96
029A 0F00FD  97    waitb2    brclr 7,porta,waitb2    ;wait for TMBE to go
                                               high (UART ready)
029D 1301    98              bclr  1,portb   ;strobe WR=0 to send byte2
029F 1201    99              bset  1,portb   ;strobe WR=1
02A1 1500   100              bclr  2,porta   ;disable byte2
02A3 1600   101              bset  3,porta   ;enable byte3
            102
02A5 0F00FD 103    waitb3    brclr 7,porta,waitb3    ;wait for TMBE to go
                                               high (UART ready)
02A8 1301   104              bclr  1,portb   ;strobe WR=0 to send byte3
02AA 1201   105              bset  1,portb   ;WR=1
02AC 1700   106              bclr  3,porta   ;disable byte3
02AE 20C8   107              bra   waitmac   ;return to beginning of the
                                               loop.
            108
```

```
                109
03F8            110             org     vectors ;vectors begin at $03F8
03F8 0200       111             fdb     rom     ;there is no timer interrupt
                                                service routine
03FA 0200       112             fdb     rom     ;there is no external ISR
03FC 0200       113             fdb     rom     ;there is no swi ISR
03FE 0200       114             fdb     init    ;reset vector


Symbol          Table

INIT            0200
INITIO          020F
RDAV            027B
WAITB0          0284
WAITB1          028F
WAITB2          029A
WAITB3          02A5
WAITDAV         027F
WAITMAC         0278
```

A3 Data Collection Program

A3.1 Program Description

The program in this appendix is used to facilitate testing of the A/D converter and accumulator. It was compiled using Think's Lightspeed C v5.0 on an Apple MacIntosh IIci. The program prompts the user for a number of data points and an output file name. Then the specified amount of data is read in through the serial port and stored in a MATLAB compatible file. The data may then be analyzed using MATLAB.

A3.2 SerialPortProgram.c

```
/*  This program receives data coming in from the modem port          */
/*  and outputs the data in a MATLAB compatible file.  To read        */
/*  in the data, use  "load filename" from MATLAB                     */
/*                                                                    */
/*  It negates the DTR line on the serial port and pauses for         */
/*  a couple of seconds to let the accumulator board synchronize      */
/*  then the DTR is asserted.  This tells the accumulator board       */
/*  to begin collecting data.  The data comes in a number of 8        */
/*  bit bytes set by DATABYTES below.  It is assumed that the         */
/*  least significant byte comes first.                               */

/*  this program is based on two similar programs,                    */
/*  SerialPortProgram does the same thing with the exception that     */
/*  it only handles 1 byte data.  GetSerialData and its wide          */
/*  version monitor the data coming in from the serial port and       */
/*  display it on the screen.                                         */

/*  This program is © 1993, Dan McMahill.  All rights reserved.       */
/*  Although its unlikely that it would be useful to anyone else,     */
/*  I give anyone and everyone permission to use any portions of      */
/*  this code as long as they don't try and prevent others from       */
/*  doing the same.                                                   */


#include <stdio.h>
#include <math.h>
#include <console.h>
#include <Serial.h>
#include <Types.h>

#define     DATABYTES   4

#define     BAUD        baud57600
#define     DATABITS    data8
#define     STOPBITS    stop10
#define     PARITY      noParity

/* if the communications settings above are modified, the */
/* SETTINGS string below should be updated */
```

```
#define     SETTINGS    "57600 baud, 8 data bits, 1 stop bit, no parity,
                              4 byte wide data"

#define     XONCHAR     0x11
#define     XOFFCHAR    0x13

#define     OUTDRIVER   "\p.AOut"
#define     INDRIVER    "\p.AIn"

#define     NEGATEDTR   18
#define     ASSERTDTR   17

#define     PAUSE       1

#define     INITSIZE    100


/**************/
/* Functions */
/**************/

void        OpeningInfo(void);
OSErr       SerialInit(void);
OSErr       AllocateBuffer(Size);
Size        GetUserInfo(void);
void        HouseKeep(void);
void        SendBufferToFile(Size);
OSErr       GetSerialData(Size *);
void        Pause(long);

/**************/
/*  Globals  */
/**************/

unsigned char     *gInBuf;
Ptr               gSerialBufferPtr;
short             gInRefNum, gOutRefNum;
FILE              *gOutputFilePtr;
Boolean           gDone;

void main(void)
{
      OSErr       err;
      short       KeyPressed;
      Size        bufferSize,i;

      gDone = false;

/* print out program title and basic information */

      OpeningInfo();

/* initialize the serial port */

      gInRefNum=0;
      gOutRefNum=0;
      if((err=SerialInit()))
      {
            printf("the serial initializations have failed id %d",err);
            gDone = true;
      }

/* main loop */
```

```
        while(gDone == false)
              {
                    bufferSize = GetUserInfo();
                    if(bufferSize == 0 )
                    {
                          gDone = true;
                    }

                    else
                    {
                    /* allocate a new buffer */

                          AllocateBuffer(bufferSize);

                    /* read in data */

                          printf("\nReceiving Data (%lu %d-byte
                                points)...\n",
                                bufferSize/DATABYTES,DATABYTES);

                          if((err = GetSerialData(&bufferSize)))
                          {
                                printf("\nUnable to get data id %d ",err);
                                HouseKeep();
                                exit();
                          }


                    /* dump data to output file */
                          printf("Received %lu bytes, (%lu %d-byte data
                                points)\n",

                                bufferSize,bufferSize/DATABYTES,DATABYTES);

                          SendBufferToFile(bufferSize);

                    /* close the output file */

                          fclose(gOutputFilePtr);

                    }

              }

        HouseKeep();
        printf("\n\nPress <Return> to Exit....\n\n");
}

/************************** OpeningInfo *************/

/* Requires: SETTINGS (a string with communications port settings that
                                is #define'd at the beginning of the
                                program */

/* Modifies: nothing */

/* Effect:  prints out some basic information */

void OpeningInfo(void)
{
        printf("\n\nDan's Serial Port Program");
        printf("\n© 1993, Dan McMahill");
        printf("\nAll rights reserved.\n\n");
        printf("\n\nThis program reads data from the serial port and");
```

```
      printf("\nsaves it in a MATLAB compatible file.  To load the");
      printf("\ndata into MATLAB, enter   load filname    at");
      printf("\nthe MATLAB prompt.  The data will now be in a vector");
      printf("\nnamed filename.\n");
      printf("\n%s\n",SETTINGS);
}

/************************* SerialInit *************/

/* Requires: the following constants are #define'd at the start of the
                              program BAUD, DATABITS, STOPBITS,PARITY,
                              INDRIVER, OUTDRIVER, FALSE, XONCHAR,
                              XOFFCHAR, INITSIZE, ASSERTDTR, NEGATEDTR,
                              PAUSE.  The following globals are also
                              required:  gInBuf, gInRefNum, gOutRefNum*/

/* Modifies:      gInBuf -- sets to pointer to newly allocated input
                              buffer
                  gInRefNum -- sets to input port reference number
                  gOutRefNum -- sets to output port reference number */

/* Effect:  SerialInit opens the serial drivers, allocates an input
                              buffer, and initializes the driver.  The
                              handshaking and communications protocols
                              are hard coded into the routine for now.
                              Should make these user setable later.
                              Negates the DTR line on the modem port*/

OSErr SerialInit(void)
{
      OSErr       err;
      SerShk      flags;
      Ptr         buf;
      Ptr         csParamPtr;

/* Open Serial Drivers */

      if((err = OpenDriver(INDRIVER, &gInRefNum)))
            return err;
      if((err = OpenDriver(OUTDRIVER, &gOutRefNum)))
            return err;

/* Reset both input and output, and assign communications protocols */

      if((err = SerReset(gInRefNum,BAUD + DATABITS + STOPBITS +
                              PARITY)))
            return err;
      if((err = SerReset(gOutRefNum,BAUD + DATABITS + STOPBITS +
                              PARITY)))
            return err;

/* allocate an input buffer and assign to input driver */

      if(!(gSerialBufferPtr = NewPtr(INITSIZE)))
            return MemError();
      if(err = SerSetBuf(gInRefNum,gSerialBufferPtr,INITSIZE))
            return err;

/* Set handshaking for the input driver */
      flags.fXOn = FALSE;
      flags.fInX = FALSE;
      flags.xOn = XONCHAR;
      flags.xOff = XOFFCHAR;
      if((err = SerHShake(gInRefNum,&flags)))
```

```
            return err;

/* negate the DTR line and pause for PAUSE seconds*/

      Control(gInRefNum,NEGATEDTR,csParamPtr);
      Pause(PAUSE);

/* allocate an input buffer */

      if(!(gInBuf = (unsigned char *) NewPtr(INITSIZE)))
            return MemError();

      return noErr;
}


/************************** AllocateBuffer *************/

/* Requires: gInBuf*/

/* Modifies: gInBuf -- sets to pointer to newly allocated input buffer
                              */

/* Effect:  Disposes of buffer allocated to gInBuf then allocates and
                              assigns a buffer of size bufferSize to
                              gInBuf. */

OSErr AllocateBuffer(Size bufferSize)
{
      Ptr   buf;
      OSErr err;

/* release current buffer */

      if(gInBuf)
            DisposPtr(gInBuf);

/* allocate a new buffer of size bufferSize and assign to gInBuf */

      if(!(gInBuf = (unsigned char *) NewPtr(bufferSize)))
            return MemError();
}

/************************** GetUserInfo *************/

/* Requires: gDone, gOutputFilePtr */

/* Modifies:      gDone--sets it to true if 0 data points are selected
                  gOutputFilePtr--sets to be a pointer to the newly
                              opened output file.*/

/* Effect:  Gets information from user on how many data points, output
                              file name.  Also opens output file.*/

Size GetUserInfo(void)
{
      Size  bufferSize=0;
      char  outputFileName[50];

      printf("\nHow Many Data Points (0 to exit)? ");
      scanf("%lu",&bufferSize);
      if(bufferSize == 0)
      {
            gDone = true;
```

```
            return(bufferSize*DATABYTES);
      }

      else
      {
            printf("Output File Name? ");
            scanf("%s",outputFileName);

      /* open output file */
            gOutputFilePtr = fopen(outputFileName,"w");

      /* verify that the file was opened ok */

            if(gOutputFilePtr == NULL)
            {
                  printf("couldn't open %s.  Sorry.....\nRET to
                              exit...",outputFileName);
                  gDone = TRUE;
                  bufferSize=0;
                  return(bufferSize*DATABYTES);
            }
            return(bufferSize*DATABYTES);

      }


}

/************************** HouseKeep *************/

/* Requires: gInRefNum, gOutRefNum,gInBuf*/

/* Modifies:      gInRefNum--closes the driver referenced by gInRefNum
                  gOutRefNum--closes the driver referenced by gOutRefNum
                  gInBuf--deallocated the buffer pointed to by gInBuf*/

/* Effect:  closes the serial drivers, releases the input buffer*/

void HouseKeep(void)
{
      if(gInRefNum)
            CloseDriver(gInRefNum);

      if(gOutRefNum)
            CloseDriver(gOutRefNum);

      if(gInBuf)
            DisposPtr(gInBuf);
}

/************************** SendBufferToFile *************/

/* Requires: an open file pointer, gOutputFilePtr, DATABYTES*/

/* Modifies:  */

/* Effect:  crunches the DATABYTES byte long data points into single 32-
                        bit data points and then sends the new
                        data to the output file pointed to by
                        gOutputFilePtr */

void SendBufferToFile(Size bufferSize)
{
      unsigned long     i,j;
```

```
        unsigned long     total;

        printf("\nProcessing data and writing to output file...\n");
        for(i=0;i<bufferSize;i+=DATABYTES)
        {
              total = 0;

              for(j=0 ; j<DATABYTES;j++)
              {
                    total += gInBuf[i+j]*pow(256,j);
              }
              fprintf(gOutputFilePtr,"%lu  ",total);
        }
}


/************************** GetSerialData *************/

/* Requires: ASSERTDTR, NEGATEDTR, gSerialBufferPtr, gInRefNum, gInBuf
                                    */

/* Modifies:       gSerialBufferPtr--set to point to a newly allocated
                                    buffer
                   gInBuf--the buffer it points to gets filled with
                                    data.*/

/* Effect: flushes the serial buffer, asserts DTR, gets new data and
                                    then negates DTR */

OSErr GetSerialData(Size *bufferSizePtr)
{
        OSErr         err;
        Ptr           csParamPtr;


/* allocate an input buffer and assign to input driver */

        if(!(gSerialBufferPtr = NewPtr(*bufferSizePtr)))
              return MemError();
        if(err = SerSetBuf(gInRefNum,gSerialBufferPtr,*bufferSizePtr))
              return err;

/* assert DTR to tell the accumulator board to start collecting data */

        Control(gInRefNum,ASSERTDTR,csParamPtr);

/* read in data */

        (void) FSRead(gInRefNum, bufferSizePtr,gInBuf);

/* negate DTR to return the accumulator board to its waitmac routine */

        Control(gInRefNum,NEGATEDTR,csParamPtr);
}


/********************************** Pause ***************/

/* Requires:  */

/* Modifies:  */

/* Effect:    pauses for length seconds */
```

```
void  Pause(long length)
{
      long  now,secs;

      GetDateTime(&now);

      secs=now;

      while(secs<now+length)
      {
            GetDateTime(&secs);
      }
}
```

A4 Power Supply

A4.1 Low Noise Power Supply Appendix

Figure A4.1-1 shown the regulated power supply that was used for the probe circuit. Unfortunately without additional heatsinking, it is not adequate to power both the probe circuit and the A/D circuit. In order to have very low ripple, a two stage regulator was used. The 7915 and 7815 provide a regulated ± 25 volt supply. Discrete regulators were then used to provide ±15 volts at the output. Commercially available 3-terminal regulators typically have very large amounts of noise on the output. This is due to the internal Zener references. In order to produce a much lower noise supply, a discrete Zener reference with a limited bandwidth was used.

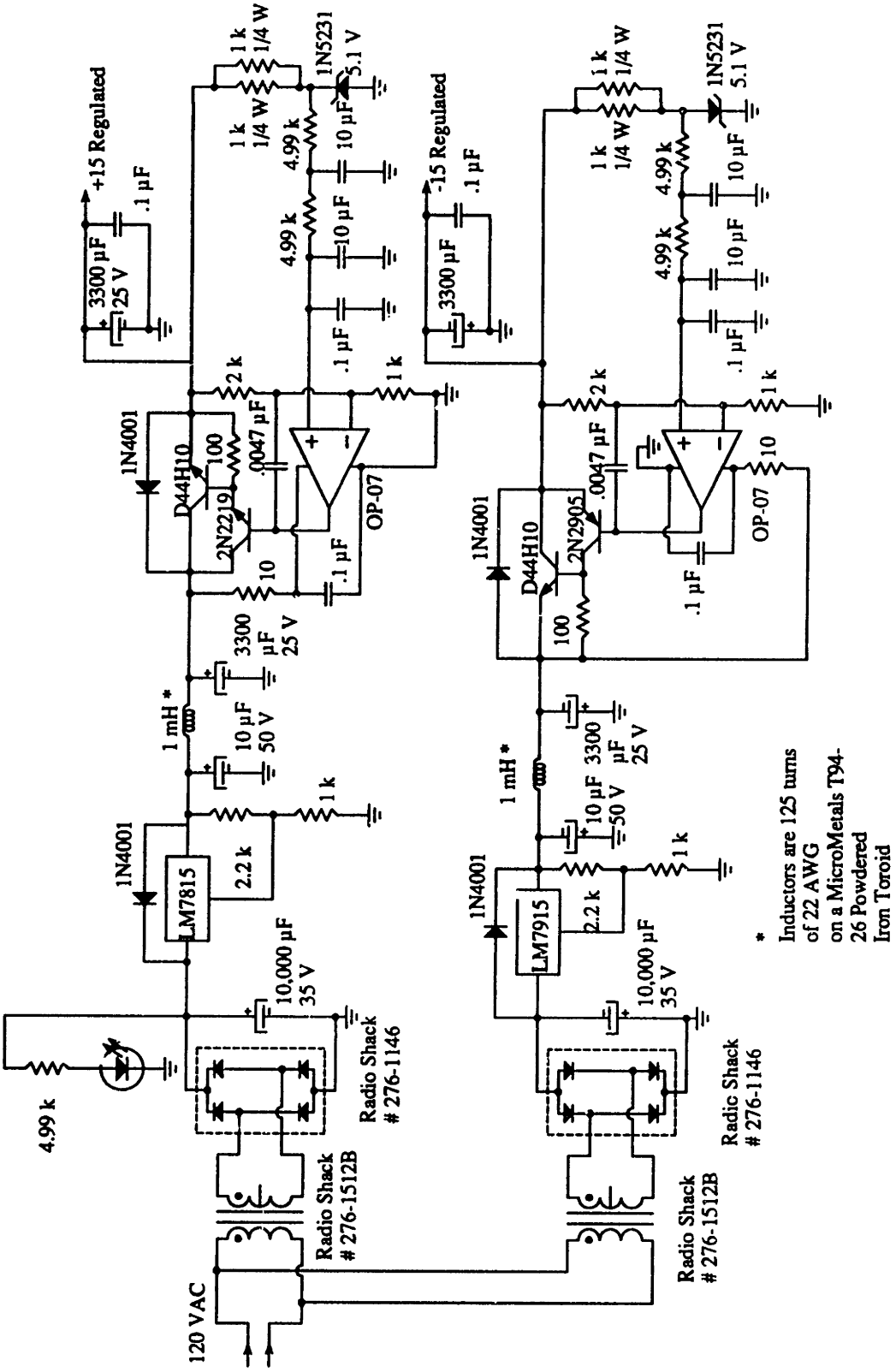

Figure A4.1-1: Regulated Power Supply

References

[ADE 88] ADE Corporation, "Using Capacitive Sensing for Noncontact Dimensional Gauging," *Sensors*, vol. 5 no. 10, 1988.

[Analog Devices 92] Analog Devices, *1992 Amplifier Reference Manual*, Analog Devices, Norwood, MA, 1992.

[Bertone 90] G. A. Bertone, Z. H. Meiskin, and N. L. Carroll, "Investigation of a Capacitance-Based Displacement Transducer," *IEEE Transactions on Instrumentation and Measurement*, pp. 424-428, vol. 39, no. 2, April 1990.

[Candy 92a] J. C. Candy and G. C. Temes, "Oversampling Methods for A/D and D/A Conversion," *Oversampling Delta-Sigma Data Converters*, IEEE Press, Piscataway, NJ, 1992.

[Candy 92b] J. C. Candy and G. C. Temes, *Oversampling Delta-Sigma Data Converters*, IEEE Press, Piscataway, NJ, 1992.

[Chapman 85] P. D. Chapman, "A Capacitance Based Ultra-Precision Spindle Error Analyzer," *Precision Engineering*, vol. 7, no. 3, July 1985.

[Cichocki 90] A. Cichocki and R. Unbehauen, "A Switched-Capacitor Interface for Capacitive Sensors Based on Relaxation Oscillators," *IEEE Transactions on Instrumentation and Measurement*, vol. 39 vo. 5, pp. 797-799, October 1990.

[Fertner 89] A. Fertner, and A. Sjölund, "Analysis of the Performance of the Capacitive Displacement Transducer," *IEEE Transactions on Instrumentation and Measurement*, vol. 38, no. 4, pp. 870-875, August 1989.

[Gray 84] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits, 2nd ed.*, John Wiley & Sons, Inc., New York, 1984.

[Gray 90] R. M. Gray, "Quantization Noise Spectra," *IEEE Transactions on Information Theory*, vol. IT-36, pp. 1220-1244, November 1990.

[Huang 88] S. M. Huang, A. L. Stott, r. G. Green, and M. S. Beck,"Electronic Transducers for Industrial Measurement of Low Value Capacitances," *Journal of Physics E: Scientific Instruments*, vol. 21, pp. 242-250, 1988.

[Jones 88] R. V. Jones and J. C. Richards, "The Design and Some Applications of Sensitive Capacitance Micrometers," *Instruments and Experiences*, John Wiley & Sons Ltd., 1988.

[Klaassen 82] K. B. Klaassen, and J. C. L. Van Peppen, "LInear Capacitive Microdisplacement Transduction Using Phase Read-Out," *Sensors and Actuators*, 3 (1982/83), pp. 209-220

[Kosel 81] P. B. Kosel, G. S. Munro, and R. Vaughan, "Capacitive Transducer for Accurate Displacement Control," *IEEE Transactions on Instrumentation and Measurement*, vol IM-30, no. 2, pp. 114-123, June 1981.

[Kudoh 91] T. Kudoh, S. Shoji, and M. Esashi, "An Integrated Miniature Capacitive Pressure Sensor," *Sensors and Actuators A*, A-29, pp. 185-193, 1991.

[Leslie 61] W. H. P. Leslie, "Choosing Transformer Ratio-Arm Bridges," *Proceedings of the IEE*, paper no. 3646 M, pp. 539-545, September, 1961.

[Neubert 63] H. K. P. Neubert, *Instrument Transducers*, Oxford University Press, London, 1963.

[Peters 92] R. D. Peters and P. J. Seibt, "An Inexpensive Synchronous Detector and Its Application to differential Capacitance Sensors," *Rev. Scientivic Instruments*, Vol. 63, No. 8, pp. 3989-3992, August 1992.

[Ramachandran 90] G. Ramachandran, K. Sampathkumar, S. Swarnamani, and M. Singh, "Reconstruction of Cardiac Displacements by Capacitance Transducer Method," *Biomedical Eng. and Perspectives: Health Care Tech. for the 1990's and Beyond--Proc. of the Ann. Conf. on Eng. in Med. and Biology , pt. 3*, IEEE, Piscataway, NJ, 1990.

[Richards 75] J. C. S. Richards, "Linear Capacitance Proximity Gauges with High Resolution," *Journal of Physics E: Scientific Instruments*, vol. 9, pp. 639-646, 1976.

[Roberge 75] J. K. Roberge, *Operational Amplifiers: Theory and Practice*, John Wiley & Sons, New York, 1975.

[Roberge 93] J. K. Roberge, U.S. Patent #5,189,376, February 23,1993.

[Sanders 91] S. R. Sanders, J. M. Noworolski, X. Z. Liu, and G. C. Verghese, "Generalized Averaging Method for Power Conversion Circuits," *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp. 251-259, April 1991.

[Scott 39] A. H. Scott, and H. L. Curtis, "Edge Correction in the Determination of Dielectric Constant," Research Paper RP1217, *Part of Journal of Research of the National Bureau of Standards*, vol 22, June 1939.

[Trumper 90] D. L. Trumper, *Magnetic Suspension Techniques for Precision Motion Control*, Ph.D. Thesis, Department of Electrical Engineering and Computer Science, M.I.T., Cambridge, MA, 1990.