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A 25 mV-Startup Cold Start System with On-Chip Magnetics for Thermal Energy Harvesting

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Abstract— Thermal energy harvesting systems use boost converters for high-efficiency low voltage operation, but lack the ability for low voltage startup without off-chip transformers. We present a cold start system that uses integrated magnetics instead of external transformers in a Meissner Oscillator to start up from ultra low voltages, with a switched capacitor DC-DC circuit for additional voltage gain. The oscillator analysis with on-chip magnetics allows device co-optimization for low voltage operation, despite 1000x lower inductance values than off-chip transformers. Co-optimized on-chip transformer and depletion-mode NMOS start up from 25 mV driven directly by a sourcemeter, or 50 mV with a 4.7 Ω series resistance, for the lowest integrated electrical startup. The co-packaged system provides proof of concept for integration with boost converter circuits on a single die to have a fully-integrated low voltage startup solution for thermal energy harvesting applications, without using off-chip transformers.

Keywords— energy harvesting; startup; on-chip; integrated; magnetics; transformer; optimization; Meissner; cold start

I. INTRODUCTION

The emerging internet of things (IoT) relies on energy harvesting to power millions of wireless sensors in smart homes, wearable electronics, and industrial applications. To harvest the limited ambient energy, thermal energy harvesting systems use inductive boost converters designed to operate from voltages down to 10 mV [1]. However, these converters need a cold start (CS) system to start up from a de-energized state (Fig. 1), most of which either have a high startup voltage or use external transformers. The integrated CS solution in [1] uses a ring oscillator to start up from 220 mV, [2] uses a ring oscillator with post-fabrication threshold voltage (V_T) trimming to start up from 95 mV, while [3] uses an inductive-load ring oscillator with negative V_T switch for 65 mV startup. A mechanical switch allows [4] to start up from 35 mV, but it is limited to applications with ambient mechanical vibrations.

Another compelling startup approach is the Meissner Oscillator (MO). [5] proposes an MO with an off-chip transformer for 20 mV startup, the lowest reported by far, as an alternative to boost converters, but with lower efficiency and higher area. This efficiency concern is addressed in [6], which uses the MO for 40 mV startup and a boost converter for normal operation, but it still needs a bulky off-chip transformer. The work in [7] uses an MO with bond-wire microtransformers for 104 mV startup. None of the existing solutions provide both low voltage startup and low area, which is needed to further the applicability of energy harvesting systems in IoT.

We present an ultra low voltage startup solution with on-chip magnetics for thermal energy harvesting systems to harvest energy even from weak ambient sources. We propose

Fig. 1 Thermal energy harvesters with efficient boost converters lack startup ability. We propose a cold start system with on-chip magnetics for low voltage startup in a small area.

- MO analysis suitable for use with on-chip magnetics
- On-chip transformer and NMOS device co-optimization based on the MO analysis
- Switched capacitor DC-DC converter design to interface with the boost converter

The co-packaged on-chip transformer, NMOS, and switched capacitor circuit demonstrate the lowest startup voltage for an integrated electrical startup solution.

II. LOW VOLTAGE COLD START SYSTEM DESIGN

The proposed CS system provides a low voltage startup without large transformers for the application in Fig. 1. A thermoelectric generator (TEG) provides DC voltage $V_{TEG} = SAT$, where S is the Seebeck coefficient and ΔT is the thermal gradient, as an input to the CS system. The CS system charges up its output capacitor to $V_{START} = 1.2$ V, which can then power the control circuitry of the boost converter until the converter starts up and takes over. To achieve a 25 mV startup with $\sim 50\times$ voltage gain to 1.2 V, the proposed CS system consists of two main cascaded stages (Fig. 2). The first stage consists of an MO with an on-chip transformer for low voltage startup, followed by a rectifier. The rectified output V_{RECT} powers the next stage, which is a switched capacitor DC-DC converter, consisting primarily of a ring oscillator and a 4-stage charge pump to boost the output voltage to 1.2 V.

Fig. 2 Proposed cold start system consists of a Meissner Oscillator with integrated magnetics and a cascaded stage of switched capacitor DC-DC circuit for a fully on-chip startup solution.

Fig. 3 Conceptual waveforms showing CS system operation sequence

The CS system also contains a voltage detection circuit to detect if the output voltage V_{START} has reached 1.2 V and to set V_{OK} to HIGH as an indication that the load, i.e. the control circuits, can start drawing power. In case of high loads, a small hysteresis window in the detection circuit allows the system to supply energy to the load over multiple cycles. Fig. 3 shows the conceptual operation sequence of the proposed system.

III. MEISSNER OSCILLATOR WITH ON-CHIP MAGNETICS

The MO is a well-known topology (Fig. 4) [5-7], but the use of on-chip transformers makes the design approach fundamentally different from the conventional approach with off-chip transformers because of two main challenges:

1. On-chip transformers have 100-1000x lower inductance than off-chip transformers, but similar parasitic resistance and capacitance.
2. On-chip transformers have high flux leakage, such that coupling coefficient $k \sim 0.6$.

These challenges can be attributed to the smaller 2-D magnetic cores in the on-chip transformers. In this work, we present a framework for designing a low voltage startup MO with on-chip magnetics, given the challenges.

A. Meissner Oscillator Analysis

Fig. 5 shows the small signal model for the MO suitable for use with on-chip magnetics, where L_p is the primary inductance, L_s is the secondary inductance, R_p is the primary resistance, R_s is the secondary resistance, M is the mutual inductance, C_s is secondary capacitance, C_g is the NMOS gate capacitance, C_t is the total capacitance, and g_m and g_{ds} are the NMOS transconductance and output conductance, respectively.

In the analysis for off-chip transformers, g_{ds} can be neglected, as done in [6], and the oscillation condition can be expressed in terms of the loop-gain, LG , as

$$LG|_{\omega=\omega_{res}} = g_m M / (R_s C_t) > 1 \quad (1)$$

where the resonant frequency, ω_{res} , is

$$\omega_{res} = 1/\sqrt{L_s C_t} \quad (2)$$

Fig. 4 The Meissner Oscillator consists of co-optimized integrated transformer and depletion mode NMOS device.

Fig. 5 Open loop small signal equivalent of the MO

For the 1:100 turns ratio Coilcraft transformer (LPR6235) used in [5-6], with $L_p=12.5 \mu\text{H}$, $R_s=340 \Omega$, $k=0.95$, and $C_s \approx 6 \text{ pF}$, $R_s C_t / M$ is $\sim 1-10 \mu\text{S}$. So, $g_m > 10 \mu\text{S}$ should be sufficient for sustained oscillations based on (1). One can use an NMOS with $V_T > 0 \text{ V}$ to operate from 25 mV supply in the above-threshold saturation region, where $g_m \gg g_{ds}$ and (1) is valid.

For on-chip transformers, $R_s C_t / M$ is in the mS range and the NMOS needs to have a much higher g_m to satisfy the oscillation condition. A negative V_T NMOS is needed for high g_m at 25 mV supply, so g_{ds} can no longer be ignored for device optimization, as discussed in the following section. For $k \neq 1$, the transfer function with g_{ds} results in a 3-pole system:

$$\frac{v_{mo}}{v_{in}} = \frac{sMg_m}{(g_{ds}(sL_p + R_p) + 1)(s^2 L_s C_t + sR_s C_t + 1) - s^3 M^2 C_t g_{ds}} \quad (3)$$

Using numerical assumptions, including $\omega_{res} \approx 1/\sqrt{L_s C_t}$, verified in the range of interest, the oscillation condition for the on-chip transformer case can be simplified to

$$LG|_{\omega=\omega_{res}} = \left(\frac{R_s C_t (g_{ds} R_p + 1)}{g_m M} + \frac{g_{ds} M}{g_m L_s} \right)^{-1} > 1, \quad (4)$$

which matches well with Spectre AC simulations, while the analysis with $g_{ds} = 0$ does not [Fig. 6(a)]. It is worth noting that when the two terms inside the parenthesis in (4) are comparable, higher M may not always be desirable.

B. Device Optimization based on Analysis

The derived loop-gain in (4) depends on both transformer and NMOS parameters. So, we co-optimize the NMOS and on-chip transformer to maximize the loop-gain and satisfy the oscillation condition.

1. **Negative V_T NMOS Design:** TI's 0.35 μm process with integrated magnetics has a native NMOS with gate length $L = 1.5 \mu\text{m}$ and $V_T = 0.39 \text{ V}$, which is unsuitable for low voltage MO operation. We use depletion mode NMOS with $V_T = -0.15 \text{ V}$ to maximize g_m to the mS range based on EKV models [8], while trading off with g_m/g_{ds} ratio by operating in the above-threshold linear region [Fig. 6(b)]. We also reduce the gate length to increase g_m further. Both of these changes can be achieved in process manufacturing. We fabricated the optimized NMOS devices with $V_T = -0.15 \text{ V}$, $L = 0.5 \mu\text{m}$, and widths ranging from 1 mm to 5 mm.

Fig. 6 (a) Derived loop-gain in (4) matches Spectre simulations. $L_p L_s$ product is kept constant to highlight the inaccuracy of (1); (b) EKV models predict optimum $V_T = -0.15 \text{ V}$ for on-chip magnetics use.

2. **On-chip Transformer Design:** The on-chip magnetics in $0.35\ \mu\text{m}$ process consist of a high permeability magnetic core with copper coils [Fig. 7(a)] [9]. Fig. 7(b) shows the top view of an integrated transformer with key geometrical design parameters: magnetic core width, W_{core} , number of primary and secondary turns, N_p and N_s , and primary and secondary copper widths, W_p and W_s . We extract electrical parameters L_p , L_s , R_s , R_p , and M from physical designs using 3-D simulations in ANSYS Maxwell, and estimate C_s from measured data for a reference transformer. To find the optimal transformer design, we predict geometrical designs based on loop-gain expression in (4), extract electrical parameters, evaluate performance with selected NMOS, and re-iterate. Fig. 8(a) shows a set of 10 simulated transformers over a wide range of geometrical parameters for reference, with $W_{\text{core}} = 0.1\ \text{mm}$ promising the highest loop-gain. Fig. 8(b) shows the effect of varying N_p and N_s on loop-gain for $W_{\text{core}} = 0.1\ \text{mm}$. Reducing W_{core} further provides benefit in simulations, but shape anisotropy is expected to degrade the effective permeability and worsen the performance. Further, closed core structures provide area savings over long transformers, but come with a performance penalty. We optimize the transformer design to maximize the loop gain in (4) with length $< 3\ \text{mm}$ for a reasonable die size.

The optimized on-chip transformer and NMOS were fabricated separately for testing, but can be co-integrated on the same die. They achieve low voltage startup in a small form factor.

IV. SWITCHED CAPACITOR DC-DC CIRCUIT DESIGN

We implemented the switched capacitor circuit in $0.18\ \mu\text{m}$ process, to which the magnetics technology can be added in future, as the $0.35\ \mu\text{m}$ process with magnetics is unsuitable for low voltage operation. The switched capacitor circuit is powered by the MO output and it must not consume more power than the MO can deliver when V_{RECT} is at the lower operating limit of the ring oscillator. We use a 7-stage ring oscillator with sub-threshold devices for low frequency, along with $100\ \text{pF}$ capacitors (C_{PUMP}) in the charge pump stage to limit the power [Fig. 9(a)]. To indicate OK status for $V_{\text{START}} > 1.2\ \text{V}$, the system needs to detect $1.2\ \text{V}$ crossing in the absence of reference voltages. The circuit in [2] works well for detecting low voltages, $\sim 0.5\ \text{V}$, but requires impractically large devices to detect $1.2\ \text{V}$, as the device size ratio scales exponentially with trigger voltage. Using a voltage divider and detecting $V_{\text{START}}/2$ instead needs very large resistors for such low power levels. We use low V_T and high V_T devices (available in the process) in the circuit from [2] to achieve the desired $1.2\ \text{V}$ trigger voltage with reasonable device sizes [Fig. 9(b)]. We use high V_T devices in the inverters for low leakage and unsymmetrical inverters to avoid false positives on V_{OK} when V_{START} is low. We use a $1.5\ \text{nF}$ on-chip storage capacitor for C_{START} to power the expected load i.e. the boost converter's control circuits.

V. MEASUREMENT RESULTS

The on-chip transformer and NMOS devices, which can be implemented on a single die in $0.35\ \mu\text{m}$ magnetics process, were fabricated on separate dies for testing. The transformer occupies $1.5\ \text{mm}^2$ area and the optimal NMOS selected from a range of test devices occupies $0.073\ \text{mm}^2$ area including bond pads. The remaining circuits occupy $< 6\ \text{mm}^2$ area in $0.18\ \mu\text{m}$ process, dominated by the capacitors. The 3 dies were co-packaged in a 72 pin QFN package (Fig. 10). Fig. 11 shows

some measured frequency characteristics of the optimized transformer for 40 samples. At $5.5\ \text{MHz}$ frequency, $L_p = 27\ \text{nH}$, $L_s = 35\ \mu\text{H}$, $R_p = 0.6\ \Omega$, $R_s = 720\ \Omega$, and $k = 0.49$, on average.

Fig. 7 Illustration of the integrated magnetics technology: (a) cross-sectional view of an inductor; (b) top view of a transformer

Fig. 8 (a) Selected transformer designs with a wide range of parameters; (b) N_s sweep on best performer from (a) with N_p and $2N_p$

Fig. 9 (a) Cross-coupled voltage doubler used as a charge pump stage; (b) detection circuit for $1.2\ \text{V}$ trigger voltage

Fig. 10 Co-packaged cold start system with components on three compatible dies that can be integrated onto a single die

Fig. 11 Measured frequency characteristics for 40 transformer samples: (a) secondary inductance; (b) secondary resistance

Fig. 12 presents measured waveforms for the system supplied directly by a Keithley meter. Fig. 12(a) shows that the MO starts up correctly as V_{IN} rises with a 1 μ s RC constant, before co-packaging. Fig. 12(b) shows that the system, after co-packaging, starts up from 25 mV with a slow input ramp up. It starts up from 50 mV with a 4.7 Ω source resistance. Fig. 12(c) shows that the system is up and ready to supply power to the control circuits within 7 ms of being connected to a TEG (Marlow TG12-4) with 5 Ω resistance and 80 mV open circuit voltage at $\Delta T=2^\circ\text{C}$. Fig. 12(d) shows 25 mV startup for 3 test boards with a step input. Fig. 12(e) shows proper V_{OK} functionality. In comparison with prior art, this work has the lowest startup voltage without any off-chip magnetics (Fig. 13). It achieves same order of magnitude as [5] despite using an on-chip transformer. The CS system can be integrated with a boost converter on a single ~ 3 mm x 3 mm die for a fully integrated startup solution (Fig. 14).

VI. CONCLUSION

In this paper, we demonstrated a cold start system that starts up from 25 mV (50 mV open circuit), which is the lowest reported startup without off-chip magnetics. The presented Meissner Oscillator analysis with on-chip transformers allows device co-optimization for low voltage startup, despite 1000x lower inductances than off-chip devices. Negative V_T NMOS and custom on-chip transformer design and fabrication result in low voltage startup. The switched capacitor DC-DC circuit provides an interface for use with a boost converter as proof of concept for a fully integrated startup solution for thermal energy harvesting. For production, the on-chip magnetics and negative V_T NMOS can be added to a newer process and the cold start system can be integrated on a single die with a boost converter for both high efficiency energy harvesting and low voltage startup without bulky off-chip transformers.

Fig. 12 Measured waveforms: (a) Meissner Oscillator startup; (b) cold start system startup from 25 mV; (c) startup with TEG at $\Delta T=2^\circ\text{C}$; (d) startup for 3 test boards with step input; (e) V_{START} and V_{OK} functionality with hysteresis

	Topology	Min. cold start voltage	Transformer	
			type	size ($l \times w \times h$ mm ³)
[1]	Ring oscillator	220 mV	N/A	-
[2]	V_{TH} tuned oscillator	95 mV	N/A	-
[3]	Inductive-load ring oscillator	65 mV	N/A	-
[4]	Mechanical switch	35 mV	N/A	-
[5]	Meissner Oscillator (MO)	20 mV	off-chip	$6 \times 6 \times 3.5^1$
[6]	MO	40 mV	off-chip	$6 \times 6 \times 3.5^1$
[7]	MO	104 mV	bond-wire	$7 \times 3 \times 0.4^2$
This Work	MO with on-chip magnetics	50 mV (open circuit)	on-chip	$3 \times 0.5 \times 0.03^3$

¹ Packaged size ² Core size only ³ Die height includes transformer and circuit layers

Fig. 13 Comparison with prior art

Fig. 14 Vision for the proposed CS system: (a) current co-packaged proof of concept; (b) envisioned implementation of the proposed CS solution in an energy harvesting system integrated on a single die; (c) discrete Coilcraft transformer used in [5-6] for size comparison

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