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Broadband electro-optical crossbar switches using low-loss $\text{Ge}_2\text{Sb}_2\text{Se}_4\text{Te}_1$ phase change material

Francesco De Leonardis¹, Richard Soref², *Life Fellow, IEEE, Fellow, OSA*, Vittorio M. N. Passaro¹, *Senior Member, IEEE, Senior Member, OSA*, Yifei Zhang³ and Juejun Hu³

¹Dipartimento di Ingegneria Elettrica e dell'Informazione, Politecnico di Bari Via Edoardo Orabona n. 4, 70125 Bari, Italy

²Department of Engineering, The University of Massachusetts, Boston, Massachusetts, 02125 USA

³Department of Materials Science & Engineering, Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, Massachusetts 02139, USA

Abstract—This theoretical modeling and simulation paper presents designs and projected performance of non-volatile broadband on-chip 1×2 and 2×2 electro-optical switches operating in the telecommunication C-band and based on the silicon-on-insulator technological platform. These optical switches consist of an asymmetric two-waveguide directional coupler and a symmetric three-waveguide directional coupler in which the optical phase change material (O-PCM) $\text{Ge}_2\text{Sb}_2\text{Se}_4\text{Te}_1$ is the top cladding layer for one of the silicon strip waveguides. Reversible cross-bar switching is attained by the amorphous (Am) to crystalline (Cr) and Cr-to-Am phase transitions in the GSST induced by heating the GSST in contact with an ITO microstrip through Joule heating. We examined device performance in terms of mid-band insertion loss (IL), crosstalk (CT) and 0.3-dB-IL bandwidth (BW). The 2×2 results for the coupling length L_c of 15.4 μm were $\text{IL} = -0.018$ dB, $\text{CT} < 31.3$ dB and $\text{BW} = 58$ nm for 17.4 μm L_c , $\text{IL} = 0.046$ dB, $\text{CT} < 38.1$ dB and $\text{BW} = 70$ nm. Simulations of the 1×2 devices at 16.7 μm L_c revealed that $\text{IL} = 0.083$ dB, $\text{CT} < 12.8$ dB along with an expanded BW of 95 nm. Thermal simulations showed that a 5 V pulse train applied to 10^{19} cm^{-3} -doped ITO would produce crystallization; however the process of amorphization required a 24 V pulse of 2.9 μs duration to raise the GSST temperature above the 900 K melting temperature.

Index Terms—Optical switching devices, electro-optical switches, directional coupler switches, integrated photonic devices, phase change materials.

I. INTRODUCTION

This theoretical paper analyzes the performance of 1×2 and 2×2 self-holding electro-optical switches based on optical phase change material (O-PCM) integrated in the silicon-on-insulator (SOI) technological platform and operating in the telecommunication C-band. The 1×2 and 2×2 switches are considered as essential “building blocks” for the creation of a large-scale on-chip matrix switch, such as a Benes network. Broadband operation of the network is important, and this paper focuses on attaining a building-block bandwidth (BW) in the 50 to 100 nm wavelength range, where BW is defined here as the range for which the optical insertion loss (IL) of the switching element (for both its Cross and Bar states) is less than 0.3 dB. For the building blocks, it is also important to have low optical crosstalk (CT) in both states. The motivation for this paper is to

demonstrate that the 1×2 and 2×2 switch metrics of IL, CT and BW are good enough to enable a large matrix such as 256×256 .

Looking at the competing SOI building blocks over the past decade, free-carrier and thermo-optic effects in silicon (which are “volatile”) produce a comparatively weak change of the real part of refractive index in the active switching region, which led to relatively large footprints and power consumption. Today, O-PCMs are seen as a good alternative because they give non-volatility and strong modulation. As a result, a number of O-PCM applications ranging from switches [2-15], to modulators [16,17], photonic memories [18-20], and light manipulation [21] have recently been explored. Chalcogenides and compounds in the germanium-antimony families were studied. In addition, it has been proven experimentally that the reversible phase change of the O-PCM from amorphous (Am) to crystalline (Cr) or from Cr to Am can be optically [22,23] (by absorbing incident laser light, thus giving temperature rise) or electrothermally [24] (by passing electric current through a micro-heater close to the O-PCM layer). Switching speeds are high and are only limited by the thermal time constant of the heater.

An examination of the prior art literature on O-PCM switches shows several recent papers [2-7, 10-13] that analyze the performances of optical devices based on $\text{Ge}_2\text{Sb}_2\text{Te}_5$ on the SOI platform and $\text{Ge}_2\text{Sb}_2\text{Se}_4\text{Te}_1$ on both silicon nitride (SiN) [8,9] and SOI platforms [14,15]. Here we propose an alternative approach based on $\text{Ge}_2\text{Sb}_2\text{Se}_4\text{Te}_1$ on SOI. We propose realizing the 1×2 and 2×2 as two-waveguide (2WG-) and three waveguide (3WG-) directional couplers, respectively, in which a microstrip heater of doped indium-tin oxide (ITO) is deposited upon the O-PCM strip to serve as top cladding for one of the intrinsic Si waveguides. The ITO is an electrically addressed “contact heater” whose Joule effect induces phase change in the contacted material.

Several aspects of the present work are novel: (1) Broadband operation found for GSST on SOI with significantly improved performance compared to those proposed in literature; (2) very low IL in the Bar state due to concentration of the optical mode in the GSST layer; (3) the contact heating described above, a method superior to prior optical approaches, and (4) the SiO_2 over-cladding of the ITO strip which allows two small electrical contacts to the strip through “vias” in the oxide. Taken together,

these should aid the development of improved routing fabrics in optical communication networks, reconfigurable logic gates in optical information processing, and spectrometer-on-a-chip [25] applications in optical sensing.

The paper is organized as follows. In the background discussion of Section II, the prior art is discussed in the context of the present work. Performance analysis is performed in Section III, where several parametric simulations are performed for 1×2 and 2×2 switches based on $\text{Ge}_2\text{Sb}_2\text{Se}_4\text{Te}_1$ on SOI. Also, detailed analysis is presented in order to demonstrate the feasibility of realizing low-IL broadband optical switches with BW in the 58 to 90 nm range. Thermal simulations are performed to demonstrate that the device state can be changed by means of applying voltage pulses along the ITO strip layer atop the $\text{Ge}_2\text{Sb}_2\text{Se}_4\text{Te}_1$ active region. Due to its non-volatile nature, $\text{Ge}_2\text{Sb}_2\text{Se}_4\text{Te}_1$ consumes energy only during the phase transformation. As illustrated below, a 5 V pulse train applied to the ITO induces crystallization, whereas a 24 V pulses of 2.9 μs and 2.3 μs duration are suitable for the re-amorphization of the 2×2 and 1×2 switches. Finally, the conclusions are summarized in Section IV.

II. BACKGROUND DISCUSSION

Recent papers based on PCM materials [8-13] provide a good basis for the present work because they showed some high merit figures for 2×2 and 1×2 switches. The most commonly O-PCM used is $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST-225). In a recent work [10], the authors demonstrated that, by exploiting an asymmetric directional coupler design, the GST-clad silicon photonic 1×2 and 2×2 switches present low insertion loss of ~ 1 dB, a compact coupling length of $\sim 30 \mu\text{m}$, and crosstalk less than -10 dB over a bandwidth of 30 nm. The design of a compact 1×1 optical on-off modulator based on a GST-clad silicon rib waveguide has been reported in [13], where a 2-5 μm long device with an extinction ratio of more than 20 dB and total insertion loss (IL) of 0.36 dB has been obtained using the GST-clad silicon rib waveguide with a 500-nm-wide silicon core, a 60-90 nm thick silicon slab, and a 15-25 nm thick GST layer.

In both cases, the authors implicitly assumed the laser heating as the main approach to induce the phase change, since a heater is not shown in the waveguide cross section and an air cover is assumed. The issue there is the difficulty of using this “all-optical” approach in attaining $N \times N$ matrix switching.

A third paper changes device state by injecting voltage pulses into the active region of the waveguide through the indium tin oxide (ITO) electrodes deposited on top of the active region [12]. In this case the authors demonstrated that a 1×1 modulator of only 920 nm in active length can exhibit high extinction ratio of 34.04 dB with IL of 0.49 dB in the On state. Similarly, they showed that the 1×2 GST-225 directional coupler switch has an extinction ratio of 18.59 dB with insertion loss of 1.90 dB for the cross state, which however is not a competitive value when integrated in large matrices. The IL is linked to the large optical “extinction” in the crystalline state of the GST material.

Reference [8] proposes a solution where the new low loss O-PCM $\text{Ge}_2\text{Sb}_2\text{Se}_4\text{Te}_1$ (GSST) is used instead of GST due to its larger figure of merit. The work explored the feasibility of obtaining very high performances for both switches 1×2 (IL of

0.4 dB and a CT of over -50 dB for the Cr state, and an IL as low as 0.06 dB and a CT of -27 dB in the Am state) and 2×2 (IL for the cross and bar states are 0.013 and 0.32 dB, and the CT for the two states are -37 and -32 dB, respectively). Their switch architecture was two- and three-waveguide directional couplers on the SiN platform where the phase change is optically induced. As mentioned above, we have adapted the approach to GSST-SOI with ITO-Joule PCM-contacted micro-heaters.

III. NUMERICAL RESULTS

The goal of this section is to present design rules for broadband switches based on $\text{Ge}_2\text{Sb}_2\text{Se}_4\text{Te}_1$ integrated on the SOI platform, in which the GSST phase change is induced by an overlaid ITO Joule heater. The optical properties of this ITO are taken into account in our model. We propose parametric simulations to evaluate the IL, CT, and BW in order to optimize the switching performances. Then, the thermal simulations are performed in order to estimate the voltage features needed to induce the phase change.

A. Optical Simulations

The architectures of both 1×2 and 2×2 switches are illustrated in Fig. 1(a) and (b), where the basic design parameters are indicated. The relevant cross sections are sketched in Fig. 2(a) and (b), where $W_L \times H_L$ and $W \times H$ represent the sizes of the passive (without PCM-clad) and active (with O-PCM-clad) SOI waveguides, respectively. Not shown in Fig. 2 are the two sub-micron “vias” in the top SiO_2 where tiny metallic contacts are made to the ITO, and where metal contact pads are available at the top surface of the SiO_2 at via locations.

In the coupling sections, the separations between adjacent waveguides is G and the PCM active length is designed to be equal to the coupling length (L_c).

Regarding the second waveguide in the 1×2 of Figure 1(a), the waveguide cross section within the coupling zone is generally different from the single-mode cross section of the first waveguide. Then, in order to construct a higher-order switching network from a group of 1×2 devices, it is necessary to join adjacent 1×2 devices smoothly from the output of the first to input of the next, so as to minimize excess insertion loss of the optical-series connection. Therefore, it is necessary for the coupling cross-section of the second waveguide to “revert” to the single-mode dimensions $W_L \times H_L$ in the fanned-out output section of the second waveguide. This means that the WG#2 output segment shall be tapered in both its X and Y cross-section dimensions to reach the desired $W_L \times H_L$.

The working principle of both the devices is the following. When GSST is amorphous, the optical waveguides are designed in order to induce the complete power transfer between the input waveguide (WG#1) and the Cross port (WG#2 or WG#3 for 1×2 and 2×2 switches, respectively).

On the other hand, when the GSST film is crystallized, input light is transferred to the Bar port with a low IL if the power exchange between input and O-PCM waveguides is minimized. As a result, a strong phase mismatch between those two waveguides is required. The GSST strip guarantees large phase detuning and good performance because the optical guided

mode becomes “bunched” in the O-PCM layer. The induced losses in GSST/Si are lower than those for the comparable GST/Si case because the extinction coefficient is lower in GSST, as shown in Fig. 3 where the real part of the refractive index (n) and the extinction coefficient (k) are plotted versus the wavelength according to the measurements presented in [26].

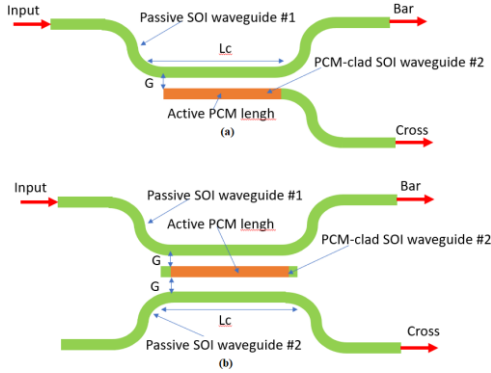


Fig. 1. Switching architecture: (a) 1x2 switch (2WG-coupler); (b) 2x2 switch (3WG-coupler).

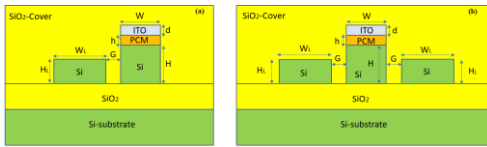


Fig. 2. Device cross section within the coupling region: (a) 1x2 switch; (b) 2x2 switch.

Thus, the PCM concentration of the optical electric field is clearly shown in Fig. 4, where the Poynting vector for the fundamental quasi-TE mode is plotted for both amorphous and crystalline phases in the WGs of Fig. 1.

In the following analysis, we include the wavelength dispersion of material complex index by considering the Sellmeier equations for both silicon and silicon dioxide, the Drude Lorentz model for ITO [27] and the GSST measurements given in [26] (see Fig. 3). Moreover, all simulations are performed using a full-vectorial mathematical model based on the finite element method (FEM) and vectorial coupled mode theory (CMT) approaches (see Ref. [28] for details). Although the two-dimensional (2D) and three-dimensional (3D) beam propagation methods (BPM) as well as the finite-difference time-domain (FDTD) method allow us to determine the overall device operation by means of the numerical solution of Maxwell’s equations in a discrete computational domain, these approaches are well known to be time- and memory-consuming. As a result, they are not suitable for any systematic design tool or for investigation of fabrication tolerances, where

a large number of parametric simulations are needed. Thus, the implementation of the full vectorial CMT and FEM can provide a good approach for parametric simulating the operation of DCs. Indeed, the flexibility and robustness of this general modelling approach has been already demonstrated in [28] where several directional coupling configurations have been simulated and compared with numerical results obtained with the three-dimensional commercial software. However, the FDTD approach can be more suitable for highly complex systems.

With the aim of finding the design trends, several parametric simulations have been carried out, analyzing first the 2x2 switch. In this sense, the 3WG-coupler behaviour can be explained in terms of supermodes. Under this approach, the column vector representing the amplitudes of the transverse field distribution in each waveguide is given by:

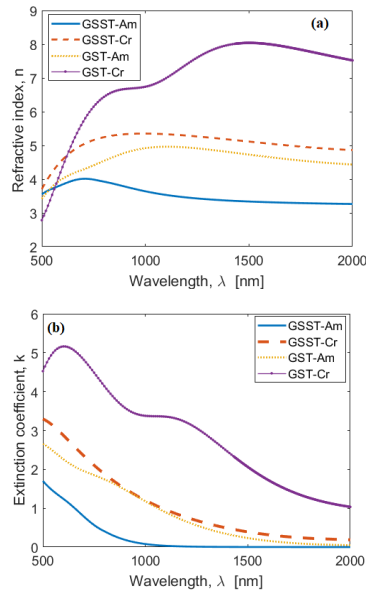


Fig. 3. (a) Spectrum of real part of the refractive index of both GSST and GST in Am and Cr phases, respectively; (b) Spectrum of extinction coefficient of both GSST and GST in Am and Cr phases, respectively

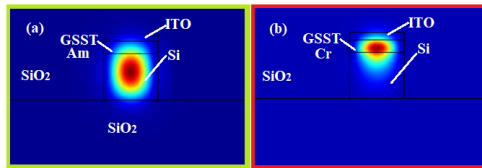


Fig. 4. Spatial distribution of Poynting vector for the fundamental quasi-TE mode: (a) GSST in Am-phase; (b) GSST in Cr-phase.

$$\begin{pmatrix} 1/\sqrt{2} \\ 0 \\ -1/\sqrt{2} \end{pmatrix}; \begin{pmatrix} a/\sqrt{2} \\ b \\ a/\sqrt{2} \end{pmatrix}; \begin{pmatrix} b/\sqrt{2} \\ -a \\ b/\sqrt{2} \end{pmatrix} \quad (1)$$

where $a^2 + b^2 = 1$.

It is possible to demonstrate that when the relationship $a = b = 1/\sqrt{2}$ holds, then the propagation constants of the three supermodes are evenly spaced.

In this sense, by setting the GSST in its Am-phase, we can assume this condition in order to allow complete power transfer from waveguide 1 to waveguide 3. As a result, the coupling length (L_c) can be estimated as:

$$L_c = \frac{2\pi L_{c0}}{\sqrt{(\Delta\beta(Am)L_{c0})^2 + 2\pi^2 - |\Delta\beta(Am)|L_{c0}}} \quad (2)$$

where $L_{c0} = \pi/(2|K_{12}|)$. The coefficient $\Delta\beta(Am) = \beta_2 - \beta_1$ is the propagation constant difference between the waveguides 1 and 2 (see Figs. 1(a) and (b)) in the absence of coupling between them and with the O-PCM in the Am-phase. The term K_{12} represents the coupling coefficient between waveguide 1 and 2 evaluated by means of the overlap integral of the vectorial electric fields.

In the following parametric investigations, a semi-standard SOI cross section of $W_L \times H_L = 500 \text{ nm} \times 220 \text{ nm}$ for passive waveguides is considered. However, for completeness, simulations for the case $W_L \times H_L = 500 \text{ nm} \times 250 \text{ nm}$ have been also carried out.

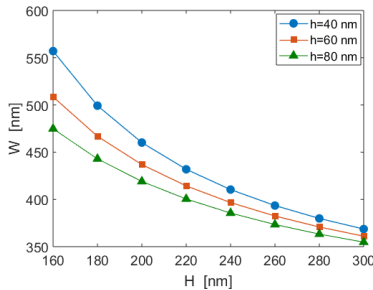


Fig. 5. Locii of the points in the plane spanned by H and W for which complete power transfer in the 2×2 optical switch occurs. GSST is in the Am-phase.

Using O-PCM thickness h as a parameter, Figure 5 shows the locii of the points in the plane spanned by H and W for which complete power transfer between waveguides #1 and #3 occurs when operating at 1550 nm.

Next, we examine the operation of our 2×2 switch operating at 1550 nm based on the Joule heating effect.

The insertion loss in Cross and Bar states for different values of the GSST layer thickness (h) are plotted in Fig. 6 as a function of the coupler gap (G). Moreover, according to the plot of Fig. 5, the central waveguide is adjusted to have $W \times H = 368.6 \text{ nm} \times 300 \text{ nm}$, $361.1 \text{ nm} \times 300 \text{ nm}$, and $354.7 \text{ nm} \times 300$

nm for $h = 40, 60, \text{ and } 80 \text{ nm}$, respectively. In the simulations, we have assumed the ITO layer thickness $d = 50 \text{ nm}$, with a free carrier concentration of $1 \times 10^{19} \text{ cm}^{-3}$, and refractive index $n(\text{ITO}) + i \times k(\text{ITO}) = 1.9615 + 0.00559i$ [27]. Moreover, according to [26] the GSST complex refractive index has been assumed as $n(\text{Am-GSST}) + i \times k(\text{Am-GSST}) = 3.3258 + 1.8 \times 10^{-4}$ and $n(\text{Cr-GSST}) + i \times k(\text{Cr-GSST}) = 5.0830 + 0.350i$, for the amorphous and crystalline phases, respectively. The loss in the amorphous phase has been extracted from waveguide cut-back measurements.

The plot indicates that for a given O-PCM thickness the IL is an increasing (decreasing) function of G for the Cross (Bar) state. Moreover, a specific value of the gap (named G_0) exists for which $\text{IL}(\text{Cross}) = \text{IL}(\text{Bar})$. Parametric simulations indicate that the value of G_0 increases by decreasing h for a fixed values of H . In addition, smaller values of G_0 are achieved by decreasing H for a given value of the GSST thickness (see the curve with asterisk markers, included for comparison reasons). Thus, the G_0 individuates two regions: $G < G_0$ and $G > G_0$, where the limiting factor is represented by $\text{IL}(\text{Bar})$ and $\text{IL}(\text{Cross})$, respectively. The data of Fig. 6 record values of G_0 ranging from 103 nm to 243.9 nm by reducing h from 80 nm to 40 nm. Under these conditions, the coupling length and the insertion loss ($\text{IL}(\text{Bar}) = \text{IL}(\text{Cross})$) range from $15.40 \mu\text{m}$ and from -0.077 dB to -0.0197 dB , respectively.

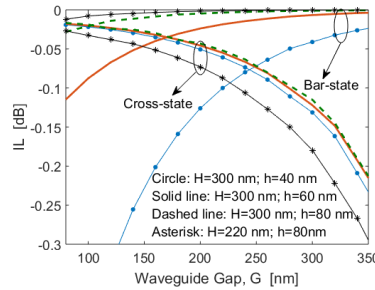


Fig. 6. Insertion loss as a function of the gap, for different values of h , in the case of 2×2 optical switch.

Let us now examine the influence of H changes on the switch performances. In this context, Fig. 7 shows the coupling length and the $\text{IL}(\text{Cross})$ as a function of the H parameter for a fixed waveguide gap, and assuming $h = 80 \text{ nm}$. In particular we have adopted $G = 103 \text{ nm}$, corresponding to the G_0 value for $H = 300 \text{ nm}$.

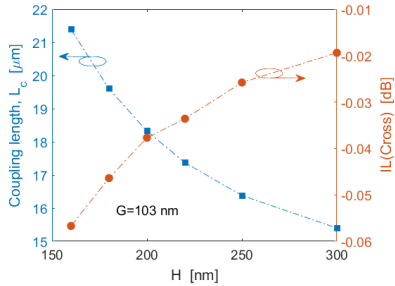


Fig. 7. Coupling length and insertion loss as a function of the H parameter, for the 2×2 optical switch. In the simulations, $G=103$ nm, and $h=80$ nm.

The plot of Fig. 7 indicates that the coupling length decreases while increasing the values of H , resulting in an improvement of the device footprint. However, the opposite trend is recorded for the $IL(Cross)$. Moreover, the increasing of H induces a reduction of the bandwidth (BW) as shown in Fig. 8, where the IL as a wavelength function is illustrated for different values of the H parameter, assuming $h = 80$ nm and $G = 103$ nm.

Although the simulations have been carried out in the wavelength range from 1500 nm to 1600 nm, the curves are plotted in a smaller wavelength range in order to better evidence the IL values above -0.3 dB (this -0.3 dB limit is used to define the switch BW in this paper). Similarly, Fig. 9 shows the relevant CT figure of merit.

The results of the parametric simulations are summarized in Table I, where other cases of interest (i.e. $W_L \times H_L = 500$ nm \times 250 nm, $G = 80$ nm, $H = 160$ nm) are included (not explicitly

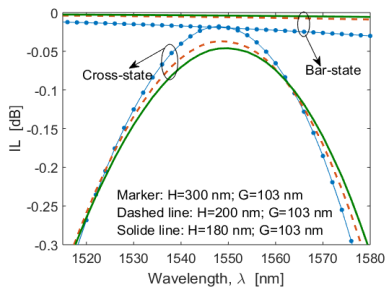


Fig. 8. Insertion loss for both Cross and Bar states as a function of the wavelength for different values of the H parameter, in the case of the 2×2 optical switch. In the simulation, $G=103$ nm, and $h=80$ nm.

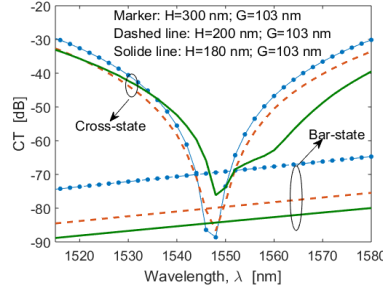


Fig. 9. Crosstalk for both Cross and Bar states as a function of the wavelength for different values of the H parameter, in the case of the 2×2 optical switch. In the simulation, $G=103$ nm, and $h=80$ nm.

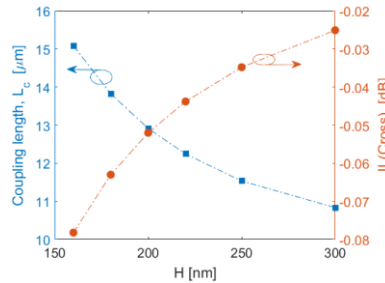


Fig. 10. Coupling length and insertion loss as a function of the H parameter, for the 1×2 optical switch. In the simulation, $G=103$ nm, and $h=80$ nm.

plotted in the figures for clarity). To the best of our knowledge, the values listed in Table I represent an important improvement of the performance for non-volatile optical switches with respect to the values proposed in literature. The IL listed in the Table is the mid-band value and the Cross state is chosen because it, rather than the Bar state, limits the performance.

It is worth outlining that only the second row case in Table I satisfies the condition $IL(Cross)=IL(Bar)$. All other considered cases could require G values smaller than 80 nm. The plot of Fig. 8 and the results summarized in Table I demonstrate, as a general trend, that the switch metrics and the bandwidth improve if the design rule $H < H_L$ is followed for a given value of G . As a result, a dual etching process must be implemented in order to fabricate switches with $H < H_L$, which is an available option in most industry-standard silicon photonic foundry processes. Although the complete power transfer in 2×2 switch occurs for the condition $H=H_L$ (as demonstrated by Fig. 5), here we accept the increasing of fabrication complexity induced by a dual etching process with the aim to demonstrate the feasibility to improve the switch metrics and bandwidth with respect to the state of art presented in literature. We note that such a dual etching process is now routinely offered in most silicon photonics foundries as part of the standard process design kit (PDK). On the other hand, if we adopt the constraint $H=H_L$ most straightforward for fabrication,

we could achieve similar levels of performance of those obtained with $H < H_L$ if a decrease of the gap between the waveguides is considered. Indeed, assuming $W_L \times H_L = 500 \text{ nm} \times 220 \text{ nm}$, $h = 80 \text{ nm}$, $H = H_L$, and $G = 50 \text{ nm}$, we record $IL(\text{Cross}) = -0.06 \text{ dB}$, $IL(\text{Bar}) = -2.2 \times 10^{-3} \text{ dB}$ at 1550 nm , $BW = 72.58 \text{ nm}$ and $CT < -38.6 \text{ dB}$. In this sense, it seems more efficient to adopt the condition $H < H_L$ instead of to reduce the gap below 50 nm .

Similar systematic investigations have been performed for the 1×2 optical switch, based on the 2WG -coupler. The numerical results are condensed in Figs. 10 and 11, and lead to the same conclusions made for the 2×2 optical switch, although several comments about the switching performances are worth mentioning. In order to compare self-consistently both 1×2 and 2×2 optical switches, we keep fixed the cross section of the passive waveguide and the gap value between adjacent waveguides. In this context, Fig. 10 shows the coupling length and the $IL(\text{Cross})$ as a function of the H parameter, assuming $W_L \times H_L = 500 \text{ nm} \times 220 \text{ nm}$, $h = 80 \text{ nm}$, and $G = 103 \text{ nm}$. The plot evidences that, by comparing 1×2 and 2×2 switches, the 2WG -coupler achieves shorter values of the coupling length, despite its slightly larger insertion losses.

In Fig. 11 (a) and (b) $IL(\text{Cross})$ and CT of the 1×2 switch are plotted as a function of wavelength. The results for the 3WG -coupler are also included for comparison. In the simulations we have assumed: $W_L \times H_L = 500 \text{ nm} \times 250 \text{ nm}$, $H = 160 \text{ nm}$, $h = 80 \text{ nm}$, and $G = 80 \text{ nm}$. The values of L_c , $IL(\text{Cross})$ at 1550 nm , and BW are $16.7 \mu\text{m}$, -0.083 dB , and 95 nm , respectively. It is worth noting that the 2×2 architecture shows the values $23.63 \mu\text{m}$, -0.06 dB , and 72.6 nm , respectively. Although the 1×2 switch presents a 22.4-nm larger bandwidth, this improvement is accompanied by a strong increase of crosstalk. The 2WG -coupler data show that, inside the bandwidth, the CT values range from -12.83 dB to -45.52 dB in the Cross state and from -47.96 dB to -52.79 dB in the Bar state. Better results are obtained for the 2×2 switch, where CT values changing from -33.84 dB to -82.11 dB in the Cross state and from -92 dB to -87.9 dB in the Bar state.

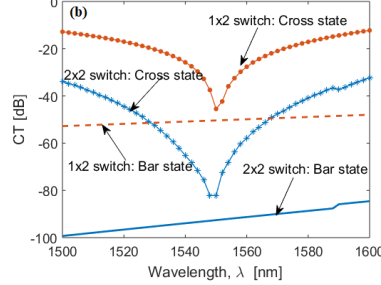
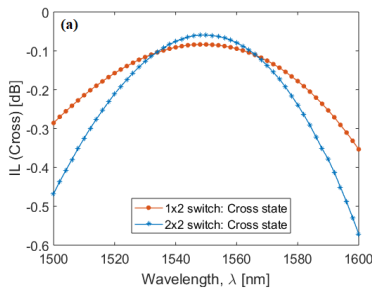


Fig. 11. (a) Insertion loss for both Cross states as a function of the wavelength; (b) Crosstalk for both Cross and Bar states as a function of the wavelength.

TABLE I
GEOMETRICAL AND SWITCHING PARAMETERS OF THE 2×2 SWITCH

	Switching parameters				
	W [nm]	L_c [μm]	BW [nm]	$IL(\text{Cross})$ (1.55 μm) [dB]	CT [dB]
$W_L \times H_L = 500 \text{ nm} \times 250 \text{ nm}$; $H = 200 \text{ nm}$; $G = 103 \text{ nm}$	465.14	23.98	65.44	-0.048	<- 36.5
$W_L \times H_L = 500 \text{ nm} \times 220 \text{ nm}$; $H = 300 \text{ nm}$; $G = 103 \text{ nm}$	354.75	15.40	58	-0.018	<- 31.3
$W_L \times H_L = 500 \text{ nm} \times 220 \text{ nm}$; $H = 200 \text{ nm}$; $G = 103 \text{ nm}$	419.02	18.32	60.72	-0.037	<- 34.4
$W_L \times H_L = 500 \text{ nm} \times 220 \text{ nm}$; $H = 180 \text{ nm}$; $G = 103 \text{ nm}$	442.9	19.60	61.78	-0.046	<- 34.6
$W_L \times H_L = 500 \text{ nm} \times 220 \text{ nm}$; $H = 200 \text{ nm}$; $G = 80 \text{ nm}$	419.02	14.94	66.94	-0.032	<- 33.5
$W_L \times H_L = 500 \text{ nm} \times 220 \text{ nm}$; $H = 160 \text{ nm}$; $G = 80 \text{ nm}$	474.79	17.43	70	-0.046	<- 38.13

B. Thermal Simulations

In this sub-section we investigate the feasibility of inducing the phase change in GSST by means of Joule heating using an ITO electrode. In this context, we describe the amorphization mechanism by FEM models in COMSOL [29], using the 3WG -coupler designed in the previous section, in which an 80 nm GSST layer is deposited on an SOI strip waveguide having a cross section $W \times H = 474.79 \text{ nm} \times 160 \text{ nm}$ and $W_L \times H_L = 500 \text{ nm} \times 220 \text{ nm}$. Moreover, a 50 nm layer of ITO is used to induce Joule heating, and the gap between the adjacent waveguides is set to 80 nm . In order to perform realistic thermal simulations, we have adopted a finite SiO_2 cover thickness, assumed to be reasonably of realistically 500 nm thick over the waveguide. The switching to the amorphous state can be achieved by means of a voltage pulse with enough energy and trailing edge in the $0.5\text{-}5 \text{ ns}$ range to rapidly melt-quench the GSST, thus favoring a disordered state [11]. As well detailed in [11], if P_{min} is the minimum pulse power able to amorphize the PCM, then, any pump pulse with fixed width and power $P_p \geq P_{min}$ is able to induce amorphization, starting from the condition of the crystalline phase.

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It is worth mentioning that under the approach presented in this work, the voltage pulse width and the electric pulse power are related to the electric conductivity of the ITO layer. A realistic value of the electrical resistivity for ITO with free carrier concentration of about $1 \times 10^{19} \text{ cm}^{-3}$ can be estimated as $\rho=0.0016 \Omega \times \text{cm}$, according to the experimental measurements presented in [30]. To consider the time evolution of the temperature upon pulse excitation, we performed 3D multiphysics simulations where the heat transfer in solids model is coupled together with the electric currents model. The time dependent study is, thus, adopted to solve the coupled thermal and electric equations under the rectangle pulse voltage excitation. The input voltage pulse is $3 \mu\text{s}$ wide, centred at $2.5 \mu\text{s}$ (rise time of 0.5 ns , see Fig. 12). The design is therefore compatible with GSST switching given the improved Am phase stability of GSST [26]. ~~To the best of our knowledge the thermal parameters of GSST are not listed available in literature.~~ Given the structural similarity between GSST and the classical GST alloy [26], so we use the GST values as a good approximation to evaluate the switching features characteristics. The material properties used in the simulations are summarized in Table II. Our results demonstrate that the process of amorphization can be obtained with a 24 V pulse, raising the GSST temperature above the melting temperature of 900 K. The energy consumed during the process is estimated as 146.970 nJ.

TABLE II
PHYSICAL PARAMETERS OF THERMAL SIMULATION

	<i>Materials</i>				
	<i>Silicon dioxide</i>	<i>Silicon</i>	<i>Am-GSST</i>	<i>Cr-GSST</i>	<i>ITO</i>
<i>Density [kg/m³]</i>	2203	2329	~6000 [11]	6150 [12]=6300 [11]	7100 [11]
<i>Thermal conductivity [W/mK]</i>	1.38	130	~0.57 [31]	~1.58 [31]	~1340 [11]
<i>Heat capacity at constant pression [J/kgK]</i>	746	700	212 [32]	212 [32]	11 [11]

Fig. 12 shows the maximum temperature (T_{max}) inside the O-PCM layer as a time function under rectangular voltage pulse excitation.

Spatial temperature distribution for the process of amorphization is shown in Fig. 13 (a), where the plane cross section placed in the middle of the O-PCM length ($L_c = 17.4 \mu\text{m}$) has been considered. Moreover, the temperature levels along the longitudinal axis of the O-PCM waveguide at both the bottom and the top surfaces of GSST layer are illustrated in Fig. 13 (b). The plot indicates clearly that the amorphization process starts to take place on the top and the middle of the GSST layer, where the temperature first reaches the melting value. Moreover, the simulations of Fig. 13 indicate that complete amorphization can be induced over the entire $L_c = 17.4 \mu\text{m}$ for the considered voltage pulse.

Similar investigations have been performed for the 1×2 switch having: $W \times H = 541.92 \text{ nm} \times 160 \text{ nm}$, $h = 80 \text{ nm}$, $G = 103 \text{ nm}$, and $W_L \times H_L = 500 \text{ nm} \times 250 \text{ nm}$. The results are plotted in Figs. 14 (a) and (b).

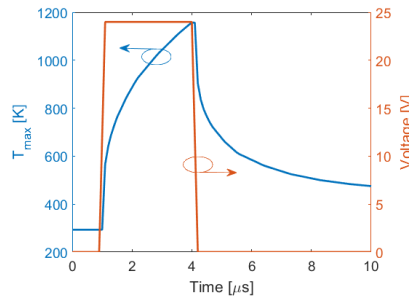


Fig. 12. Maximum temperature in the O-PCM layer as a function of time for rectangular pulse heating.

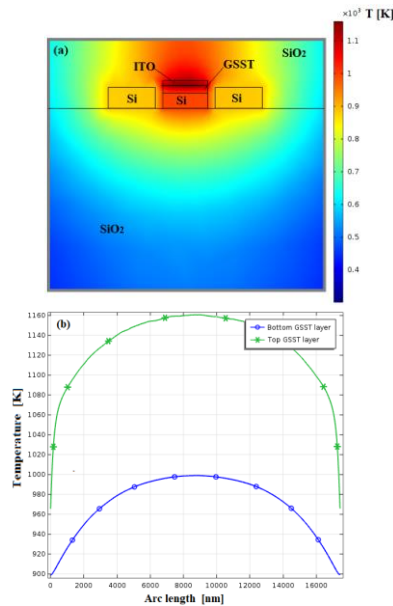


Fig. 13. (a) Temperature distribution in the plane cross section placed at the middle of the O-PCM length in the case of 2×2 optical switch. (b) Temperature profile as a function of the longitudinal coordinate at the top and bottom O-PCM layer su

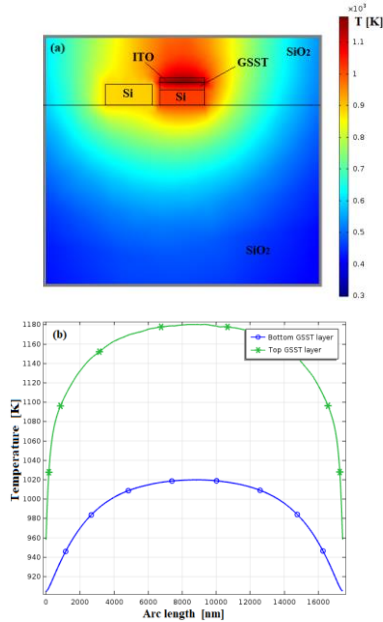


Fig. 14. (a) Thermal distribution in the plane cross section placed at the middle of the O-PCM length in the case of 1×2 optical switch. (b) Temperature profile as a function of the longitudinal coordinate at the top and bottom O-PCM layer surface.

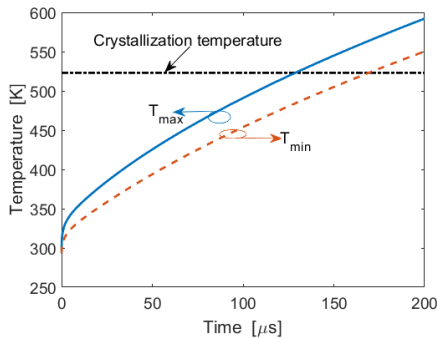


Fig. 15. Maximum and minimum temperature in the O-PCM layer as function of time for pulse-train heating.

It is worth noting that here a 24 V pulse of 2.5 μs duration is required to induce the complete amorphization, as a result of the different material distribution. The energy consumed during the process is estimated as 122.485 nJ.

To induce re-crystallization, the GSST needs to be heated above the crystallization temperature (~ 523 K) but below the melting point, for a critical amount of time. Although the operative temperature is lower than the melting temperature, this process is demonstrated to be more challenging. Indeed, while a single

pulse is needed to induce the transition from crystalline to amorphous phase, several pulses are required for crystallization [26]. In this sense, we apply a pulse train consisting of 20 pulses with a period of 4 μs and duty cycle of 50% at 5 V. The energy consumed corresponding to the applied voltage is 425.586 nJ. Thus, the maximum and the minimum temperature inside the O-PCM layer is recorded as a time function. The results are illustrated in Fig. 15, demonstrating that low energy consumption is required to induce the change from amorphous to crystalline phase. Regarding the 24 V pulse amplitude that induces amorphization (starting from Cr), there is a way to improve the switching performance significantly, i.e. by increasing the ITO doping of to the order of 10^{20} cm^{-3} . Indeed, assuming the an ITO resistivity $\rho=4 \times 10^{-4}$ $\Omega \times \text{cm}$ (for carrier concentration around 2×10^{20} cm^{-3} [27]), our simulations record that the complete amorphization can be obtained with a voltage pulse of 24 V and 0.15 μs wide width or alternatively by means of a 12 V pulse having a duration of 2.9 μs . However, optical simulations indicate that for the ITO carrier concentration of 10^{20} cm^{-3} , IL(Cross) is larger than 0.37 dB for $G > 80$ nm. Thus, the best trade-off between conflicting requirements such as switching performance and low IL, can be achieved under the hypothesis of designing a single switch. However, here we propose the design of the O-PCM switches under the perspective of realize-realizing a large-scale on-chip matrix switch, such as a Benes network. In this sense to preserve low IL, we elected not to pursue the high-doping strategy.

IV. CONCLUSIONS

In this paper, manufacturable on-chip nonvolatile broadband 1×2 and 2×2 switches are designed and analyzed theoretically. The switches consists of asymmetric two-waveguide and symmetric three-waveguide couplers in which the Cross or the Bar state is induced by setting the O-PCM in the amorphous or the crystalline phase, respectively. In each switch, the O-PCM is $\text{Ge}_2\text{Sb}_2\text{Se}_4\text{Te}_1$ deposited as top-cladding on one of the coupled SOI strip waveguides. The photonics platform assumed in this work is the foundry-compatible and CMOS-compatible SOI platform operating in the telecommunication C-band. The passive waveguide are assumed to have a cross section of $W_L \times H_L = 500 \text{ nm} \times 220 \text{ nm}$ or $W_L \times H_L = 500 \text{ nm} \times 250 \text{ nm}$. The cross section of the active PCM have been chosen to satisfy the requirements of low insertion loss (less than 0.3 dB) over a large wavelength bandwidth, as a result of the parametric investigations. The O-PCM phase is changed by means of the ITO heater strip atop the O-PCM layer, inducing Joule effect as a result of applying voltage pulses.

The simulations have demonstrated the feasibility of obtaining O-PCM 2×2 switches with high performances across a large bandwidth ranging from 58 to 72 nm around 1550 nm. Moreover, all the devices have been designed to have the Cross state as limiting the switching performances. A representative example for the compact 15.4 μm coupling length is an IL(Cross) of -0.048 dB with CT lower than 38.1 dB over the 70-nm -0.3dB-IL bandwidth. The 1×2 architecture is even more compact, for which the coupling length changes from 11 μm to 16.7 μm . Regarding the switching condition, we find that a 24 V pulse of 2.9 μs (2×2 switch) and 2.3 μs (1×2 switch) in duration is required to raise the GSST temperature above the

melting temperature of 900 K in order to induce the amorphization process. Moreover, thermal simulations indicate that complete amorphization occurs over the entire O-PCM length. Complete crystallization is also possible by applying a pulse train of 20 or more pulses with a period of 4 μ s and duty cycle of 50% at 5 V. This work represents an important improvement with respect to the performances of ultra-compact and non-volatile electro-optical switches reported in the literature.

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