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***Abstract*—Applications such as plasma generation require the generation and delivery of radio-frequency (rf) power into widely-varying loads while simultaneously demanding high accuracy and speed in controlling the output power across a wide range of power levels. Attaining high efficiency and performance across all operating conditions while meeting these system requirements is challenging, especially at high frequencies (10s of MHz) and power levels (1000s of Watts and above). This paper evaluates different architectures that directly address these challenges and enable efficient high-frequency operation over a wide range of output power levels and load impedances with the capability of fast output power control (e.g., within a few microseconds). We review techniques for achieving fast output power control and evaluate their suitability in efficient rf systems demanding accurate and fast control of output power. Two dc-to-rf system architectures utilizing the discussed power control techniques are presented to illustrate both the achievable performance benefits as well as their robustness to load impedance variation, and are compared using time-domain simulations. The results indicate the ability of the proposed architectures to maintain high efficiency ($>90\%$) across a very wide range of output power levels (e.g., over a factor of up to 85x) while being robust to load impedance variations.**

***Index Terms*—RF power generation, RF architectures, variable load impedance, output power control, impedance matching**

I. Introduction

In applications such as plasma generation in semiconductor manufacturing, high frequency (HF, 3-30 MHz) inverters (or power amplifiers) are used to generate and deliver a desired output power at a fixed or narrowband operating frequency. Plasma generation for semiconductor processing in particular imposes challenging requirements on the HF inverter systems, including the ability to accurately and rapidly adjust the output power (e.g., within a few microseconds), deliver the desired output power to a wide load impedance range, and maintain high efficiency and performance across a wide range of power levels and operating conditions [1], [2]. Attaining high efficiency over a very wide range of power levels is challenging since, depending on the power control scheme, the losses generally do not back off proportionately to the output power. In addition, the performance of many high-frequency (HF, 3-30 MHz) switched-mode power amplifiers or inverters degrades quickly with variations in load impedance (e.g., [3], [4]). This performance degradation can be reflected in a substantial loss of efficiency with load variations (e.g., owing to loss of zero-voltage switching (ZVS)), an inability to deliver a rated power as load changes, or both. Common ways of addressing this include utilizing tunable matching networks (TMNs) between the inverter and load to dynamically-transform the variable load into a fixed impedance seen by the inverter or power amplifier [5]–[7], but often come at the expense of increased size, cost, complexity, or limited response times. Other solutions utilize variable-load inverters (e.g., class D or E [4], [8]) that can maintain ZVS with variable resistive/inductive loading and thus extend high efficiency operation to a wider load range; however, these solutions alone can be effective only over a limited range of power levels.

This paper provides a detailed overview of power control techniques in high power HF power amplifier/inverter systems and assesses their suitability in applications demanding high-bandwidth power control at high efficiency. Section II illustrates a generalized rf system architecture, and Section III evaluates techniques for output power control. Section IV assesses the usefulness of these techniques in two dc-to-rf architectures for high efficiency operation across a very wide power range, and presents simulation results affirming the achievable performance benefits and indicating robustness to load impedance variations. Finally, Section V concludes the paper.

II. Generalized RF System Architecture

Fig. 1 shows a generalized architecture of an rf power system driving a dynamically-varying load. This architecture captures the key subsystems present in such an rf system considering a general form that would be effective for the stated goals. This architecture includes an inverter/power amplifier subsystem that generates rf power according to a set of control

inputs (e.g., gate drive amplitude and phase signals, supply voltage level, etc.). It also includes a power supply subsystem which provides the dc supply voltages required by the power amplifier subsystem, a control subsystem to command the required supply voltages as well as gate drive signals for the inverters, a power combiner subsystem to combine the power from the (possibly) multiple inverters, and an impedance transformation subsystem to scale and/or compress the load impedance range into one that results in impedances suitable for driving by the inverter(s). In addition, a measurement and monitoring subsystem provides feedback information from the various subsystems to the control subsystem, so that appropriate command signals are generated.

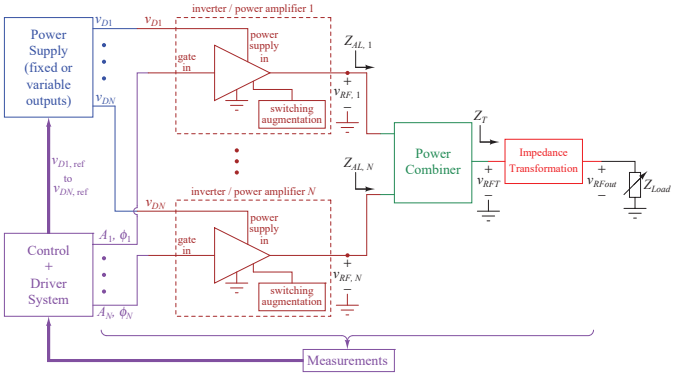

Fig. 1. Generalized rf system architecture for an efficient high-frequency, wide power range, and wide load range power amplifier.

This general architecture and its subsystems realize two primary system functions: (a) rapidly and accurately controlling the power delivered to the load; and (b) managing the rapidly and widely-varying load range such that the performance of the power amplifier subsystem is not compromised. There are several ways these two system functions can be achieved. The next section evaluates the suitability of common power control techniques in realizing efficient rf systems demanding accurate and fast control of output power. For purposes of this paper we assume that a separate impedance transformation system is able to compress the operating load impedance range to an acceptable level, e.g., $\pm 20\%$ in resistive and reactive impedance from a nominal load resistance.

III. Techniques for Output Power Control

A major function of most dc-to-rf power systems is the ability to accurately and rapidly control the power delivered to a load. For high efficiency operation at HF, it is desirable for the inverter/power amplifier subsystem in Fig. 1 to comprise inverters capable of achieving ZVS transitions of the transistors across a wide range of operating conditions. For example, one such inverter can be a class D or DE inverter [9], [10] having either a matching network, or an inductive pre-load network as implemented in the (L_{zvs}, C_{dc}) branch of Fig. 2 [8], such that soft switching can be achieved with a variable resistive/inductive load. Other variable-load single-switch inverters such as class E or class ϕ_2 inverters (e.g., [4]) can also be used, though the variable-load class D inverter has a relatively superior switch utilization [11], so may be preferred at frequencies and voltage levels at which its high-side device can be effectively driven.

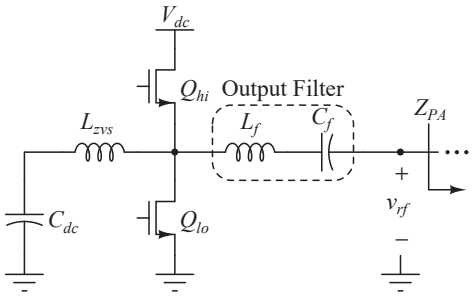

Fig. 2. HF variable-load class D inverter cell driving an effective impedance Z_{PA}. The (L_{zvs}, C_{dc}) branch provides inductive current necessary to achieve ZVS.

It is important to note that in many switched-mode inverters two dominant loss mechanisms that can limit achievable performance include switch conduction losses and output capacitor losses. Switch conduction losses arise from the on-state resistance of the switch including any dynamic on-state resistance effects [12], [13]. Switch C_{OSS} losses refer to the loss in charging/discharging of the transistors' output capacitance C_{OSS} (which is often slew-rate dependent and not well represented as ohmic conduction loss) [14]–[16]. (Such C_{OSS} losses are extremely important for HF operation in GaN devices and some Si devices, and are more modestly important in SiC devices.) These two loss mechanisms, respectively, can be expressed as follows:

$$P_{cond} = k_{cond} \cdot \frac{1}{A} \cdot (i_{rf} + i_{zvs})^2_{\text{rms}}, \quad (1)$$

$$P_{C_{OSS}} = k_{C_{OSS}} \cdot A \cdot f_{sw}^{\alpha} \cdot V_{dc}^{\beta}, \quad (2)$$

where P_{cond} and $P_{C_{OSS}}$ are the device conduction and C_{OSS} losses, respectively, k_{cond} is a constant proportional to the switch on-state resistance, $k_{C_{OSS}}$, α, and β are device- and/or waveform-specific constants [14], [16], A is the device area, i_{rf} is the load rf current, i_{zvs} is the inductive current through L_{zvs} necessary to achieve soft switching, f_{sw} is the switching frequency, and V_{dc} is the inverter supply voltage shown in Fig. 2. Using these quantities, and denoting output power by P_{out}, one can express the inverter efficiency η as follows (ignoring other losses such as owing to inductors and capacitors):

$$\eta = \frac{P_{out}}{P_{out} + P_{cond} + P_{C_{OSS}}}. \quad (3)$$

In the next two subsections, we use the inverter structure in Fig. 2 to discuss the suitability of common power control strategies in achieving rapid power control (e.g., within several microseconds) over a wide power range at HF, as desired in many plasma applications [1], and describe how the loss terms above and resulting efficiency are affected as the output power backs off.

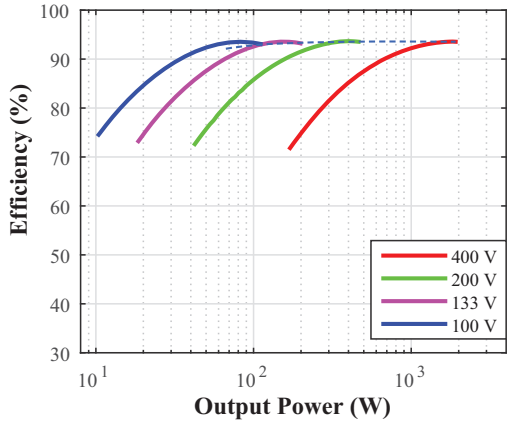

Fig. 3. Simulated efficiency vs. output power characteristic for drain modulation and load modulation for the inverter structure in Fig. 2 at 13.56 MHz using 2x Panasonic GaN devices, PGA26E07BA, L_{zvs} = 272 nH, C_{zvs} infinite (implemented as dc source at $V_{dc}/2$), L_f = 880 nH, C_f = 156 pF. Each solid curve corresponds to sweeping the inverter's output resistance by a factor of 10 (from 15 Ω to 150 Ω) at a fixed dc voltage. The dotted curve shows the efficiency for a fixed load resistance as dc voltage changes.

A. Supply Voltage Modulation

A widely used technique to control output power is by modulating the inverter supply voltage V_{dc} in Fig. 2 in a continuous or discrete manner. Techniques using continuous supply voltage modulation include envelope elimination and restoration (EER) and envelope tracking. The supply voltage is commonly adjusted using a dc-dc converter such that the inverter output rf voltage amplitude v_{rf} (see Fig. 2) is varied continuously as desired. A key challenge in using envelope tracking or EER is the constraint on the supply voltage range beyond which the inverter's performance starts to degrade (e.g., due to ZVS loss owing to the nonlinearity of the transistors' C_{OSS}). This problem can be alleviated by limiting operation to voltage ranges over which C_{OSS} remains somewhat constant, or by using devices whose C_{OSS} stays relatively constant over a wider voltage range (e.g., PGA26E07BA devices shown in Fig. 3). Another challenge associated with continuous drain modulation is the practical difficulty in realizing supply voltage modulators that have both high efficiency and very high bandwidths [17], [18].

Alternatively, one can utilize discrete drain modulation whereby a supply modulator simply switches the inverter's supply among multiple discrete levels [8], [19], [20]. This can be very effective since it removes the requirement for a very high bandwidth dc-dc supply modulator, yet enables extremely rapid adjustment of inverter supply voltages using a switching network to select one from among available dc voltage levels. However, this necessitates that each of these dc levels be individually available, resulting in additional hardware circuitry and complexity if too many discrete levels are desired. This scheme also necessarily requires another means of secondary control to allow continuous and seamless modulation of output power (e.g., using load modulation) [19]–[21].

To understand the effect of modulating supply voltage on the device losses and efficiency, consider the inverter in Fig. 2 when its supply voltage V_{dc} is reduced by a factor of k. Since the output voltage v_{rf} is simply the fundamental component of the switching node voltage, its peak voltage also reduces by a factor of k, resulting in a reduction of output power by a factor of k^2. Furthermore, both the ZVS inductor current i_{zvs} and the output current i_{rf} reduce by a factor of k, resulting in a reduction of conduction losses by a factor of k^2. By inspecting equation (2), we find that $P_{C_{OSS}}$ reduces by a factor k^β, resulting in the following efficiency relation (assuming a linear C_{OSS}):

$$\eta' = \frac{P_{out}}{P_{out} + P_{cond} + k^{(2-\beta)} P_{C_{OSS}}}. \tag{4}$$

where η' denotes the resulting efficiency when the supply voltage is reduced by a factor of k.

An important consequence of this is that if the device β parameter is close to 2, and if we ignore inductor losses, the efficiency remains almost unaffected as the output power backs off in operating voltage regimes where the device C_{OSS} remains relatively constant. Fortunately, it has been experimentally determined (e.g., [14]) that for several GaN devices β is generally between 1 and 2, and in some cases closer to 2. Thus, if an inverter is loaded with an impedance that maximizes efficiency at a given dc voltage, then this efficiency remains relatively unaffected as output power backs off via drain modulation. This makes drain modulation an attractive means of achieving output power control.

B. Load Modulation

Another means of controlling output power is by effectively modulating the load seen by the inverter (Z_{PA} in Fig. 2) [22], [23]. A common way of modulating the load seen by a switched-mode inverter is by outphasing [22], [24]–[26], whereby two or more inverters are phase-shifted with respect to each other and coupled to the load via a power combining network. By controlling the relative phase of the two (or more) inverters, the output load voltage (and thus power) can be controlled, as illustrated in Fig. 4. This can be a very effective means for controlling delivered power as it provides opportunity for continuous and high-bandwidth power control.

Key to attaining high efficiency with this structure is the choice of power amplifiers and the design of the combining network [24], [25], [27], [28]. For example, when the amplifiers in Fig. 4 are implemented as variable-load inverters (e.g., as in Fig. 2) and when an appropriate lossless combiner network is used (e.g., see Section IV), high-efficiency operation can be achieved across variable inverter loading by maintaining the ZVS transitions necessary for high efficiency inverter operation at HF.

While attractive, outphasing alone can enable high efficiency operation only over a limited output power range. One reason for this can be understood by considering the effect of modulating the load impedance on the device losses and efficiency. Consider the inverter in Fig. 2 when its effective load impedance Z_{PA} is increased by a factor of k^2. At a fixed

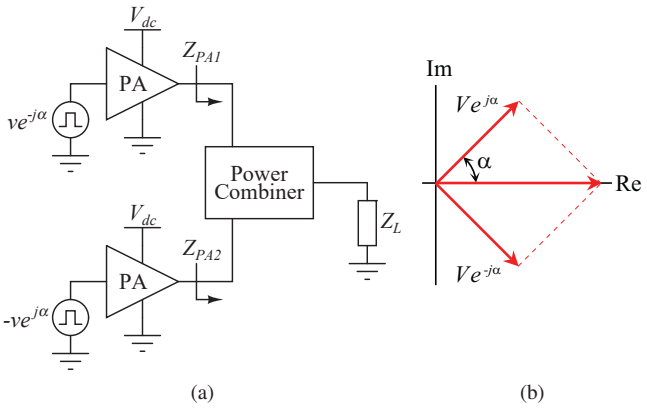

Fig. 4. Illustration showing load modulation by outphasing using two power amplifiers and a power combining network. Each amplifier can be a class D inverter as in Fig. 2.

supply voltage V_{dc}, the output voltage v_{rf} remains unchanged; as a result, both the output current i_{rf} and output power reduce by a factor of k^2. The ZVS current i_{zvs} and the C_{OSS} loss remain unchanged since they are both dependent on V_{dc}. The conduction loss changes by a factor $F(k)$ which depends on both the ZVS current (which is unchanged via load modulation) and the output current (which reduces by a factor of k^2). One can express $F(k)$ in terms of the ratio of ZVS current to output current, denoted here by $m \equiv i_{zvs}/i_{rf}$, using equation (1) as follows:

$$F(k) = \left(\frac{1 + mk^2}{k^2 + mk^2} \right)^2 . \tag{5}$$

This formulation allows one to express the efficiency resulting from load modulation as follows:

$$\eta' = \frac{P_{out}}{P_{out} + k^2 F(k) P_{cond} + k^2 P_{C_{OSS}}} . \tag{6}$$

To obtain insight from equation (6), one can consider the dependence of $k^2F(k)$ on k for values of m that are typical of variable-load inverters, somewhere between 0.75 and 3[1] [4], [29]. One can then notice that the quantity $k^2F(k)$ rapidly increases beyond 1 as k increases, resulting in rapid efficiency degradation as output power backs off. The equations reveal that not only does C_{OSS} loss remain unchanged as output power backs off, but also the device conduction loss does not back off proportionately to output power. Instead, the conduction loss backs off somewhat slower relative to output power due to the ZVS current being unaffected by load modulation. This effect can be clearly seen in the solid curves of Fig. 3, which show the efficiency of the variable-load inverter as the loading impedance Z_{PA} seen at its output varies (in this case a resistor at the inverter output is stepped from 15 Ω to 150 Ω). The advantages of outphasing, including the ability to continuously and rapidly control power, can be leveraged by combining it with drain modulation to realize architectures capable of high-bandwidth power control over a much wider power range, as discussed in Section IV.

[1]These typical values of m result from the fact that the current through L_{zvs} required to achieve ZVS for variable loads is often in the vicinity of or greater than the maximum load current.

C. Structural Modulation

A third means for achieving output power control is through structural modulation, whereby the structure of the dc-to-rf system is dynamically adjusted, effectively changing the output power. This can be achieved by utilizing dynamically adjustable networks (e.g., a TMN) to dynamically change the loading of the inverters (e.g., [5], [30]). Alternatively, the system can utilize dynamic interactions between a number of inverters to achieve output power control while maintaining acceptable inverter loading for high efficiency operation [11], [31]. A further possible approach is to turn on and off individual inverter or power amplifier subsystems to cause load modulation of active units (and reduce power loss otherwise associated with inactive units), e.g., [32]. In essence, structural modulation often utilizes combinations of supply modulation and load modulation in a dynamic fashion to achieve power control over a desired operating power range. An architecture utilizing this power control scheme using switched-mode amplifiers with the capability of high-bandwidth power control over a wide power range is illustrated in Section IV.

IV. Variable-Load High Efficiency dc-to-rf System Architectures

By combining appropriate power control schemes with a suitable impedance transformation network/TMN, one can realize high performance dc-to-rf architectures capable of driving a very wide load impedance range and operate over wide power levels. In this context, the primary purpose of a TMN block is to present an impedance that is suitable for the inverter and power combining system (e.g., Z_L in Fig. 4(a)); several such suitable TMNs have been reported in the literature [6], [7], [33]–[36]. The next two subsections outline two dc-to-rf architectures demonstrating the usefulness of multiple power control schemes in achieving fast and efficient wide-power- and wide-load-range operation at HF, and present supporting simulation results.

Both of these architectures use load modulation via outphasing as a means of achieving continuous power control [22], [24]–[26]. Key to attaining high efficiency with outphasing is the choice of a power combiner which couples power from the inverter system to the load [22], [24]. A major consideration in a combiner design is its ability to maintain acceptable loading for the amplifiers/inverters being combined. To achieve acceptable loading, a compensated (or modified) Chireix combiner can be used where compensating reactances are added to the combiner inputs to (a) provide nearly resistive loading to the inverters as power is varied, and (b) provide some additional inductive offset reactance such that both inverters see a resistive/inductive load as required for maintaining ZVS [7], [24], [37]. Furthermore, to maintain acceptable loading to both inverters, the range of allowable outphasing angles is also limited [7], [24], [37]. The next two subsections

compare two switched-mode dc-to-rf architectures that use such a compensated combiner to achieve high efficiency over a wide operating power range.

A. Multilevel Outphasing

Fig. 5 shows an example of a dc-to-rf architecture that utilizes a combination of discrete supply modulation (DSM) and outphasing as a means for achieving power control, and a TMN to compress the wide load impedance range [6], [7], [33]–[36]. In this architecture, which is referred to as multilevel outphasing [19], [20], two power amplifier (PA) blocks fed from power supplies that may be switched among different levels are outphased and combined to deliver a desired output power. This architecture leverages the benefits of discrete supply voltage modulation and load modulation (via outphasing) such that a very wide operating power range can be achieved while maintaining acceptably high efficiency values and extremely fast response times.

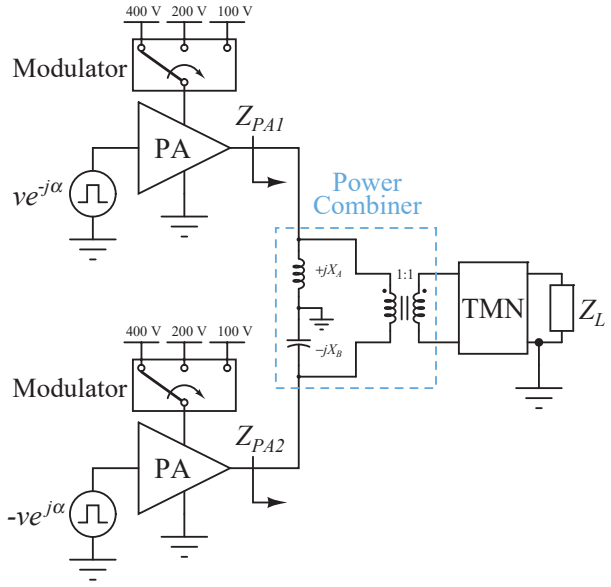

Fig. 5. Architecture based on discrete supply modulation and outphasing.

The version of the multilevel outphasing architecture explored here is fundamentally different than that investigated in the previous literature in that it uses a (nonisolating) compensated Chireix combiner with inverters expressly designed for variable load impedances, whereas the previous literature has explored the use of isolating combiners (either lossy isolating combiners or those incorporating energy recovery) and power amplifiers suitable for fixed-load operation. These differences give it a very different efficiency and response profile compared to other architectural variants using discrete drain modulation and outphasing. The operation of a particular implementation of this architecture is described below.

For this multilevel outphasing system we implement each inverter as a switched-mode variable load inverter as in Fig. 2 using 8x PGA26E07BA devices[2]. Each PA block in this example can have one of three different supply voltages: 400 V, 200 V, and 100 V. These voltage levels are selected to provide discrete steps in output power by a factor of 4 (6 dB) without sacrificing efficiency (see Section III-A) and to provide adequate margin with respect to device voltage limits of many available GaN switches. When operating the PAs at a given supply voltage level (e.g., 400 V), this architecture uses load modulation via outphasing and combining (using a compensated Chireix combiner) over only some limited outphasing angle range $\alpha \in [24.30°, 65.70°]$ corresponding to a limited range of output power, namely a factor of 4, thereby preventing the substantial efficiency degradation discussed in Section III-B. Once output power backs off by a factor of 4 via outphasing (by varying α from α_{min} to α_{max}) within a given operating PA supply voltage (e.g., 400 V), the supply modulator selects the next lower supply voltage (e.g., 200 V) and the outphasing angle is reset to α_{min}. Now within this lower supply voltage (e.g., 200 V) the system once again achieves output power back-off via outphasing by varying α from α_{min} to α_{max}. The result of this is that the load variation seen by each PA remains unchanged across each supply voltage domain. The reason this is beneficial is that it allows the PAs to be optimized for high efficiency only over this limited operating load impedance range, while allowing such high efficiency to be maintained across different voltage domains.

The achievable efficiency benefits of this approach in high-power HF inverters are illustrated in the simulation results shown in Fig. 6. The solid plots show the achievable system efficiency vs. output power when operating at each voltage domain for a nominal resistive load of $3\,\Omega$ at the combiner output. It can be seen that the optimized efficiency curve is almost replicated at each voltage domain, resulting in efficiency exceeding 90% across a very wide output power range of about 85x. The other dotted plots show the effect of having $\pm 20\%$ load impedance variations at the combiner output in resistance, reactance, or both on the system efficiency. The results indicate that the system still maintains an overall acceptably high efficiency across a wide output power range despite the $\pm 20\%$ resistive and reactive load variations. Furthermore, it can be observed that the system is somewhat more tolerant to variations in reactance compared to resistance. (This can be a consideration in the design of a TMN that handles the wide load impedance range associated with a plasma load.)

B. Outphasing with Multi-Inverter Discrete Back-off (MIDB)

Fig. 7(a) shows another dc-to-rf architecture, termed multi-inverter discrete back-off (MIDB) [37], that uses a form of

[2]In a given inverter implementation, once the inverter parameters (e.g., device area, L_{zvs}, L_f, C_f, and Z_{PA} in Fig. 2) are optimized for efficiency at a given supply voltage, the network components and device area can be scaled to deliver higher/lower power levels at the same efficiency. In this example, the inverter uses 8x PGA26E07BA devices to allow direct comparison with the other dc-to-rf architecture presented in this section.

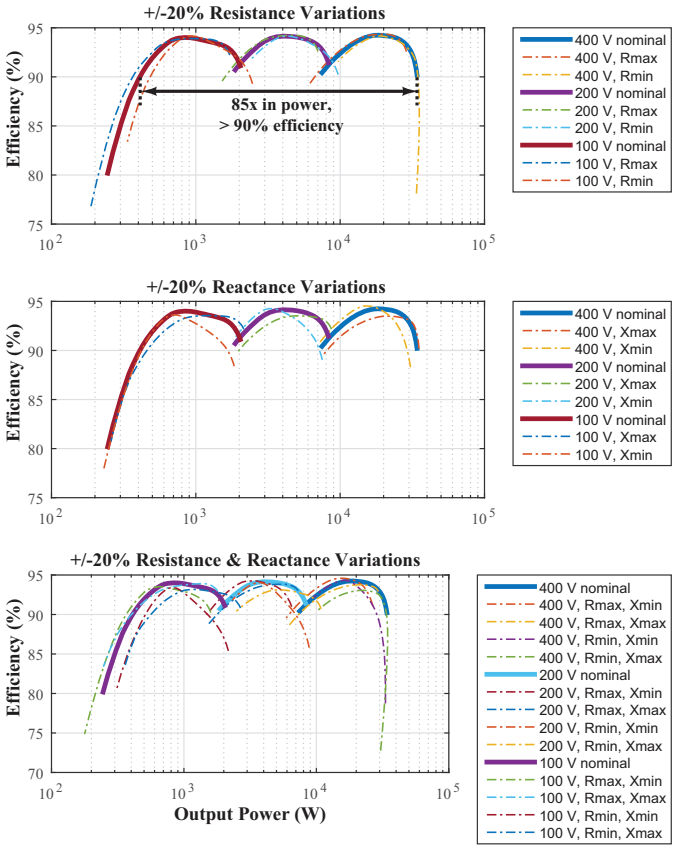

Fig. 6. Simulated efficiency vs. output power for the architecture based on discrete supply modulation and outphasing shown in Fig. 5 at 13.56 MHz. Each PA is simulated with L_{zvs} = 270 nH, C_{zvs} = 10 nF, L_f = 411 nH, C_f = 335 pF, and deadtime 13% of rf period. Output combiner compensation: 35 nH and 2.93 nF. The simulated nominal load resistance is 3 Ω connected to the combiner output directly.

structural modulation and outphasing to achieve control of output power, along with a TMN to compress the wide load impedance range [6], [7], [33]–[36]. This architecture consists of two sets of identical amplifiers, where the amplifiers in each set are in phase and are combined such that the voltage at the combiner output is the average of the individual amplifier output rf voltages within the set. One way this can be accomplished is by using the current-splitting combiner structure (or interphase transformer) shown in Fig. 7(a) which equalizes currents at its inputs and averages voltages at its output. (Many lossless combiner structures can provide similar characteristics.) By phase-shifting amplifiers in one set with respect to those in the other set and combining them using, for example, a compensated Chireix combiner, one can achieve continuous outphasing power control just as with the architecture in the previous subsection.

Another means for backing off power in addition to outphasing is in the form of structural modulation via dynamically shutting down amplifier pairs where a pair consists of an amplifier from each set (e.g., one pair as shown in Fig. 7(b), two pairs, etc.) [37]. By "shutting down" it is meant that a PA has its output placed at a fixed potential so that it forms an ac ground at the combiner input; this is easily accomplished with the class D PAs considered here. This on/off power control technique with subsets of amplifiers effectively provides the ability for fast discrete stepping of the voltage at the output of each current-splitting combiner, thereby discretely and rapidly modulating output power. An advantage of such a scheme is the ability to achieve fast discrete stepping in output voltage/power without requiring a supply modulator to reconfigure the dc voltage supplied to the inverters as in the multilevel outphasing architecture described in the previous subsection. This means of stepping voltage at the combiner output by turning off PA pairs, however, also differs from discrete supply modulation in that it affects the load impedance seen by the other PA pairs that are still on, and has different power backoff characteristics, as described below.

In the example in Fig. 7(a), four identical PA pairs with a 400 V supply are used to evaluate the performance of this architecture. Each PA is implemented as a switched-mode variable load inverter as in Fig. 2 using 2x PGA26E07BA devices (i.e. a single PA in the previous multilevel outphasing architecture can be thought of as consisting of four paralleled PAs in this MIDB architecture, resulting in the same total device area used to simulate and compare both architectures). We now consider the effect of shutting down a PA within a given set (e.g., the left set of four PAs in Fig. 7(a)). If each PA has a peak rf output voltage V and all PAs are on, the peak rf voltage at the combiner output is V. If one PA is turned off (e.g., by keeping the bottom switch of the inverter in Fig. 2 on and the top switch off), the peak rf voltage at the combiner output is $(3/4)V$. With a fixed combiner output impedance, this results in the output current reducing by a factor of 3/4, which causes the impedance seen at the output of the three running PAs to increase by a factor of 4/3. In a general set consisting of N identical PAs having peak output voltages V and with M PAs turned off, the combined output voltage peaks at $[(N-M)/N]V$ and results in an increase in output impedance to the $(N-M)$ running PAs by a factor of $N/(N-M)$. Each operating PA thus delivers less power (for the same loss). So, while losses indeed back off (by removing the losses of the inactive PAs), power backs off more quickly than loss. Consequently, this scheme of structural modulation causes a dynamic effective load modulation to the running PAs which can lead to a slight efficiency degradation as power backs off. Nevertheless, the MIDB architecture can still enable fast power control with acceptably high efficiency across a wide operating range, and it benefits from not having the cost or complexity associated with supply modulation.

The benefits provided by this architecture are illustrated in the simulation results shown in Fig. 8. The curves shown reveal the efficiency vs. output power characteristics for the MIDB system in Fig. 7 with all PA pairs on, 3 PA pairs on, 2 PA pairs on, and 1 PA pair on. It can be seen that an efficiency exceeding 90% is achieved over a factor of 21x in output power. Furthermore, it can be seen that efficiency somewhat degrades as more PAs are turned off, as expected owing to

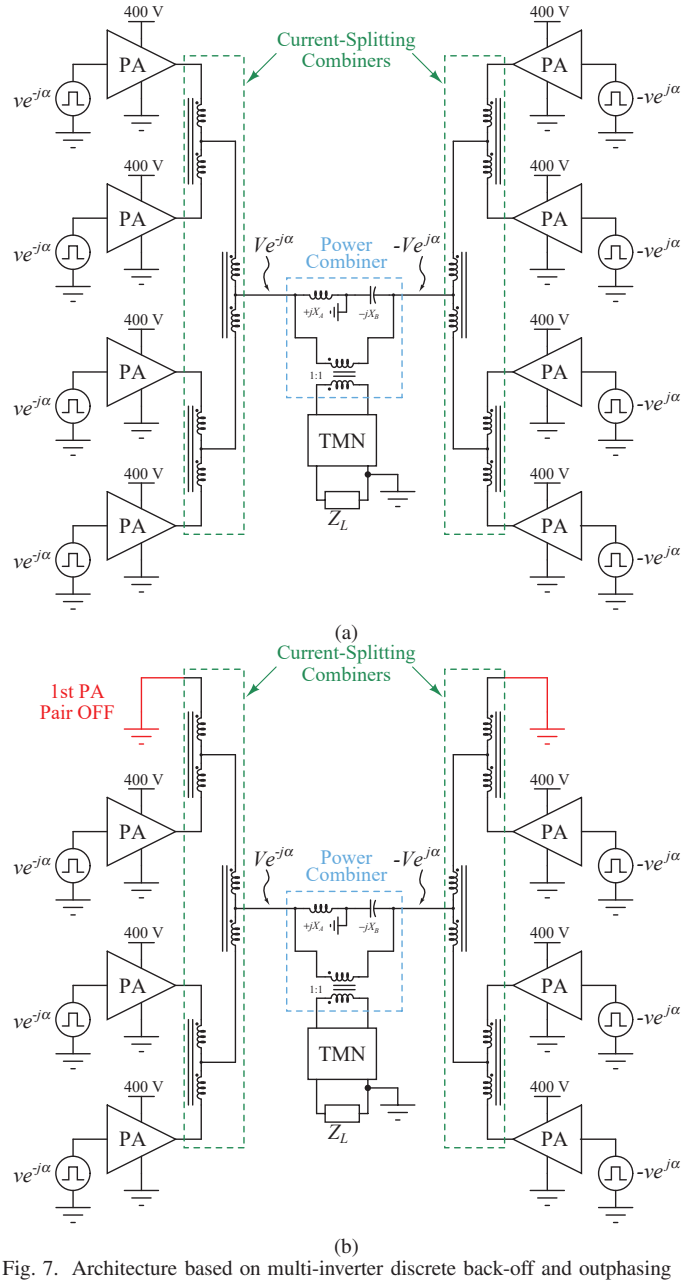

Fig. 7. Architecture based on multi-inverter discrete back-off and outphasing (a): with all PA pairs on; (b): with one PA pair off.

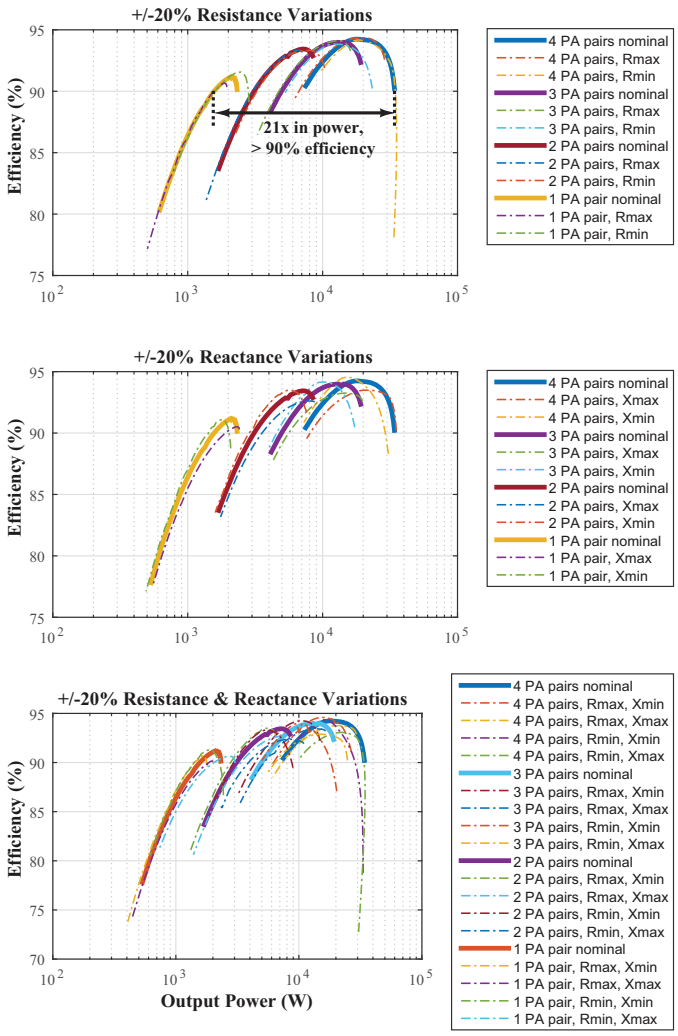

Fig. 8. Simulated efficiency vs. output power for the architecture based on multi-inverter discrete back-off and outphasing shown in Fig. 7 at 13.56 MHz. Each PA is simulated with L_{zvs} = 270 nH, C_{zvs} = 10 nF, L_f = 411 nH, C_f = 335 pF, and deadtime 13% of rf period. Output combiner compensation: 35 nH and 2.93 nF. The simulated nominal load resistance is 3 Ω connected to the combiner output directly.

the load modulation effects (which do not occur with discrete supply voltage steps in the DSM-based architecture). As with the previous example, the effects of load variations at the output of the compensated Chireix power combiner (shown in blue in Fig. 7(a)) are also illustrated in the dotted curves in Fig. 8. This shows that the MIDB architecture is similarly robust to variations in the load seen at the Chireix combiner output and as a result, similar considerations apply to the design of a TMN to handle load impedance variations.

V. Conclusion

This paper overviews ways power control techniques can be leveraged to realize dc-to-rf architectures having high efficiency over a very wide range of load impedances and power levels, while providing opportunity for high-bandwidth control of power. The paper analyzes the efficiency characteristics of the power control methods and discusses their tradeoffs and limitations. It also illustrates two dc-to-rf architectures for high efficiency operation across a very wide load impedance and power range, and presents simulation results affirming the achievable performance benefits. Such architectures are well-suited for applications such as plasma generation where the load impedance and operating power levels vary over extremely wide ranges.

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