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Dislocations behavior in highly mismatched III-Sb growth and their impact on the fabrication of top-down n+InAs/p+GaSb nanowire tunneling devices

S. El Kazzi, A. Alian, B. Hsu, P. Favia, C. Merckling, W. Lu, J. A. del Alamo, and N. Collaert

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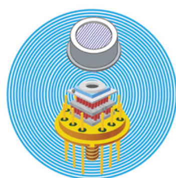

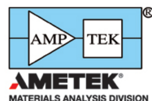

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Dislocations behavior in highly mismatched III-Sb growth and their impact on the fabrication of *top-down* n + InAs/p + GaSb nanowire tunneling devices

S. El Kazzi,[1] A. Alian,[1] B. Hsu,[1] P. Favia,[1] C. Merckling,[1] W. Lu,[2] J. A. del Alamo,[2] and N. Collaert[1]
[1]*Imec, 75 Kapeldreef, 3001 Heverlee, Belgium*
[2]*Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA*

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We study in this work the growth and fabrication of *top-down* highly doped n + InAs(Si)/p + GaSb(Si) Esaki tunneling diodes on (001) GaAs substrates. A careful investigation on the highly mismatched GaSb/GaAs growth is first conducted by means of Reflection High-Energy Electron Diffraction (RHEED), Atomic Force Microscopy (AFM), and X-Ray Diffraction (XRD) analyses. These results are expected to pave the way to methods for III-Sb buffer layer's integration with low threading dislocation (TD) densities. A comparison between AFM, XRD, defect revealing by chemical etching and transmission electron microscopy (TEM) is then presented to calculate the precise TD density and its influence on the device structure. In the last part, we report on first operating sub-30 nm III-V vertical NW tunneling devices on (001) commercial GaAs substrates. *Published by AIP Publishing.* https://doi.org/10.1063/1.5049900

INTRODUCTION

In the pursuit of low power consumption and transistor scaling, vertical nanowire (NW) III-(As,Sb) Tunnel Field Effect Transistors (TFETs) have emerged to be one of the most promising devices which can achieve turn-on devices with Subthreshold Slopes (SS) less than 60 mV/dec.[1,2] Even if devices were fabricated using these materials,[3] none of them still meet the target input characteristics predicted by theory which will eventually allow TFETs to compete with MOSFETs. Besides the traditional difficulties encountered during any III-V transistor fabrication (Integration on Si, gate stack, contacts, etc.), the main challenge of TFETs remains in controlling the defects at the channel tunneling interface. In the target to focus on the latter challenge and avoid the problem of the high-*k*/semiconductor, we have proposed to use III-V Esaki diodes instead of TFETs to study the influence of band alignment,[4] doping,[5] and interface stoichiometry[6] on Band to Band Tunneling (BTBT) of III-V tunneling interfaces. These works are done on lattice-matched substrates where threading dislocations coming from the channel/substrate growth are avoided. In parallel, other reports on III-V Esaki diodes on mismatched commercial substrates (like GaAs and Si) are performed by different groups[7,8] and the effect of threading dislocations on BTBT is carefully studied.[9] Unfortunately, these latter studies are achieved on diodes with very big dimensions. Furthermore, the effect of dislocations on a promising TFET process flow, which is CMOS-compatible, is still missing.

In this vein, we present here the growth and fabrication of narrow n + InAs(Si)/p + GaSb(Si) broken gap NW Esaki diodes (reaching 30 nm diameter) on highly mismatched (001) commercial substrates. The growth is performed by using III-Sb buffer layers which are relaxed by 90° misfit dislocations (MDs) at the buffer/substrate interface to integrate the tunneling active region on (001) GaAs substrates. Then, a developed Alcohol-based III-V Digital Etching technique[10] is used to achieve homogeneous and narrow III-V NW devices.

In this paper, we start by giving a detailed investigation on the GaSb growth on GaAs while providing insights into how low TD density III-Sb buffer layers can be attained. The structural quality of the full n + InAs/p + GaSb growth is then examined by calculating the Threading dislocations (TDs) density by means of Atomic Force Microscopy (AFM), X-ray diffraction (XRD), and chemical etching along with detailed cross-section Transmission Electron Microscopy (TEM) analyses of the full NW tunneling device. Finally, the J-V characteristics of the NW Esaki diodes are illustrated showing the promise of this process for future III-V TFET integration on (001) commercial substrates.

EXPERIMENTAL AND GaAs SURFACE PREPARATION

All samples are grown on 2 in. (001) p+ GaAs substrates using a III–V Riber MBE 49 chamber equipped with As and Sb valved cracker cells. The growth rates of In, Ga, Sb_2, and As_2 molecular beams are determined by Reflection High Energy Electron Diffraction (RHEED) oscillations on InAs, GaAs, and GaSb substrates. For all samples, the typical Ga (In) evaporation rate of 0.5 ML s^{-1} is used for the GaSb (InAs) deposition. The surface morphology is examined by atomic force microscopy (AFM) using a Bruker AFM machine system, working in the tapping mode. The structural properties are further investigated by X-ray diffraction (XRD) and transmission electron microscopy (TEM) using, respectively, an X'Pert PANalytical tool and a Titan G2 aberration corrected TEM from FEI including both energy-dispersive X-ray spectroscopy (EDS) and electron energy loss spectroscopy (EELS) analysis detectors. The Esaki diodes with vertical architecture at different dimensions (junction area ranging from 0.0025 mm^2 to 2.5 mm^2 measured by Scanning Electron

Microscopy) are fabricated per the process flow described in Ref. 11 and detailed in Fig. 4(a) where a novel alcohol-based digital etch technique for III-V NW is used.

The GaAs substrate deoxidation is first achieved by heating the sample in the MBE chamber at 600 °C under As flux. Then, a 250 nm GaAs layer is grown to smooth the surface at 580°C at a pressure chamber $P_{chamber} = 4 \times 10^{-8}$ Torr. Our aim is then to send Sb on a Ga-rich pre-treated surface to minimize Sb/As intermixing and minimize threading dislocations in the GaSb layer.[12] We choose to do this on a (4 × 6) Ga-rich surface which exhibits a smoother surface than the (4 × 2) Ga-rich which we only obtain by pumping As at high temperatures (>550 °C).[13] Therefore, after the GaAs growth at 580 °C, all shutters are closed and the sample temperature is rapidly decreased to the GaSb growth temperature (450–510 °C). Interestingly, even if no As is sent to the surface at this stage, the (2 × 4) As-rich reconstruction is still observed by RHEED which confirms the As bond stability on the surface at this high temperature range.[14] When the desired GaSb growth temperature is reached, a stabilization step of few minutes is used to further pump the As background in the chamber. The RHEED pattern switches to a Ga-rich (4 × 6) only when the chamber pressure reaches ranges below 1×10^{-9} Torr. Sb flux is then sent to the surface for 2 min and a (2 × 8) Sb-rich occurs which is known to be the most suitable reconstruction for 90° misfit dislocation (MDs) array at the GaSb/GaAs interface.[15]

GaSb GROWTH ON (001) GaAs

Besides the surface preparation, the growth temperatures in the range of 450 °C–520 °C[16] with different Sb/Ga ratios have been tested for the highly mismatched GaSb/GaAs growth (~7%) where depending on the epitaxy conditions, different growth modes are reported.[17] Even if using 90° MDs array at the interface showed promising low TD density value,[18] the growth mechanisms leading to this goal are still unclear. Here, we use RHEED analyses to understand the influence of the growth conditions on the GaSb nucleation on GaAs. Figures 1(a) and 1(b), respectively, compare the in-plane lattice constant and the specular beam intensity (Sbi) deducted from the RHEED images recorded during the first GaSb MLs growth on GaAs of 3 different samples: sample A (T = 480 °C; Sb/Ga = 3), sample B (T = 510 °C; Sb/Ga = 3), and sample C (T = 510 °C; Sb/Ga ~ 2). From Fig. 1(a), one can notice that the GaSb in sample A (black line) grown at 480 °C relaxes both lower and slower than samples B and C (blue and red lines, respectively) which are

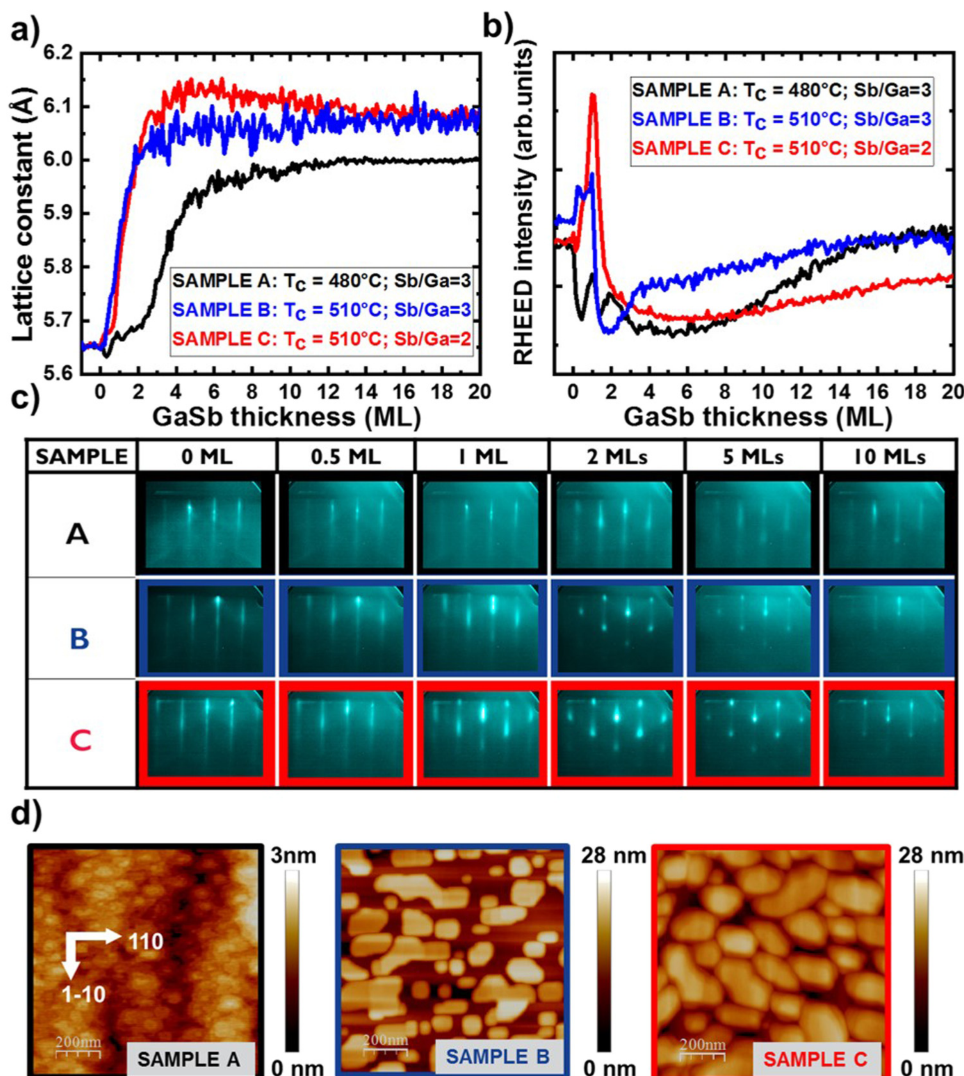

FIG. 1. (a) In plane lattice constant and (b) specular beam intensity evolution during the deposit of 20 MLs GaSb on GaAs of sample A (black line), sample B (blue line), and sample C (red line). (c) The RHEED images taken along the [1−10] direction at different thicknesses for different samples. (d) The (1 × 1) μm^2 AFM images of the 3 samples after 20 MLs GaSb growth.

grown at 510 °C. Furthermore, sample C with an Sb/Ga = 2 shows a slightly higher in-plane relaxation than sample B at the beginning of growth. From the Sbi of sample A [Fig. 1(b)], clear RHEED oscillations appear as soon as the GaSb starts, attesting a 2D growth mode at the beginning of the epitaxy. After nearly ∼2 MLs, the intensity starts to decrease due to the start of the epi-layer relaxation and a slight 3D-like island growth [see the RHEED images of this sample in Fig. 1(c)]. For samples B and C, the RHEED intensity first increases when the growth begins which also indicates a 2D layer growth at the start of the epitaxy. But for these 2 samples, the intensity drastically drops after ∼1 ML and a clear 3D island RHEED appears [see Fig. 1(c)]. Hence, we can deduce that the same growth mode (Stranski-Krastanov) is observed for all the samples but the difference is in the thickness of the wetting layer before the island formation. The AFM images of the 3 samples after 20 MLs growth are presented in Fig. 1(d). One can observe for sample A a nearly coalesced layer with an average height of 1.3 nm. For sample B, the islands are more elongated in the [110] direction than the ones of sample C but nearly the same average height of ∼14 nm.

To understand the above results, we combine our observations with the ones already reported on the GaSb mismatched growth. It is shown that a high Sb/Ga overpressure and a low growth T lead to the formation of high density of small islands which directly coalesce due to the lower Ga diffusion length.[19] The same observation can be seen in our case for sample A. Also, the fact that this sample shows by RHEED analyses [Fig. 1(a)] the lowest relaxation, is believed to be related to the formation of pure closely spaced 90° MDs at the interface which are formed in a quasi-2D growth mode.[20] At higher temperatures, the growth is more a 3D-island mode where 60° MDs are created at the islands edge and then glide toward the interface to react with each other.[21] This can explain the higher relaxation value of the lattice constant [Fig. 1(a)] in samples B and C compared to sample A. At last, lowering the Sb/Ga ratio at high T like in sample C, leads to the appearance of more elliptical shape islands. This is believed to further increase the distance between 2 MD cores and induce more 60° dislocations and/or stacking faults.[19] It can hence explain the slight overrelaxation value observed at the beginning of the growth of sample C [Fig. 1(a)].

A second set of samples is grown with the same conditions of samples A, B, and C at different thicknesses to evaluate the thickness effect on the epi-layer property. Figure 2(a) depicts the XRD ω-2θ scans measured with a triple axis

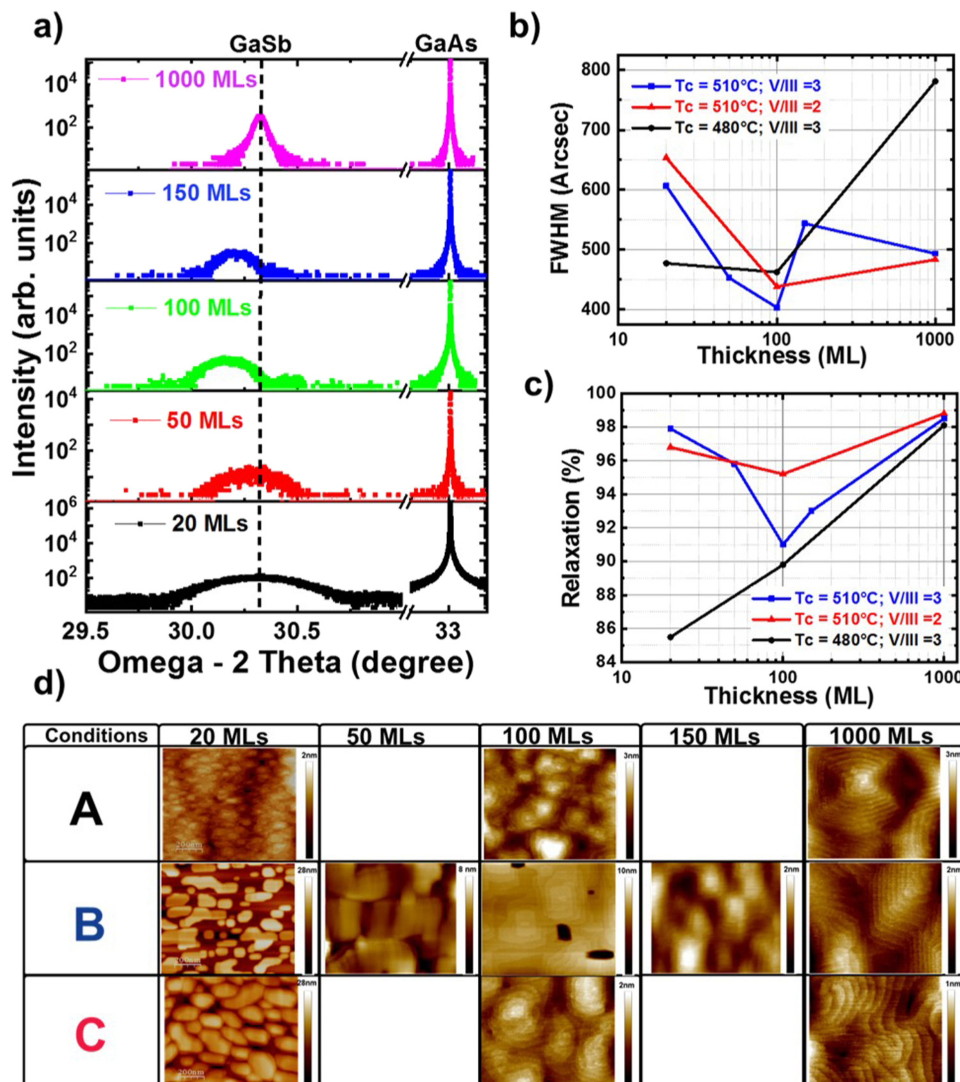

FIG. 2. (a) XRD ω-2θ scans along the (004) reflection of the samples grown with the same conditions of sample B at different thicknesses. (b) and (c) are, respectively, the out-of-plane relaxation and the Full Width of Half Maximum (FWHM), deduced from the (004) GaSb diffraction peak position for each sample with the different conditions A, B, and C. (d) are AFM images of the different samples at different thicknesses as a function of each growth condition.

detector along the (004) reflection of the samples grown with the same conditions of sample B ($T = 510\,°C$, Sb/Ga ~ 3). It is obvious how the (004) GaSb diffraction peak position is varying with the thickness. Figure 2(b) compares the deduced out-of-plane relaxation as a function of the thickness for the 3 conditions. We first notice that the relaxation decreases at the coalescence stage (from 20 to 100 MLs) for the samples grown with condition B (blue line). By looking at the AFM images of these samples [Fig. 2(d)], we notice that the layer is still not fully closed at 100 MLs. On the other hand, the AFM images show closed layers for thicker layers (≥150 MLs) where the out-of-plane relaxation starts to increase [see Fig. 2(b)]. This would mean that the out-of-plane relaxation behavior in the GaSb/GaAs system is strongly related to the surface morphology. This is also seen for sample C (Sb/Ga ~ 2) where the out-of-plane relaxation decreases from 20 to 100 MLs. But for these conditions, the AFM image at 100 MLs shows already a fully closed layer implying that the coalescence happened much faster than that of sample B. Therefore, the out-of-plane relaxation of sample C is lower at 20 MLs and higher at 100 MLs. On the other hand, the out-of-plane relaxation does not show any decrease with the thickness in the conditions of sample A (low growth T). This is obviously due to the early layer closure in this sample seen already at 20 MLs.

For the GaSb/GaAs system, this out-of-plane strain behavior at these thicknesses has never been reported to our knowledge. An anisotropic strain relaxation has been observed for the in-plane relaxation by both cross-section TEM[22] and XRD analyses[23] but all these reports show that the relaxation always increases with the thickness and independently of the stage of growth. In our case, our XRD tool does not allow us to perform accurate (224) Reciprocal Space Mapping (RSM) scans in both [110] and [1−10] directions for the very thin layers with the triple axis detector. If a rocking curve detector is used, the GaSb peak is so broad and an accurate determination of the relaxation is very challenging for thin layers. Since we observe the same in-plane relaxation trend than that of Refs. 22 and 23 for thick layers (not shown here), we assume that the in-plane relaxation is also increasing for our thin layers. This would mean that the GaSb Scherrer component is changing during the coalescence causing a disagreement between the 004 (out of plane) and 224 (in-plane) stress on the crystallite. Ongoing experiments are now being conducted to confirm this latter conclusion.

The Full Width of Half Maximum (FWHM) extracted from the ω-scans of the (004) GaSb Bragg reflections are depicted in Fig. 3(c). For the B and C conditions, we notice that the FWHM decreases with the thickness until the range of ~100 MLs. However, since the layers are not fully closed at these thicknesses, the FWHM values are strongly dependent on the Scherrer component which is related to the grain size[24] and thus these values cannot be considered as good representatives of the layer quality. A good comparison between the samples is however valid when the layers are fully closed. We can notice that conditions B and C exhibit nearly the same FWHM at 1000 MLs whereas condition A shows a much higher value. This is obviously due to the difference in the nature of the dislocations and their behavior in each sample. As mentioned before, high T samples (B and C) exhibit more paired 60° MDs. The thickness has a positive effect in these samples in decreasing the TDs density and thus the total FWHM value decreases. On the other hand, the low T condition (A) samples have more confined 90° MDs and the system is less relaxed at the first stage of growth. As the layer volume increases, the system would require additional MDs to sufficiently relax[25] or would need to dissociate the

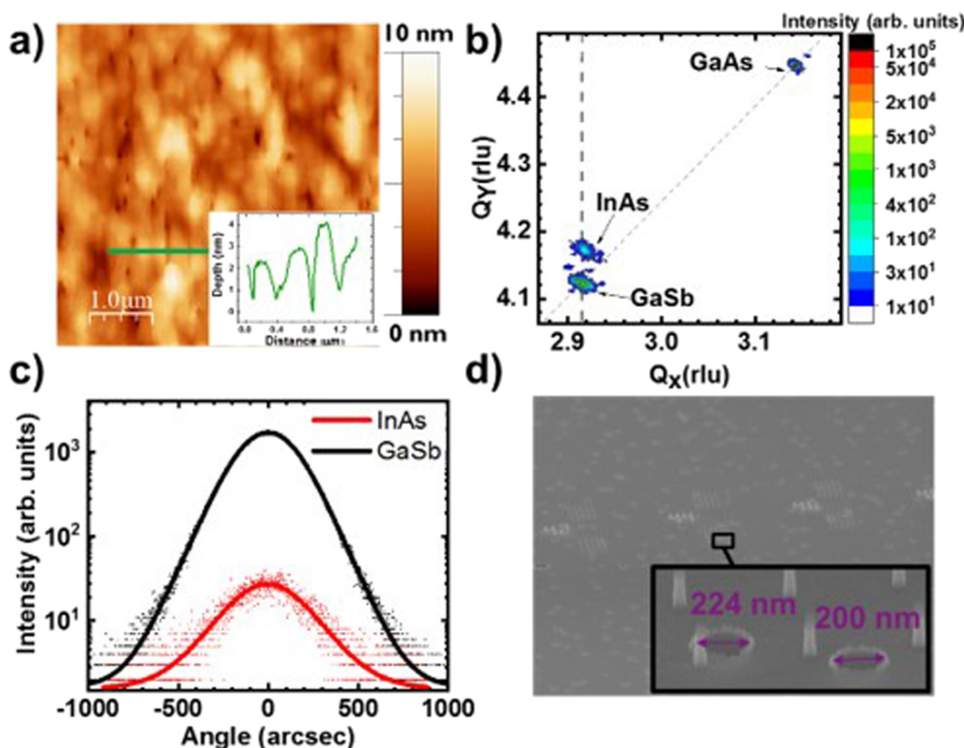

FIG. 3. (a) and (b) are, respectively, the $(1 \times 1)\,\mu m^2$ AFM and (224) RSM of the grown n + InAs/p + GaSb stack grown on the (001) GaAs substrate. The green line on the AFM image presents a line profile of multiples pits with different dimensions. (c) The comparison between the (004) ω-scans diffraction peaks of InAs and GaSb. (d) $(32 \times 24)\,\mu m^2$ SEM images taken during the device fabrication [see Fig. 4(a)] after the III-V NW etching step. The inset is a zoomed area in the image showing both nanowires and pits with dimensions of ~200 nm.

existing Lomer dislocations to 60° MDs pairs as observed by Wang *et al.*[26] In both cases, an increase in the TD density is hence expected.

In the light of these results, we can conclude that two approaches can be considered in the future for the growth of low TD density GaSb layers on GaAs:

(1) The first one is the use of a high growth temperature combined with a very high V/III overpressure where the idea is to avoid any 3D growth mode at high temperatures. This would offer closed 60° MD pairs with ideal cores which do not thread in the layer and fully relaxes the layer at the beginning of the growth. Thicker layers in this case would not introduce any additional MD.
(2) The second way is a low growth temperature with a low V/III overpressure to promote a 2D growth mode and compact 90° dislocation cores. However, this method can be only used for low thicknesses since the mismatch is only partially accommodated at the beginning of growth. Thick layers would require the introduction of new MD to fully relax the system and thus a risk to introduce more TD.

The use of the above solutions to integrate III-V TFET on commercial (001) substrates is ongoing. However, we are interested in this paper to investigate the influence of TDs on the device. Therefore, the growth of the full Esaki diode in the following uses the same GaSb growth conditions than sample B where the idea is to determine an accurate way to calculate the TD density and study its influence on the device performance.

n + InAs(Si)/p + GaSb(Si) GROWTH AND DEVICE FABRICATION

The highly doped n + InAs(Si)/p + GaSb(Si) Esaki diode growth starts by depositing 600 nm of Si-doped GaSb on p+ GaAs substrates. Then, as described in Ref. 6, a careful MBE shutter sequence is used to prepare an InSb-like interface for the subsequent growth of 50 nm n + InAs (Si) and a doping concentration at the interface of ($9 \times 10^{19}/cm^3$). The $(5 \times 5)\,\mu m^2$ AFM image of the final heterostructure displayed in Fig. 3(a) shows an InAs RMS value of 1.2 nm. It also shows the formation of pits on the surface with a density of $\sim 1.2 \times 10^8/cm^2$. These pits are known to be originated from threading dislocations formed at the GaSb/GaAs nucleation step rather than at the GaSb/InAs interface transition.[27] This is further confirmed in the (224) Reciprocal Space Mapping (RSM) scan of the heterostructure in Fig. 3(b). The diode scan shows that GaSb is relaxed on GaAs (~99.5%), whereas InAs is fully strained on GaSb and thus no TD formation is expected at the tunneling interface. Furthermore, the ω-scan of the (004) InAs Bragg reflection [Fig. 3(c)] exhibits a FWHM value of 300 arcsec close to the one of GaSb one (~360 arcsec) which is another proof that no additional dislocations are introduced at the interface. The TD density calculated from the FWHM of the (004) InAs Bragg reflection ω-scan is equal to $\sim 1.3 \times 10^8/cm^2$. This value is comparable to the one obtained by counting the pits on the AFM image implying that both methods are comparable enough to determine TD density. Another more accurate method to determine TD density would be the use of chemical etching for defect revealing.[28] Figure 3(d) shows $(32 \times 24)\,\mu m^2$ SEM images taken during the device

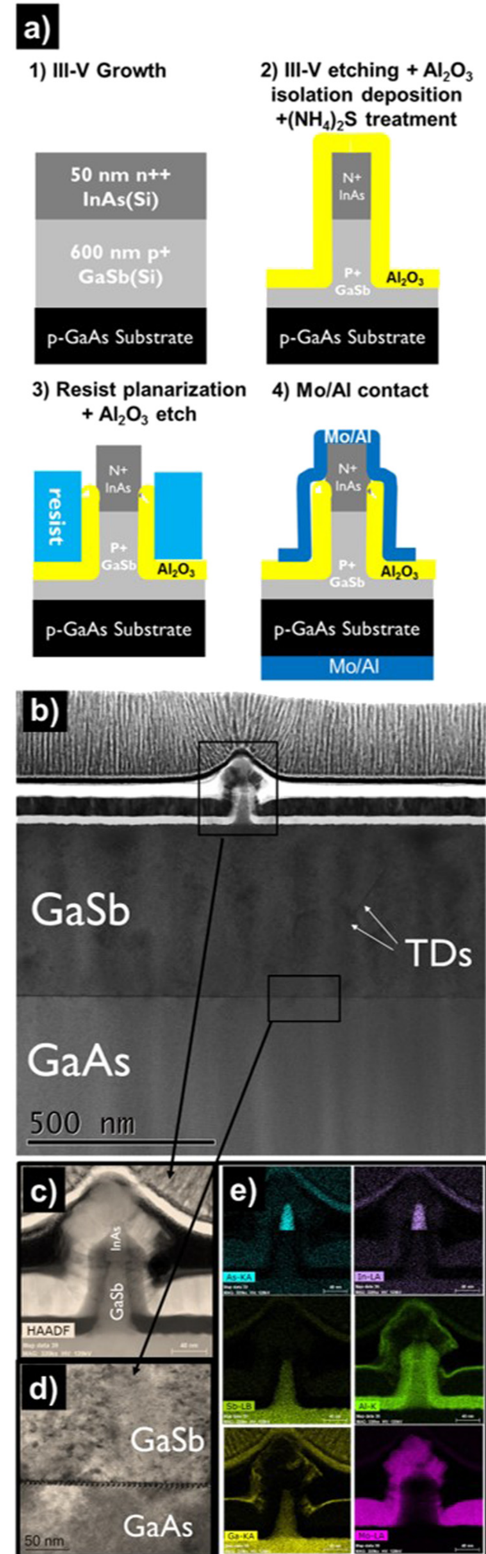

FIG. 4. (a) A schematic of the process flow and device details. (b) and (c) are cross-section Angular Bright field (ABF) STEM images of a fabricated n + InAs/p + GaSb NW Esaki diode on GaAs. (d) High-Resolution (HR) TEM image of the GaSb/GaAs interface showing the formation of an array of 90° MDs. (e) EDS elemental analysis maps of As, In, Sb, Al, Ga, and Mo.

fabrication after the III-V NW etching step [see Fig. 4(a)]. From these images, we can observe that besides NWs, pits coming from some of the TDs are clearly revealed. It is, however, important to mention that the mask to define the dry etch of the wires is possible to land directly on top of a dislocation thread and not all dislocations can be revealed with this technique. Other dislocations threading inside the active area or at the side surface of the NW are difficult to be seen here. In all cases, these images show the necessity to further lower the TD density during the III-V growth, which is one of the fundamental requirements to make this integration route CMOS-compatible.

Figures 4(b)–4(e) depict the cross-sectional TEM analyses of an NW Esaki diode device with a target diameter of 50 nm. From Fig. 4(b), we can observe 3 clear TDs in the GaSb layer volume lying in both (111) and (−1 −1 1) planes (marked by white arrows) over a length of 1 μm image. We can hence estimate a TD density of $3.5 \times 10^8/\text{cm}^2$ in these layers which is not far from the AFM and XRD results obtained above. This also confirms our previous statement that TDs coming from 60° MDs are expected in these layers even if a well-formed periodic 90° MDs array is seen at the GaSb/GaAs interface [Fig. 4(d)]. On the other hand, the HAADF-STEM image of the device area [Fig. 4(c)] shows that Digital Etching leads to a pyramidical shape of the nanowire which opens a way for further optimization of the etching process for these kinds of materials. Furthermore, the $(NH_4)_2S$ treatment which is employed after the 30 nm ALD deposition of Al_2O_3 leads to an undercut at the p + GaSb side[1] which shrinks the actual tunnel junction diameter by nearly 10 nm. Also, the Al_2O_3 passivation layer covers well the tunneling interface reaching nearly half of the n + InAs layer. Finally, EDS analyses confirm the abrupt interface at the tunnel junction as well as the homogeneity of the III-V material across the NW area at these very low dimensions.

After the full fabrication, only 50% of our NW devices led to diode-like behavior. The rest shows ohmic-like devices (∼35%) or no current (∼15%). The real reason for the latter 2 cases is challenging since it can be related to either non-idealities in the process (spin coating, lift-off, etc.) or to dislocations which thread outside the wire but still affect the NW behavior. In Fig. 5, we only illustrate the diode-like behavior devices where 2 typical J-V characteristics (black and red lines) are observed. For the devices with a black line, a dominant BTBT current is observed where negative differential resistance (NDR) is shown in forward bias (Vnp < 0) with an average BTBT peak current density of Jp = 8 mA/μm^2. This value is similar to the one reported in Ref. 6 where the same n + InAs(Si)/p + GaSb(Si) system is grown on matched GaSb substrates (blue line). This implies that even if a highly mismatched growth is used, the same BTBT current can still be achieved. On the other hand, the J-V characteristics of the other diode-like devices (red line) show no NDR. Since TDs have already shown to increase the valley current in Esaki diodes,[7,8] we believe that the NDR suppression of some of the diode-like devices is due to the presence of TDs which are threading inside the NW and reaching the tunneling interface.

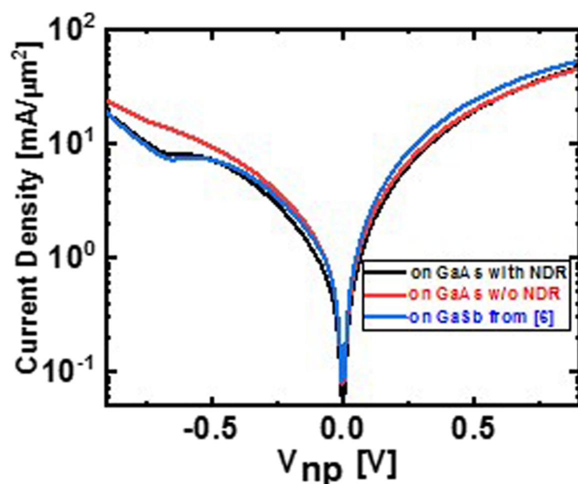

FIG. 5. J-V characteristics comparison between n + InAs(Si)/p + GaSb(Si) Esaki diodes grown pseudomorphically on GaSb substrates from Ref. 6 (blue line) and mismatched GaAs substrates (red and black lines).

CONCLUSION

In conclusion, we have presented in this work a detailed investigation on the growth and fabrication of a III-V n + InAs(Si)/p + GaSb(Si) NW tunnel device on commercial (001) GaAs substrates. In the first part, we have detailed the growth of III-Sb buffer layers on mismatched substrates which are considered among the most interesting materials for future (opto)electronic applications. Insights into how to reach low TD buffer layer are given and influence of TD density on tunneling Esaki devices are discussed. To our knowledge, these are the first vertical tunneling devices demonstrated at these low dimensions (reaching 30 nm diameter) with a full *top-down* III-V digital etching on (001) commercial substrates. This work provides evidence that the growth of III-Sb buffer by means of 90° MDs on commercial (001) substrates along with the right NW digital etching would pave the way to the integration of III-V NW devices onto large area CMOS compatible (001) Si substrates.

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