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First Demonstration of a Self-Aligned GaN p-FET

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Abstract— In this work, we demonstrate a self-aligned p-FET with a GaN/Al_{0.2}Ga_{0.8}N (20 nm)/GaN heterostructure grown by metal-organic-chemical vapor deposition (MOCVD) on Si substrate. Our 100 nm channel length device with recess depth of 70 nm exhibits a record ON-resistance of 400 Ω -mm and ON-current over 5 mA/mm with ON-OFF ratio of 6×10^5 when compared with other p-FET demonstrations based on GaN/AlGaIn heterostructure. The device shows E-mode operation with a threshold voltage of -1 V, making it a promising candidate for GaN-based complementary circuit that can be integrated on a Silicon platform. A monolithically integrated n-channel transistor with p-GaN gate is also demonstrated. The potential of the reported p-FET for complementary logic application is evaluated through industry-standard compact modeling and inverter circuit simulation.

I. INTRODUCTION

In order to keep up with the ever increasing demand of cloud computing, data centers and electric vehicles, power electronic circuits need to be more energy efficient and demonstrate higher power density levels. AlGaIn/GaN High Electron Mobility Transistors (HEMTs) have shown great promise towards that end, thanks to their lower switching loss (attributed to lower terminal capacitances) and the higher switching speed enabled by their high electron mobility. However, in today's power electronic circuits, GaN power transistors are typically switched at relatively lower frequency (hundreds of kHz) in order to avoid voltage instabilities caused by the parasitic inductance between the Silicon driver chip and that GaN switch [1]. To eliminate this parasitic inductance, it is necessary to monolithically integrate GaN-based complementary driver circuits with the GaN power transistors. However, this has been difficult until now due to the limited performance of p-channel GaN transistors. Most of the two-dimensional hole gas (2-DHG) based p-FETs demonstrated in the literature show normally-ON operation with ON-resistance over 1 k Ω -mm [2]–[6]. GaN/AlInGaIn heterostructure-based p-FET shows low ON-resistance because of higher 2-DHG density and hole mobility but with D-mode operation [7]. Ref. [8] demonstrated E-mode p-FET based on GaN/AlN heterostructure with R_{ON} of 640 Ω -mm. However, n-FET integration with this p-FET requires regrowth. While most of the demonstrations are on Sapphire substrate, Ref. [9] was the first demonstration on Silicon substrate. The utilization of GaN-on-Si platform offers lower cost, availability of 200-mm-diameter substrates, and potential to integrate with high performance logic and analog functionalitv

A key reason for the poor performance in p-FETs is their low hole mobility [2]. This could be circumvented by aggressive device scaling. A self-aligned device with scaled gate length and no access region is an effective way to achieve greater performance in terms of on resistance. In this work, we demonstrate a novel fabrication technique to fabricate a self-aligned gate-recessed p-FET with $L_g=100$ nm. The demonstrated technology provides a pathway for high performance GaN-based p-FET which can enable GaN-based complementary circuit technology on a Si substrate. A monolithically integrated n-channel is also fabricated. The potential of the demonstrated p-FET for complementary logic application is evaluated through circuit simulation employing the MIT Virtual Source GaN-FET (MVSF) model [10].

II. EPITAXIAL STRUCTURE

The epitaxial stack used in this work was grown by Enkris Semiconductor, Inc. on a 6 inch, 1-mm-thick Si (111) substrate using MOCVD method. The structure is as follows, 20 nm p⁺⁺-GaN (Mg: 6×10^{19} cm⁻³ with 2–3% activation at room temperature), 50 nm p-GaN (Mg: 10^{19} cm⁻³), 20 nm UID-GaN (Si: 5×10^{16} cm⁻³), 20 nm Al_{0.2}Ga_{0.8}N (Si: 5×10^{16} cm⁻³), 150 nm UID-GaN (Si: 5×10^{16} cm⁻³), 3.8 μ m buffer and Si substrate (see Fig. 1 (a)). Fig. 1(b) shows the Transmission Electron Microscopy (TEM) image of the GaN/AlGaIn/GaN double heterostructure. The p-channel FET uses the polarization-induced 2-DHG at the interface of the top UID-GaN/AlGaIn heterostructure. The top p⁺⁺-GaN layer enables good ohmic contact. The 20 nm UID-GaN layer that separates the p-GaN and AlGaIn layers helps to achieve higher hole mobility. Using Hall measurement, the 2-DHG density and hole drift mobility are measured to be 8×10^{12} cm⁻² and 11 cm²/V·s respectively. Fig. 1(c) shows the band diagram of the epitaxial structure exhibiting the Fermi level crossing the valence band energy level giving rise to 2-DHG (as shown in Fig. 1 (d)).

III. SELF-ALIGNED TRANSISTOR FABRICATION

Fig. 1(e) shows the key processing steps for fabricating the self-aligned device. First, electron beam lithography is used for the formation of source and drain contacts. Then, a Ni (20 nm)/Au (30 nm)/Ni (20 nm) metal stack are deposited using electron beam evaporation and lifted off in acetone. Next, a blank etch is performed by Cl₂/BCl₃-based Inductively Coupled Plasma-Reactive Ion Etching (ICP-RIE) process. This step helps to form the gate recess. Here, the top 20 nm Ni on the source and drain metal serves as the etch mask and protects the ohmic contact from the etch damage. The etch depth is controlled by the etch time (see Fig. 1(f)). Then, the mesa etch is performed by

Cl_2/BCl_3 -based ICP-RIE process using photoresist mask. The photoresist is then removed by oxygen plasma etching. Following the etch steps, the sample is dipped into heated Tetramethylammonium hydroxide (TMAH) for about 15 min in order to remove the photoresist and reduce the etch-induced roughness. After that, ~ 30 nm of Al_2O_3 gate dielectric is deposited by Atomic Layer Deposition (ALD). Finally, a Ni (20 nm)/Au (100 nm) gate metal electrode is formed by e-beam evaporation and lift-off technique. Fig. 1(g) exhibits the Scanning Transmission Electron Microscopy (STEM) image of the cross-section of the fabricated device. Fig. 1(h) shows the smooth interface between the GaN and gate dielectric attesting to the high quality of gate recess process with low surface roughness.

IV. RESULTS AND DISCUSSION

Fig 2 (a) shows the transfer characteristics of the p-FET with $I_{\text{ON}}/I_{\text{OFF}} = 6 \times 10^5$ and low gate leakage in the range of 1 nA/mm. In the OFF-state, the drain leakage current is limited by gate leakage. The high gate leakage in the OFF-state is because of the high electric field that exists across the gate dielectric at the sidewall of the gate recess, and between the gate and drain terminals. Fig. 2(b) shows the $I_{\text{DS}} \text{ vs } V_{\text{GS}}$ characteristics in the linear scale, demonstrating E-mode operation with a threshold voltage of -1 V. Fig. 2(c) shows the $g_m \text{ vs } V_{\text{GS}}$ characteristics of the p-FET showing a maximum transconductance of 0.9 mS/mm at $V_{\text{DS}} = -1.5$ V and $V_{\text{GS}} = -4$ V. Fig. 2(d) shows the output characteristics of the self-aligned p-FET with R_{ON} of ~ 400 $\Omega\text{-mm}$ at $V_{\text{GS}} = -7$ V (which is calculated by taking an inverse slope at low V_{DS} regime of the output characteristics). The figure also shows an ON-current density of > 5 mA/mm at $V_{\text{GS}} = -7$ V and $V_{\text{DS}} = -5$ V.

Fig. 3 shows the output characteristics of the self-aligned p-FET with 300 nm channel length for different recess depths. The depths are estimated based on time of etch using a calibrated etch recipe (as shown in Fig 1(f)). The device performance is found to be dependent on recess depth – shallower recess depth results in more ON-current but weaker current modulation with respect to gate voltage.

Fig. 4(a)-(b) shows the $I_{\text{DS}} \text{ vs } V_{\text{DS}}$ characteristics of self-aligned p-FET with 500 nm channel length, at room and cryogenic temperatures, respectively. A ~ 20 % drop in ON-current at low temperature could be observed from the results, which is attributed to the increase in contact resistance at low temperature because of low Mg activation. This is attested in Fig. 4(c) which shows the linear TLM measurements both at room and cryogenic temperatures.

A key advantage of the proposed p-FET device architecture is that it allows for the monolithic integration of self-aligned p-FET and n-channel GaN FET on the same Si wafer (Fig. 5(a)). The $I_{\text{DS}} \text{ vs } V_{\text{GS}}$ characteristics of the fabricated n-channel FET are shown in Fig. 5(b). Fig. 5(c) shows the output characteristics of the n-channel transistor with an R_{ON} of 19 $\Omega\text{-mm}$ and ON-current over 200 mA/mm. A threshold voltage of 0.2 V is obtained from the monolithically integrated n-FET. A p-GaN gated device without the 20 nm UID GaN layer and thinner AlGaIn layer (~ 15 nm), which is typically used for E-mode p-

GaN gated AlGaIn/GaN HEMTs, yields a threshold voltage of 2 V (Fig. 5(d)). A more positive threshold voltage for p-GaN gated n-FET using the epitaxial layer of Fig. 1(a), could be achieved by FinFET or nanoribbon structure [11].

Fig. 6 benchmarks the performance of the fabricated self-aligned p-FET in this work with other p-channel transistors reported in the literature in terms of ON-resistance and ON-OFF ratio. As shown, the device in this work shows record performance in terms of ON-resistance and ON-OFF ratio when compared with GaN/AlGaIn and InGaIn/GaN based p-FETs. It should be noted that, GaN/AlInGaIn based p-FETs show slightly lower resistance compared to the self-aligned p-FETs in this work because of very high 2-DHG density provided by large negative polarization charge at the III-N heterointerface but with normally-ON operation. The p-FET reported in this work has the additional advantage of having a 2-DEG beneath the 2-DHG which facilitates on-chip n-channel transistor with the same epitaxial structure without any regrowth. The reported p-FET also shows E-mode operation, which is absent in most of the devices reported in the literature so far.

To evaluate the potential of the reported p-FET and n-FET monolithic integration, for GaN-based complementary logic applications, circuit simulation was conducted using Cadence Virtuoso and compact models for the devices obtained using the industry-standard MVSG compact model. The inverter circuit and simulation methodology are presented in Fig. 7(a). A DC bias of 5 V was used. The n-FET and p-FET have gate widths of 25 μm and 250 μm , respectively. The simulated voltage transfer curves for the complementary logic inverter are presented in Fig. 7(b), which shows a maximum voltage gain of 48 at $V_{\text{IN}} = 0.68$ V. The DC current drawn by the inverter (I_{DD}) has a peak of 0.52 mA at $V_{\text{IN}} = 0.70$ V, which is the switching point of the inverter. The switching behavior of the inverter was studied by applying a capacitive load of 35 pF. As shown in Fig. 7(c)-(d), the fall and rise times of the circuit are 60 ns and 301 ns, respectively. The longer rise time is mainly due to the high R_{ON} of the p-FET.

V. CONCLUSION

In this work, we demonstrate self-aligned GaN p-FET with 100 nm gate length for the first time, with ON-OFF ratio 6×10^5 and threshold voltage of -1 V. The demonstrated device shows record ON-resistance of 400 $\Omega\text{-mm}$ with ON-current of > 5 mA/mm when compared with other GaN/AlGaIn heterostructure-based p-FET demonstrations. The capability for monolithic integration of this p-FET with p-GaN gated n-FET on a Si substrate makes this technology an ideal candidate for GaN complementary logic for integrated power driver circuits.

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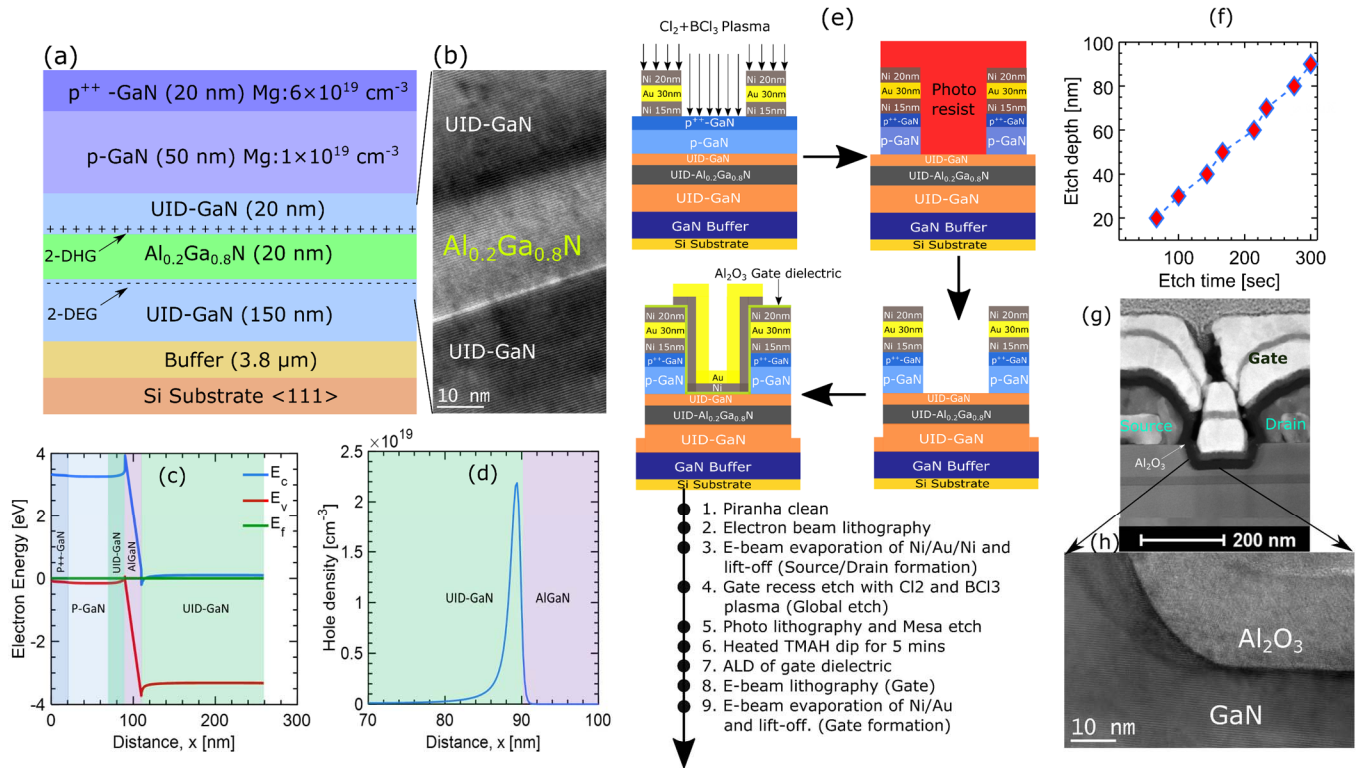


Fig. 1: (a) MOCVD grown epitaxial structure on 6-inch Si wafer. (b) TEM image of the GaN/AlGaIn/GaN double heterostructure. (c) Simulated electron energy band diagram of the epitaxial structure. (d) 2-DHG at the interface of GaN/AlGaIn heterostructure (2-DHG density = $8 \times 10^{12} \text{ cm}^{-2}$). (e) Illustrative process flow for the formation of self-aligned E-mode p-channel FET. Here, the gate recess is enabled by 20 nm of Ni on top of Ni/Au ohmic contact which serves as the etch mask and protects the ohmic contact from the plasma damage. (f) Etch depth vs etch time for the gate recess etch. (g) STEM cross-section view of the fabricated self-aligned device. (h) TEM image of the GaN / gate dielectric interface showing the high quality of gate recess with low surface roughness.

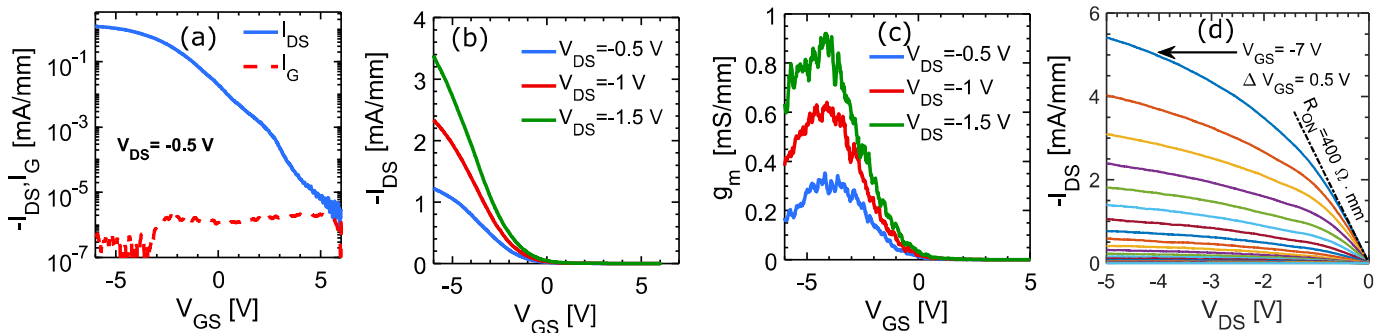


Fig. 2: (a) Semi-log plot of I_{DS} vs V_{GS} at $V_{DS} = -0.5 \text{ V}$ demonstrating an ON-OFF ratio of 6×10^5 . In the ON-state, the gate leakage current is quite small in the range of 1 nA/mm. However, an increase in gate leakage is observed in the OFF-state of the device, mainly because of the high electric field at the drain-end of the transistor. (b) Linear scale plot of I_{DS} vs V_{GS} demonstrating a threshold voltage of -1 V . (c) Measured g_m vs V_{GS} characteristics with a peak transconductance of 0.9 mS/mm. (d) Measured I_{DS} vs V_{DS} characteristics demonstrating record ON-resistance of $400 \Omega \cdot \text{mm}$.

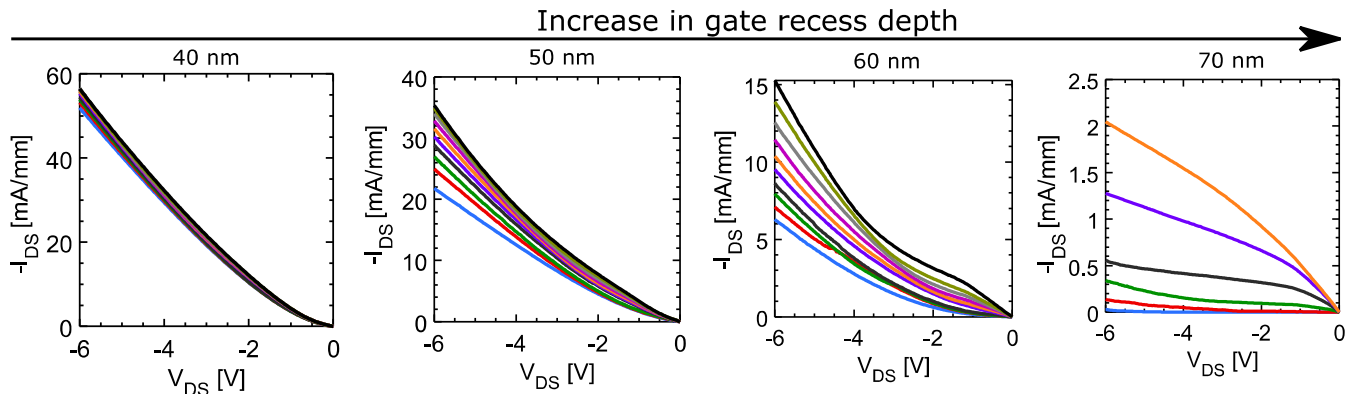


Fig. 3: I_{DS} vs V_{DS} characteristics of the self-aligned p-FET with different recess depths, demonstrating that a shallow recess yields higher ON-current at the expense of low ON-OFF ratio (here, $V_{GS, \min} = -5 \text{ V}$ and $\Delta V_{GS} = 1 \text{ V}$). Devices with less than 70 nm recess depth could not be fully turned off because of the conduction through the un-etched p-GaN beneath the gate.

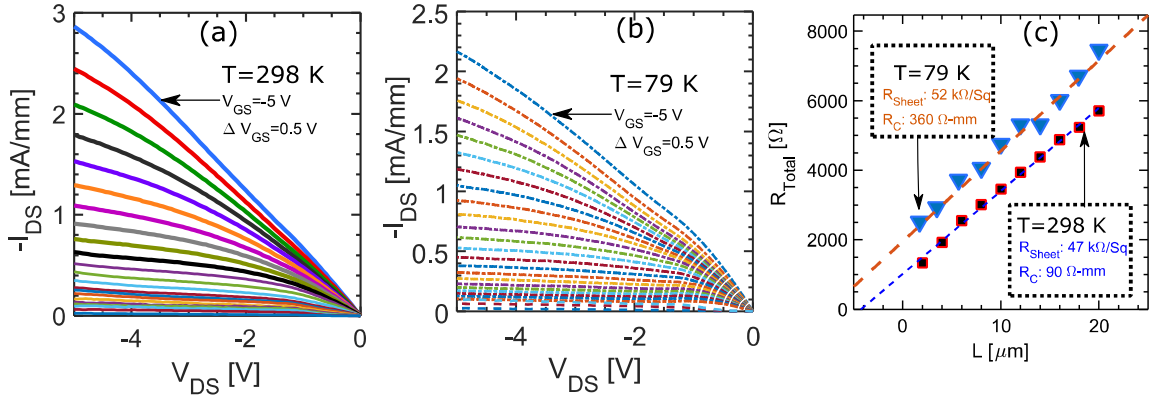


Fig. 4: I_{DS} vs V_{DS} characteristics of the self-aligned p-FET with 500 nm channel length and 70 nm recess depth at (a) room temperature $T=298$ K and at (b) cryogenic temperature $T=79$ K. It is quite evident that at low temperature, drain current is reduced by $\sim 20\%$ for the same gate voltage. This reduction in current can be explained in terms of the increase in contact resistance at low temperature. (c) Linear TLM measurement results at $T=298$ K and $T=79$ K. As shown here, a reduction in temperature leads to an increment of both the sheet resistance and the contact resistance. This is because of the lower activation ratio of Mg at low temperature.

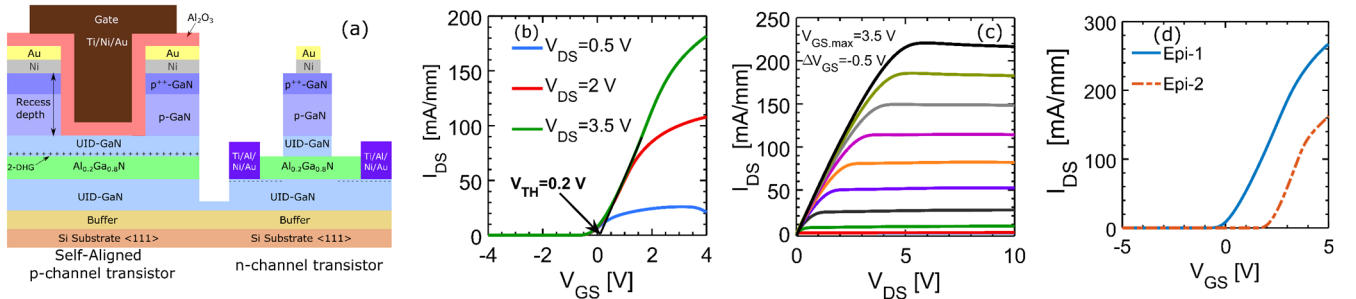


Fig. 5: (a) Monolithic integration of self-aligned p-FET and p-GaN gated n-FET. (b) I_{DS} vs V_{GS} characteristics of the n-FET in linear scale demonstrating a threshold voltage of 0.2 V. (c) I_{DS} vs V_{DS} characteristics of the n-channel FET. (d) I_{DS} vs V_{GS} characteristics of the p-GaN gated n-FETs fabricated using two different epitaxial structures described as follows, *Epi-1*: same as epi-structure used in this work (see Fig. 1(a)), *Epi-2*: Epi-structure used for conventional E-mode p-GaN gated AlGaIn/GaN HEMT – 70 nm p-GaN (Mg: 10^{19} cm^{-3}), 15 nm $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ (Si: $5 \times 10^{16} \text{ cm}^{-3}$), 150 nm UID-GaN (Si: $5 \times 10^{16} \text{ cm}^{-3}$). This reflects that insertion of UID-GaN layer and thickening of AlGaIn layer shifts the threshold voltage towards zero which can be resolved by using FinFET structure.

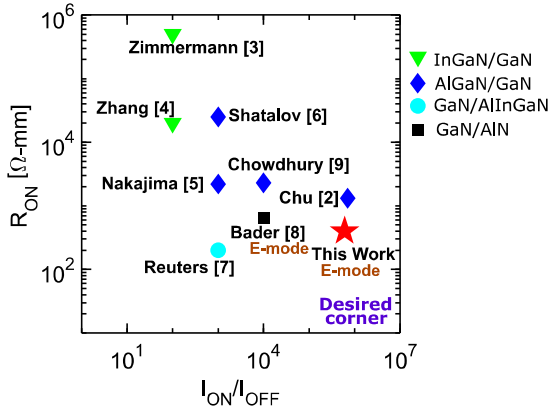


Fig. 6: Benchmarking of the reported self-aligned p-FET with other demonstrated p-FETs in the literature in terms of ON-resistance and ON-OFF ratio. It is quite evident that the reported device is closest to the desired corner exhibiting an ON-resistance of $400 \Omega \cdot \text{mm}$ with excellent ON-OFF ratio of 6×10^5 . The p-FET in this work enables easy integration with on-chip n-FET without any regrowth, as illustrated in Fig. 5(a). The device is E-mode with -1 V threshold voltage. This work shows record ON-resistance and ON-OFF ratio for any GaN-based E-mode p-FET, making it a promising candidate for GaN-based complementary logic.

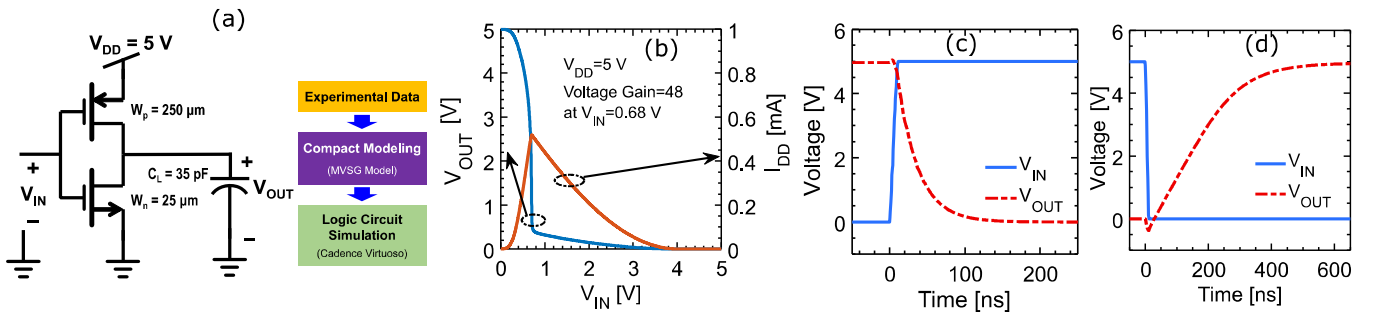


Fig. 7: (a) Circuit diagram and methodology used in this work to simulate the GaN-based complementary logic inverter. (b) Voltage transfer curve of the GaN-based complementary logic inverter. The n-FET and p-FET have gate widths of 25 μm and 250 μm , respectively. Simulated waveforms showing the (c) fall and (d) rise edge of the output signal from the inverter. The rise/fall time of the input signal is 10 ns. The fall and rise times of the output signal are 60 ns and 301 ns, respectively.