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A Two-stage Universal Input Charger with Wide Output Voltage Range

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Abstract—This paper presents the design of a two-stage 50W portable charger architecture with universal ac input and 5V/25W, 9V/45W, 12V/50W output. A 98.5% efficient valley-switched boost converter operating at 0.5-2MHz enables a 47% reduction in the buffer capacitor volume while a stacked-bridge LLC converter with a Variable-Inverter-Rectifier-Transformer (VIRT) offers greater than 96% efficiency across the wide output voltage range. The design demonstrates the potential and trade-offs of a two-stage architecture at this operating power.

I. INTRODUCTION

While miniaturization is highly desirable for ac/dc chargers, it is difficult to achieve due to the dual requirements of reducing volume and increasing efficiency [1]. Passive components in particular present a critical bottleneck towards miniaturization as advancements in passive components have lagged active devices. Magnetic passives suffer from poor scaling laws for miniaturization [2], and energy buffer capacitors must accommodate stubborn second-line-harmonic buffering requirements.

Most portable chargers rated below 75W utilize the architecture shown in Fig. 1¹. At their input they accept a “universal” ac input range (e.g. 90-265 Vac) and on their output they provide a fixed or variable dc bus, typically between 5V and 20V. Within the charger, a full-bridge rectifier feeds a capacitive energy buffer in order to establish an internal dc bus which has an undesirable but unavoidable second-line-harmonic voltage ripple. This bus then connects to an isolated dc/dc converter which is responsible for regulating the output voltage while also establishing isolation to satisfy safety requirements. Finally, input EMI filtering is required to satisfy EN55022 Class B requirements. In this architecture, the capacitive energy buffer, the transformer in the isolated dc/dc converter stage, and the EMI filter typically comprise the dominant contributions to passive component volume.

The minimization of these three passive component blocks is governed by distinct design considerations. The size of the EMI filter can be reduced by increasing the switching frequency of the dc/dc converter, as this increases the required filter corner frequency and therefore enables smaller filter inductance and capacitance values. The transformer’s size and efficiency may also be improved by operating at higher frequencies, up to the performance limits of available

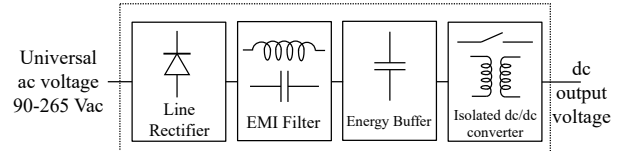


Fig. 1: Conventional architecture for portable chargers.

core materials and winding technologies [3]. Additionally, because the transformer is employed as part of a dc/dc converter, the properties of that converter can be leveraged to better utilize the transformer and improve performance. For example, the recently-proposed Variable-Inverter-Rectifier-Transformer (VIRT) structure enables transformers with effective fractional-turn secondaries while also enabling voltage gain reconfiguration to accommodate a wide output voltage range; these properties can be especially valuable in portable charger designs [4], [5]. On the other hand, the size of the capacitive energy buffer is dictated by the maximum voltage ripple that the dc/dc converter stage can tolerate and cannot be reduced by operating the dc/dc converter at higher frequency.

An electrolytic capacitor is typically used to implement the energy buffer. The volume of the capacitor is related to the peak energy it stores, namely $E_{pk} = CV_{ac,max}^2$, where C is the capacitance and $V_{ac,max}$ is the maximum ac rms input voltage (265 Vac). Thus, the buffer size can only be reduced by using a lower capacitance value. However, the capacitance is limited by the voltage range requirements of the dc/dc converter stage. This can be seen by evaluating the energy stored in the capacitor,

$$E_{stored} = \frac{1}{2}C(V_{bus,max}^2 - V_{bus,min}^2), \quad (1)$$

where $V_{bus,max}$ and $V_{bus,min}$ are the maximum and minimum voltages across the capacitor, respectively. E_{stored} is dictated by the operating power and line frequency and $V_{bus,max}$ is set by the input ac voltage, leaving only $V_{bus,min}$ to be reduced in order to reduce C . Note that with a conventional passive front end, the capacitance must be sized for the worst-case energy storage condition where $V_{bus,max}$ is smallest, corresponding to the lowest applied ac input voltage.

The contradiction at the heart of sizing the energy buffer is that the capacitance is selected to satisfy ripple requirements

¹Note that converters rated below 75W are not subject to EN61000-3-2 line current “power factor correction” (PFC) regulations.

when the input voltage is lowest, but it must be physically sized for the voltage rating when the input voltage is highest. This motivates the concept of an “active buffer” in which an additional conversion stage is interfaced to the capacitor in order to better utilize its energy storage capability. This idea has primarily been investigated in higher power designs employing power factor correction (PFC) stages [6], but some work has considered this concept in lower-power applications as well. For example, [7] evaluates the use of a boost- or buck-based PFC in a 60W ac-dc charger application, where the PFC is operated in a conventional manner as in higher power designs, and [8] proposes a merged rectifier and boost topology to reduce the buffer size both by increasing the minimum dc bus voltage and by enabling the injection of harmonic currents. The architecture presented in this paper is distinct as it leverages a high efficiency miniaturized boost converter for the active buffer which effectively serves as a drop-in replacement for the capacitor itself. In particular, it does not control for a specific input power factor and it can be used with the rectification structure of the designer’s choice.

In this paper, we investigate a two-stage charger design accommodating universal ac voltage at its input and a configurable output of 5V/25W, 9V/45W, and 12V/50W. The design employs a 0.5-2MHz valley-switched boost converter as an active front end, used expressly for miniaturization of the energy buffer, and a 0.5-1.3MHz stacked-bridge LLC converter with a Variable-Inverter-Rectifier-Transformer (VIRT) for the isolated dc/dc converter stage to achieve small size of the power stage for wide output range.

First, we elucidate the design considerations involved in selecting the minimum and maximum bus voltage value and explore the trade-off between an active buffer and a passive buffer. This discussion then frames a quantitative analysis of the trade-off between buffer capacitor volume reduction and second-stage efficiency associated with selection of the minimum bus voltage. Then, we provide detail on the design of the two stages once the bus voltage profile has been selected. Finally, experimental results of the prototype two-stage conversion architecture are presented.

II. BUS VOLTAGE DESIGN CONSIDERATIONS

Selection of the bus voltage represents a key design parameter in the proposed two-stage design and affects the performance and operation of both of the stages. In this section, we elucidate the key design considerations involved in choosing the bus voltage profile.

A. Isolated dc-dc Converter Architecture

Given the wide output voltage range of 5V, 9V, and 12V and relatively high operating currents of 5A, 5A and 4.17A, respectively, the stacked-bridge LLC+VIRT converter [4] is an attractive candidate for this application. The circuit schematic is shown in Fig. 2. The operating principles of the VIRT architecture are explained in detail in [4]; here we instead

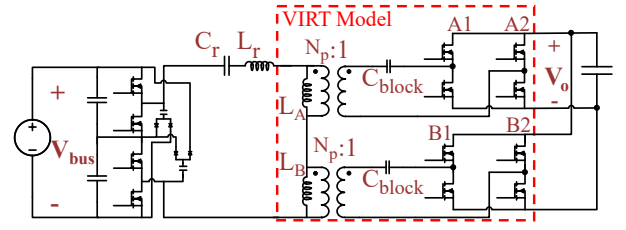


Fig. 2: Stacked-bridge LLC+VIRT, converter, implementing the isolated dc/dc converter stage in Fig. 1.

focus on its salient design features. The voltage gain of the stacked-bridge LLC+VIRT converter is

$$\frac{V_o}{V_{bus}} = M_{g,LLC} M_{inv} \frac{N_s}{N_p} \quad (2)$$

where $M_{g,LLC}$ represents the voltage gain of the LLC resonant tank, which is variable and controlled by the switching frequency of the inverter, M_{inv} is the gain of the inverter topology, and N_s/N_p represents the effective transformer turns ratio which is set by the VIRT operating mode,

$$\frac{N_s}{N_p} = \begin{cases} \frac{1}{2N_p}, & \text{FB/FB mode} \\ \frac{2}{3N_p}, & \text{FB/HB mode} \\ \frac{1}{N_p}, & \text{HB/HB (or FB/0) mode} \\ \frac{2}{N_p}, & \text{HB/0 mode.} \end{cases} \quad (3)$$

M_{inv} is a controllable quantity due to the stacked-bridge topology and the ability to operate in “variable frequency multiplier” (VFX) mode [9]:

$$M_{inv} = \begin{cases} 1/2, & \text{Inverter Mode 1} \\ 1/4, & \text{Inverter Mode 2 (VFX).} \end{cases} \quad (4)$$

This converter topology offers a high degree of flexibility in accommodating input and output voltage variations. In particular, assignment of the VIRT operating modes in (3) and the number of primary turns N_p are used to accommodate the output voltage range, as discussed in Section IV, while M_{inv} and $M_{g,LLC}$ accommodate input voltage variations and are therefore critical to consider in selecting the bus voltage as discussed below.

B. dc-dc Inverter Design

Considering the maximum ac input voltage of 265Vac, a natural maximum value of V_{bus} is 380V. While the boost front-end in principle enables larger $V_{bus,max}$, increasing this value aggravates the step-down burden of the dc-dc stage and compromises its performance.

The proposed stacked-bridge inverter offers two key advantages over the half-bridge inverter topology typically employed in LLC designs [10]. First, the voltage-quarterming gain in (4) can be beneficial for reducing the step-down burden of the LLC transformer. Second, while the stacked-bridge inverter requires twice the number of switches and the addition of a

voltage balancing circuit (ref. Fig. 2), each of the switches has half the voltage rating of the switches in the half-bridge inverter. This is highly beneficial in this design as it enables the use of 350V rated Gallium Nitride (GaN) devices instead of 600/650V rated devices, which currently represent the next available voltage class of this technology. In particular, we employ 350V EPC2050 devices which have an $R_{on} * C_{oss}$ figure-of-merit that outclasses any available 600/650V devices at the time of writing. Further, these devices have a footprint of 4 mm² such that four of them together have a lower area footprint than a single 600/650V device of interest (e.g. 33 mm² for a GS66504B device or 64 mm² for a PGA26E07BA device). This reduction in packaged device area is partly driven by the difference in creepage distances and resulting packaging for these different voltage ratings. Thus, the ability to employ these lower voltage devices strongly mitigates the drawback of the increased switch count of the stacked-bridge inverter and the topology is well-suited for miniaturization in this application.

It is sensible to operate the inverter in Mode 2 (multiplier mode, with small gain) when V_{bus} is at its maximum in order to minimize the step-down burden of the dc-dc stage. However, the question of when to operate in Mode 1, or if to operate in this mode at all, depends on further design considerations which we address in Section III.

C. LLC Converter Gain Variation

When operating at the resonant frequency defined by L_r and C_r in the LLC converter, $M_{g,LLC} = 1$ in (2). This is typically the most efficient operating point of this topology [10]. Although $M_{g,LLC}$ may be greater than or less than unity depending on operation below or above the resonant frequency, respectively, we focus on operation at or below resonance as is conventionally done to ensure Zero Voltage Switching (ZVS) of the inverter switches [10]. In this case, we assign the maximum bus voltage $V_{bus,max} = 380V$ to the resonant frequency and primarily use the increase in gain below the resonant frequency to accommodate decreases in the input voltage. Thus, the required LLC converter gain variation, and in particular the maximum gain $M_{g,LLC,max}$, is defined by the minimum energy buffer voltage, $V_{bus,min}$.

While the selection of $V_{bus,max}$ is naturally dictated by the maximum input voltage requirement, selecting $V_{bus,min}$ represents the key design trade-off of this two-stage architecture. As $V_{bus,min}$ is decreased, the gain burden of the LLC converter is increased, which tends to reduce the efficiency of the dc-dc converter stage as discussed in Section IV-A. However, this also reduces the required buffer capacitance for the same energy storage capability as described in (1), which can help to minimize the volume of the buffer capacitor. For the purposes of discussion, we initially restrict the LLC gain to be less than or equal to two. This constraint is revisited in Section IV.

III. TRADE-OFF BETWEEN AN ACTIVE AND PASSIVE BUFFER

Based on the inverter gain profile in (4) and a maximum LLC gain of two as discussed in Section II-C, the allowed bus

voltage range is 190-380V (operating the inverter in Mode 2) or 95-190V (operating in Mode 1).

First, we consider the design of the energy buffer if only a passive rectifier front end and bulk electrolytic capacitor is used. In this case, with no boost capability, sizing of the energy buffer capacitor is dictated by the minimum input voltage of 90Vac ($127V_{pk}$). In this case, we operate the inverter in Mode 1 and a 100 μ F buffer capacitor² is required to keep the bus voltage above 95V under a constant 50W power draw. A good 400V/100 μ F candidate is EPCOS-TDK B43644A9107M000, which has a volume of 9.5 cm³ and an ESR of 0.87 Ω corresponding to approximately 0.63W of loss at 50W.

An alternative to using an electrolytic capacitor is to use a bank of ceramic capacitors. Ceramic capacitors generally have much lower ESR but suffer from a capacitance that is highly dependent on the applied voltage. For example, the 400V/2.2 μ F EPCOS-TDK C5750X6S2W225K250KA has been identified as having excellent energy density capability [11], but has a capacitance derating to approximately 0.44 μ F at 400V. ESR data for ceramic capacitors is typically provided for frequencies above 1kHz, since they have not conventionally been designed or marketed with low-frequency energy buffering in mind. By extrapolating manufacturer-provided data for ESR, we estimate an ESR of 2.6 Ω per capacitor. Considering a capacitance derating to 1.1 μ F at a dc bias of 120V, 91 pieces of the ceramic capacitor are required, yielding a total volume of 6.5 cm³ and a negligible net ESR of 28.6m Ω at 100Hz³. This makes the ceramic buffer solution attractive for miniaturization compared to an electrolytic buffer, but it leverages a very high number of ceramic capacitors which may be prohibitive from a cost and/or manufacturing perspective.

An active front-end boost converter enables use of a greatly reduced buffer capacitance value, and can help make the use of high energy density ceramic capacitors more viable. This is because it enables energy to be buffered at high voltage even for low ac voltage conditions, and permits energy to be drawn from the line over a more desirable fraction of the line cycle. The selected front-end valley-switched boost converter and its gating logic are shown in Fig. 3. The converter is topologically simple, requiring only one low-side switch, and a recently proposed optimization approach offers a means to achieve high efficiencies in volume-constrained designs operating at MHz frequencies [12].

For the valley-switched boost converter to operate efficiently it must achieve ZVS which is theoretically possible only when its output voltage is at least twice the input voltage. It is important here to note that the universal input ac connection does not represent a continuously serviceable range and is instead split into a set of “low-range” voltages (90-132Vac) and “high-range” voltages (198-265Vac) associ-

²In this study, capacitor sizing is determined via a MATLAB/Simulink simulation of a diode bridge rectifier interfaced to a buffer capacitor in parallel with a constant power load.

³Measurements in lab confirm that this ceramic capacitor bank has negligible loss compared to the electrolytic capacitor alternative.

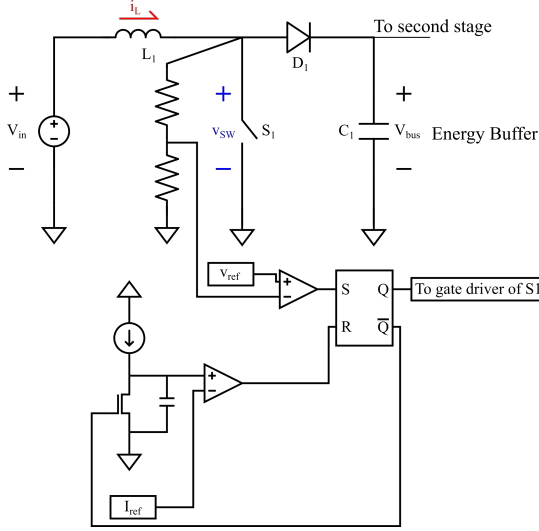


Fig. 3: Valley-switched boost converter, including control logic used to implement valley switching [12].

ated with Japanese/American and European voltage ranges, respectively. The maximum low-range voltage of 132 Vac corresponds to 187V peak, which is slightly less than half of the selected maximum bus voltage of 380V. Thus, by choosing to boost to 380V we can in principle operate the converter with ZVS over the entire low-range. On the other hand, we cannot achieve ZVS for all of the high-range voltages. Instead, we bypass the converter in this regime and rely on passive buffering⁴. In this case, we operate the inverter exclusively in Mode 2 and utilize a 17 μ F buffer capacitor, corresponding to 26 pieces of C5750X6S2W225K250KA accounting for voltage de-rating at 250V, the minimum required to keep the bus voltage above 190V under a constant 50W power draw. Note that the buffer capacitance requirement is reduced by approximately 5.9 times compared to the case without boost capability owing to the energy buffering occurring at much higher voltages and the larger spread between the minimum and maximum voltage (i.e. 190-280V bus voltage ripple in this case versus 95-127V worst-case ripple with no boost capability).

IV. QUANTITATIVE ANALYSIS OF $V_{bus,min}$ TRADE-OFF

In the previous section we assumed a maximum LLC gain of two in order to assess the benefit of an active buffer in this application. Here, we consider the impact of different values of $M_{g,LLC,max}$ on the capacitor buffer volume and second-stage efficiency when an active front-end is employed.

A. LLC Efficiency Impact

In general, LLC design is an iterative process that involves choosing the inductance ratio $L_n = L_r/L_m$, where L_r and

⁴In principle, one can enter a partial boosting mode in this regime such that the converter provides boost capability up to 190V at the input, and then enters pass-through mode above this voltage. This can further reduce the buffer capacitance at the cost of increased operational complexity.

TABLE I: Example influence of $M_{g,LLC,max}$ on LLC loss and buffer size using C5750X6S2W225K250KA capacitors, assuming $L_n = 5$.

$M_{g,LLC,max}$	$V_{bus,min}$	Relative LLC i_{pk}^2	C [μ F]	Num. pcs.
1.25	304	1.0	-	-
1.5	253	1.7	60	100
1.75	217	2.4	25	39
2.0	190	3.1	17	26
2.25	170	4.0	14	21

L_m are the resonant and effective magnetizing inductance, respectively, and choosing the effective quality factor $Q_e = 2\pi f_r L_r / R_e$, where f_r is the resonant frequency and R_e is the effective load resistance mapped to the primary [4], [10]. The LLC is capable of servicing a wide gain range, but by focusing on the resonant operating point of the LLC converter we can glean useful insight into the efficiency impact of the choice of $M_{g,LLC,max}$. Further, since this point typically represents the most efficient operating regime of the LLC converter [10], it is a useful representation of overall converter performance.

At the resonant frequency of the LLC converter, a square wave voltage is imposed on the magnetizing inductance such that the resulting current waveform is triangular with a peak value of

$$i_{pk} = \frac{V_o}{R_e} \frac{\pi N_p}{2 N_s} \frac{1}{L_n Q_e}. \quad (5)$$

The maximum gain of a given LLC design is associated with the boundary between the capacitive and inductive mode in below-resonance operation [13]. This constrains the design according to

$$L_n Q_e \approx \sqrt{\frac{1 + L_n (1 - M_{g,LLC,max}^{-2})}{M_{g,LLC,max}^2 - 1}}. \quad (6)$$

Eqns. (5) and (6) show that the peak magnetizing current is reduced when the $L_n Q_e$ product is increased, and this is associated with minimizing $M_{g,LLC,max}$. The peak value of the magnetizing current is important for achieving ZVS of the inverter switches, but otherwise represents an unavoidable component of circulating current which increases loss in the LLC converter. Thus, in principle, the lower the maximum gain requirement of the LLC, the more efficiently it can be operated⁵. The squared value of the peak current in (5) is representative of the loss impact of this circulating current, and relative values of i_{pk}^2 for different values of $M_{g,LLC,max}$ are enumerated in Table I. This table is generated for an example value of $L_n = 5$, which is a typical starting point in LLC designs [10], and a similar trend exists for other values of L_n according to (6).

⁵Note that ZVS can be achieved for a given value of $M_{g,LLC,max}$ through selection of the values of L_n , Q_e , and f_r .

TABLE II: Nominal mode voltages associated with each VIRT mode for varying N_p .

N_p	FB/FB	FB/HB	HB/HB
8	6.0	8.0	11.9
10	4.8	6.3	9.5

B. Capacitor Buffer Sizing

For the example range of $M_{g,LLC,max}$ in Table I we can determine the buffer capacitance that is required to satisfy the associated minimum bus voltage requirement and compute the required number of C5750X6S2W225K250KA pieces considering appropriate voltage derating. The results of this analysis are shown in Table I. Note that there is no capacitance entry for the $M_{g,LLC,max} = 1.25$ case since the associated minimum bus voltage cannot be accommodated when the input voltage is 198Vac.

C. Selecting $V_{bus,min}$

The results in Table I offer a guide for selecting $V_{bus,min}$. For example, if the given design has the volume budget for 100 ceramic capacitor pieces, the use of the boost converter allows the LLC to be operated with $M_{g,max} = 1.5$ whereas a passive buffer would require $M_{g,max} = 2$ (ref. Section III). This corresponds to a more efficient LLC design.

In practice, our aim is to utilize the boost converter to reduce overall converter volume. Table I shows that increasing the maximum gain from 1.5 to 1.75 yields a substantial capacitor volume savings of 4.4 cm³ for a relative loss penalty increase of 41%. Moving from a maximum gain of 1.75 to 2.0 yields a further volume reduction of 0.92 cm³ while incurring a loss penalty increase of 30%. A further increase to 2.25 maximum gain yields only a 0.36 cm³ volume reduction at the cost of an additional 29% relative loss penalty increase. We see that there are diminishing returns on overall volume reduction for increasing the maximum LLC gain, and a maximum gain of around two is a good trade-off in this example between LLC performance and capacitor volume reduction.

V. DESIGN OF THE TWO CONVERSION STAGES

With an understanding of the design trade-offs involved with selecting $V_{bus,min}$ we can now complete the design of the two stages of the converter.

A. VIRT Mode Assignment

As discussed previously, we operate the LLC inverter in Mode 2 and associate the LLC resonance with $V_{bus,max} = 380V$. Using (2) we can enumerate the output voltage associated with each VIRT mode at resonance as we vary the number of primary turns N_p . We refer to these as the “nominal” mode voltages and they, in principle, represent the most efficient operating voltage in each VIRT mode. The nominal voltage of each VIRT mode for different values of N_p are shown in Table II, where we omit HB/0 mode due to the 4x gain variation offered by this mode having limited value in this application.

Achieving high efficiency in both the 9V/45W and 12V/50W cases is important to minimize the total loss of the converter. The efficiency of the 5V/25W case is of less concern (e.g. 2W of loss corresponds to a predicted 96% efficiency at 50W, 95.6% efficiency at 45W, and 92% efficiency at 25W). From this perspective, $N_p = 8$ appears to be an attractive choice, as it places 9V and 12V near the nominal voltage of the FB/HB mode and HB/HB modes, respectively. However, this places the 5V operating point well above FB/FB resonance. Although the efficiency in this mode is not of primary concern, designing the LLC to achieve attenuation to 5V in this case compromises the achievable efficiency in the other two modes, as part of the available design freedom is lost to meeting this attenuation constraint rather than optimizing performance in the higher power modes. On the other hand, $N_p = 10$ comfortably sets 5V in FB/FB mode, and 9V and 12V in HB/HB mode, with only approximately 5% attenuation required in HB/HB mode to achieve 9V operation. This relatively low attenuation is typically achievable in many LLC designs without requiring special consideration.

B. LLC Converter Design

The required gain curve can be implemented by many pairs of Q_e and L_n , and the choice of these parameters is typically an iterative process associated with meeting the gain requirements within a desired frequency window while also achieving realizable passive component values. From a miniaturization perspective, it is desirable for the resonant inductance to be entirely sourced from the leakage inductance of the transformer, as this eliminates the need for an additional external inductor. To achieve this, we employ a non-interleaved design in which the primary and secondary windings straddle opposite ends of the core window as indicated in Fig. 4 and discussed in [14]. Further, we utilize 450/48 Litz wire on the primary and secondary in order to mitigate the detriment of the non-interleaved configuration. A resonant frequency of around 1MHz is selected in order to aid future EMI filter miniaturization efforts while also enabling the use of high-performance-factor ML91-S core material, and a back-to-back EQ20 core configuration is selected in order to minimize transformer loss while also enabling a core window arrangement that is beneficial for achieving the desired leakage inductance value.

An optimal design has L_r equal to the leakage of the transformer, places the resonant frequency at or near 1MHz, and operates with the largest possible $Q_e L_n$ product to minimize circulating currents while also achieving ZVS of the inverter switches and meeting the required gain profile. The resulting design is shown in Table III and the components used in the prototype are listed in Table IV.

C. Valley-switched Boost Converter Design

The front-end boost converter is optimized according to the approach detailed in [12]. The resulting converter operates between 0.5-2MHz and the prototype parameters are listed in Table IV. However, high efficiency boost operation to 380V

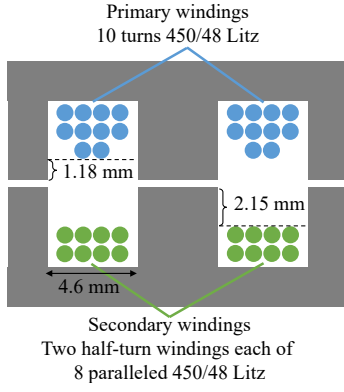


Fig. 4: Winding arrangement of EQ20/EQ20 back-to-back core halves (spacing of 0.004" in each leg) used in the prototype. The primary winding comprises 10 turns of 450/48 Litz wire, while the two half-turn secondaries each comprise 8 paralleled 450/48 Litz wire segments.

TABLE III: LLC parameters

Parameter	Value
Resonant frequency	1.13 MHz
Operating frequency range	0.5 - 1.3 MHz
Inverter operating mode	Fixed Mode 2
Number of primary turns (N_p)	10
VIRT Mode Assignments: 5; 9; 12V	FB/FB; HB/HB; HB/HB
Resonant capacitance (C_r)	4.88 nF
Resonant inductance (L_r)	4.1 μ H
Magnetizing inductance (L_M)	30.5 μ H

cannot be maintained over the entire input line cycle due to large losses associated with the large conversion ratio required when the input voltage is low. Thus, we apply segmented operation of the boost converter in which the bus voltage is regulated to 380V when the instantaneous input voltage is above 70V, marking the value around which boost converter efficiency is compromised, and we run the converter with a constant boost ratio below this value. As a result of this segmented operation, bus voltage ripple will exist even in low-range conditions where the boost converter is active. However, the resulting ripple is well above the minimum bus voltage requirement owing to buffering at voltages near 380V, and sizing of the capacitor for passive buffering in the worst-case high-range operation.

VI. EXPERIMENTAL EVALUATION

The two stages of the prototype converter are shown in Figs. 5 and 6, respectively, and the component volumes are listed in Table V. The net (displacement) volume of the VIRT transformer, rectifiers, output capacitors, LLC resonant capacitors, and the stacked-bridge inverter and balancer is 10 cm³. Note that we omit the volume of logic and control circuitry in this metric as these represent circuit components

TABLE IV: Components used in prototype

Component	Value
Second-stage Inverter	
GaN FETs	350V EPC2050
Gate drivers	LMG1210
Signal isolators	Si8620
Balancer diodes	MMBD3004BRM
Balancer capacitors	1uF/450V/1812
VIRT Rectifiers	
MOSFETs	30V TPN2R703NL
Gate drivers	LM5113
Blocking capacitors	3x 4.7uF/25V/0805 per rectifier
Decoupling capacitors	2x 4.7uF/25V/0805 per half-bridge
Output capacitors	8x 10uF/25V/1210
LLC	
Resonant capacitor	3300pF/1kV/C0G/1210 + 1000pF/2kV/C0G/1812 + 470pF/2kV/C0G/1812 + 100pF/2kV/C0G/1206
Resonant inductor	4.1 μ H derived from transformer
VIRT Transformer	
Core	EQ20+EQ20/ML91-S, 0.004 " gap on all legs
Primary windings	Ten turns of 450/48 Litz wire wound in three layers (4/4/2).
Secondary windings	Two half-turn secondaries each comprising 8 paralleled 450/48 Litz wire segments.
Front-End Boost Converter	
S_1	GS66504B
D_1	C3D1P7060Q
Input and output decoupling capacitors	ea. 1x C5750X6S2W225K250KA
Boost inductor	41.4 μ H, RM6/3F46, 21 turns 450/48 AWG Litz wire
Buffer capacitors	24x C5750X6S2W225K250KA (\approx 16 μ F effective)
Line Rectifier	
Rectifier	Z4DGP406L

that can be miniaturized by other established means, such as implementation in an integrated circuit. We also do not quote an overall box volume as the prototypes are not optimally packaged. However, these component volumes provide insight into the achievable power density of this architecture.

The measured overall ac-dc system efficiency of the prototype (including the loss of the line rectifier) is shown in Fig. 7a. These results are obtained under closed-loop control with the front-end (line-interface) stage adjusting the on-time of the boost converter switch in order to regulate the bus voltage, and the back-end (dc-dc stage) adjusting its operating frequency in

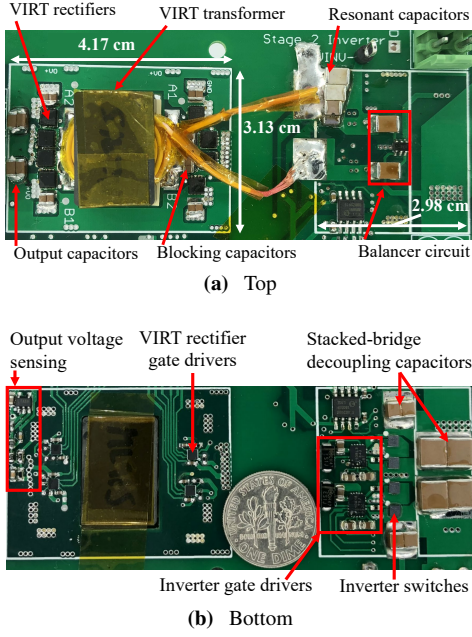


Fig. 5: Stacked-bridge LLC+VIRT prototype

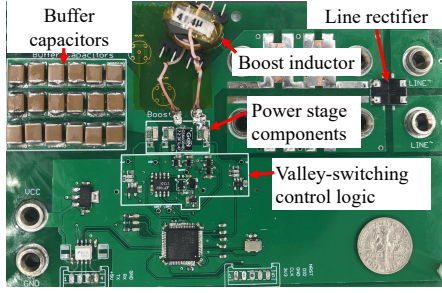


Fig. 6: Valley-switched boost converter prototype

order to regulate the output voltage to the desired value. The individual power-stage efficiencies of the front-end and back-end are shown in Figs. 7b and 7c, respectively. The high-range efficiencies in Fig. 7a are much higher than the low-range efficiencies because the boost converter is bypassed (i.e. switch S_1 is held off) and the input current yields lower line rectifier loss at higher input voltages. The limiting condition in terms of overall converter loss is 90 Vac, 12V/50W in which 3.25W loss is generated. If rectifier losses are omitted, the worst-case loss is in the 132 Vac, 12V/50W case. This is expected from the drop-off in the front-end efficiency above 145V in Fig. 7b. We note that this drop in efficiency does not impact sub-100Vac operation since the input voltage remains less than 130V in this regime, and that above this regime the boost converter only partially operates at these less efficient operating points. In the worst case of 132Vac the input voltage is above 145V approximately 44% of the time. We also note that although there is a drop-off in 5V/25W efficiency at 132Vac in Fig. 7a, the associated loss of 2.4W is well below the limiting case of 3.25W in the 90Vac 12V/50W operating mode, affirming the relative unimportance of this lower power condition on overall

TABLE V: Prototype component volumes

Component	Volume [cm ³]
Isolated dc/dc Stage	
Transformer	5.3
VIRT circuitry and output capacitors	2.5
Stacked-bridge inverter circuitry and by-pass capacitors	2.1
LLC resonant capacitors	0.1
Total	10
Front-end Stage	
Power stage components	0.97
Boost inductor	2.3
Buffer capacitors	1.7
Gate driver (AND gate buffer)	0.05
Total	5.02
Line Rectifier	
Line Rectifier	0.26

converter loss.

The back-end efficiency in Fig. 7c is reduced for bus voltages near 190V, which is expected since here we must operate the LLC well above its resonance, near its maximum gain. However, when the boost converter is active for the low-range inputs, the bus voltage is kept within a tight range of 320-380V in the worst-case where the second stage delivers 50W to the load as shown in Fig. 8. Thus, when the boost converter is active the second-stage is operated with high efficiency and this helps to mitigate the increased loss incurred from boost operation. Similarly, when the boost converter is bypassed for high-range inputs, the bus voltage swings down to approximately 190V, thus incurring higher loss in the second-stage. However, this increased loss is mitigated by the elimination of much of the boost converter losses, and overall efficiency remains high. Finally, we see in Fig. 7b that the front-end boost stage operates with greater than 98.5% efficiency for much of the line cycle (below $\sim 140V$). At 50W this corresponds to a loss of approximately 0.75W. In Section III we noted that a 400V/100 μ F B43644A9107M000 electrolytic capacitor could satisfy the bus voltage requirements in the 90Vac/50W case in lieu of an active buffer, with a loss penalty of approximately 0.63W. Thus, by using the active buffer we incur approximately 120 mW of additional loss in this limiting case (0.2% efficiency at 50W) but are able to reduce overall buffer volume by about 50% corresponding to an overall reduction in converter component volume of approximately 23%. This can be an attractive trade-off for miniaturization in portable charger designs.

VII. CONCLUSION

This paper presents a two-stage 50W charger architecture with a valley-switched boost converter on the front-end and a stacked-bridge LLC+VIRT converter on the back-end. Two-stage architectures at this power level are shown to be both

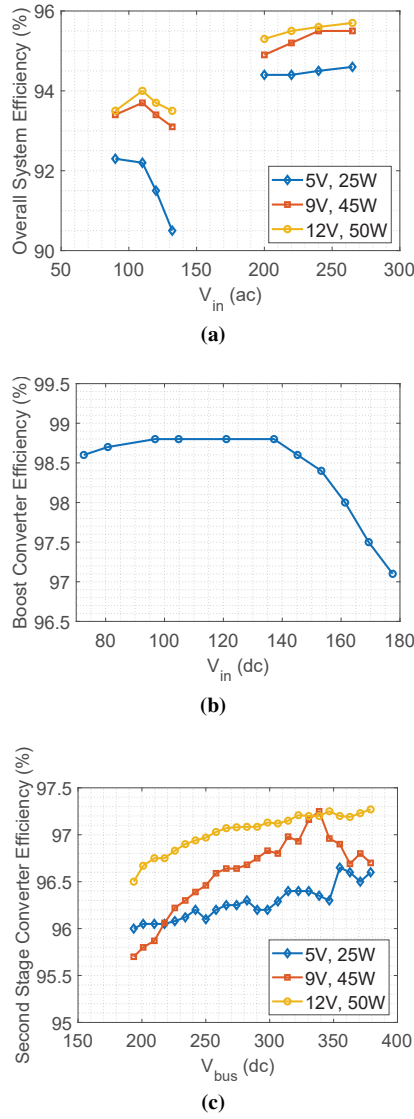


Fig. 7: Experimentally measured power-stage efficiencies. (a) Overall system conversion efficiency. (b) Front-end valley-switched boost converter efficiency at 50W. (c) Isolated dc-dc converter stage efficiency.

viable and advantageous from a component size perspective, owing to the ability to design high-performance miniaturized front-end converters, even in applications with variable voltage and load conditions. The design considerations involved in selecting the bus voltage profile are presented, and a quantitative framework for understanding the trade-off between capacitor buffer volume and second-stage efficiency is discussed. Experimental results demonstrate the efficiency and volume savings of the two-stage architecture, with an approximately 50% reduction in energy buffer volume corresponding to a 23% reduction in converter component volume.

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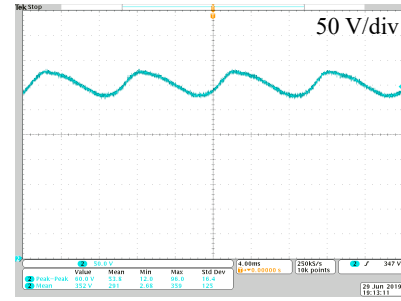


Fig. 8: Example bus voltage profile with a 90Vac, 50Hz input voltage and the second-stage delivering 50W to the load.

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