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R&D of Back-End Electronics for improved Resistive Plate Chambers for the Phase 2 upgrade of the CMS end-cap muon system

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Abstract

Purpose: The Large Hadron Collider (LHC) at European Organization for Nuclear Research is planned to be upgraded to the high luminosity LHC. Increasing the luminosity makes muon triggering reliable and offline reconstruction very challenging. To enhance the redundancy of the Compact Muon Solenoid (CMS) Muon system and resolve the ambiguity of track reconstruction in the forward region, an improved Resistive Plate Chamber (iRPC) with excellent time resolution will be installed in the Phase-2 CMS upgrade. The iRPC will be equipped with Front-End Electronics (FEE), which can perform high-precision time measurements of signals from both ends of the strip. New Back-End Electronics (BEE) need to be researched and developed to provide sophisticated functionalities such as interacting with FEE with shared links for fast, Slow Control (SC) and data, in addition to Trigger Primitives (TPs) generation and Data AcQuisition (DAQ).

Method: The BEE prototype uses a homemade hardware board compatible with the MTCA standard, the Back-End Board (BEB). BEE interacts with FEE via a bidirectional 4.8 Gbps optical paired-link that integrates clock, data, and control information. The clock and fast/slow control commands are distributed from BEB to the FEE via the downlink. The uplink is used for BEB to receive the time information of the iRPC's fired strips and the responses to the fast/slow control commands. To have a pipelined detector data for cluster finding operation, recover (DeMux) the time relationship of which is changed due to the transmission protocol for the continuous incoming MUXed data from FEE. Then at each bunch crossing (BX), clustering fired strips that satisfy time and spatial constraints to generate TPs. Both incoming raw MUXed detector data and TPs in a time window and latency based on the trigger signal are read out to the DAQ system. Gigabit Ethernet (GbE) of SiTCP and commercial 10-GbE are used as link standards for SC and DAQ, respectively, for the BEB to interact with the server.

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Results: The joint test results of the BEB with iRPC and Front-End Board (FEB) show a Bit Error Rate of the transmission links less than 1×10^{-16}, a time resolution of the FEB Time-to-Digital Converter of 16 ps, and the resolution of the time difference between both ends of 160 ps which corresponding a spatial resolution of the iRPC of approximately 1.5 cm.
Conclusion: Test results showed the correctness and stable running of the BEB prototype, of which the functionalities fulfill the iRPC requirements.

Keywords CMS · iRPC · BEE · TP · DAQ · SC

1 Introduction

The increased energy and luminosity of future upgrades of the Large Hadron Collider (LHC) will bring harsh background environments and high pile-up, which will impact many of the detectors used in the experiment. Compact Muon Solenoid (CMS) is one of the four major experiments of LHC with muon detectors that accurately identify and measure the momentum of individual muons. One of the tasks for the Phase-2 CMS upgrade is to install an improved Resistive Plate Chamber (iRPC) in the forward region to enhance the redundancy of the Muon system and to obtain a robust track reconstruction[1,2]. The iRPC is a double-gap detector with signal pickup strips in the middle and read out by a new Front-End Electronics (FEE) with Time-to-Digital Converter (TDC). As shown in Fig.1, the FEE measures the signal time at both ends of the strips and thus allows an estimation of the hit position along the strip in addition to the perpendicular one. The position of the strip with hit represents the information of the X coordinate, and the calculated time difference (position along the strip) represents the information of the Y coordinate of hit. The FEE has an excellent timing resolution of about 11–20 ps, resulting in a positional resolution of about 1.7 cm along the strip for iRPC[3,4]. The system configuration and time measurement of the FEE rely on the fast and Slow Control (SC) provided by the Back-End Electronics (BEE). The high-precision time information of the iRPC system requires high synchronization of each part and real-time transmission. CMS trigger system comprises two main layers, Level 1 (L1) Hardware Trigger and software High-Level Trigger. The L1 Trigger of the CMS trigger system collects the Trigger Primitives (TPs) from all the subsystems and provides a trigger decision, the Level-1 Accept (L1A) signal. The Level-1 hardware trigger system upgrade requires an L1A of 750 kHz and a latency of 12.5 μs[7]. The upgraded CMS Data AcQuisition (DAQ) system will allow detector data readout at rates up to 50 Tb/s and event rates up to 750 kHz[8]. The DAQ system also requires the BEE to provide the raw detector data and TPs associated with each L1A signal. Therefore, the design and development of the BEE are very critical.

The upgrade plan for iRPC will be in two significant periods. The prototype system is first developed compliant with the Micro Telecommunication and Computing Architecture (MTCA)[12] standard, taking full advantage of the development experience of the Beijing team during the CMS Phase-1 upgrade.

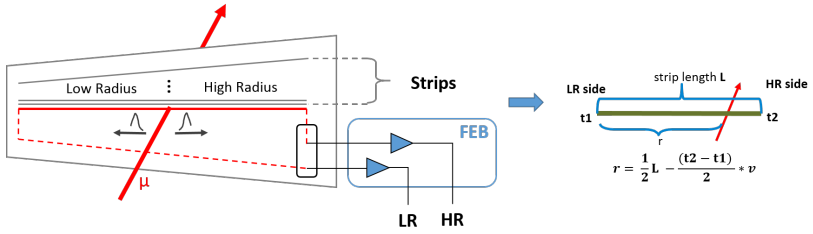

Figure 1: Illustration of the iRPC position measurement along the strip.

It is used for joint testing with iRPC detector, demonstrator, slice test, and detector installation for preliminary running. Then construct the final system of BEE based on the Advanced Telecom Computing Architecture[10] standard will be installed for the system running. This paper describes an MTCA-based iRPC Back-End Board (BEB) prototype with its functionalities that integrate fast and slow control, data reception, processing, and readout. Joint tests with the FEB and iRPC detector are performed together with data analysis, and test results are given with discussion.

2 Principle of Design

The structure of the iRPC electronic system is shown in Fig.2. Each half of the iRPC has 48 signal pickup strips, and a FEB is responsible for reading out at both ends, so each FEB needs to measure the arrival time of 96 channel signals. The FEB is equipped with 3 FPGAs, and each FPGA implements a 32-channel TDC. The 96 TDC channels need to have a unified time reference, and the time measurement of the signal should be consistent. The TDC data of the two FPGAs on the left and right are concentrated in the middle FPGA and then continuously output to the BEE. Therefore, the information interaction between the Front-End (FE) and Back-End (BE) includes fast control signals (time reference, etc.), SC commands (parameter configuration, etc.), and data (time information, etc.). To reduce the number of connections between the FE and BE, the clock, data, and control information are integrated into a single, bidirectional, serial optical link based on the idea of a shared link. According to the simulation of iRPC hit rate during high luminosity LHC[4], the data bandwidth of each FEB is 2.1 Gb/s.

The 4.8 Gbps GBT link[5] is selected to realize the point-to-point connection between the FEE and BEE, and the shared link design is realized through the secondary encapsulation of the GBT protocol. FEB adopts the radiation-tolerant GBT chipset[11] customized by CERN. The GBT chipset can be simplified into two parts: GigaBit Transceiver chipset (GBTx) and Slow Control Adapter (SCA). BEB implements the GBT link based on a full library (GBT-FPGA)[6] that can be instantiated on an FPGA.

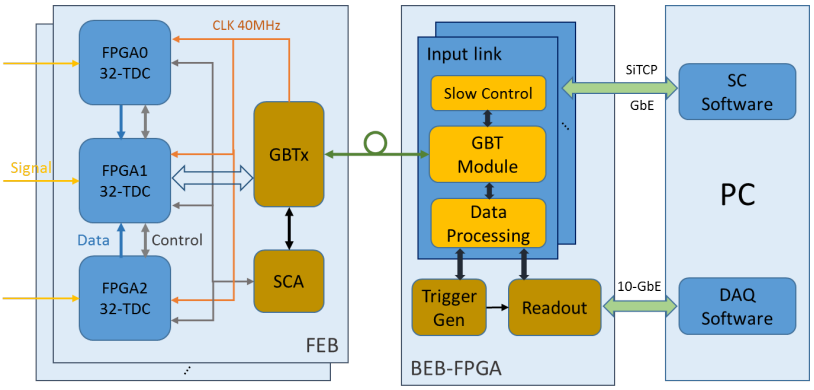

Figure 2: Schematic of the iRPC electronics system structure.

FEE is based on data-driven output, that is, continuous output as long as the signal is collected. FEB sorts the data generated by the 96 TDC channels by channel number, and the time relationship between the data is changed as it is sent. Therefore, BEE must receive and process in real-time, recovering the time relationship between incoming detector data. BEE then converts the detector data into the fired strips' position and time information and clusters these individual hits to produce TPs. TP is output to the next layer of the trigger system at bunch crossing (BX, 25 ns). This process does not allow dead time, so BEE must adopt the pipeline idea. Under the premise of calibrating the latency between the trigger signal and data, BEE selects raw detector data and TPS based on the trigger signal, packs and sends these data to the DAQ system according to the specified data format. This mechanism means that only relevant data regarding events of interest will be read out, thus making the data rate acceptable.

The firmware development of the BEB is the focus of this paper. To make single-board development more flexible and convenient, BEB implements the SC link with the server based on the SiTCP[9] protocol, and the commercial 10-GbE is used to realize the DAQ link with the server. The integration of SiTCP and 10-GbE in firmware is based on the gigabit transceivers (i.e., GTH) embedded in the FPGA of the BEB. The supporting SC and DAQ software is developed on the server.

3 Function Implementation

3.1 Back-End Board Hardware

The BEB is a modified version of a high-throughput MTCA-compliant electronic module [13–15] designed and developed by IHEP trigger team, as shown in Fig.3. The form factor of the BEB is a double-width size that conforms to

MTCA standards. The BEB uses one FPGA (XC7K70T) for board control and clock management, one FPGA (XC7V690T) for core algorithm implementation, one 128MB flash drive for automatic firmware loading after board power-up, one microprocessor (AT32UC3A1512) for implementing the MTCA crate intelligent management protocol, and three pairs of photoelectric conversion transceivers (Avago MiniPOD) to provide 36 bidirectiona up to 10.3125 Gbps high-speed optical links.

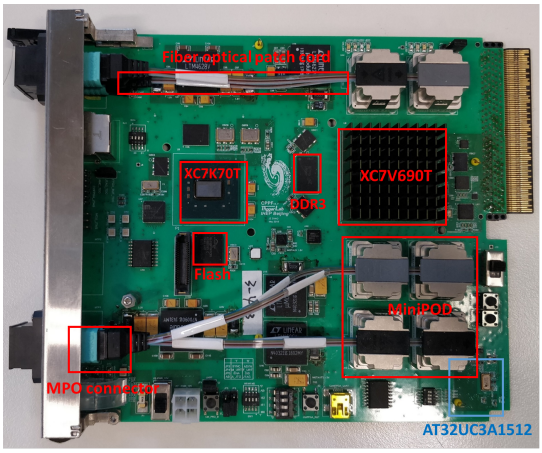

Figure 3: A photograph of the BEB.

3.2 Firmware Development

The functional architecture of the BEB developed is shown in Fig.4. Each BEB can handle inputs from multiple FEBs independently. The BEB buffers the uplink frames received via the GBT link, performs cross-clock processing and disassembles them into GBT SC and user data. Whether it is a TDC data or a FEE SC answers is determined from the FEB for user data. The DeMux algorithm recovers the time and positional relationship of the TDC data. Then the TDC data is clustered to give the spatial position of the hit as the TP output. TDC data and TPs are read out to the server according to the trigger signal for storage and offline analysis. GBT SC data and FEE SC answers were routed to the respective sub-modules for processing.

3.2.1 Transmission Link between FE and BE

The data frame width of the GBT link is 120 bits, the link clock is 40 MHz, and the line rate reaches 4.8 Gbps after parallel-serial conversion. The GBT link supports two encoding modes: GBT Frame and Wide Bus Frame. Fig.5(a)

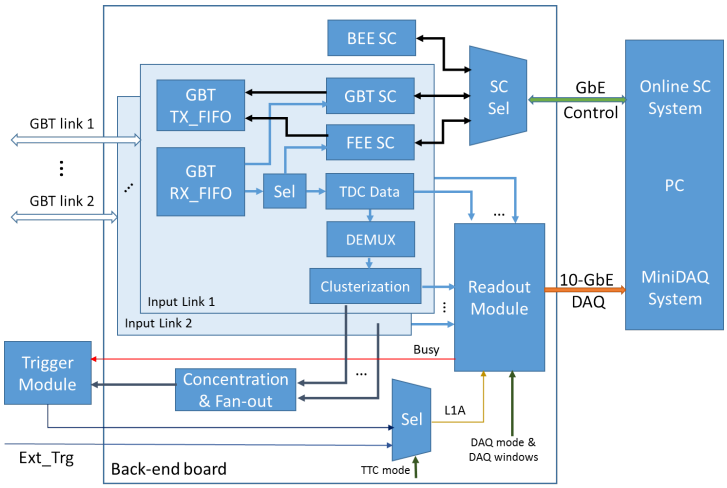

Figure 4: BEB function block diagram.

shows the GBT Frame encoding scheme. The highest 4 bits are used for the frame header (H), the next 4 bits are used for SC information, the lower 32 bits are used for error detection and forward error correction (FEC), and the other 80 bits are user-defined parts. Therefore, the effective data bandwidth in GBT Frame mode is 3.2 Gbps. In the Wide Bus Frame mode, the FEC field does not exist. As shown in Fig.5(b), the FEC field is replaced by user data at the cost of no error detection nor correction capability, the available bandwidth is 4.48 Gbps. The uplink from the FE to the BE adopts the Wide Bus Frame mode with higher bandwidth. Since the FEE is located in an intense radiation environment, the downlink from the BE to the FE adopts the GBT Frame mode with an error correction function.

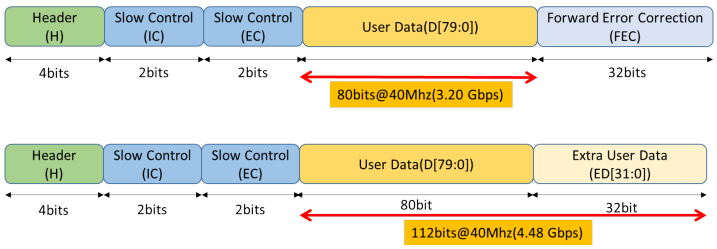

Figure 5: Top (a): GBT Frame encoding scheme. Bottom (b): Wide Bus Frame encoding scheme.

For the 4 bits of SC information in the GBT protocol, the upper 2 bits are ignored, and the lower 2 bits are used for the SC at the FEB level, based

on the SCA protocol[16]. The SCA protocol frame is split through the time-division multiplexing technology, and 2 bits of information are transmitted and processed in each clock.

The downlink user data (80 bits) carries two types of information: fast control signals and FEE SC requests. These two types of information are integrated through the definition of the data structure, as shown in Fig.6. FEE SC requests are divided into request and payload frames. SC transaction must always start with a request frame, which defines the read/write mode, data length, and access address of this transaction. The uplink user data (112 bits) carries three types of information: fast control status, response to SC read requests, and collected detector data (i.e., "TDC data"), which are integrated by defining the data structure, as shown in Fig.7. The multiplexing of TDC data and SC responses is based on a straightforward rule: TDC data always takes precedence over SC responses. Each frame is allowed to transmit up to 3 TDC data, and the TDC data is composed of 8-bit position and 24-bit time information.

Slow Control Request Frame	Fast Control							Slow Control Request Information				Slow Control Payload	
Field Name	Resync	BC0	Reset SCPath	Flush DataPath	Mute Channels	RSVD	FPGASel	RSVD	Wr Request	Length	Address	WrData0	WrData1
Field length	1	1	1	1	1	10	3	7	1	8	16	16	16

Slow Control Payload Frame	Fast control							Slow Control Payload			
Field Name	Resync	BC0	Reset SCPath	Flush DataPath	Mute Channels	RSVD	FPGASel	WrData(N)	WrData(N+1)	WrData(N+2)	WrData(N+3)
Field Length	1	1	1	1	1	10	3	16	16	16	16

Figure 6: Downlink data format from BE to FE. The top for FEE SC request frames and the bottom for FEE SC payload frames.

Data Frame	Fast Control Status						TDC Data Payload					
							TDC data		TDC data		TDC data	
Field Name	MiscStatus	SCFifoFull	DataFifoFull	SCFrame	RSVD	DataValid	TDC channel	Time value	TDC channel	Time value	TDC channel	Time value
Field Length	3	3	3	1	3	3	8	24	8	24	8	24

Slow Control Reply Frame	Fast Control Status					Slow Control Reply Payload					
						FPGA0		FPGA1		FPGA2	
Field Name	MiscStatus	SCFifoFull	DataFifoFull	SCFrame	DataVaild	RdData(N)	RdData(N+1)	RdData(N)	RdData(N+1)	RdData(N)	RdData(N+1)
Field Length	3	3	3	1	6	16	16	16	16	16	16

Figure 7: Uplink data format from FE to BE. The top for detector data frames and the bottom for FEE SC reply frames.

The BEE embeds the clock into the serial data stream via the GBT link and distributes the bunch crossing zero (BC0) signal to the FEE as a time reference, thereby synchronizing the FE and BE. Different FEBs have different physical connections to the BEBs due to their different positions on the detector, in short, different fiber lengths. Longer fibers will cause the signal to be delayed more due to transmission. By calibrating and compensating for the delay of each link, the inconsistency of the link connection is corrected. SC commands to calibrate the delay is embedded in the GBT link, so the measurement accuracy is 25ns.

3.2.2 Triggering Preprocessing

One of the tasks of BEE is processing the detector data to provide TPs, which will serve as the smallest unit in the downstream trigger object reconstruction algorithm. The fired strips of iRPC are clustered by setting constraints on time and space, and the position and each cluster's time information is transformed to obtain TP.

Due to the limited transmission bandwidth, the TDC data collected by the FEE at the same BX require multiple uplink frames to be completely sent to the BEE. However, the FEE sorts the TDC data by channel number, which causes the time relationship between the data to be changed. The DeMux algorithm is used to recover the time relationship of the received TDC data to the time of generation on the BX scale. The BEE distributes the clock and BC0 signal to the FEE via the downlink, so the FE and BE will have the same time reference. The difference between the bunch crossing number (BCN) of the BEB and the timestamp carried by the TDC data is the delay between the transmission and generation of TDC data. According to this "delay", TDC data is placed in different positions of the two-dimensional buffer. One dimension represents the delay value of the data, and the other dimension represents the number of TDC data buffered at a specific delay value. This buffer contains time information, which needs to be updated under each BX, and the time relationship of the TDC data output by each BX buffer has been recovered. Since the size of the buffer cannot be infinite, the delay of the TDC data received by the BE exceeds the allowable range and will be discarded. A suitable size is selected for the buffer through software simulation.

The TDC data output by each BX of the dynamic buffer is mapped as fired strips, and then a clustering algorithm is used to combine the fired strips that satisfy the time and spatial constraints as a cluster. For cluster size determination, multiple processes are used, and the idea of a sliding window is used in each process to scan 48 strips of half iRPC detectors. For each cluster, determine its central strip, and calculate the hit positions along the strip based on the time difference at both ends of the central strip. Then, the strip number and the hit position along the strip are mapped according to the lookup table, and the spatial position information of the muon hit is obtained. Each BX sends the encoded cluster information as TPs to the downstream trigger system via a 10 Gbps optical link. The output link is implemented with a Gigabit high-speed serial transceiver embedded in the FPGA.

The latency allowed by the L1 hardware trigger system is 12.5 μs or 500 BX, so the latency requirement for individual subsystems is very small. The latency introduced by the firmware of the BEE is only 39 BX.

3.2.3 Data Acquisition

The BEE must read out the raw detector data, the TDC data received by the BE, and TPs according to the trigger signal. These two parts of data will be cached locally before the trigger signal arrives. Based on the pipeline design,

as long as the latency between the trigger signal and the data is known, the latency value can be converted into the address offset of the buffer to read out the data related to the trigger signal directly. The time spent by the BEE from receiving the uplink frame carrying "TDC data" to giving the TPs is fixed, so it is only necessary to calibrate the time relationship between the trigger signal and the TDC data. As shown in Fig.8, after calibrating the latency between the trigger signal and the data, read the TDC data input from the FE and the TPs output from the BE in a certain window, package the data of multiple links and assemble them into an event, and then upload the event to the DAQ system through the 10-GbE link.

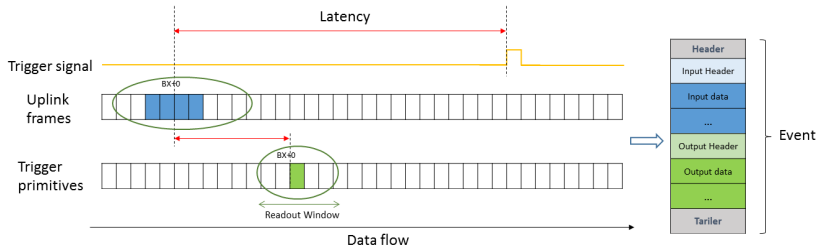

Figure 8: Schematic of reading data based on the trigger signal.

The trigger signal is not periodic, and sometimes the interval between two trigger signals is very short. Due to the limited processing capability of the multi-link packetization state machine, the trigger signal is buffered. A "Busy" mechanism is designed to prevent trigger signal and data buffer overflow by suppressing the release of the trigger signal. The Busy signal is generated by "OR" the half-full flag of the buffer, taking into account the depth of the buffer so that the complete event data can be buffered before the Busy signal suppresses the trigger signal. In addition, the trigger signal comes from the global hardware trigger system. Some trigger signals received by the BEE may not have corresponding raw detector data and TPs. In this case, the data readout based on the trigger signal is invalid, i.e., "zero data". A "zero suppression" mechanism is added to the firmware to discard zero data during event packing, saving upload bandwidth. Based on the current design, one BEB can support the readout of data input by 8 FEBs at an event rate of 750 kHz.

3.2.4 Slow Control

The essence of SC is read and write operations on registers in electronic devices, and the key to implementing SC functions in BEE is protocol conversion. BEB uses the Remote Bus Control Protocol (RBCP) in the SiTCP library as the protocol for the GbE transmission link to interact with the PC. The RBCP protocol is a 32-bit address and variable-length data in bytes (8 bits). The FEE

SC protocol is used to configure the parameters of the FEB (such as calibration, threshold, mode, etc.) and defines a 16-bit address and variable-length data in words (16 bits). The BEE SC is used to configure the proper operating parameters for the BEB, which are 16-bit address and 16-bit data. GBT SC is based on the SCA protocol to monitor the FEB (such as power-on, firmware loading, current and temperature monitoring, etc.), consisting of 24-bit control symbols and 32-bit data. The protocol conversion layer is implemented through firmware to perform bidirectional matching of different protocol interfaces.

The BEB parses the received RBCP packets and determines whether or not they are SC commands distributed to the BEE, FEE, or GBT via address mapping. For BEE SC, the register at the specified address in the RBCP packet can be read and written directly. For GBT SC, a request frame must be generated according to the SCA protocol and embedded in the GBT downlink. The request and response of the SCA protocol correspond one by one, so after the response is wholly received, data and status are extracted to generate an RBCP reply packet. The read operation of FEE SC is similar to that of GBT SC, and the difference is that the reply of the read operation has no boundary character, only the content according to the read length. The FEE does not give a response for write operations, so the BEE generates RBCP reply packets autonomously.

4 System Testing and Analysis

4.1 Bit Error Rate

When the FEB is set to loopback mode by sending the SC command from the BEB, the FEB returns the received data to the BEB. The BEB sends cyclic incremental data, checks whether or not the data from the FEB conform to the cyclic incremental rule, and calculates the BER of the GBT transmission link. In the actual test, no error bits were received, and the bit error rate was less than 1×10^{-16}, as shown in Fig.9, which proves the stability and reliability of the bidirectional transmission link between the FEB and BEB.

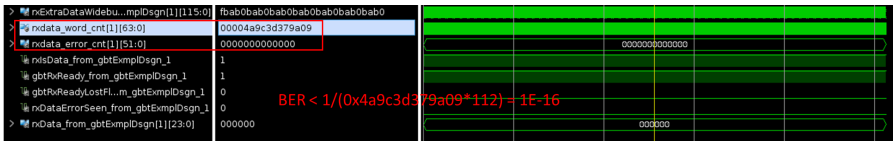

Figure 9: BER results from the Integrated Logic Analyzer (ILA) tool. A total of 0x4a9c3d379a09 (hexadecimal) data frames are received; each frame of data is 112 bits, and no wrong data frames are received; therefore, so the BER is less than 1×10^{-16}.

4.2 BEB Integration Test with FEB

The joint test system for the BEB and FEB was set up in the RPC laboratory of the CMS, as shown in Fig.10. The test bench used a signal generator to generate periodic pulses, which were shaped by the signal injection board and injected into the FEB to simulate the process of injecting signals into the FEB after the iRPC is hit by the muon. The FEB and BEB use optical fibers for point-to-point link transmission, and the BEB can simultaneously receive inputs from multiple FEBs via integrated optical fibers. The BEB is connected to the server via fiber to realize the 10-GbE DAQ and the GbE SC links. SC and DAQ software to control the system's operating status and obtain operation results.

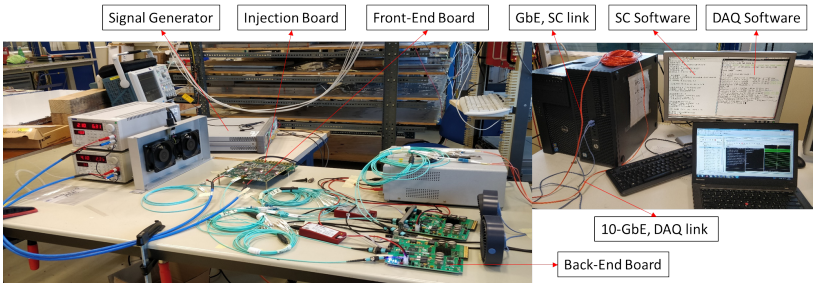

Figure 10: Joint test system setup for the BEB and FEB.

The output of the signal generator is divided into two parts by the splitter, one is used as the reference channel, and the other is added to the delay line as the test channel. Both channels simultaneously feed charges to the FEB. The BEB sets the alignment parameters for the FEB via SC commands so that all TDC channels of the FEB keep consistent time measurements of simultaneously input signals. Therefore, the time difference between the two channels obtained after DAQ and offline analysis should be consistent with the delay line. Fig.11(a) shows the statistical distributions of the measured time difference between the test and reference channels when the delay is zero, that is, when no delay line is added, with a root-mean-square (RMS) of 23 ps. Dividing the RMS value by $\sqrt{2}$ gives the approximate time resolution of the RMS value for one channel as 16 ps. By adding different delay lines to the test channel, the time difference between the test and reference channels changes linearly as the delay increases. Fig.11(b) shows that as the value of the delay line increases, the time difference between the two channels also increases linearly, with a maximum deviation of 0.1 ns and an integral nonlinearity of 0.32%.

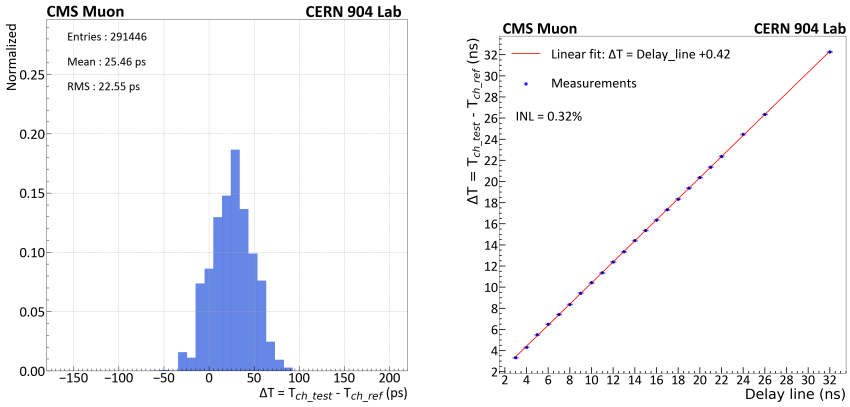

Figure 11: Left (a): Statistical distributions of the measured time difference between two channels without delay line. Right (b): Change the regularity of the time difference between the test and reference channels by changing the delay line.

4.3 BEB Integration Test with iRPC

The joint test system of the BEB and iRPC equipped with the FEB was also set up in the RPC laboratory, as shown in Fig.12. The system uses the coincidence of two scintillators to generate a cosmic-ray trigger that is connected by a cable to the BE external trigger interface. The scintillator trigger signal generated using the standard plug-in provided by CMS must pass through an adapter before the BEB can use it. The BEB performs DAQ continuously based on the received external trigger signal and analyzes the acquired data offline. Before the experiment, the BEB needs to configure the parameters for the FEB through the SC command, make the FEB have the same responsiveness to the input signal of each iRPC readout strip, and set an appropriate threshold for the FEB to eliminate noise as much as possible.

The system's performance is analyzed by using two very small scintillators placed vertically, collimated by increasing their distance apart. In Fig.13(a), the two scintillators are placed vertically such that the length of the coincidence area along the strip is only 1 cm for one strip. The raw detector data and TPs in each event read by the BEB are closely related to the placement of the scintillator, allowing analysis of positional resolution along the strip based on the time difference between both ends of the strip. A strip is randomly chosen within the coincidence area of the two scintillators, the time difference distribution between both ends is shown in Fig.13(b), and σ is 160 ps after rejecting the noise. The signal propagates on the strip at 0.67 times the speed of light, which translates to a positional resolution of 1.5 cm along the strip using the formula $\Delta y = (v \times \Delta T)/2$.

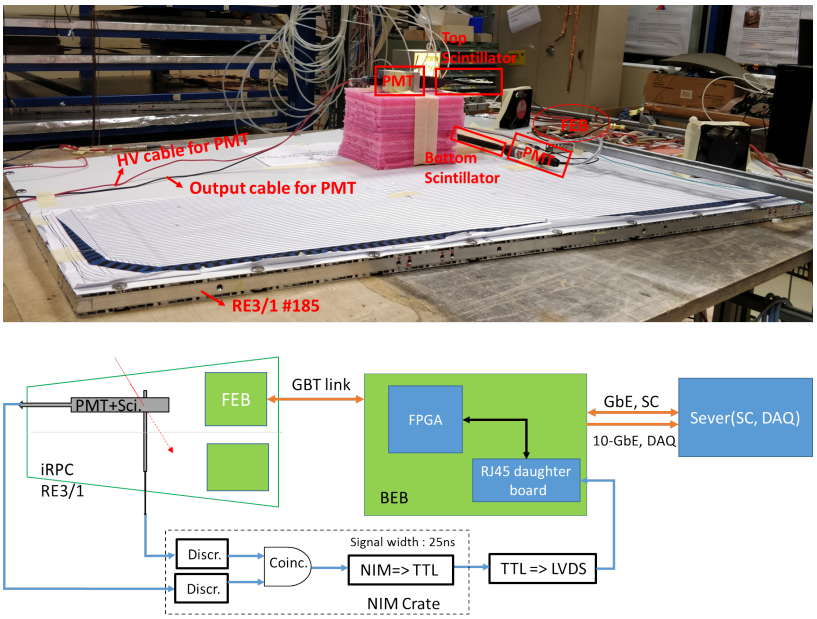

Figure 12: Photograph (top) and Schematic diagrams (bottom) of iRPC, FEB, and BEB joint test system.

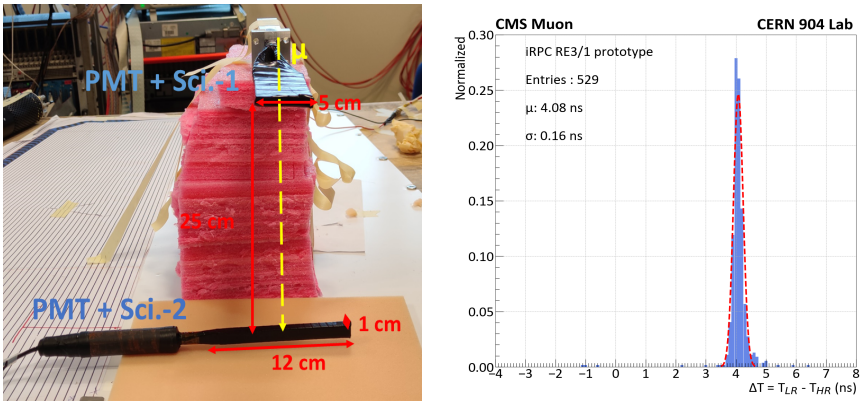

Figure 13: Left (a): Photograph of the two scintillators placed vertically. Right (b): Statistical distribution of time difference at both ends of the strip.

5 Conclusions

This study presents a Back-End Board (BEB) prototype for an iRPC developed to meet the CMS upgrade requirements. The functionality of the BEB prototype includes high-speed transmission links for front-end and back-end interaction, fast and Slow Control (SC), trigger primitives generation, Data AaQquisition (DAQ), and transmission links for the SC and DAQ. The test results gave a time-to-digital converter Root Mean Square (RMS) of 23 ps, time resolution of 16 ps in RMS, and an integral nonlinearity of 0.32%, which are good agreement with expectations. The results show that the BEB prototype functions correctly and operates reliably, meets the FEE requirements, and provides fast and SC functions such as parameter configuration, system clock, and timing reference. The test results of 1.5 cm position resolution verify the performance of the iRPC system, further verifying the BEB prototype's function, indicating that the BEB prototype satisfies the requirements of readout iRPC at both ends.

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