Low-Noise Preamplifier for Capacitive Sensors

by

Shida Iep

Submitted to the

DEPARTMENT OF ELECTRICAL ENGINEERING
AND
COMPUTER SCIENCE

in partial fulfillment of the requirements for the degrees of

BACHELOR OF SCIENCE
and
MASTER OF SCIENCE

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June, 1995

Author .....
Shida Iep
Department of Electrical Engineering and Computer Science, May 19, 1995.

Certified by .....
Professor James K. Roberge
Thesis Supervisor, Department of Electrical Engineering and Computer Science

Certified by .....
Eric M. Hildebrant
Thesis Supervisor, Charles Stark Draper Laboratory, Inc.

Accepted by .....
F. R. Morgenthaler
Chair, Department Committee on Graduate Students

Low-Noise Preamplifier for Capacitive Sensors

by

Shida Iep

Submitted to the Department of Electrical Engineering and Computer Science on May 19, 1995, in partial fulfillment of the requirements for the degrees of Bachelor and Master of Science

Abstract

Silicon microfabricated sensors often use electrostatic (capacitive) techniques to achieve controlled motion. The small output signals of these microfabricated sensors require extremely low-noise amplifiers to take advantage of the lower range of signal levels. This study explores noise issues in designing low-noise preamplifiers for high impedance sources such as micromechanical gyroscopic sensors.

Three amplifier designs have been investigated for a capacitive sensing gyroscope developed by the Charles Stark Draper Laboratory. Two of the designs have been constructed using discrete and monolithic parts, and the third is to be fabricated in the Orbit 1.2μm CMOS process.

An input referred noise of $6.7\frac{nV}{\sqrt{Hz}}$ at 27kHz has been achieved with one of the discrete preamplifiers. Predicted noise for the CMOS preamplifier at 27kHz is $9.3\frac{nV}{\sqrt{Hz}}$.

Thesis Supervisor: James Roberge
Title: Professor of Electrical Engineering and Computer Science

Acknowledgments

I would like to thank my Draper Advisor Eric Hildebrant for his guidance and inspiration. He has always been there to encourage me and to share his experience, knowledge, and wisdom. I would like to thank my MIT thesis Advisor Professor James K. Roberge for his insights and ideas.

I would also like to thank others who have contributed in many ways to this project: Ralph Haley for his patience and great understanding, Bill Kelley for his assistance in various aspects of the project and for teaching me how real engineers construct circuits, and also Paul Ward for his experience and ideas.

There are many others who have made it especially fun at Draper Labs: Matt Lobner (for his cheerfulness), my two 6A advisors Martin Miller and Steve Hoeschele (for guidance and friendship), and Harold Bussey (for all the color printings).

I would also like to thank the very special people in my life: my family (Mom, Dad, Raymond, and Ochide) and my wonderful fiancé Angel . Finally, I'd like to thank God for His many blessings and love.

This thesis was prepared at the Charles Stark Draper Laboratory, Inc., under the Internal Research and Development Project No. C312.

Publication of this thesis does not constitute approval by Draper or the sponsoring agency of the findings or conclusions contained herein. It is published for the exchange and stimulation of ideas.

Table of Contents

List of Figures

List of Tables

Chapter 1

The Capacitive Sensor and the Preamplifier

1.1 Introduction

Many micromechanical devices make use of capacitive sensing techniques to measure mechanical displacement. One such device is the micromechanical gyroscope developed at the Charles Stark Draper Laboratory. Advancements in the field of microfabrication technology will provide the capability of building sensors cheaply with silicon. The aforementioned capacitive techniques involve applying a constant voltage across two capacitor plates. One plate is made stationary and the other mobile. As the mobile plate moves and changes the distance between the stationary plate, charge is generated having a value proportional to the displacement of the moving plate. Changing charge values create a current which serves as the output of the sensor.

The sensor's output is then processed for a specific application. The output signals of these micromachine devices can be very small which creates a problem because of the processing inaccuracy resulting from the presence of noise signals of comparable level to the signal.

There are several types of noise that contribute to the contamination of the information signal: noise from the external electrical environment such as the 60-Hz power lines, noise from the sensor itself, and noise from the processing circuits.

The noise in the sensor itself has been reduced considerably, potentially offering extremely high sensitivity. External noise can be reduced by proper shielding, and the rest by common-mode rejection and power supply rejection of the preamplifier. However, the internal noise of the preamplifier can only be minimized by careful design.

Amplification of the signal is necessary to make the signal more robust and thus less sensitive to noise along the processing stream. Whether amplification is accomplished in few or many steps, the circuit that interfaces with the sensor must be designed with care in order to minimize the noise it introduces onto the signal. If amplification is obtained with more than one step, the first circuit is often called the preamplifier, a low-noise circuit which offers the signal a fraction of the desired amplification and allows loosening of the noise specification of the succeeding amplification stages.

This paper will detail the design of three low-noise preamplifiers that will be used to amplify capacitive sensor signals. Microfabricated capacitive sensors tend to have high impedances. This impedance level dictates the type of preamplifier that will offer good noise performance. Two preamplifiers were realized with the use of commercially available monolithic and discrete parts. The third is an integrated circuit to be fabricated in a CMOS process. The latter solution was pursued for its ease of production, low-cost, small size, and low power.

1.2 The Capacitive Gyroscope

The new tuning fork gyroscope developed by the Charles Stark Draper Laboratory is made of single-crystal silicon. Figure 1.1 shows its structure. The motor drive electrodes and the motor sense electrode are stationary structures with tines (or fingers) on the side(s). The two proof masses (also with tines on the sides) are then forced to move back and forth in the x-direction by the motor signal through electrostatic attraction. Proof mass A and proof mass B are made to move in opposite directions. When the sets of fingers move toward each other and interlace, their overlap areas form capacitors. As these fingers move in and out of each other, a changing capacitance results and the information is read by the motor sensing charge amplifier (U1). This signal (the output of U1) relates informa-

tion about the positional amplitude of the motor and is used in a feedback network to control the motor's amplitude and also to reference the gyroscopic information.

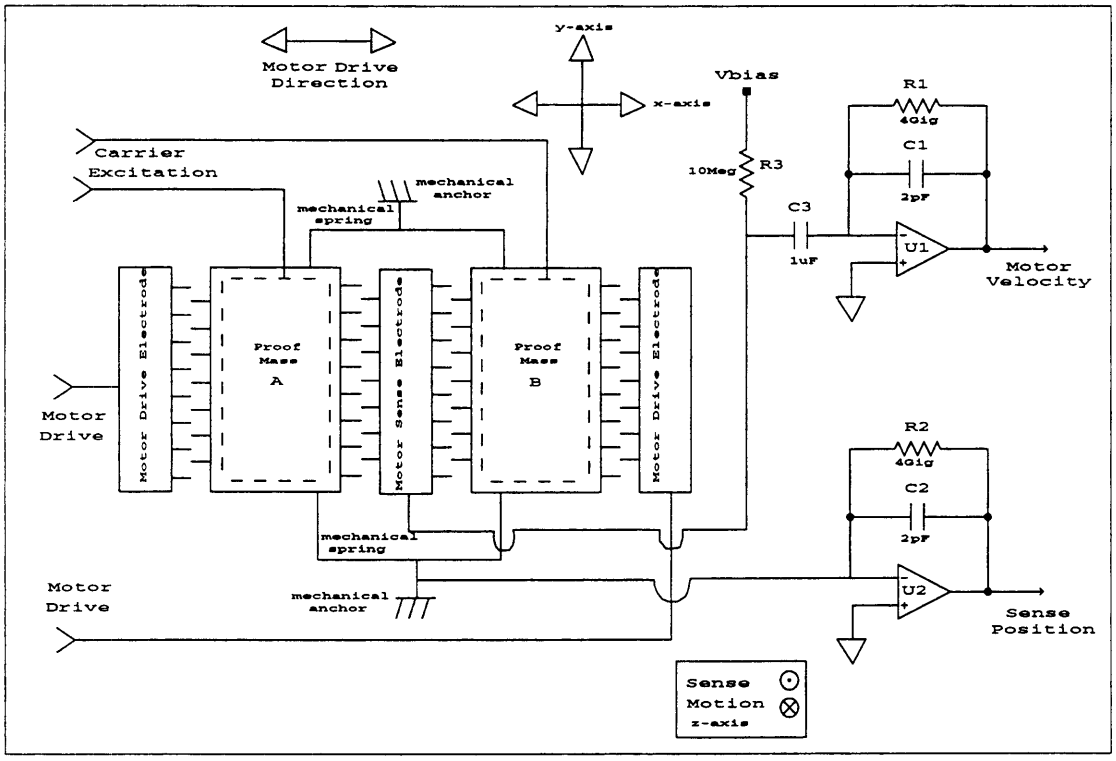

Figure 1.1: Draper Gyroscope Schematic Diagram

The proof masses are suspended by mechanical springs attached to mechanical anchors. Under each proof mass, there is a layer of gold, which has been referred to as the stationary capacitance plate. With these stationary plates, the proof masses form two capacitors. During the gyroscope's operation, the proof masses are always moving back and forth along the x-axis at the motor's frequency (22kHz to 32kHz, with a nominal frequency of 27kHz). When a rotation about the y-axis occurs, Coriolis force in the positive z direction (out of the paper) is applied to the proof mass A and a force in the negative z direction (into the paper) is applied to proof mass B. If static (equal and opposite) voltages are applied to the stationary plates underneath the proof masses, the change in the capaci-

tances made by the moving proof masses generates a current proportional to the velocity of the proof mass. A preamplifier is hooked up to the sensing node and the current signal is read and converted to a voltage signal proportional to the position of the sense plate [1].

The plates could not be made larger than 200μm X 200μm, otherwise they would curl. This limitation allows only for small capacitor values, thus resulting in a system with a high source impedance. Larger capacitor values must be achieved by paralleling more than one of these capacitor structures. However, paralleling defeats the purpose of miniaturization. The sensor's impedance (6 Megohms to 3 Megohms at 27kHz) is very large and will significantly affect the design of an optimal low noise preamplifier.

The two sets of plates create very small capacitor values (1pF to 2pF), and the plate displacements are in the sub Angstrom to Angstrom range (from 0.04 Angstrom to 6.25 Angstrom). This displacement results in capacitive value changes (ΔC_s) that range from 0.6 attofarad to 100 attofarad (1 attofarad = 1 X 10^{-18} Farad). As the capacitance changes, it creates a flow of charge (ΔQ) proportional to an applied DC bias (V_{bias}):

$$\Delta Q = \Delta C_s (V_{bias}) \tag{1.1}$$

The mechanism generates a charge flow ranging from 3.0 X 10^{-18} Coulombs to 5.0 X 10^{-16} Coulombs, (or 19 to 3,125 electrons). Because the charges are generated by capacitor plates oscillating at 27kHz, the information from the gyroscope is therefore a current signal ranging from 81fA to 13.5pA.

Instead of working with changing capacitance, we can remodel the sensor as a combination of a static capacitor with a varying voltage source oscillating at 27kHz, $V_s = A\sin(wt)$ where $w = 2\pi(27kHz)$ (see Figure 1.2). The model still generates the proper current signal $i_s = jwC_sV_s$.

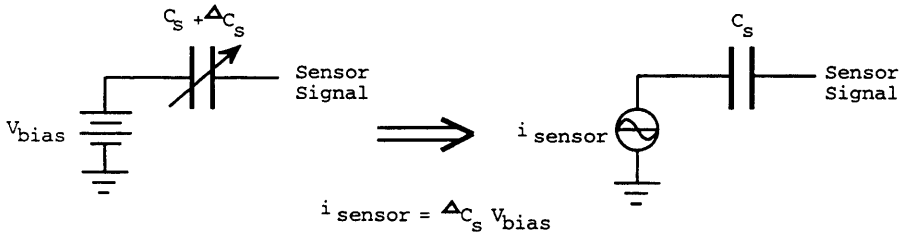

Figure 1.2: .Circuit Model of the Capacitive Plates

This modeling will simplify analyses of the circuit in later sections.

1.3 The Preamplifier

Along with the desired signal, any noise present at the output node of the sensor will be amplified by the preamplifier and subsequent amplifiers. The noise introduced by the preamplifier will determine the smallest signal level that can be discerned from noise. If the preamplifier generates X amount of noise at its output, the smallest information signal it can read is $\frac{X}{A}$, where A is the gain provided by the preamplifier circuit. This scenario results in an output signal level that is equal to the output noise level (a signal to noise ratio of 1:1). Any sensor signal that is smaller than $\frac{X}{A}$ will be virtually drowned out by the noise of the preamplifier. Thus the goal of designing a low-noise preamplifier is to obtain as much gain A as possible while keeping the generated noise X as small as possible. Once the desired signal is amplified to a sufficiently high level, introduction of any other noise in subsequent stages will not affect the desired signal to any significant level.

The noise of the preamplifier depends on several factors: (1) topology, (2) type of devices, (3) device dimension, (4) operating frequency, and (5) parasitics. We have design control over topology, types of devices, device dimensions, and device parasitics; however the operating frequency is dictated by the sensor. The circuit below shows a closed-loop

configuration of the preamplifier circuit connected to the sensor circuit shown in Figure 1.1.

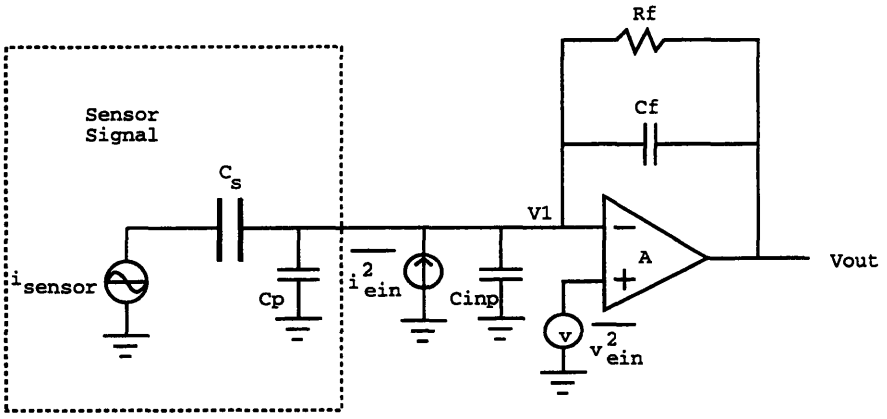

Figure 1.3: Sensor and Amplifier Connection

The current source i_{sensor} and the capacitor C_s represent the sensor, the "A" module is the low-noise preamplifier (which is an operational amplifier) with a DC gain of A, C_p is the parasitic capacitance from the sensor pin and wiring, C_{inp} is the parasitic input capacitance contributed by the input device of the op-amp, C_f is the feedback capacitor, and R_f is the feedback resistor necessary for DC stabilization of the preamplifier. Current $\overline{i_{ein}^2}$ is the op-amp's mean squared noise current source and $\overline{v_{ein}^2}$ is the op-amp's mean squared noise voltage source. These sources represent the noise contributed by elements inside the op-amp so that the preamplifier A can be modeled as a noiseless amplifier. The voltage value of $\overline{v_{ein}^2}$ is obtained by taking the measured output noise value of the preamplifier and dividing it by the noise gain (which is approximately $\frac{C_f+C_s+C_p+C_{inp}}{C_f}$). The noise current depends mainly on the biasing current or parasitic currents of the input devices of the preamplifier.

The circuit in Figure 1.3 works in the following ways: (1) The sensor generates a current. (2) The current then flows into the summing node (v_1) of the preamplifier. (3) The

charge accumulates on one side (V_1 side) of the feedback capacitor plates and balancing charges accumulate on the other side (the V_{out} side). (4) The C_f capacitor converts the current signal to a voltage signal at the output of the amplifier. Depending on the type of devices used in the input stage of the preamplifier, negligible to significant levels of current flow in or out of the negative terminal of the preamplifier. This current can be due either to the current used to bias the device, leakage current created by imperfect junction isolation between the gate and the device channel, or parasitic currents. This DC current will continuously charge up C_f and eventually saturate the output. Saturation of the output can be avoided by providing a path for this DC current to flow. This path is achieved through the feedback resistor R_f.

Chapter 2

Types of Noise

2.1 Introduction

Noise is caused primarily by the quantum nature of the charge flowing in electrical components [2, 3]. There are various types of noise that we will be dealing with: (1) shot, (2) thermal, and (3) flicker. Noise signals are generally random, with random phase and no known polarity. Because of this, noise is often conveniently expressed in root mean squared (RMS) values.

2.2 Thermal Noise

Thermal noise is due to random thermal motion of particles in any resistive (energy dissipative) element. In a resistor of value R, the voltage fluctuation is given by

$$\overline{v_{nt}^2} = 4kTR\Delta f \tag{2.1}$$

where $\overline{v_{nt}^2}$ is the squared mean value of the expected voltage v_{nt}, k is the Boltzman's constant ($1.38\text{x}10^{-23}$ W-s/K), T the absolute operating temperature, and Δf the bandwidth of interest in Hertz (Hz). This noise type can be modeled in two ways: as a current source in parallel with a noiseless resistor of value R or a voltage source in series with the noiseless resistor R.

The current source can be expressed as

$$\overline{I_{nt}^2} = 4kTG\Delta f \tag{2.2}$$

where $G = \frac{1}{R}$. The decision to use one model over the other is usually made based on the ease of analysis.

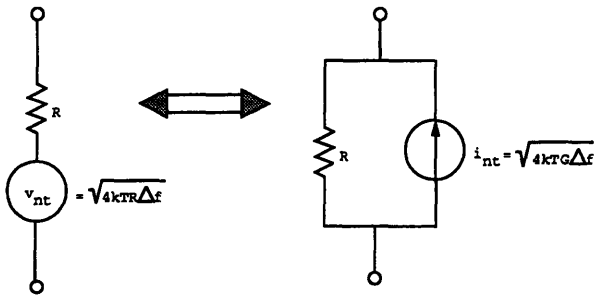

Figure 2.1: Noise Model of a Resistor

The direction shown in the noise current source (in Figure 2.1) has no significant meaning as noise has random phase.

This thermal noise is unaffected by direct current flow (or DC voltage drop) since typical electron drift velocities in a conductor are much less than electron thermal velocities. Because of this, people often call thermal noise the fundamental noise. The noise is proportional to absolute temperature T, approaching zero at zero Kelvin. For example, the thermal noise spectral density of a 1k-ohm resistor is

$$\frac{\overline{v_{nt}}^2}{\Delta f} = 4kT(1k) = 16x10^{-18}\frac{v^2}{Hz} \tag{2.3}$$

or equivalently,

$$\frac{v_n}{\Delta f} = 4\frac{nV}{\sqrt{Hz}} \tag{2.4}$$

It can also be expressed as a noise current with a value of

$$\frac{I_{th}}{\Delta f} = \sqrt{4kT(\frac{1}{1k})} = 4.07\frac{pA}{\sqrt{Hz}} \tag{2.5}$$

The amplitude distribution of the thermal noise is a Gaussian, and has a flat frequency spectrum (i.e. the spectral power density at 1Hz is the same as at 100kHz). Noise with a

flat spectrum is referred to as a white noise. Thermal noise exists in circuit elements such as resistors and conducting channels in semiconductor devices [2, 3].

2.3 Shot Noise

Shot noise exists when there is a direct current flow across a potential barrier, such as those in semiconductor junctions. Currents in these devices do not flow smoothly but rather in pulses at random intervals. For an average direct current flow of I_d, the current variation I_{ns} is given by

$$\overline{I_{ns}^2} = 2qI_D\Delta f \tag{2.6}$$

where q is 1.6 X 10^{-19} C (the magnitude of the electron charge), and Δf is the bandwidth [4]. The unit of $\overline{I_{ns}^2}$ is $(Ampere)^2$. Shot noise is also a white noise, having flat spectral density over frequency and a Gaussian amplitude distribution. Shot noise exists in the p-n junctions of diodes, bipolar transistors, and junction field effect transistors [2, 3].

2.4 Flicker Noise

Flicker noise is generally referred to as $\frac{1}{f}$ noise. As suggested by its second name, the noise is inversely proportional to frequency, dominating in the low frequency regions. The major cause of $\frac{1}{f}$ noise in modern semiconductor devices is the generation and recombination of carriers. This noise is found in all active devices, as well as in some passive elements. In transistors, flicker noise could very well be caused by traps created by contamination and crystal defects in junctions or interfaces between materials (such as the silicon channel and silicon-dioxide insulation interface in MOSFETs). These traps capture and release carriers in a random fashion with random time constants, which give rise to noise signals with energy concentrated at low frequencies.It has been shown that $\frac{1}{f}$ noise

results in equal noise power in each decade of frequency. The noise power integrated from 1Hz to 10Hz is equivalent to the noise power integrated from 1kHz to 10kHz [2, 3].

Flicker noise is associated with a flow of direct current and displays a spectral density of the form

$$\overline{I_f^2} = K\frac{I^\alpha}{f^\beta}\Delta f \tag{2.7}$$

where:

I_f is the flicker noise current
Δf is the small bandwidth at frequency f
I is the direct current
K is the constant dependent on the device
α is a constant ranging from 0.5 to 2
β is a constant near unity
Δf the bandwidth of interest

2.5 Capacitance Shunting of Thermal Noise: $\frac{kT}{C}$ Noise

The thermal noise expression $v_{nt} = \sqrt{4kTR\Delta f}$ predicts that the noise of an open circuit (infinite R) has infinite noise voltage. This result is not observed in practice because the noise generator is always shunted by some capacitive element (parasitic or intentional). This capacitance limits the resistor thermal noise voltage. Consider the shunt resistor and capacitor circuit in Figure 2.2 [2]:

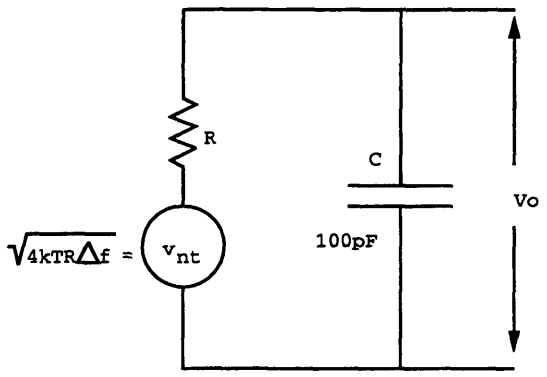

Figure 2.2: Capacitive Shunting of the Resistor's Thermal Noise

If we consider $v_{nt} = \sqrt{4ktR\Delta f}$ as an input source, the output is related to the input by the equation:

$$v_o = \frac{\frac{1}{jwC}}{R + \frac{1}{jwC}} v_{nt}$$

As v_{nt} increases with $\sqrt{R}$, the transfer function $\frac{\frac{1}{jwC}}{R + \frac{1}{jwC}}$ starts attenuating (as $\frac{1}{R}$) the signal v_{nt}, with a -3dB point at frequency $f = \frac{1}{2\pi RC}$. So as R increases, thus increasing the noise voltage v_{nt}, the bandwidth decreases by the same amount. The figure below shows the noise voltage spectral density for different values of R.

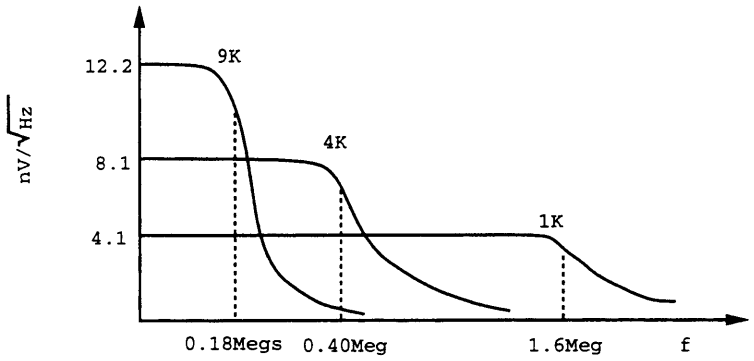

Figure 2.3: Spectral Density of the Capacitively Shunted Noise

The areas under each curve are equal. This phenomenon can be considered as a low-pass filter. Although a high resistor value will introduce more noise, the cut off frequency of the RC network is also lower. The resistor noise has significantly less effect at the higher frequencies, a preferred situation for circuits with high operating frequencies. The limiting of v_{nt} by the shunt capacitance was rigorously shown in [2] as follows:

$$v_n^2 = \int_0^\infty v_n^2 \left| \frac{\frac{1}{jwC}}{R + \frac{1}{jwC}} \right| df = \int_0^\infty \frac{v_n^2}{1 + (wRC)^2} df \qquad (2.8)$$

To integrate, we'll let $f = f_2 \tan\theta$, $f_2 = \frac{1}{2\pi Rc}$, $df = f_2 \sec^2\theta d\theta$ and change the upper limit to $\pi/2$.

$$v_{no}^2 = \int_0^{\frac{\pi}{2}} \frac{v f_2 \sec^2\theta}{1+\tan^2\theta} d\theta = \int_0^{\frac{\pi}{2}} v_n^2 f_2 d\theta \tag{2.9}$$

$$v_n^2 = 4kTR\Delta f \tag{2.10}$$

$$v_{no}^2 = \int_0^{\frac{\pi}{2}} 4kTRf_2 d\theta = 2\pi kTRf_2 \tag{2.11}$$

and

$$f_2 = \frac{1}{2\pi RC} \tag{2.12}$$

$$v_{no}^2 = \frac{kT}{C} \tag{2.13}$$

Equation 2.13 is called the noise limit, the maximum noise from any resistor. The output rms noise voltage is independent of resistance value, and depends only on T and C. The noise is concentrated at low frequencies.

2.6 Addition of Noise Sources

Noise addition is performed in root mean squared (RMS) arithmetic. For example, the addition of two noise generators of $v_{n1} = 3\frac{nV}{\sqrt{Hz}}$ and $v_{n2} = 4\frac{nV}{\sqrt{Hz}}$

$$v_{ntotal}^2 = v_{n1}^2 + v_{n2}^2 \tag{2.14}$$

$$v_{ntotal} = \sqrt{\left(\frac{3nV}{\sqrt{Hz}}\right)^2 + \left(4\frac{nV}{\sqrt{Hz}}\right)^2} = 5\frac{nV}{\sqrt{Hz}} \tag{2.15}$$

This arithmetic assumes that there is no correlation between the two sources v_{n1} and v_{n2}. The characteristics of RMS addition allows for easy noise calculations in circuits, as small noise values can be neglected without significantly affecting the accuracy of the total calculated noise value. We can neglect the smaller of two noise sources if their RMS values are in a 10:1 ratio, since the smaller signals adds less than 1% to the total noise voltage. An rms ratio of 3:1 has only 10% effect on total noise. Also, when adding the noise volt-

ages of different resistors, we can simplify noise calculations if we simplify the resistive networks first and consider it as a single resistor with a single noise generator. For example, when there are two resistors in series, the noise voltage of a resistor value of R= (R_1+R_2) can be calculated first and the total noise voltage is $\sqrt{4kTR\Delta f}$.

Noise signals originating from physically different sources are not correlated. Correlation must be considered for noise signals from the same source. The equation below shows the addition of two correlated signals.

$$v_{ntotal}^2 = (v_{n1} + v_{n2})^2 = v_{n1}^2 + v_{n2}^2 + 2v_{n1}v_{n2} \tag{2.16}$$

The last term gives the correlation. Two signals are 100% correlated if the two waveforms have the same shape, even if the amplitudes are different. Sometimes, the calculation can be difficult if the waveforms are partially correlated. Then the total noise is written with a correlation factor:

$$v_{ntotal}^2 = v_{n1}^2 + v_{n2}^2 + 2Cv_{n1}v_{n2} \tag{2.17}$$

where C is the correlation coefficient which can vary between -1 and +1.

In practice, noise signals are assumed to be close to being uncorrelated (C=0) without losing much accuracy. Summing totally correlated equal value signals gives two times their separate rms values, whereas summing uncorrelated signals give 1.4 times their separate rms values. The maximum error caused by assuming no correlation is 30%. If the signals are totally correlated and one is much larger than another, the error from the uncorrelated assumption is even smaller than 30%. If one signal is ten times the other and totally correlated, the uncorrelated assumption produces a maximum error of only 8.6% [2].

Chapter 3

Noise in Various Electrical Components

3.1 Introduction

Amplification is made possible through the use of active devices, which contain all the noise types mentioned in Chapter 2. However, one noise type may be more prominent in one device type than in another. Understanding the noise mechanisms of each device helps us to make better decisions in device and circuit topology selections for a particular application.

This chapter briefly discusses the noise mechanisms in the bipolar transistor, the metal-oxide-semiconductor field effect (MOSFET) transistor, the junction field effect (JFET) transistor, and the buried-channel MOSFETs. The buried-channel MOSFETs are not generally selected for typical analog circuits, but they are worth further investigation for low-noise applications.

3.2 Noise Model of the Bipolar Transistor

The noise sources of the bipolar transistors are illustrated in Figure 3.1a. It is often easier to represent the transistor's noise with equivalent input noise generators. The circuit shown in Figure 3.1b represents the same circuit (as well as the same noise behavior) as the circuit in Figure 3.1a. The internal noise sources of Figure 3.1a are replaced by the equivalent input noise voltage generator $\overline{v_{ein}^2}$ and equivalent input noise current generator $\overline{i_{ein}^2}$ (as shown in Figure 3.1b). Both voltage and noise current generators are necessary to adequately represent the circuit's noise performance with different values of source resistance. The $\overline{v_{ein}^2}$ value can be calculated by shorting the inputs of circuits 3.1a and 3.1b and equating the output noise currents i_o's [3].

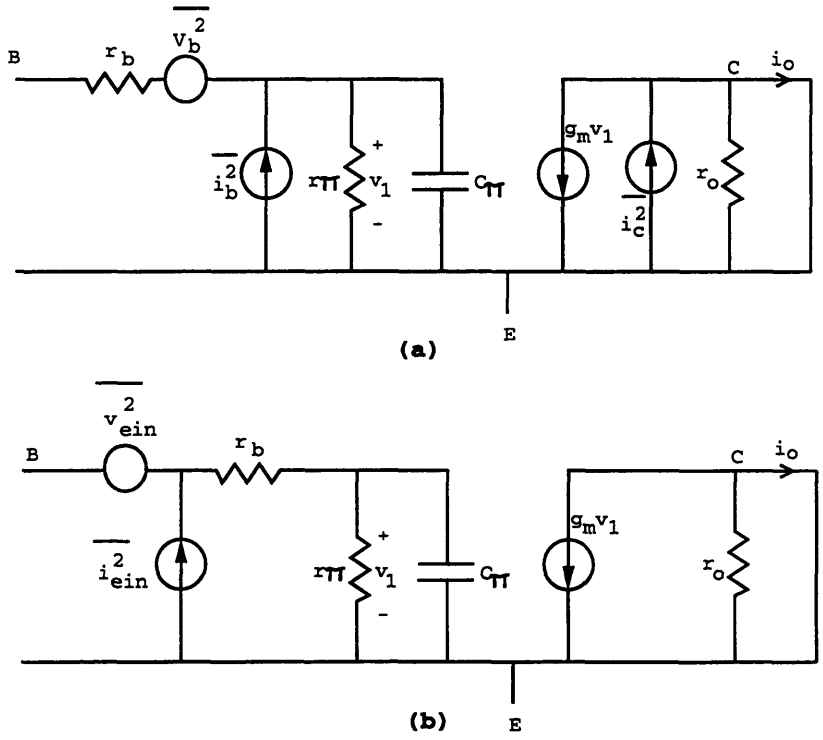

Figure 3.1: BJT Small-Signal Model with Noise Sources

$$\overline{v_{ein}^2} = 4kTr_b + \frac{2qI_c}{g_m^2} = 4kT(r_b + \frac{1}{2g_m}) \tag{3.1}$$

where r_b the base resistance, I_c is the collector operating current, and g_m is the transistor's transconductance.

The last expression was arrived at by using the relation $\frac{kT}{q} = \frac{I_c}{g_m}$. The first noise term in Equation 3.1 is caused by the thermal noise of the base resistance r_b from the base-emitter contact area. The second term is the shot noise from the collector current referred to the input.

The equivalent input noise voltage in Equation 3.1 does not account for flicker noise sources or the shot noise $\overline{i_b^2}$ across r_b. Flicker noise sources in bipolar transistors have very low corner frequency (100Hz or lower), so this noise source can be ignored for most applications. The shot noise $\overline{i_b^2}$ across r_b was ignored because r_b is small, and the contribution would be insignificant compared to the two noise terms in Equation 3.1. Typical low-noise

bipolar transistors used in low-noise amplifiers can have a v_{ein} value ranging from $1\frac{nV}{\sqrt{Hz}}$ to $5\frac{nV}{\sqrt{Hz}}$.

A typical spectral density of v_{ein} is shown in Figure 3.2.

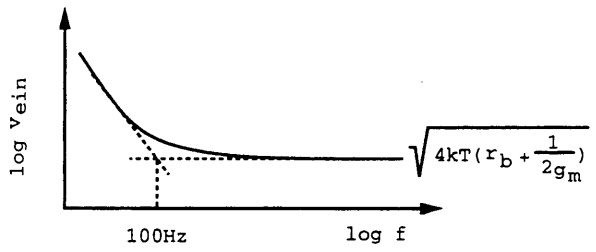

Figure 3.2: Spectral Density of the Bipolar Transistor's Noise Voltage

The increase in noise as the frequency decreases is due to the flicker component, which can be ignored in our application.

To calculate the equivalent input current generator $\overline{i_{ein}^2}$, the inputs of the circuits 3.1a and 3.1b are open circuited and the output noise currents i_o's are equated.

$$\overline{i_{ein}^2} = \overline{i_b^2} + \frac{\overline{i_c^2}}{|\beta(j\omega)|^2} \tag{3.2}$$

$$\frac{\overline{i_{ein}^2}}{\Delta f} = 2q\left(I_B + \frac{K}{2q}\frac{I_B^\alpha}{f} + \frac{I_c}{|\beta(j\omega)|^2}\right) \tag{3.3}$$

where I_B is the base operating current, K is a constant highly dependent on the manufacturing process, f is the operating frequency, and $\beta(j\omega)$ is the transistor's current gain.

The first term in Equation 3.3 is from the shot noise of the base current; the second term is the flicker component of the base current; and the third term is the shot noise from the collector current. Shot noise contributed by I_c can be reduced by using a transistor with large $\beta(j\omega)$. The current gain $\beta(j\omega)$ decreases with increasing frequency, so the equiva-

lent input noise current tends to increase at high frequencies (see Figure 3.3). A typical value for i_{ein} of typical bipolar amplifiers can be $20\frac{fA}{\sqrt{Hz}}$ or higher.

The corner frequency f_b (in Figure 3.3) can be pushed to a higher frequency value by using bipolar transistors with high f_t (the maximum frequency at which the transistor can operate). At low frequency range, there is a flicker effect that goes up as $\frac{1}{f}$ with decreasing frequency. After the second corner frequency f_b, the noise current begins to increase at a rate of f^2.

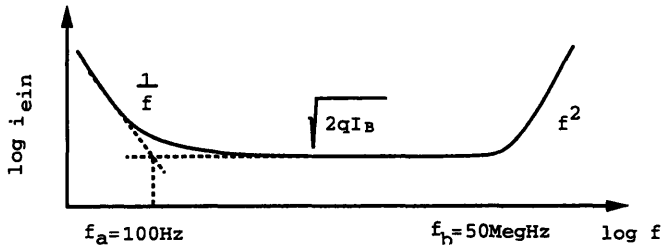

Figure 3.3: Spectral Density of the Bipolar Transistor's Noise Current

3.3 Noise Model of the Junction Field Effect Transistor

The junction field effect transistors are diffusion devices, with reverse biased junctions as the isolation element between the gate and the channel. As this is not a perfect isolation, there is some small leakage current from the gate to the channel. The cross section of a typical n-channel JFET device is shown in Figure 3.4.

The JFETs are constructed by placing a channel (the white region) between two gates (the black regions). In the example shown in Figure 3.4, the gate is a p-type material, and the channel is an n-type material. When V_D is zero, there is a small depletion region (the gray regions) between the gate and the channel from the built-in potential. As V_D increases positively, the depletion region widens because the junctions between the (p-type) gate and the (n-type) channel become more reverse biased.

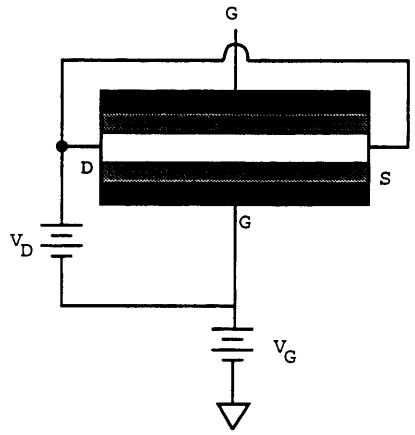

Figure 3.4: Cross Section of a JFET

These depleted regions are very resistive, so current will prefer the less resistive channel region. When the channel becomes completely depleted, the transistor turns off and allows very little current to flow. As shown in Figure 3.4, there is no current flow because there is no voltage drop between the source and drain terminals. Current flows when the drain is more positively biased than the source as shown in Figure 3.5

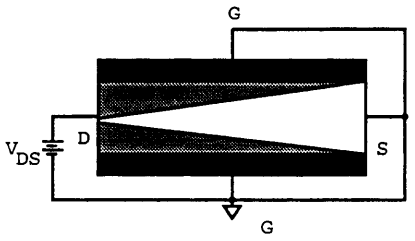

Figure 3.5: JFET Operating in the Saturation Mode

In amplifiers, the JFET is usually operated in the saturation region, with the drain connected to some high voltage, and the source to a lower voltage. The gate node must be at a potential lower than the drain and the source in order to avoid forward biasing the gate-channel junction.The transconductance of a JFET is as follows:

$$g_m = 2I_{DSS}(1 - \frac{V_{GS}}{V_P})\frac{1}{V_P} \tag{3.4}$$

However, when the gate is connected to the same potential as the source, as shown in Figure 3.5, the transistor operates at a maximum drain current I_{dss}. This mode offers the highest transconductance. The equation for g_{max} is

$$g_{max} = \frac{2I_{DSS}}{V_P} \tag{3.5}$$

where V_p (the pinch off voltage) is the negative V_{gs} voltage necessary to turn the transistor off. I_{dss} can be made larger or smaller by increasing or decreasing, respectively, the gate width to gate length ratio ($\frac{W}{L}$) of the transistor.

The noise sources ($\overline{i_g^2}$ and $\overline{i_d^2}$) of a JFET are shown in Figure 3.6. The noise source $\overline{i_g^2}$ represents the shot noise from the gate current (the leakage current across the reverse biased gate-channel junction). The noise source $\overline{i_d^2}$ represents the thermal noise from the resistance of the channel. If the operating frequency is sufficiently low, flicker noise should be included in both $\overline{i_g^2}$ and $\overline{i_d^2}$ noise sources.

To calculate the equivalent input noise voltage $\overline{v_{ein}^2}$, the inputs of circuits 3.6a and 3.6b are short circuited and the output noise currents i_o's are equated.

$$\overline{v_{ein}^2} = \frac{\overline{i_d^2}}{g_m^2} \tag{3.6}$$

$$\overline{v_{ein}^2} = \frac{8kT}{3g_m} + K\frac{I_D^\alpha}{WL_{eff}C_{ox}g_m^2 f} \tag{3.7}$$

where:

I_d is the drain bias current
K is a (Flicker) constant dependent on the device's process
α is a constant between 0.5 and 2
g_m is the device's transconductance at a selected operating point
W is the gate width
L is the gate length
C_{ox} is the oxide capacitance

f is the operating frequency

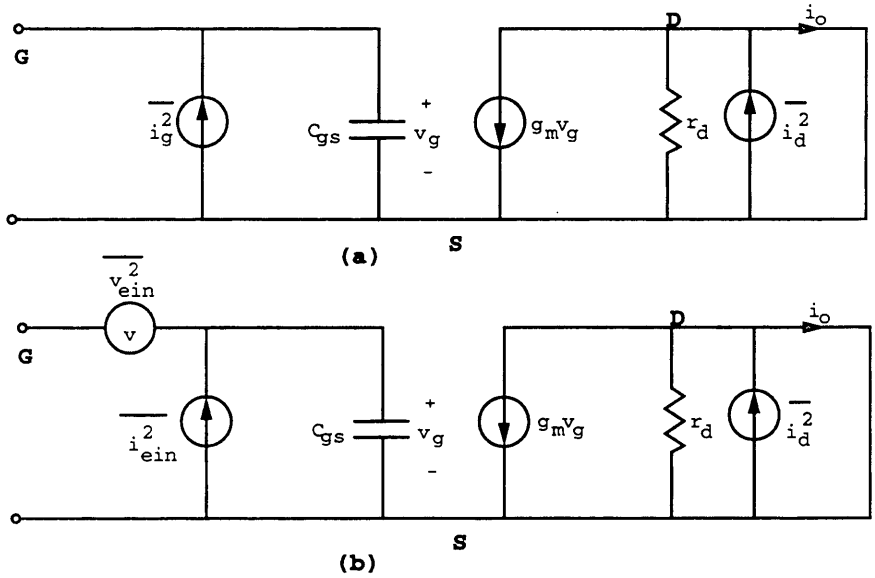

Figure 3.6: JFET Small-Signal Model with Noise Sources

The first term of Equation 3.7 represents the thermal noise in the channel which is made of a resistive material. The second therm is the channel's flicker component. Figure 3.7 shows a typical spectral density of v_{ein}.

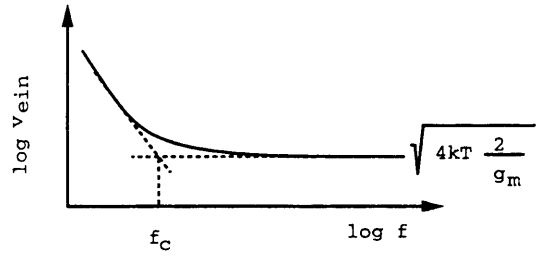

Figure 3.7: Spectral Density of the JFET's Noise Voltage

At low frequencies, the flicker noise dominates. At high frequency, the channel thermal noise dominates. The flicker corner frequencies of most low-noise JFET devices are

in the 1kHz to 10kHz range. Typical values for v_{ein} of low-noise JFET input amplifiers range from $3\frac{nV}{\sqrt{Hz}}$ to $10\frac{nV}{\sqrt{Hz}}$ [5].

The equivalent input noise current is calculated by open circuiting the inputs of circuits 3.6a and 3.6b and equating the output noise currents i_o's.

$$\overline{i_{ein}^2} = \overline{i_g^2} + \overline{i_d^2}\left(\frac{\omega C_{gs}}{g_m}\right)^2 \tag{3.8}$$

$$\overline{i_{ein}^2} = 2qI_G + \left(4kT\frac{2}{3}g_m + K\frac{I_D^\alpha}{fC_{ox}WL_{eff}}\right)\left(\frac{\omega C_{gs}}{g_m}\right)^2 \tag{3.9}$$

where I_G is the DC gate current, C_{gs} is the gate-source capacitance, and ω is $2\pi f$, where f is the operating frequency.

The first term is the shot noise from the gate leakage; the second and third terms are the coupling of the channel noise (thermal and flicker) to the input. At low frequency, the noise current is dominated by the gate leakage current I_G. Noise performance at low frequency is degraded if I_G has a flicker component. At high frequency, the second term of Equation 3.9 dominates because it is directly proportional to f^2. The spectral density of i_{ein} is shown in Figure 3.8. Typical i_{ein} values for low-noise JFET input amplifiers (at the flat region of Figure 3.8) range from $0.5\frac{fA}{\sqrt{Hz}}$ to $3\frac{fA}{\sqrt{\ }}$ [5].

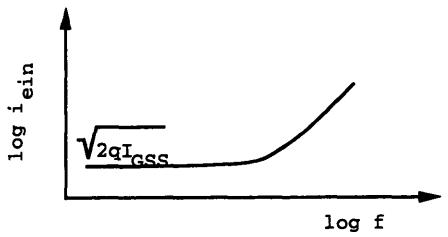

Figure 3.8: Spectral Density of the JFET's Noise Current

3.4 Noise Model of the Metal-Oxide-Semiconductor Field Effect Transistor

The MOSFETs noise model is very similar to the JFETs noise model shown in Figure 3.6. The exceptions are as follow. Because the gate of the MOSFET is isolated by an insulator (SiO2), there is essentially no current flow between the gate and channel, except for extremely small leakage current (<< 1pA). This characteristic of the MOSFETs make them ideal for high impedance source signals.

The MOSFETs are generally operated in the saturation region for optimal noise performance. In this region, the operational drain current equation can be modeled as:

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{3.10}$$

The last parenthesized term models the channel length modulation, and can here be ignored as a second order effect. The transconductance is:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \sqrt{2\mu C_{ox}\frac{W}{L}I_D} \tag{3.11}$$

The noise models of a MOSFET are shown in Figures 3.9a and 3.9b.

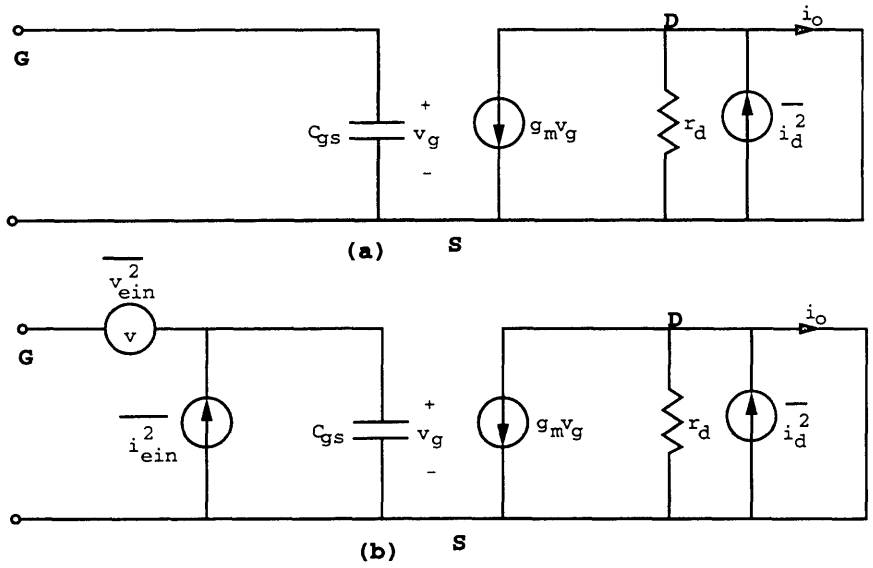

Figure 3.9: MOSFET Small-Signal Model with Noise Sources

The only noise source is $\overline{i_d^2}$ (the channel thermal and flicker noise). And because flicker noise is significant in MOSFETs, the flicker component should be considered during the designing process. The gate current of a MOSFET is extremely small, so it is generally neglected. The equations for Figure 3.9b are:

$$\overline{v_{ein}^2} = \frac{\overline{i_d^2}}{g_m^2} \tag{3.12}$$

$$\overline{v_{ein}^2} = \frac{8kT}{3g_m} + K\frac{I_D^\alpha}{g_m^2 f} \tag{3.13}$$

$$\overline{i_{ein}^2} = \overline{i_d^2}\left(\frac{\omega C_{gs}}{g_m}\right)^2 \tag{3.14}$$

$$\overline{i_{ein}^2} = \left(4kT\frac{2}{3}g_m + K\frac{I_D^\alpha}{fC_{ox}WL_{eff}}\right)\left(\frac{wC_{gs}}{g_m}\right)^2 \tag{3.15}$$

where:

I_D is the operating drain current (typically 100μA to 1000μA)
Cgs is the gate-source capacitance (typically 2pF to 5pF)
$\omega=2\pi f$, f being the operating frequency

g_m is the transistor's transconductance (typically 0.001mho to.006mho)
K is the flicker coefficient (typically 3.4 X 10^{-24}) [3]
α the flicker exponent (0.8 to 1.2)
W is the gate width of the transistor (1000μm to 3000μm)
L is the gate length of the transistor (1.2μm to 3μm)
C_{ox} is the oxide capacitance

The channel noise $\overline{i_d^2}$ can be reduced by operating the transistor in a high transconductance state. In general, the flicker is a large source of noise in MOS devices in the DC to kilohertz range, so a device with large gate area can help reduce flicker noise. However a large gate will result in larger gate capacitance, which will increase the noise gain of the system (which will be discussed in section 4.3). The flicker noise is caused by the trapping centers at the boundary between the silicon channel and the silicon-dioxide interface. It increases with temperature and density of the surface state. Also, it decreases with increasing gate area and with increasing C_{ox}. Large C_{ox} can be achieved by decreasing the oxide thickness, T_{ox}. It is known that the flicker noise in an n-channel MOSFET is three times higher than in a p-channel MOSFET [4]. A MOSFET used in low-noise applications can have noise value v_{ein} of $15\frac{nV}{\sqrt{Hz}}$ or higher.

3.5 The Buried Channel MOSFETs

The buried-channel (BC) MOSFETs are a cross between the conventional JFETs and the conventional MOSFETs. The silicon-dioxide insulation between the gate and the channel (similar to the MOSFETs) offers better gate to channel leakage isolation than the p-n junction of the JFETs [6]. The n-channels are the most popular because of their higher transconductance.

Isolation between the channel and the insulator (SiO_2) eliminates the higher level of flicker problem of the MOSFET, so using the lower mobility of the p-type material is no longer a necessity. Instead of having the channels right underneath the silicon dioxide

insulator, the BC MOSFETs channels are deeper within the substrate and therefore isolated from the silicon dioxide by the substrate. This allows for less defects between the silicon dioxide and the channels, as in most conventional MOSFETs. The buried-channel devices are found to be attractive as they have the low gate leakage current of the conventional MOSFETs, and also have lower flicker noise since the channel is away from the silicon dioxide insulator. This lowers trapping in the interstate of the MOSFET's interface.

Buried-channels are commercially available in foundries that have charge coupled devices (CCD) capabilities. They have sufficiently acceptable transconductance (about 1mSiemen). One disadvantage is that they require larger voltages for a typical amplifier's linear operations. Also, like JFETs, they tend to run at much higher currents, but have a lower transconductance than the JFETs.

3.6 Excess Noise in Resistors

Most resistors exhibit both thermal as well as some excess noise, such as flicker. Excess noise in a resistor results when DC current flows through it. It is believed that this noise occurs at the contact point between the conductor. This problem is aggravated by the discontinuity in the conducting material. Very large valued resistors, which are produced by reducing the concentration of the conductive material, are known to have higher excess noise because of the greater discontinuity in the conductor material.

Chapter 4

Noise Calculations in Circuits

4.1 Introduction

Reference [7] presents some guidelines concerning the designing of low-noise amplifiers. These are summarized below.

(1) Impedance matching at the amplifier input and source matching techniques for the best noise performance are entirely different. Matching the source for noise reduction involves matching the $\frac{v_{ein}}{i_{ein}}$ ratio to the source impedance (where v_{ein} is the input referred noise voltage and i_{ein} is the input referred noise current). Let's assume that we have a source with a real input impedance of R_S, which generates a noise value of $4kTR_S$. Minimum noise will be added into the system if the op-amp interfacing this source is designed to have an input referred noise characteristic so that $\frac{v_{ein}}{i_{ein}} = R_s$. From this relationship, we can see that i_{ein} should be kept small if R_S is very large. We can see that only the bipolars are suited for low source resistance applications as i_{ein} of a bipolar can be large. Because i_{ein} of the FET's can be smaller, FETs are good for high source resistance applications

(2) Noise performance of amplifiers, besides being dependent on the amplifiers, is also a function of the signal source impedance and frequency range. These two factors determine the optimum input stage. For example, for a low impedance source, the effect of the noise current at the input of the op-amp would not be as detrimental as for a source with higher impedance.

(3) For narrow-band reactive sources, the noise gain can be reduced by the addition of a suitable (inverse, cancelling) reactance at the amplifier input. An LC network can be used to tune out the element contributing to the noise gain.

(4) The noise performance of the FET's at low frequencies is related to flicker noise, mid-band noise is related to g_m, and at high frequencies to the coupling of the gate-drain parasitic capacitor and f_t. of the device. Low-noise junction transistors should have a high current gain $\beta(j\omega)$, a minimum base resistance r_b, and a high cutoff frequency f_t.

(5) Noise performance of monolithic amplifiers is usually inferior to that of discrete amplifiers because processing of discrete components involves less contamination. However, for most wideband applications, monolithic amplifiers may prove sufficient and should be considered first as discrete amplifiers may have inferior high frequency performance. Also, discrete amplifiers cost more due to more manufacturing steps.

(6) High precision in noise calculations serves little purpose, not only because of manufacturing spread of the parameters but also because noise sources are nearly always uncorrelated. As a result, secondary noise sources, such as second stage noise, should have only minor effect.

(7) The common-emitter (common-source for FETs), common-base (common-gate), and common-collector (common-drain) have the same equivalent input noise generators. For most application, the common-emitter is the best configuration for low-noise applications because it has high voltage and high current gain so that any noise at its output terminal is attenuated by some gain when referred back to the input terminal. Common-base is generally considered unsuitable for low-noise application because its current gain is approximately one. Any noise current at its output terminal is referred directly to the input without any reduction. The common-collector (or the emitter-follower) has unity voltage gain, so any noise voltage at its output is referred back to the input without reduction. Though its unity gain characteristic makes the emitter-follower less attractive as a low-noise input stage configuration, careful design can make it acceptable for certain applications, using its high input impedance and low output impedance as a buffer stage.

4.2 Noise Models of Amplifiers

In order to facilitate the noise analyses of amplifiers, a simple model has been developed to assist in understanding noise issues. The noise model is made simple by referring the noise source to the input terminals. Not only does this allow us to model the amplifier as a noiseless element, but we can consider the noise signal as a typical input signal and can easily see how the amplifier circuit respond to it. The Figure 4.1a shows two noisy single-ended amplifiers with gains of A_1 and A_2 and output noise readings of v_1 and v_2 respectively. For simplicity, we will keep the analysis to noise voltage sources only. The equivalent input noise values of these two amplifiers are v_{in1} and v_{in2}, the output noise readings divided by the different gains.

$$\overline{v_{in1}^2} = \frac{\overline{v_1^2}}{A_1^2} \tag{4.1}$$

$$\overline{v_{in2}^2} = \frac{\overline{v_2^2}}{A_2^2} \tag{4.2}$$

We now cascade the two amplifiers (see Figure 4.1b). The output noise from the first stage measured at node v_{o1} is $A1(v_{in1})$; and taking into account the noise contribution from the second amplifier, the total noise at v_{o1} is $[(a_1 v_{in1})+v_{in2}]$. The noise contribution at v_{o2} comes from noise of the second system as well as from the first; however noise from the first system is also multiplied by the gain of the second system, so

$$\overline{v_{o2}^2} = A_2^2\overline{v_{in2}^2} + A_2^2(A_1^2\overline{v_{in1}^2}) \tag{4.3}$$

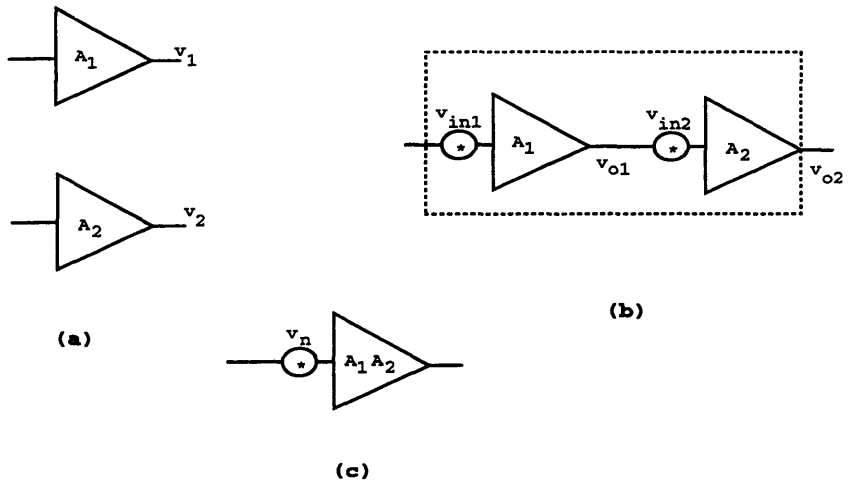

Figure 4.1: Noise Model of the Single-Ended Amplifier

The output noise is strongly dominated by noise from the first amplifier if gain $A_1 > 1$. To keep the total output noise (v_{o2}) small, it is important to keep v_{in1} as small as possible.

If we were to combine the two stages into one amplifier, now with a gain of A_1A_2 (see Figure 4.1c) the equivalent input noise of the system is now:

$$\overline{v_{in}^2} = \frac{\overline{v_{o2}^2}}{A_1A_2} = \frac{\overline{v_{in2}^2}}{A_1} + \overline{v_{in1}^2} \tag{4.4}$$

In order to keep the noise to a minimum v_{in} must be kept small, by making v_{in1} small.

In our preamplifier circuit, we will be using an amplifier with two input terminals, usually with a differential pair input stage consisting of two separate single-ended stages. If we use JFET or Bipolar input devices, we will need to deal with noise current as well. The noise model of a typical op-amp is shown in Figure 4.2a.

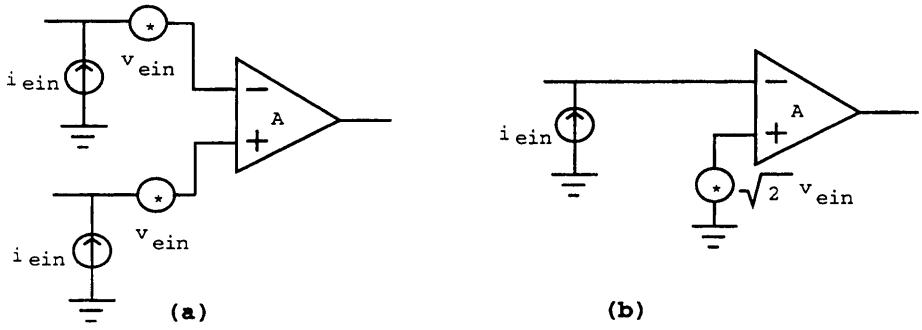

Figure 4.2: Noise Model of the Differential Amplifier

Amplifier noise is represented completely by a zero impedance voltage generator v_{ein} in series with the input port and an infinite impedance current generator i_{ein} in parallel with the input. Both v_{ein} and i_{ein} are required to represent the noise characteristic of the amplifier. When the source resistance (impedance) is very large, the noise current dominates and the noise voltage has a less significant effect and vice-versa. Generally there is no correlation between the voltage generator and the current generator.

Because we will be connecting the non-inverting terminal to a low-impedance source, the effect of the noise current is negligible, so the current source can be removed from the non-inverting terminal (Figure 4.2b). The noise voltage sources of Figure 4.2b can be combined and placed either at the inverting or non-inverting terminal. It has been a convention to place the combined noise voltage sources $2\overline{v_{ein}^2}$ at the non-inverting terminal. The noise current at the inverting terminal will generate a noise voltage if there is a finite impedance at the non-inverting node. The resulting noise model for the amplifier circuit in our application is shown in Figure 4.2b.

In practice, we are generally interested in the signal-to-noise ratio (SNR) at the output of the system. As suggested in the discussion of Equation 4.3, increasing A_1 not only increases the gain of the information signal but that of the noise as well. If we can increase

A_1 without increasing the input noise voltage v_{in1}, then we may win with the signal to noise ratio.

4.3 The Closed-Loop Amplifier

The circuit shown in Figure 4.3 shows the preamplifier in the desired configuration for our application (as mentioned in Section 1.3).

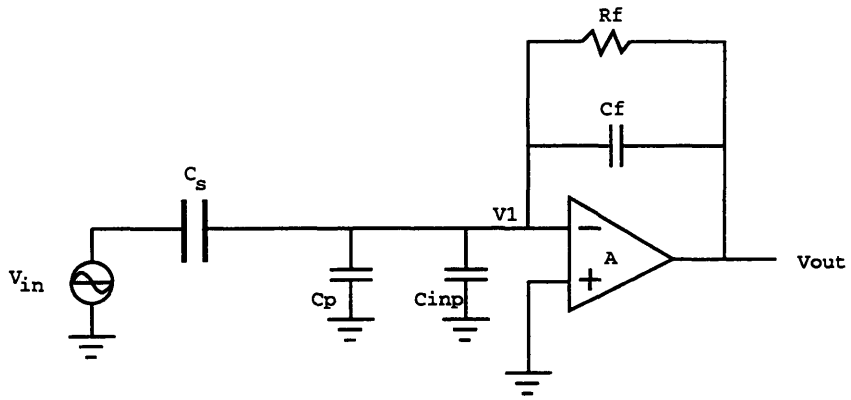

Figure 4.3: Closed-Loop Amplifier with Parasitic Capacitances and DC Stabilization

The feedback resistor R_f was chosen to be very much larger than the impedance of the feedback capacitor C_f at 27kHz so that the signal current will flow through C_f instead of R_f. If R_f is chosen to be very large, it will generate a large thermal noise voltage ($4kTR_f$).- Because of the shunting capacitive effect of C_f as discussed in section 2.5, the higher resistor value provides a lower cut-off frequency, thus providing lower noise at 27kHz. However, the output offset voltage (I_GR_f) due to the DC current I_G (the gate current of the input device) at the input of the op-amp will limit how big R_f can be.

Assume for now that the system in Figure 4.3 is noiseless. We will consider the circuit's response to the input signal. If the op-amp's finite low-frequency gain is A, the signal gain at low frequency (from V_{in} to V_{out}) is

$$\frac{V_{out}}{V_{in}} = -\frac{C_s}{C_f + \frac{C_s + C_p + C_f + C_{inp}}{A}} \tag{4.5}$$

If A is made sufficiently large, then the system gain simplifies to

$$\frac{V_{out}}{V_{in}} \cong -\frac{C_s}{C_f} \tag{4.6}$$

This transfer function is valid at a frequency when the op-amp's gain is still sufficiently large. The signal gain is increased as C_s (the sensor capacitance) is made large and C_f is made small. As mentioned in Section 1.2, C_s is limited to 1pF to 2pF. C_f cannot be made too small before its value becomes comparable to the parasitic capacitances. Once parasitics contribute to the value of C_f, then the signal gain $\frac{C_s}{C_f}$ becomes uncontrollable and unpredictable. Thus a value of 2pF was chosen for C_f.

The noise signal exists simultaneously with the information signal. If we short out the information signal generator, we can consider the noise response (see Figure 4.4). Remember that the charge amplifier's noise is modeled as noise voltage at the non-inverting terminal of the op-amp. This noise voltage generator will be called $\overline{v_{ein}^2}$ and will represent the total input referred noise voltage of the op-amp. The noise value $\overline{v_{ein}^2}$ must be divided by 2 if an input noise voltage of one terminal (or half circuit of the op-amp) is used. We will ignore the parasitic gate leakage current for now since the gate-current is MOSFETs is practically zero.

Assuming the noise from the feedback resistor R_f and the noise current $\overline{i_{ein}^2}$ are negligible, the low frequency response of this circuit to the noise source $\overline{v_{ein}^2}$ is

$$\frac{V_{out}}{v_{ein}} = -\frac{C_s + C_f + C_p + C_{inp}}{C_f + \frac{C_s + C_f + C_p + C_{inp}}{A}} \tag{4.7}$$

Again if we design the operational amplifier to have a sufficiently large gain A (A>>1), then the noise's gain, simplifies to

$$NoiseGain \cong -\frac{C_s + C_f + C_p + C_{inp}}{C_f} \tag{4.8}$$

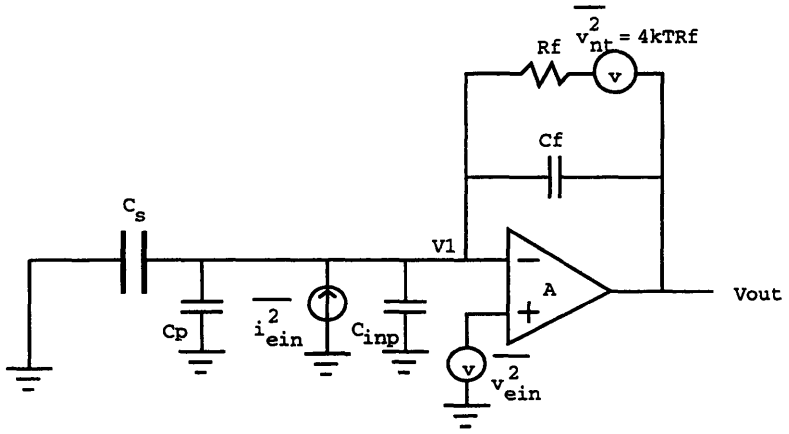

Figure 4.4: Closed-Loop Amplifier with Noise Sources

If we compare the noise gain to the signal gain, we can see that the noise gain becomes much larger than the signal's gain with increasing parasitic capacitance, C_{inp} which is created by the input device of the amplifier at the summing node.

As mentioned earlier, an input FET device with large gate area reduces flicker noise and that a large $\frac{W}{L}$ ratio (which also contributes to a larger gate area) offers lower noise by increasing the transconductance. These actions to reduce noise, of course, increase the gate capacitance of the amplifier's input device. Thus there is a trade-off between the reduction of noise and the increase in noise gain with increasing device size.

The best way to resolve this trade-off is to consider the signal-to-noise ratio (SNR) instead of just the absolute noise value. Evaluating the SNR will offer us a means to design the input device for an optimal noise performance.

The SNR of the circuit in Figure 4.3 is defined as:

$$SNR = \frac{V_{in}\frac{C_s}{C_f}}{v_{ein}(\frac{C_s+C_f+C_p+C_{inp}}{C_f})} = \frac{V_{in}C_s}{v_{ein}(C_s+C_f+C_p+C_{inp})} \tag{4.9}$$

where v_{in} is the input signal and v_{ein} is the noise signal. The noise source v_{ein} of a MOS-FET is:

$$v_{ein} = \frac{8kT}{3g_m} + \frac{K_f I_d^{\alpha}}{fWL_{eff}C_{ox}g_m^2} \tag{4.10}$$

which is described in Section 3.4. The input capacitance C_{inp} represents the gate-source capacitance of the input device.

As we increase the device size, v_{ein} decreases, and C_{inp} will increases. The SNR plot for the Orbit 1.2 process is shown below (for a current of 500μA and a gate length (L) of 1.8μm).

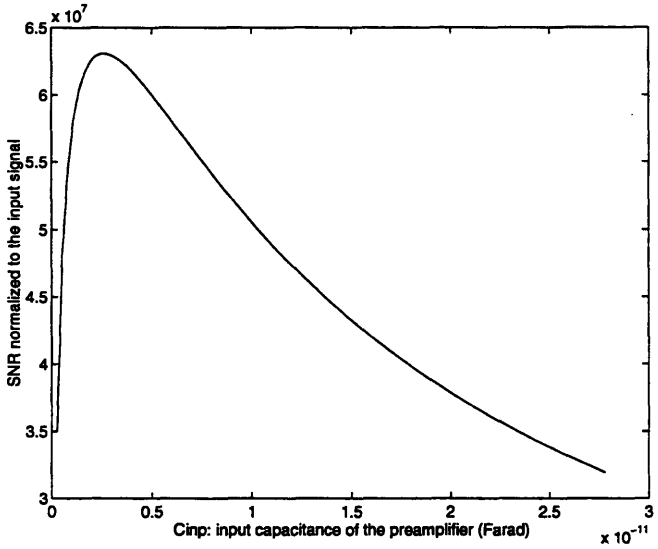

Figure 4.5: Normalized SNR for Different Device Sizes

The curve can give us an idea of what the optimal device size that is a width and length resulting in 2.5pF of gate capacitance, which offers the best signal-to-noise ratio.

When the flicker coefficient is incorporated into the calculation of SNR versus C_{inp}, the curve looks similar to that in Figure 4.5 (see Figure 4.6), but the larger area needed may shift the optimal point to the right (> 5pF), as we might need more W for a chosen L to get the necessary area to reduce flicker.

A large gate length L has the most significant effect in the reduction of flicker noise, however, large L increases the input capacitance of the op-amp as well as degrades frequency performance. Thus it is better to choose an L that is a little longer than the minimum length (to reduce the flicker noise and short channel length effect) without sacrificing too much frequency response. Then find the optimal W for highest SNR. There is no assurance that the flicker coefficient is the same for every device, so it is best to optimize for best SNR with the thermal noise only and then increase the W and L by the same proportion to keep the flicker noise down.

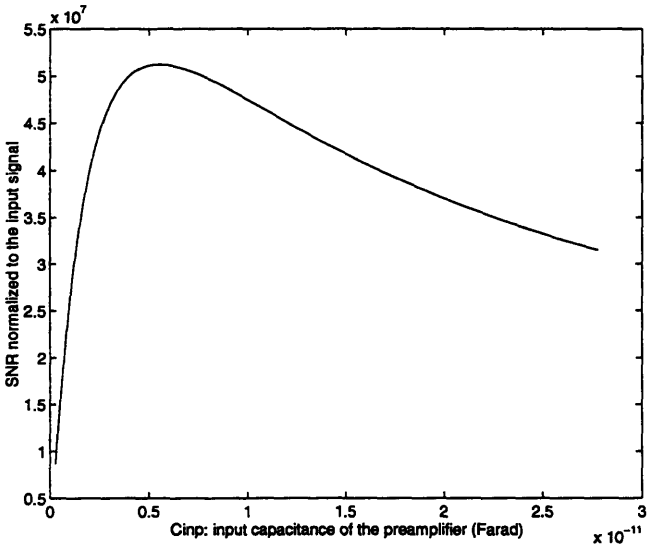

Figure 4.6: Normalized SNR for Devices with Flicker Noise

4.4 Input Device Selection for a Source Impedance

When designing low-noise amplifiers for capacitive sensors, the source impedance is a good indicator of which types of input devices to use. The gyroscope has a capacitance of 1pF (and 4 pF stray wire bond capacitance). At 27kHz operation, the gyroscope's impedance is about 6Meg ohms. This source impedance makes the bipolars impractical for a low-noise design because bipolars require relatively large input currents. The shot noise contribution ($I_G\frac{1}{\omega C_f}$) would then be a large noise source. Typical low-noise bipolar input op-amps have input currents in the nanoampere range. For example, if the input current is 1nA, the noise current is $i_g = \sqrt{2qI_G} = 17.89\frac{fA}{\sqrt{Hz}}$, resulting in a noise voltage of $(i_g\frac{1}{\omega C_f}) = 52\frac{nV}{\sqrt{Hz}}$. If I_G is 1pA instead, then the noise current is only $0.57\frac{fA}{\sqrt{Hz}}$ and, at 27kHz, the noise contribution would only be $1.67\frac{nV}{\sqrt{Hz}}$. This is an acceptable noise contribution and can probably be neglected in this system.

For low impedance sources, even if the noise current is the dominant source, a low impedance minimizes the effects of the noise current. Bipolars are generally good for these types of sources because of their very low noise voltage and low input noise current. Low-noise amplifier can therefore be achieved with bipolar transistors.

For high source impedance (such as most micro-capacitive sensors) input devices with little (1pA or less), or no input current, are necessary to keep the noise current contribution low. With a source impedance in the Megohm range, interaction with the larger input current of the bipolar will contribute noise in the $50\frac{nV}{\sqrt{Hz}}$ to $100\frac{nV}{\sqrt{Hz}}$ range.

If we were to choose a FET device (JFET or MOSFET), we can reduce the effect of the noise current. Though FET devices tend to have higher thermal noise voltage because of their lower transconductance, we win by taking advantage of the significantly lower noise current.

JFETs are usually a good choice for overall low noise current and low noise voltage performance. Though its noise voltage is not as low as the bipolar, the JFETs have significantly lower input current than the bipolars. Low-noise JFET input currents tend to range from sub-pico amperes to 20 pico-amperes, resulting in a noise current from sub-$\frac{fA}{\sqrt{Hz}}$ to $20\frac{fA}{\sqrt{Hz}}$. The noise current of a JFET is higher than that of a MOSFET (which has practically no input current). However, MOSFETs are plagued by flicker noise components, even at frequencies as high as 100kHz.

4.5 The Load Device

The loads of the input stage are the second largest noise sources in most monolithic amplifiers. Though many experts advise ignoring secondary noise sources, their contribution can be significant if the loads are not properly designed. Resistors loads should be used for low-noise performance, however the large resistor values required for the typical input stage gain of an operational amplifier make this option impractical in integrated circuit technology that has mainly polysilicon resistors available. In integrated circuits, an active load (accomplished with a transistor) is generally employed to obtain high gain. However, because transistors introduce many more noise sources beside the thermal noise, the active load introduces noise beyond the fundamental thermal noise of a resistor.

Chapter 5

Designing Low-noise Amplifiers from Commercial Parts

5.1 Introduction

There are many commercial bipolar input op-amps with extremely low input noise voltage ($3\frac{nV}{\sqrt{Hz}}$ or less). One of them is the OP-27 from Analog Device Inc. As mentioned in Section 5.4, the problem with a bipolar input stage is the high level of input current necessary to operate the transistors. This input current generates shot noise that can be significant if there is a high impedance current path at the op-amp's input.

A simple solution to this problem is to isolate the high impedance summing node of the preamplifier from the input current of the OP-27. This is accomplished by placing an input stage with low-noise devices to buffer the high impedance input node from the noise current of the OP-27. Depending on the circuit of the front end, this strategy can introduce instability. The OP-27 has a gain margin of approximately 7dB (or 2.24). If the new input stage adds gain that exceeds the gain margin, the new amplifier will be unstable for near unity-gain configurations. Neverthless, besides the simplicity and convenience it offers, this solution also currently results in the best noise performance for capacitive sources.

This chapter will detail the construction of two low-noise preamplifiers, both realized with an OP-27 and an add-on input stage composed of discrete parts. One uses a differential pair front end and the other a dual source follower front end.

5.2 Input Device Selection

The merit of discrete transistors is their superior processing quality. Device integration introduces a lot more noise because of the extra processing steps and variables which lead to more contamination. As mentioned in chapter 5, the high impedance of the source restricts us to FET input devices (JFETs or MOSFETs). The MOSFETs were rejected for

their unpredictable quantization of the flicker noise component as well as for their lower transconductances.

The chosen device was an N-channel JFET device called the U440 from Siliconix. Specification sheets state that it has a low typical input referred noise ($3\frac{nV}{\sqrt{Hz}}$) as well as low input capacitance (1pF) and a low gate leakage current (1pA max at room temperature). The input current will introduce a noise current of $0.6\frac{fA}{\sqrt{Hz}}$, which is sufficiently small for the feedback impedance of $\frac{R_f}{1+jwRfC_f}$ (where f ranges between 22kHz and 32kHz). The corner frequency of the flicker component was below 1kHz, so the voltage flicker noise will not be a problem at the operating frequency of 27kHz.

5.3 Input Stage Topology

In order to keep the noise as low as possible, choosing a simple input topology was important. Two popular input configurations used in this type of circuit are the source follower and the common-source. Because it is crucial to keep the two input terminals of the preamplifier balanced for common-mode rejection, we used the differential pair configuration and the dual source follower. The balanced input stages will reduce the voltage offset into the OP-27 stage. The two input JFET devices need to be highly matched in order to acquire superior quality in input offset voltage, common-mode rejection ratio, and power supply rejection ratio.

The differential-pair configuration with the operational amplifier second stage is shown in Figure 5.1.

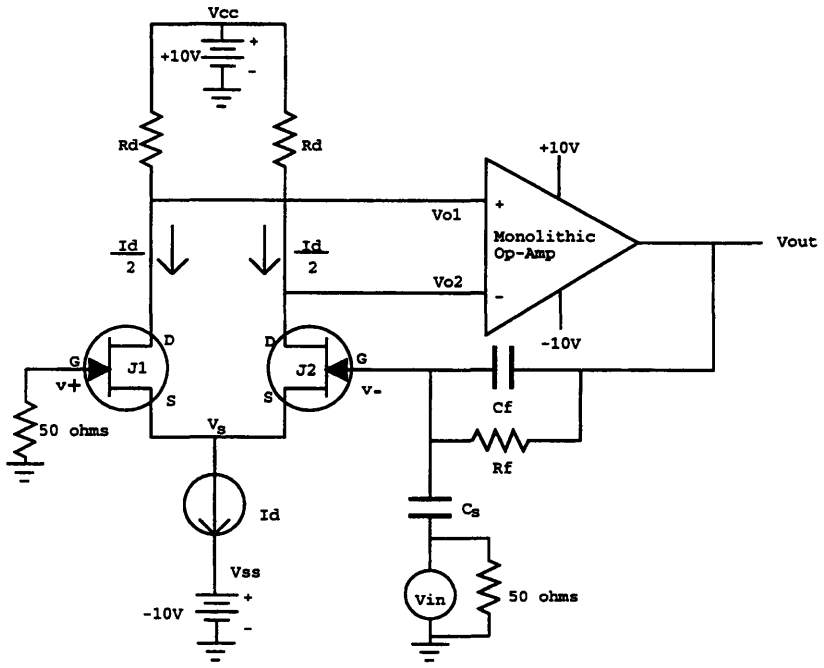

Figure 5.1: The Differential Pair Input Stage

The input terminals of the new op-amp are *v+* and *v-*; the output terminal is *Vout*. The gates of J1 and J2 are kept as close as possible to ground (the midpoint between the +10V and -10V supplies). The 50-ohm resistors are used to suspend the preamplifier circuit above the ground plane. Components are directly connected to each other without sockets or other intermediate connecting interfaces, thus resulting in minimal parasitics.

The current source I_d forces $\frac{I_d}{2}$ to flow through each leg of the differential pair. The current $\frac{I_d}{2}$ and R_d set the transistor's drain voltages (v_{o1} and v_{o2}). The FETs then set the source voltage V_s necessary to conduct $\frac{I_d}{2}$. The source voltage node V_s must be kept positive so that the gate-channel junction is kept reverse-biased. If the junction becomes forward biased ($V_{gs}>0$, which implies a negative V_s value), then a large current will flow through the gate, causing a great deal of shot noise. Most FETs do offer some limited room for positive V_{gs}, but this is not a suitable mode of operation for low-noise application.

The JFET source follower front end, with the second stage operational amplifier is shown in Figure 5.2:

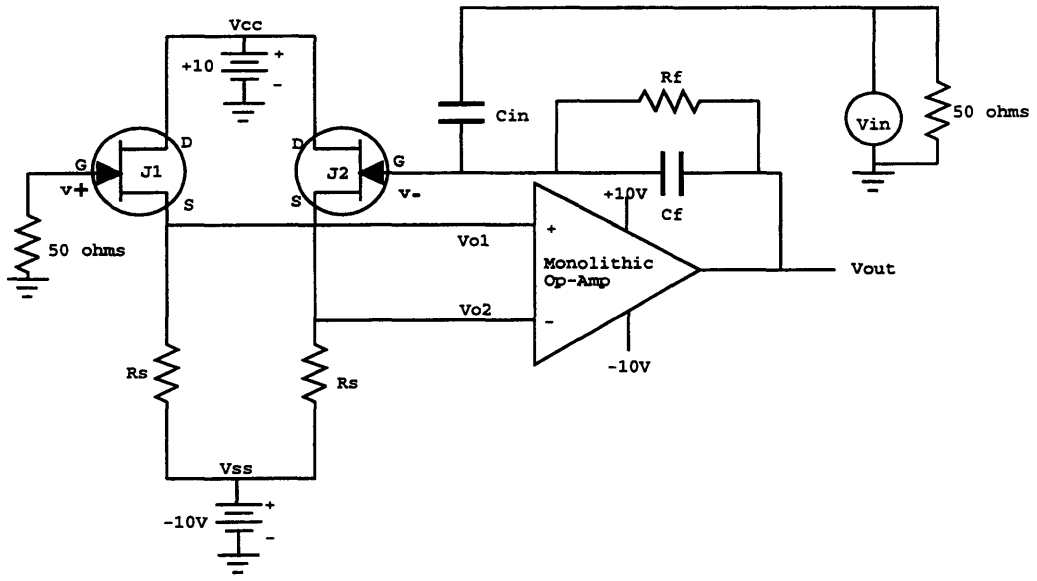

Figure 5.2: The Dual Source Follower Input Stage

Unlike the differential pair, each source follower exists as a separate circuit. Each JFET is biased by a source resistor R_s. Given a JFET transistor with known I_{dss} and $V_{gs(off)}$, the V_{gs} required to conduct a current I_d is:

$$V_{gs} = \frac{V_{gs(off)}}{(1 - \frac{I_d}{I_{dss}})^{\frac{1}{k}}} \tag{5.1}$$

where k varies from 1.7 to 2, depending on the process by which the transistor was made. The R_s necessary is $R_s = \frac{V_{gs}}{I_d}$. Usually, it is easier to bias the circuit using the load line method. Most specification sheet will give an I_d versus V_{gs} curve such as the one shown in Figure 5.3. The load line representing $\frac{1}{R_s}$ can be drawn from the origin to the current curve to find the operating current. The higher the R_s value, the smaller the slope and the lower the operating current I_d.

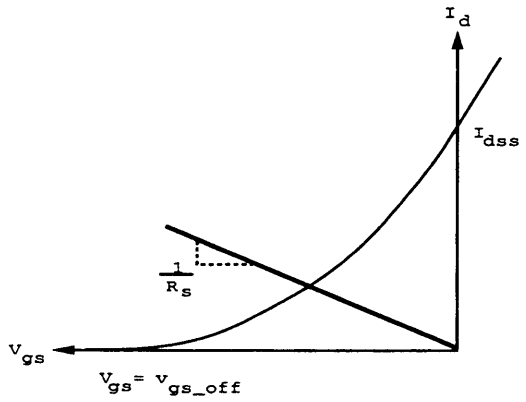

Figure 5.3: Load Line of the Source Follower

5.4 Noise Measurement Set-Up

The spectrum analyzer used had a noise floor of $30\frac{nV}{\sqrt{Hz}}$, so measuring any noise values lower or comparable to this value would require some amplification. This amplifier circuit is generally called a postamplifier. The postamplifier circuit below (Figure 5.4) was connected to the output of the preamplifier when measuring the preamplifier's noise

The circuit provides a gain of 400. Care was taken to make it a low-noise amplifier, so its noise contribution would not overwhelm the system's noise. If there is sufficient gain in the previous stage, then the postamplifier noise will not be significant. Due to AC coupling necessary (C1 in Figure 5.4) to keep the postamplifier stage from saturating, the postamplifier introduces a high pass filter with a cut off frequency of $\frac{1}{2\pi\,(1kohm)\,(0.047\mu F)} = 3kHz$. This low-frequency attenuation does not significantly affect our frequency of interest (22kHz to 32kHz), which is one decade higher.

The noise of the postamplifier comes mainly from the 1k-ohm resistor at the input terminal and the equivalent input noise of the OP-27. The 1k resistor contributes $4.2\frac{nV}{\sqrt{Hz}}$ and the OP-27 contributes $3\frac{nV}{\sqrt{Hz}}$. Together they contribute $5.2\frac{nV}{\sqrt{Hz}}$ of noise signal, which was verified by measurement.

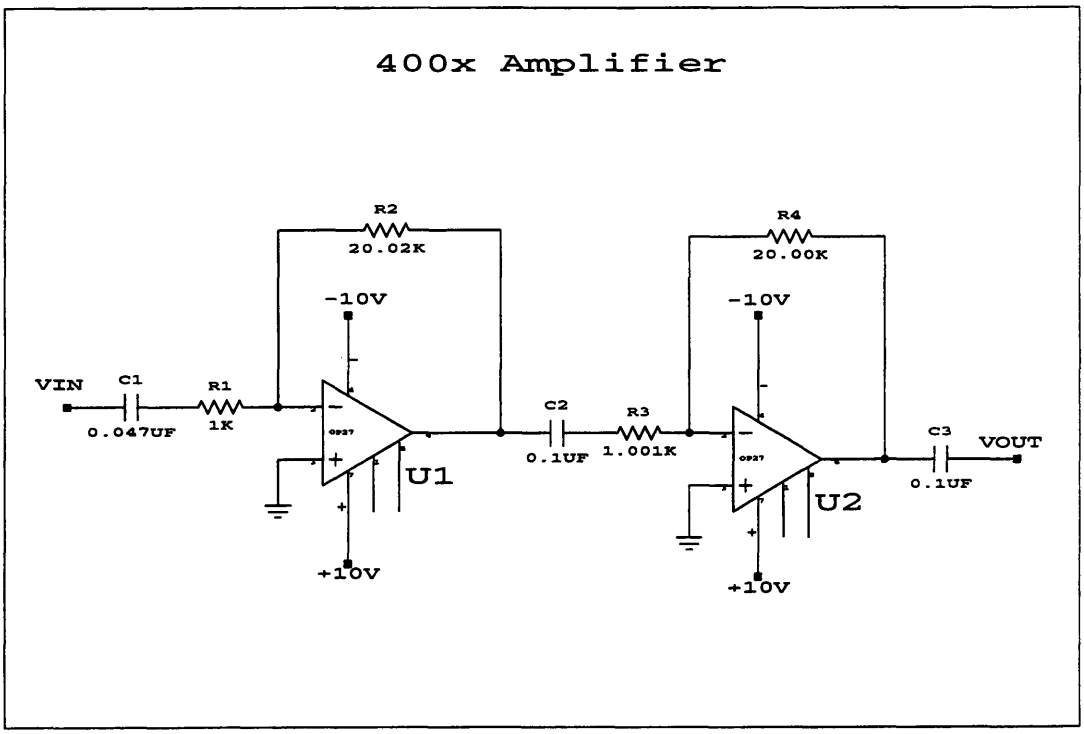

Figure 5.4: 400 Gain Amplifier Used in Noise Measurements

The analyzer measured the noise at the output of the postamplifier. The read out value divided by the 400 gain, gives a noise value referred to the output of the preamplifier (which is also the input of the postamplifier).

5.5 Noise Analysis of the Differential Pair

The differential pair front end amplifier was constructed using the components listed in Table 5.1. Specified or calculated noise voltage and noise current values (at room temperature) are also included. Silvered mica capacitors were used for their low leakage characteristic (thus low noise); and 1% metal film resistors were used because they are excellent for low-noise, wideband applications [2, 8].

Noise sources in the differential pair front end circuit are shown in Figure 5.5. All circuit components, with the exception of the capacitors, contribute noise. The half circuit

noise models in Figure 5.6a and 5.6b are used to calculate values for the equivalent input noise current and input noise voltage generators. Figures 5.6a and 5.6b consider the open-loop circuit which does not contain the capacitor C_s and the feedback network of C_f and R_f.

Component	Part No. or Material	Ein	Iin
Monolithic Amplifier	OP-27 @1kHz	$3\frac{nV}{\sqrt{Hz}}$ max: $3.8\frac{nV}{\sqrt{Hz}}$	$0.4\frac{pA}{\sqrt{Hz}}$ max $0.6\frac{pA}{\sqrt{Hz}}$
J1, J2	U440 (matched JFETs)	$3\frac{nV}{\sqrt{Hz}}$	$0.1\frac{fA}{\sqrt{Hz}}$
Cs	1pF, Silvered Mica	extremely low	extremely low
Cf	2pF, Silvered Mica	extremely low	extremely low
Rf	3.9 Gohms, Thick Film	$8.04\frac{uV}{\sqrt{Hz}}$	$2.06\frac{fA}{\sqrt{Hz}}$
Rd	500 ohms, 1% Metal Film	$2.88\frac{nV}{\sqrt{Hz}}$	$5.75\frac{pA}{\sqrt{Hz}}$
R50	50 ohms, 1% Metal Film	$0.91\frac{nV}{\sqrt{Hz}}$	$9.1\frac{pA}{\sqrt{Hz}}$

Table 5.1: Parts Used in the Differential Pair Front End

The noise source $\overline{i_d^2}$ (in Figures 5.6a and 5.6b) represents the channel's thermal and flicker noise; (1) $\overline{i_{R_d}^2}$ is the thermal noise from the resistor R_d expressed as a noise current; (2) $\overline{i_{op27}^2}$ is the noise current of the OP-27; (3) and $\left(\frac{v_{OP27}}{\sqrt{2}}\right)^2$ is the input noise voltage from the half circuit of the OP-27. The given noise value of the OP-27 ($3\frac{nV}{\sqrt{Hz}}$) is the total contribution from both input terminals of the OP-27. In the half-circuit models shown in Figures 5.6a and 5.6b, only half of the OP-27 op-amp is considered. The noise of the 50Ω resistor was neglected because its noise contribution is only $1\frac{nV}{\sqrt{Hz}}$, which is insignificant compared to the noise from the other noise sources.

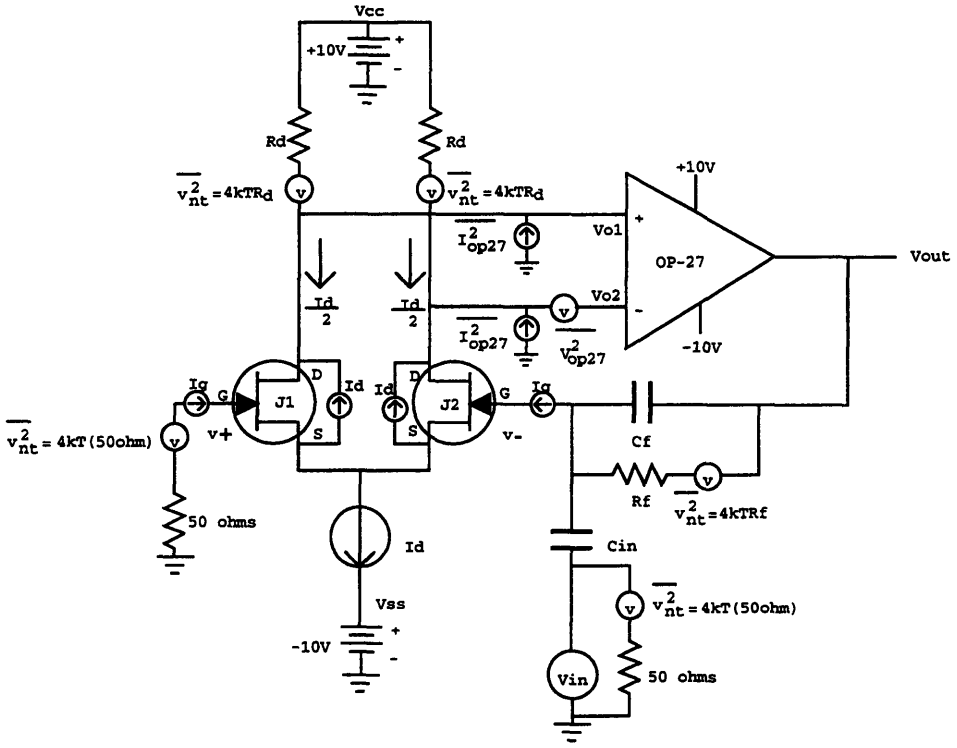

Figure 5.5: The Differential Pair Input Stage with Noise Sources

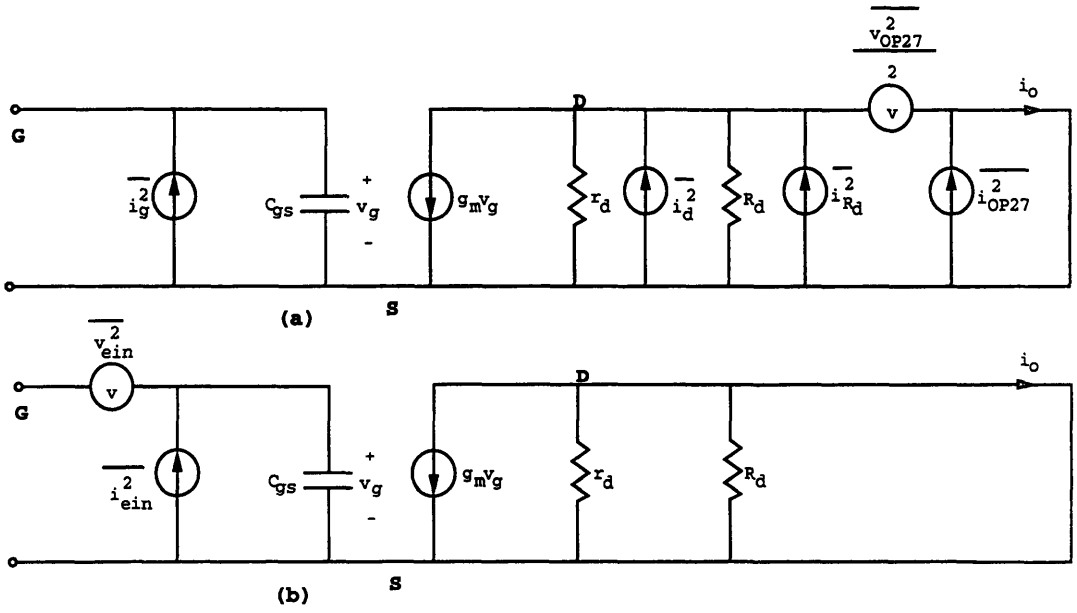

Figure 5.6: Noise Model of Differential Pair Front End Preamplifier

The simplest way to calculate the equivalent input noise values is to consider one noise source at a time (by turning all the other noise sources off). The law of superposition applies because we assume linearity in the small signal model. Using the transistor noise analyses discussed in Section 3.3 (Noise Modeling of the JFET), the equivalent input noise voltage $\overline{v_{ein}^2}$ and the equivalent input noise current $\overline{i_{ein}^2}$ of the differential pair front end amplifier are

$$\frac{1}{2}\overline{v_{ein}^2} = \overline{v_{ein\_u440}^2} + \frac{4kT}{R_d(g_m)^2} + \frac{\overline{I_{OP27}^2}}{(g_m)^2} + \left(\frac{\overline{v_{OP27}^2}}{2}\right)\left(\frac{1}{g_m R_d}\right)^2 \tag{5.2}$$

$$\overline{i_{ein}^2} = 2qI_G + \frac{8kT}{3}g_m\left(\frac{2\pi fC_{gs}}{g_m}\right)^2 + \overline{I_{OP27}^2}\left(\frac{2\pi fC_{gs}}{g_m}\right)^2 + \left(\frac{\overline{v_{OP27}^2}}{2}\right)\left(\frac{3g_m}{2}\right)^2\left(\frac{2\pi fC_{gs}}{g_m}\right)^2 \tag{5.3}$$

where g_m is the transconductance of the transistor, R_d the load resistor value, $\overline{v_{ein\_u440}^2}$ the input referred noise voltage of the U440 transistor, $\overline{I_{OP27}^2}$ the OP-27's noise current, $\overline{v_{OP27}^2}$ the input noise of the OP-27, I_G the U440's input current, C_{gs} the gate-source capacitance of the U440, and f the operating frequency. Equations 5.2 and 5.3 neglect flicker noise, so they are valid only for the high frequency range that is sufficiently greater than the flicker corner frequency. The first term $\overline{v_{ein\_u440}^2}$ of Equation 5.2 is usually expressed as $4kT\frac{2}{3g_m}$, however that model does not properly predict the noise voltage measured from the U440 devices. Such discrepancy of the measured noise from the typical noise model is usually due to processing issues. The measured noise voltage values were in agreement with the noise values stated in the specification sheet. For this reason, the U440 specified noise values were used to perform the circuit's noise calculation for comparison with the measured noise values.

In an attempt to account for the noise voltage source $\overline{v_{ein\_u440}^2}$, the preamplifier was constructed in a unity-gain configuration (see Figure 5.7). The output capacitor (0.4uF) and resistor (1KΩ) are the effective impedance (from the postamplifier) seen by the noise cur-

rent source $\overline{i_{ein}^2}$. Because the impedance Z is small, the noise current has little effect. This allows us to measure $\overline{v_{ein\_u440}^2}$ with greater ease.

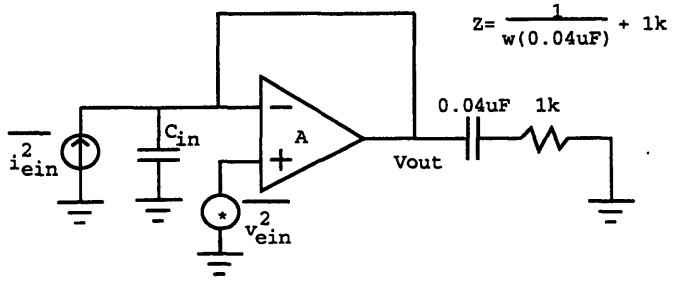

Figure 5.7: Unity-Gain Configuration of the Differential Pair Front End Preamplifier

Noise calculations were performed at room temperature and 100kHz when the flicker effect was not a factor. The output noise measured at the output of the unity-gain circuit at these conditions is $6.9\frac{nV}{\sqrt{Hz}}$. The variables in Equation 5.2 and 5.3 are listed in the table below with values dictated by the operation of the differential pair front end circuit.

Variable	Value	Variable	Value
g_m	6 mmhos	I_{OP27}	$0.4\frac{pA}{\sqrt{Hz}}$
R_d	500 ohms	v	$3.0\frac{nV}{\sqrt{Hz}}$

Table 5.2: Variables Used in Equations 5.2 and 5.3

Equation 5.2 comes now becomes

$$\frac{1}{2}\overline{v_{ein}^2} = \left(3\frac{nV}{\sqrt{Hz}}\frac{1}{\sqrt{2}}\right)^2 + \frac{4kT}{(500)\,(6\times10^{-3})^2} + \left(0.4\frac{pA}{\sqrt{Hz}}\frac{1}{6\times10^{-3}}\right)^2 + \left(3\frac{nV}{\sqrt{2}\sqrt{Hz}}\frac{1}{(500)\,(6\times10^{-3})}\right)^2 \quad (5.4)$$

$$\frac{1}{2}\overline{v_{ein}^2} = 4.5\times10^{-18}\frac{V^2}{Hz} + 9.2\times10^{-19}\frac{V^2}{Hz} + 4.44\times10^{-21}\frac{V^2}{Hz} + 5.0\times10^{-19}\frac{V^2}{Hz} = 5.9\times10^{-18}\frac{V^2}{Hz} \quad (5.5)$$

$$\frac{1}{\sqrt{2}} v_{ein} = 2.4\times10^{-9} \frac{V}{\sqrt{Hz}} \tag{5.6}$$

The total noise voltage of the entire amplifier is $\sqrt{2}$ times the value in Equation 5.6. Because the gain of the circuit (Figure 5.7) is one, the calculated v_{ein} is also the calculated output noise.

$$v_{out\_noise} = v_{ein} = \sqrt{2}\,(2.40\frac{nV}{\sqrt{Hz}}) = 3.44\frac{nV}{\sqrt{Hz}} \tag{5.7}$$

Because the unity gain amplifier is connected to the postamplifier, the input noise from the postamplifier ($5.23\frac{nV}{\sqrt{Hz}}$) is a significant noise source and must also be accounted for. So the noise measurement taken at the output of the unity-gain circuit in Figure 5.7 is

$$\overline{v^2_{out\_total}} = (3.44\frac{nV}{\sqrt{Hz}})^2 + (5.23\frac{nV}{\sqrt{Hz}})^2 = 3.92\times10^{-17}\frac{V^2}{Hz} \tag{5.8}$$

$$v_{out\_total} = 6.26\frac{nV}{\sqrt{Hz}} \tag{5.9}$$

This calculated noise value is close to the measured noise value of $6.9\frac{nV}{\sqrt{Hz}}$. The measured spectral density of the noise of the unity-gain configuration is shown in Figure 5.11. The spectral density is generally flat at the range of frequency we are interested in. It appears that there is no significant flicker noise in the preamplifier's noise voltage.

To observe the effects of the noise current on the closed-loop network, the noise of the circuit configuration shown in Figure 5.5 (simplified in Figure 5.8) was measured. This configuration is the one we will use in our application

The noise at the output ($\overline{v^2_{out\_total}}$)now consists of the $\overline{v^2_{ein}}$ noise source multiplied by the circuit's noise gain, $\overline{i^2_{ein}}$ (the impedance seen at the summing node), the thermal noise of R_f, and the input noise from the 400x amplifier. The measured noise gain is 2.4.

$$\overline{v^2_{out\_total}} = \overline{v^2_{ein}}\,(2.4)^2 + \overline{i^2_{ein}}\,(\frac{1}{2\pi f C_f})^2 + \frac{4kTR_f}{(1+2\pi f C_f R_f)^2} + \overline{v^2_{400x}} \tag{5.10}$$

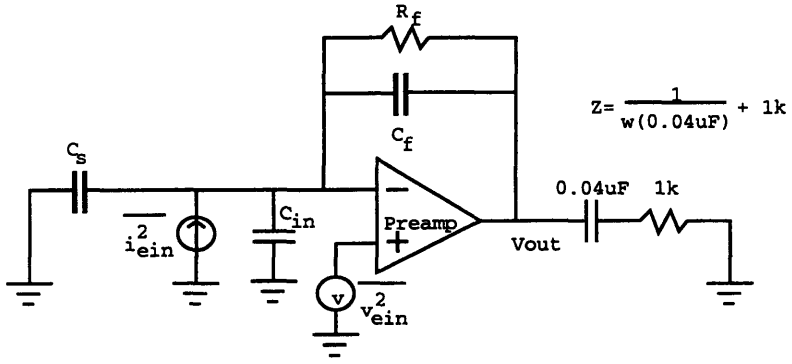

Figure 5.8: Typical Closed-Loop Configuration of the Preamplifier

At 100kHz and using the values shown in Table 5.3 for the equation variables, $\overline{i_{ein}^2}$ is

$$\overline{i_{ein}^2} = 3.2\times10^{-31}\frac{A^2}{Hz} + 6.5\times10^{-30}\frac{A^2}{Hz} + 1.58\times10^{-32}\frac{A^2}{Hz} + 3.6\times10^{-29}\frac{A^2}{Hz} = 4.3\times10^{-29}\frac{A^2}{Hz} \tag{5.11}$$

$$i_{ein} = 6.6\times10^{-15}\frac{A}{\sqrt{Hz}} = 6.6\frac{fA}{\sqrt{Hz}} \tag{5.12}$$

So the total output noise value of the circuit in Figure 5.8 is

$$\overline{v_{out\_total}^2} = \left(3.44\frac{nV}{Hz}(2.4)\right)^2 + \left(\frac{6.6\frac{fA}{\sqrt{Hz}}}{1.26\times10^{-6}}\right)^2 + \frac{4kT(3.9\times10^9)}{\left(1+2\pi(100k)\,(2pF)\,(3.9\times10^9)\right)^2} + \left(5.23\frac{nV}{\sqrt{Hz}}\right)^2 \tag{5.13}$$

$$v_{out\_total}^2 = 6.8\times10^{-17}\frac{V^2}{Hz} + 2.7\times10^{-17}\frac{V^2}{Hz} + 2.7\times10^{-18}\frac{V^2}{Hz} + 2.7\times10^{-17}\frac{V^2}{Hz} = 1.3\times10^{-16}\frac{V^2}{Hz} \tag{5.14}$$

$$v_{out\_total} = 11.2\frac{nV}{\sqrt{Hz}} \tag{5.15}$$

The noise measured at 100kHz (at room temperature) is $15\frac{nV}{\sqrt{Hz}}$, which is significantly more than what was calculated ($11.2\frac{nV}{\sqrt{Hz}}$). The discrepancy between the experimental result and the analysis can be explained in two ways. Due to parasitics at the summing node, we do not know exactly the impedance seen by the noise current source $\overline{i_{ein}^2}$. The

second reason is that we do not know the noise characteristic of the thick film 3.9 Gigaohm feedback resistor. This resistor can contribute excess noise due to its processing properties. Also, it is known that high value resistors tend to contain more impurities and material discontinuity, and thus are more noisy.

5.6 Noise Analysis of the Dual Source Follower

If stability is an issue, an alternative topology to consider is the dual source follower front end preamplifier. The source follower will offer the isolation between the input of the OP-27 and the high impedance summing node (the sensor's output node) without introducing any additional gain. Figure 5.9 shows the preamplifier with the dual source follower input stage and its noise sources when used in the desired gain configuration. The component values are listed the Table 5.3.

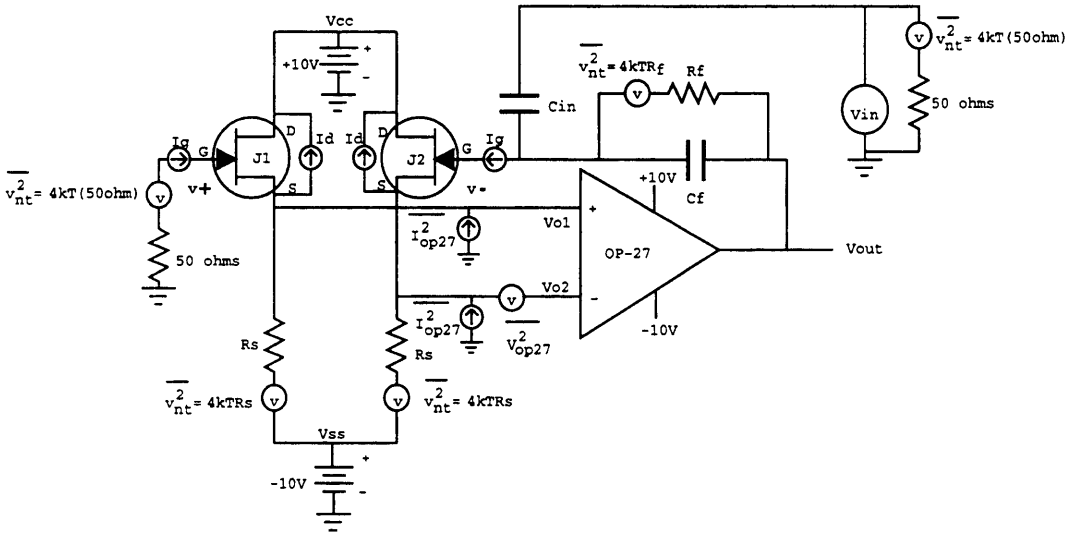

Figure 5.9: The Dual Source Follower Input Stage with Noise Sources

If we were just to consider the open-loop preamplifier (with Cs, Cf, and Rf removed from the circuit), the equivalent input voltage and noise current sources can be calculated.

Component	Part No. or Material	Ein	Iin
Monolithic Amplifier	OP-27 @1kHz	$3\frac{nV}{\sqrt{Hz}}$ max: $3.8\frac{nV}{\sqrt{Hz}}$	$0.4\frac{pA}{\sqrt{Hz}}$ max $0.6\frac{pA}{\sqrt{Hz}}$
J1, J2	U440 (matched JFETs)	$3\frac{nV}{\sqrt{Hz}}$	$0.1\frac{fA}{\sqrt{Hz}}$
Cs	1pF, Silvered Mica	extremely low	extremely low
Cf	2pF, Silvered Mica	extremely low	extremely low
Rf	3.9 Gohms, Thick Film	$8.04\frac{uV}{\sqrt{Hz}}$	$2.06\frac{fA}{\sqrt{Hz}}$
Rs	500 ohms, 1% Metal Film	$14.16\frac{nV}{\sqrt{Hz}}$	$1.17\frac{pA}{\sqrt{Hz}}$
R50	50 ohms, 1% Metal Film	$0.91\frac{nV}{\sqrt{Hz}}$	$9.1\frac{pA}{\sqrt{Hz}}$

Table 5.3: Parts Used in the Dual Source Follower

Figures 5.10a and 5.10b show the circuit models used to calculate the values for equivalent input noise voltage and noise current generators ($\overline{v_{ein}^2}$ and $\overline{i_{ein}^2}$) of the preamplifier:

$$\frac{1}{2}v_{ein}^2 = v_{ein\_u440}^2 + \frac{4kT}{R_s(g_m)^2} + \frac{I_{OP27}^2}{(g_m)^2} + \left(\frac{v_{OP27}}{\sqrt{2}}\right)^2 \tag{5.16}$$

$$\overline{i_{ein}^2} = 2qI_G + \frac{8kT}{3}g_m\left(\frac{wC_{gs}}{g_m}\right)^2 + \overline{I_{OP27}^2}\left(\frac{wC_{gs}}{g_m}\right)^2 + \left(\frac{v_{OP27}}{\sqrt{2}}\frac{3}{2}g_m\right)^2\left(\frac{wC_{gs}}{g_m}\right)^2 \tag{5.17}$$

Note that the equivalent input noise current generator of the dual source follower front end has the same terms as that of the differential pair front end preamplifier. However, the equivalent input noise voltage generator $\overline{v_{ein}^2}$ has a different expression for the noise contribution (fourth term of Equation 5.17). The noise voltage of the OP-27 comes directly to the $\overline{v_{ein}^2}$ source without any reduction.

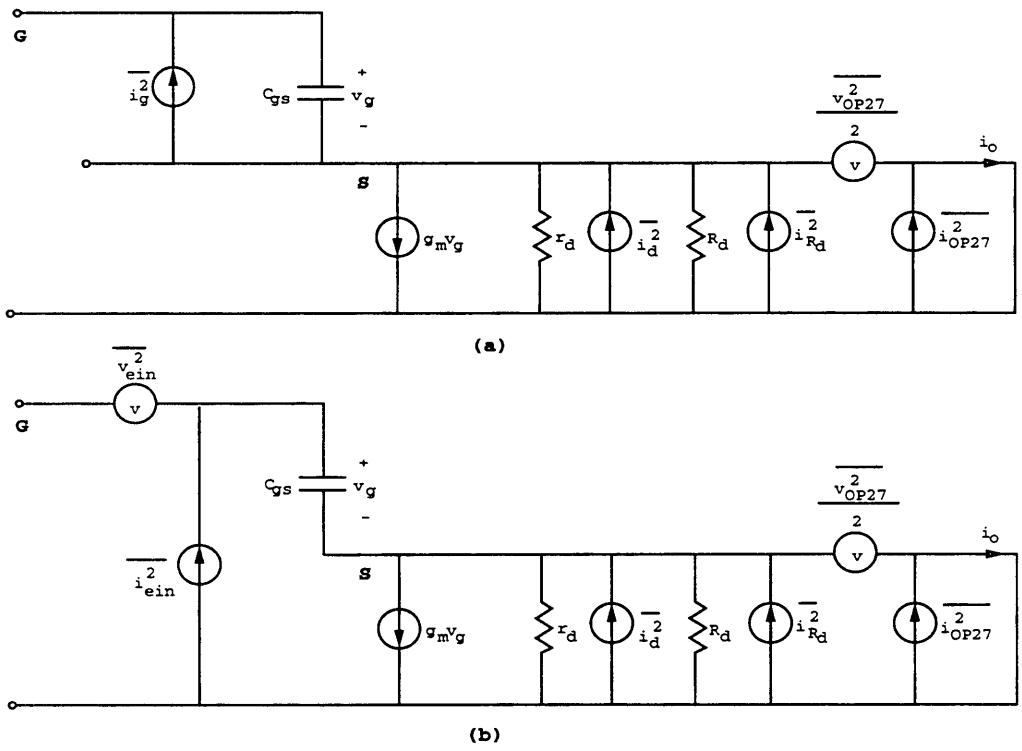

Figure 5.10: Noise Model of the Dual Source Follower Front End Preamplifier

Table 5.4 shows the variables and their values that will be used in analyzing equations 5.16 and 5.17.

Variable	Value	Variable	Value
R_s	12K ohms	I_G	1pA
g_m	4 mmhos	I_{OP27}	$0.4\frac{pA}{\sqrt{Hz}}$
$v_{ein\bar{n}u440}$	$3\frac{nV}{\sqrt{Hz}}$	v_{OP27}	$3\frac{nV}{\sqrt{Hz}}$

Table 5.4: Variables Used in the Noise Calculations for the Dual Source Follower

At room temperature (T=300K) and at 100kHz (or any other frequency where flicker is not a significant noise source), the values of v_{ein} and i_{ein} are

$$\frac{1}{2}\overline{v_{ein}^2} = (3\frac{nV}{\sqrt{Hz}})^2 + \frac{4kT}{(12K)(4\times10^{-3})^2} + (0.4\frac{pA}{\sqrt{Hz}}\frac{1}{4\times10^{-3}})^2 + (3\frac{nV}{\sqrt{Hz}}\frac{1}{\sqrt{2}})^2 \quad (5.18)$$

$$\frac{1}{2}\overline{v_{ein}^2} = 4.5\times10^{-18}\frac{V^2}{Hz} + 8.6\times10^{-20}\frac{V^2}{Hz} + 1.0\times10^{-20}\frac{V^2}{Hz} + 4.5\times10^{-18}\frac{V^2}{Hz} = 9.1\times10^{-18}\frac{V^2}{Hz} \quad (5.19)$$

$$v_{ein} = \sqrt{2}(3.02\frac{nV}{\sqrt{Hz}}) = 4.27\frac{nV}{\sqrt{Hz}} \quad (5.20)$$

As we expected the v_{ein} generator has a larger value than that of the differential pair. When configured in a unity-gain configuration, the noise measured at the output was $7.33\frac{nV}{\sqrt{Hz}}$. The unity-gain noise curve is shown on the next page (Figure 5.11). The calculated noise would be:

$$\overline{v_{out\_total}^2} = (4.27\frac{nV}{\sqrt{Hz}})^2 + (5.23\frac{nV}{Hz})^2 = 4.6\times10^{-17}\frac{V^2}{Hz} \quad (5.21)$$

$$v_{out\_total} = 6.75\frac{nV}{\sqrt{Hz}} \quad (5.22)$$

At 100kHz, and room temperature (300K),

$$\overline{i_{ein}^2} = 2q(1pA) + \frac{8kT}{3}(8.9\times10^{-10}) + (0.4\frac{pA}{\sqrt{Hz}})^2(2.22\times10^{-7}) + (3\frac{nV}{\sqrt{Hz}}\frac{1}{\sqrt{2}}\frac{3}{2})^2(2.22\times10^{-7}) \quad (5.23)$$

$$\overline{i_{ein}^2} = 3.2\times10^{-31}\frac{A^2}{Hz} + 9.8\times10^{-30}\frac{A^2}{Hz} + 3.6\times10^{-32}\frac{A^2}{Hz} + 3.6\times10^{-29}\frac{A^2}{Hz} = 4.6\times10^{-29}\frac{A^2}{Hz} \quad (5.24)$$

$$i_{ein} = 6.8\frac{fA}{\sqrt{Hz}} \quad (5.25)$$

When configured as shown in Figure 5.9 (where Cs, Cf, and Rf are included), the noise measured at 27kHz and 100kHz are

	27kHz	100kHz
v_{out_total}	$29\frac{nV}{\sqrt{Hz}}$	$19\frac{nV}{\sqrt{Hz}}$

Table 5.5: Noise of the Dual Source Follower at Room Temperature

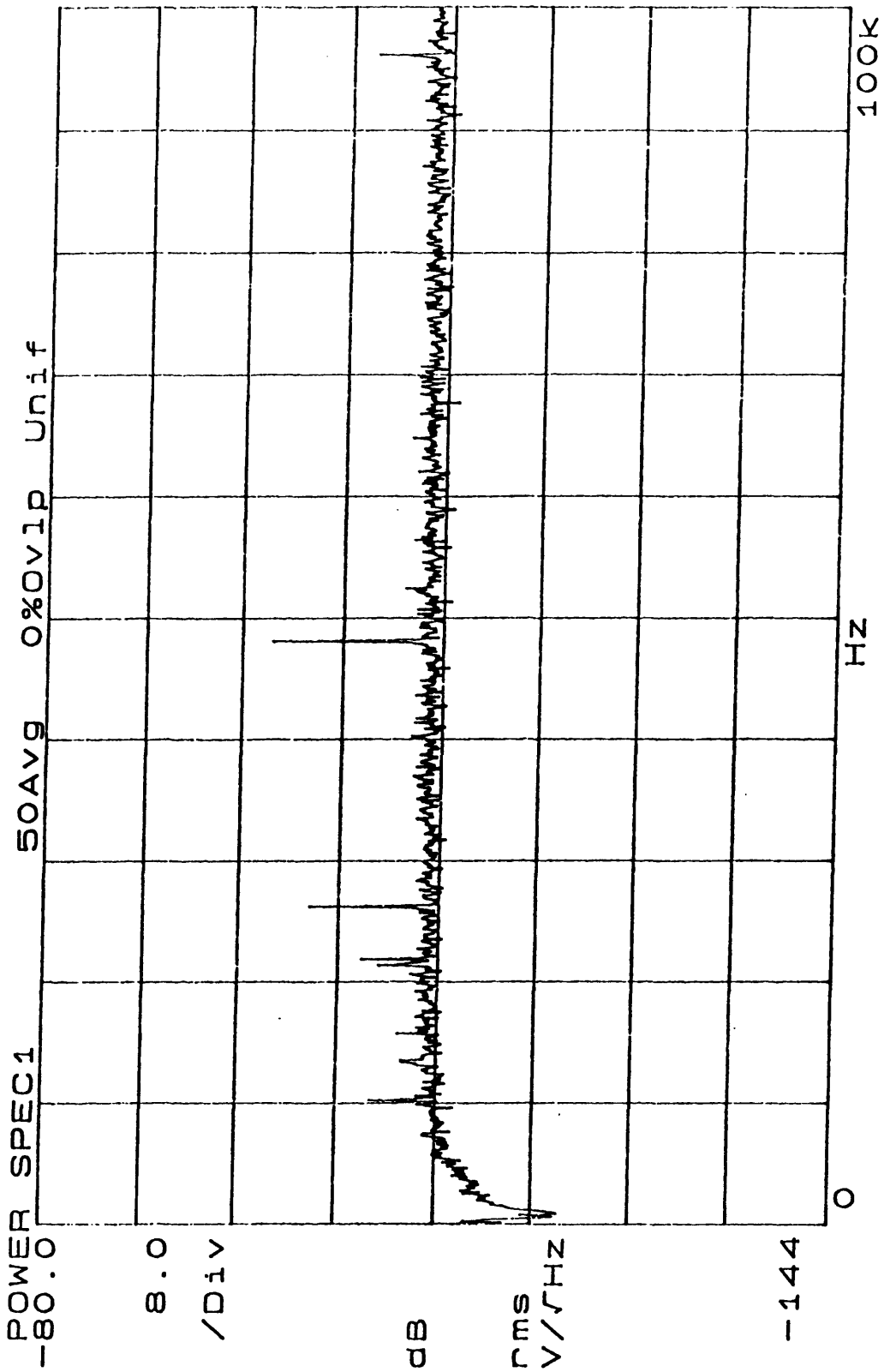

Figure 5.11: Output Noise of the Unity-Gain Dual Source Follower at Room Temp.

The new configuration (with a noise gain of 2.5) has a calculated noise of

$$\overline{v_{out\_total}^2} = \overline{v_{ein}^2}(2.5)^2 + \overline{i_{ein}^2}\left(\frac{1}{wC_f}\right)^2 + \frac{4kTR_f}{(1+wC_fR_f)^2} + \overline{v_{400x}^2} \tag{5.26}$$

$$v_{out\_total}^2 = 1.1\times10^{-16}\frac{V^2}{Hz} + 2.7\times10^{-17}\frac{V^2}{Hz} + 2.7\times10^{-18}\frac{V^2}{Hz} + 2.7\times10^{-17}\frac{V^2}{Hz} = 1.7\times10^{-16}\frac{V^2}{Hz} \tag{5.27}$$

$$v_{out\_total} = 13.1\frac{nV}{\sqrt{Hz}} \tag{5.28}$$

Again, the discrepancy between the calculated noise value and the measured output noise may be due to excess noise in the high value thick film resistor and parasitics at the summing node interacting with parasitic currents.

The output noise curve is shown on the next page in Figure 5.12.

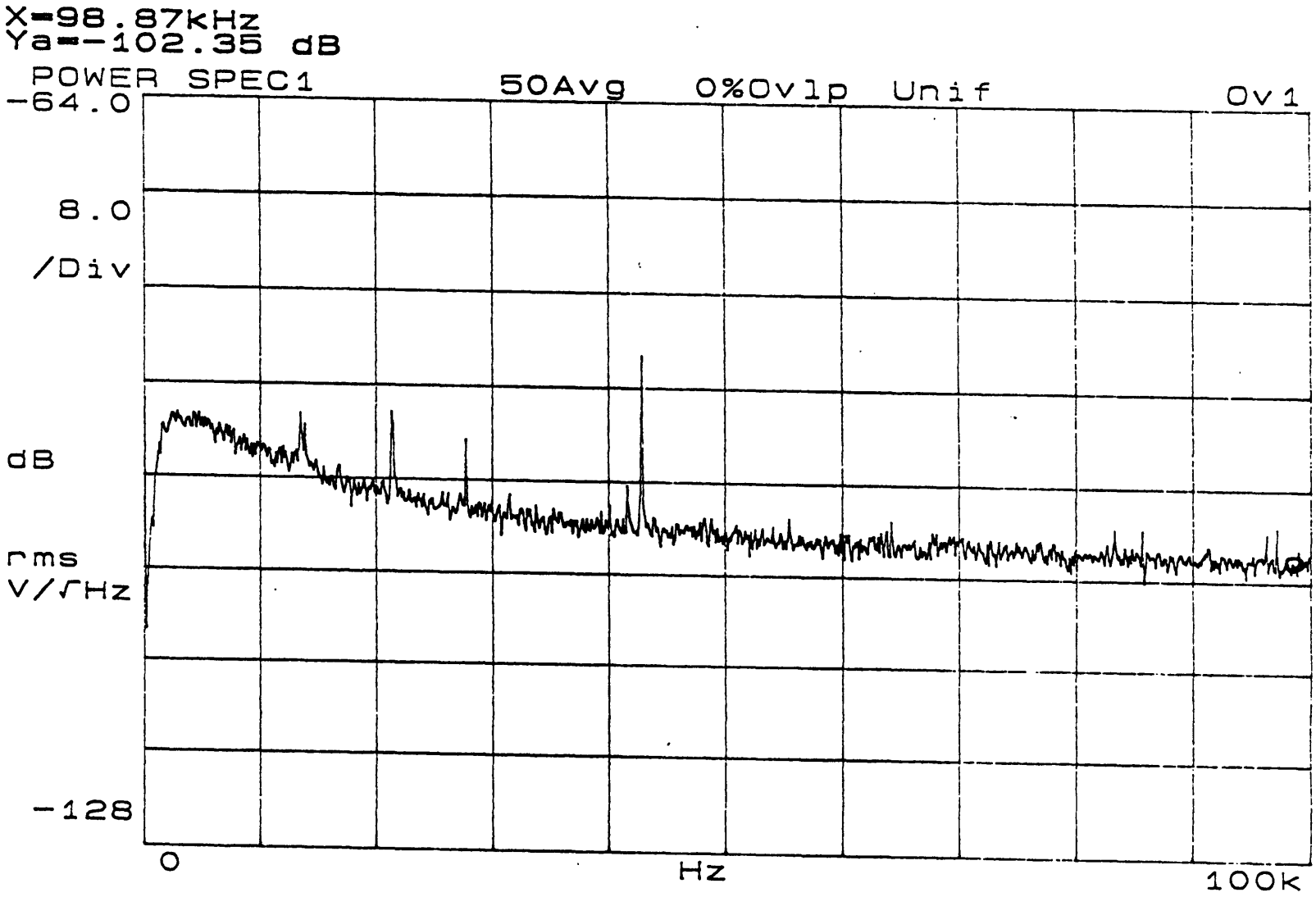

Figure 5.12: Output Noise of the Dual Source Follower in Half-Gain Configuration at Room Temperature

5.7 Circuit Performance Over the Specified Temperature Range

The circuit must perform over the temperature range of -40C to 85C. The operating gate current of the JFET is known to double with every 10 degrees increase in temperature. This increase in noise current can be a problem when we operate the preamplifier circuit at high temperatures. Besides the gate noise current, other shot and thermal noise sources also increase with increasing temperature.

The specified operating temperature range is -40C to 85C. The circuits were placed in dye-cask boxes blown with cold or hot air so that the ambient temperature inside the box settled to a desired temperature. Three temperature settings were chosen to measure the preamplifier's noise performance. The table below shows the circuit's performance at -40C, 28C, and 85C at 27kHz and 100kHz.

Topologies	-40C	28C	85C
@ 27kHz			
Differential Pair	$23.2 \frac{nV}{\sqrt{Hz}}$	$22.6 \frac{nV}{\sqrt{Hz}}$	$31.7 \frac{nV}{\sqrt{Hz}}$
Dual Source Follower	$23.17 \frac{nV}{\sqrt{Hz}}$	$29.44 \frac{nV}{\sqrt{Hz}}$	$41.83 \frac{nV}{\sqrt{Hz}}$
@ 100kHz			
Differential Pair	$16.8 \frac{nV}{\sqrt{Hz}}$	$16.7 \frac{nV}{\sqrt{Hz}}$	$21.8 \frac{nV}{\sqrt{Hz}}$
Dual Source Follower	$15.34 \frac{nV}{\sqrt{Hz}}$	$19.07 \frac{nV}{\sqrt{Hz}}$	$23.57 \frac{nV}{\sqrt{Hz}}$

Table 5.6: Output Noise of Preamplifiers at Various Temperatures

The source follower showed a reasonable trend of noise decrease with decreasing temperature. The differential pair showed little temperature dependence. A possible explanation for this behavior is that the noise of the differential pair is dominated by the noise of

the FETs, which are designed to have little performance variation over the specified temperature range.

5.8 Other Circuit Performance Tests

The other two tests performed on these amplifiers were the common-mode rejection ratio (CMRR) and the power supply rejection ratio (PSRR). As mentioned in Chapter 1, these two figures of merit are essential for rejecting other noise sources (mainly external and power supply noise). Fortunately these types of noise can be better controlled by other means. The PSRR can be improved by superior decoupling of the power supplies, and the common-mode signal can be reduced by proper shielding so the specification of the CMRR can be loosened.

The circuit below was used to measure the CMRR.

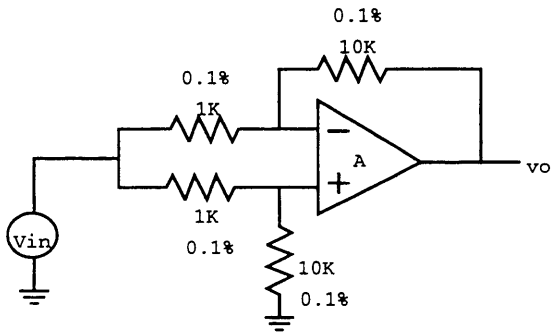

Figure 5.13: CMRR Test Circuit

If the preamplifier A in Figure 5.13 is ideal and the resistor values are exactly as specified, the output voltage is zero, exhibiting its ability to completely suppress the common-mode voltage V_{in}. Because the preamplifier is not ideal, and there is some small variation in the resistors, the output will not be zero. If there is any mismatch between the 1K-ohm resistors or the 10K-ohm resistors, the voltage values at the input terminals of the preamplifier would be unbalanced. Any difference at the preamplifier inverting and non-inverting ter-

minal will be amplified by a factor of 10. Precision resistors (0.1% accuracy) were used to minimize mismatch.

Besides the mismatching of the resistors, CMRR is also highly dependent on the mismatching of the JFET input pair. Therefore, it is extremely critical that the input devices are highly matched. The CMRR can be calculated with the following equation

$$CMRR = 20\log(10\frac{1}{vo}) \tag{5.29}$$

The multiplier 10 comes from the differential gain set by the resistor networks.

The $PSRR^+$ was measured using the circuit below [9].

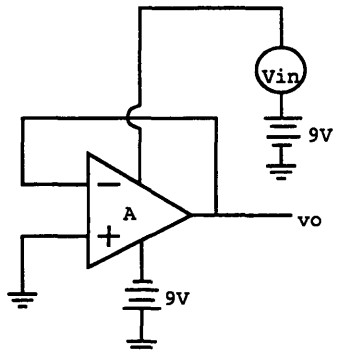

Figure 5.14: PSRR Test Circuit

The PSRR was calculated using the following equation:

$$PSRR = 20\log(\frac{1}{vo}) \tag{5.30}$$

where vo is the output. The smaller the vo is, the better the PSRR performance.

Typical CMRR and PSRR measurement curves are shown on the next page (Figure 5.15 and Figure 5.16, respectively).

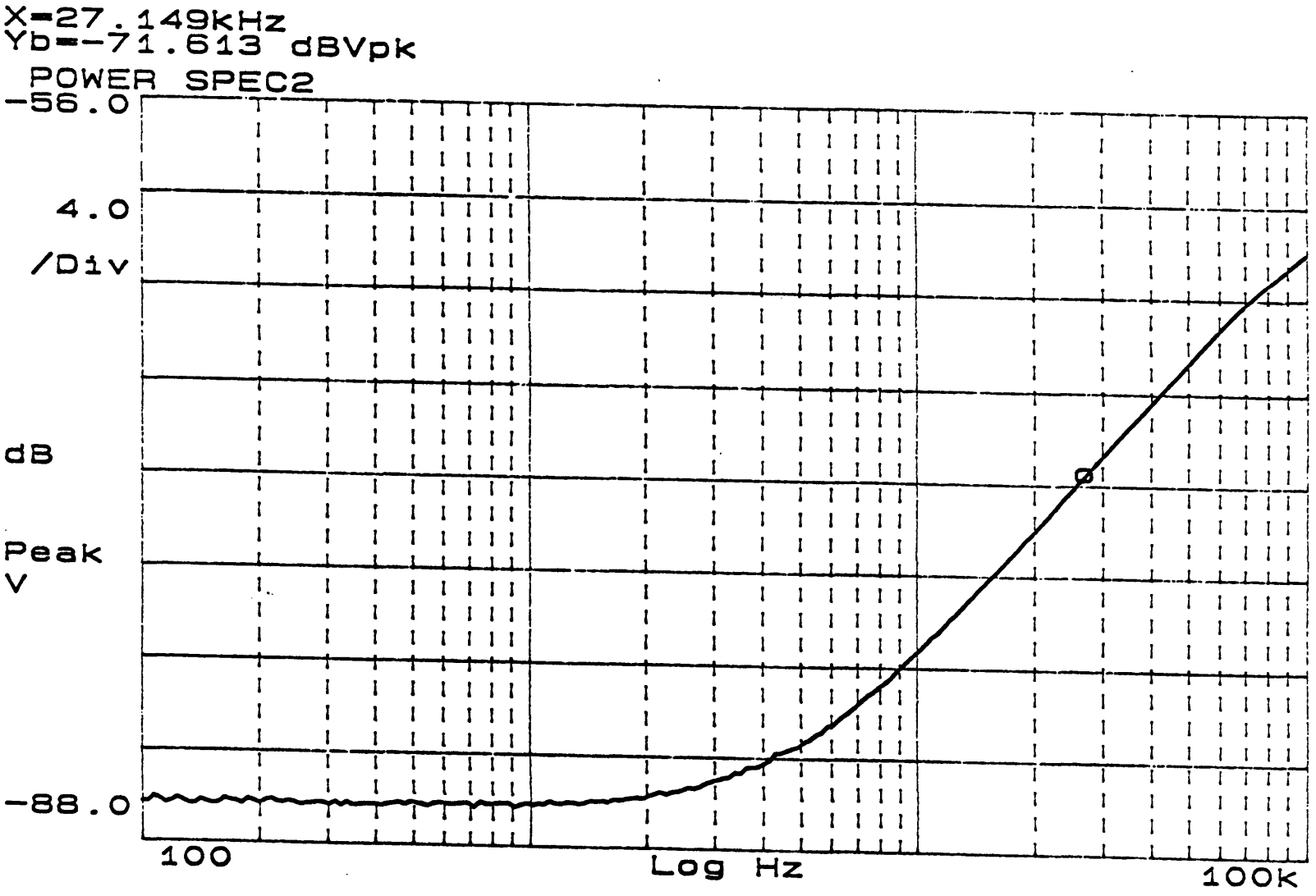

Figure 5.15: Common-mode Gain of the Dual Source Follower at Room Temperature

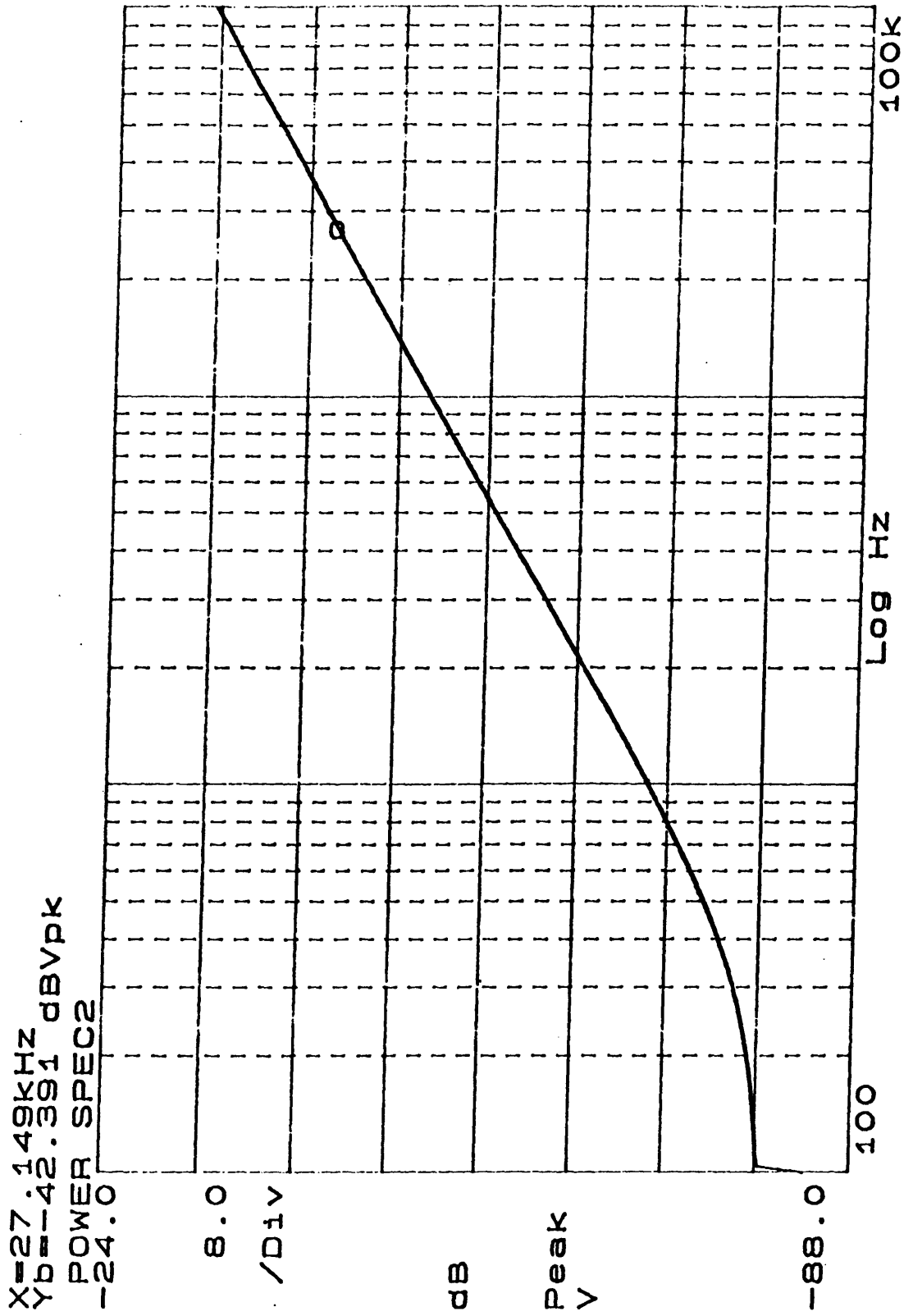

Figure 5.16: The PSRR+ of the Dual Source Follower at Room Temperature

Table 5.7 shows the CMRR and PSRR performances of the preamplifier with the differential pair input stage at 27kHz and 100kHz.

Specification	27kHz	100kHz
CMRR	53.84 dB	50.84 dB
PSRR+	85.86 dB	71.97 dB
PSRR-	46.35 dB	34.94 dB

Table 5.7: CMRR, PSRR+, and PSRR- of the Differential Pair

Table 5.8 shows the CMRR and PSRR performance of the dual source follower front end amplifier at 27kHz and at 100kHz.

Specification	27kHz	100kHz
CMRR	91.63 dB	82.00 dB
PSRR+	42.39 dB	31.63 db
PSRR-	50.72 dB	40.32 dB

Table 5.8: CMRR, PSRR+, and PSRR- of Dual Source Follower

These are acceptable CMRR and PSRR values for most FET amplifiers. The PSRR of the differential pair is better than that of the dual source follower because of the superior symmetry of the differential pair.

5.9 Conclusion

There are a few advantages and disadvantages in using either the source follower or the differential pair. Table 5.9 shows the strengths and weaknesses of the two topologies

In terms of noise performance, the differential pair is the better choice; however, it suffers the risk of instability. By cascading the differential pair to the op-amp, we introduce

additional gain into system, thus reducing the phase margin. If large gain is introduced into the system, instability will occur.

Differential Pair PROs	Differential Pair CONs	Dual Source Follower PROs	Dual Source Follower CONs
1. Insensitivity to Op-Amp noise	1. Sensitivity of gm to temperature	1. Insensitivity of gm to temperature	1. Sensitivity to Op-Amp noise
2. Good PSRR	2. Degraded phase margin	2. Good phase margin	2. Inferior PSRR
	3. Inferior CMRR	4. Closed loop characteristics independent of current	

Table 5.9: Pros and Cons of the Differential Pair and the Dual Source Follower

This stability issue make the differential input stage somewhat impractical for mass production because of the performance variations of the JFET parts. One JFET may have more transconductance than another, thus introducing gain variation from package to package, leading to possible failure for stability.

Because the dual source follower has unity voltage gain, the input noise of the OP-27 is referred to the input of the preamplifier with reduction from the source follower stage. Thus this topology can result in low-noise performance only if the OP-27 stage has a noise voltage lower than that of the JFETs. However, it offers more performance reliability with the performance variation of the discrete JFET transistors. Therefore the dual source follower is a less sensitive to device variations such as current and transconductance, and thus will increase the yield of the circuit production. Therefore the dual source follower is the better choice.

Chapter 6

The IC CMOS Preamplifier

6.1 Introduction

Though the amplifiers composed of commercial parts offer an excellent solution for low-noise amplifiers, variations in the input device performance as well as its bulkiness make this solution not suitable in the trend for miniaturization. The preamplifiers suggested in chapter 5 are also costly, requiring more construction time and expensive parts.

What is desired is an inexpensive integrated circuit solution that offers the small size and less variability in component performance and mismatch. This chapter describes the design steps of a low-noise IC preamplifier to be fabricated in a CMOS process. Spice simulations were used to evaluate the design.

6.2 Device Selection

The optimal situation is to find a JFET/Bipolar foundry that can deliver the quality JFETs comparable to what Siliconix offers with the U440. Of all the foundries with full-custom JFET capability, none could make JFETs of the quality needed to realize an amplifier superior to what is already commercially available. Though mass production of integrated circuits is cheaper than assembly of discrete parts, the start up cost of an integrated project can be extremely high, especially for high quality analog circuits. The high start up cost of JFET processes and the realization that we could not do better (with the JFET foundries) than what was commercially available led us to halt the pursuit for a full-custom JFET preamplifier.

When surveying for high quality JFET/Bipolar foundries, three specifications were critical: high transconductance versus input capacitance as well as low gate leakage cur-

rent. No foundry could come close enough to the low noise voltage, low input current, and low input capacitance of the U440.

In the end, we had to resort to exploring a solution in CMOS technology because of its low cost fabrication as well as accessibility. CMOS is the trend in IC design, thus it is in our interest to explore means of obtaining better noise performance in this technology.

6.3 The Differential Pair with Active vs. Resistive Load

A typical differential pair is shown below in Figure 6.1.

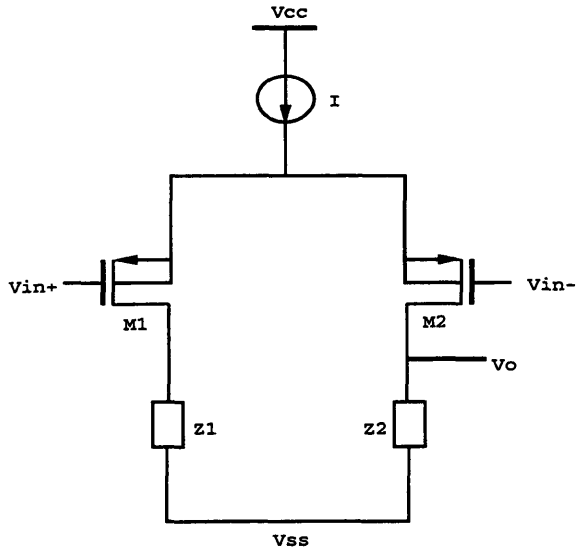

Figure 6.1: Typical Differential Pair

The loads can be a resistor, diode-connected transistor, or a transistor used as a current source. The following are the equivalent input noise voltage equations for a resistively loaded differential pair.

$$\overline{v_n^2} = \frac{8kT}{g_{m_2}} + \frac{K_f I_D}{fC_{ox}WL_{eff}g_m^2} + \frac{4kT}{Rg_m^2} \tag{6.1}$$

The first term is the channel's thermal noise, the second the channel's flicker noise, and the third the load resistor's thermal noise. Equation 6.2 is the input equivalent noise voltage equation of the actively loaded differential pair.

$$\overline{v_n^2} = \frac{8kT}{g_{m_2}} + \frac{K_f I_D}{fC_{ox}WL_{eff}} + \frac{8kT}{g_{m_4}g_{m_2}^2} + \frac{K_f I_D}{fC_{ox}WL_{eff}g_{m_2}^2} \tag{6.2}$$

Resistive loads are generally not chosen in IC design because practical resistor values require extremely large die areas. Resistors in integrated processes also have high variations in value (20% to 30% variation from the specified value). Such variation would make biasing of subsequent stages in the op-amp extremely unreliable. Diode-connected transistors also provide a small improvement in gain for reasonable die area. Its impedance is only $\frac{1}{g_m}$ and is chosen only in processes with single type devices (PMOS only or NMOS only). The current source transistor, also known as the active load, offers the best gain performance. However, the active load can contribute a significant amount of excess noise (mainly flicker noise). With careful design, the active load may offer adequate noise performance as well as excel in other circuit performance variables.

Lets look at the noise performance of a simple active load differential pair.

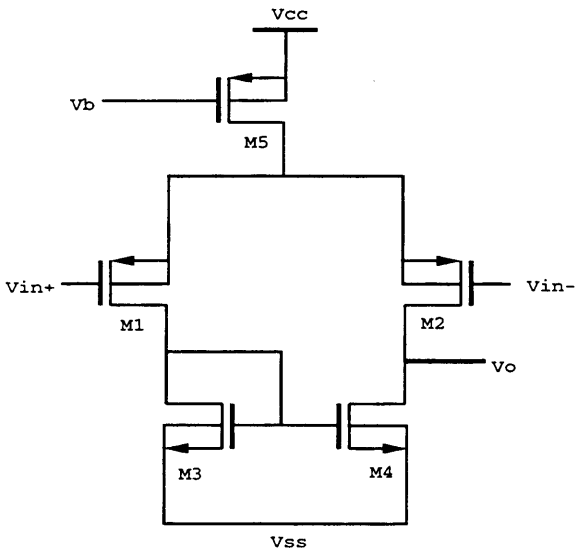

Figure 6.2: A Typical Differential Pair with Active Loads

Transistors M1 and M2 are assumed to be matched, so their operating points and circuit behaviors are equivalent. The same assumption applies to M3 and M4. Such balance

between the two sides of the differential pair allows us to cut the circuit in half and analyze using the half-circuit model.

The small-signal half-circuit is shown below in Figure 6.3

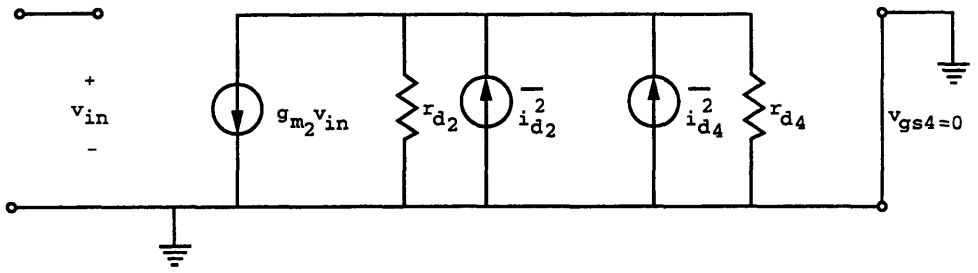

Figure 6.3: Small-Signal Equivalent Half Circuit of the Differential Pair

Ignoring the flicker noise, the thermal noise referred to the gate of the non-inverting input terminal is:

$$\overline{v_{ein}^2} = \frac{8kT}{3g_{m2}} + \frac{8kTg_{m4}}{3g_{m2}^2} = \frac{8kT}{3g_{m2}}\left(1 + \frac{g_{m4}}{g_{m2}}\right) \tag{6.3}$$

The input referred noise from each side of the differential pair consists of the noise from the input transistor plus the noise from the load transistor. Note how the equivalent input noise voltage can be reduced by operating the input transistor M2 (and also M1) to have a large transconductance (g_{m2}). The goal is to keep the transconductance of M2 as high as possible and the transconductance of M4 as low as possible. This can be accomplished by keeping the $(\frac{W}{L})_2 > (\frac{W}{L})_4$. Because the differential pair has two legs, the total noise voltage is $\sqrt{2}$ times more. This noise voltage is then referred back to the input.

6.4 Designing the Input Stage

A rule of thumb in designing low-noise circuits is to use simple topologies. There are generally two types of input stages used in making an operational amplifier. One popular

topology is the folded cascode. The other is the simple two-stage amplifier, which was discussed in the previous section (6.3). We will compare the two topologies to better understand how topologies influence noise performance.

There are some general rules to keep in mind when designing a low-noise input stage for an op-amp. First, the $\frac{W}{L}$ of the input device should be made large and most of the op-amp's gain should be achieved in the first stage. However, the gain of the first stage need not be extremely large compared to the gain of the second stage. If an output noise contribution of the second stage is 10% or less of the noise contribution from the first stage, the noise of the second stage can be neglected. High gain can be accomplished with a large transconductance or low-noise cascoding techniques.

Let's look at the folded cascode (see Figure 6.4). This topology is popular because it offers high gain and high frequency as well as an easy compensation scheme. In the two-stage op-amp, Miller capacitance compensation is usually used whereas the load capacitance is the compensating capacitance in the folded-cascode.

In the folded cascode, M3 and M4 now need to be much larger than the simple differential topology because M3 and M4 must also support the current from the cascoded paths. This requires M3 and M4 to have a larger $\frac{W}{L}$ ratio. Using equation 6.3, this condition makes the noise contributions from the load transistors much larger. For this reason, the folded cascode should be avoided unless high bandwidth is essential. However, cascoding the input stage will help if the gain improvement from the cascoding exceeds the increase in noise.

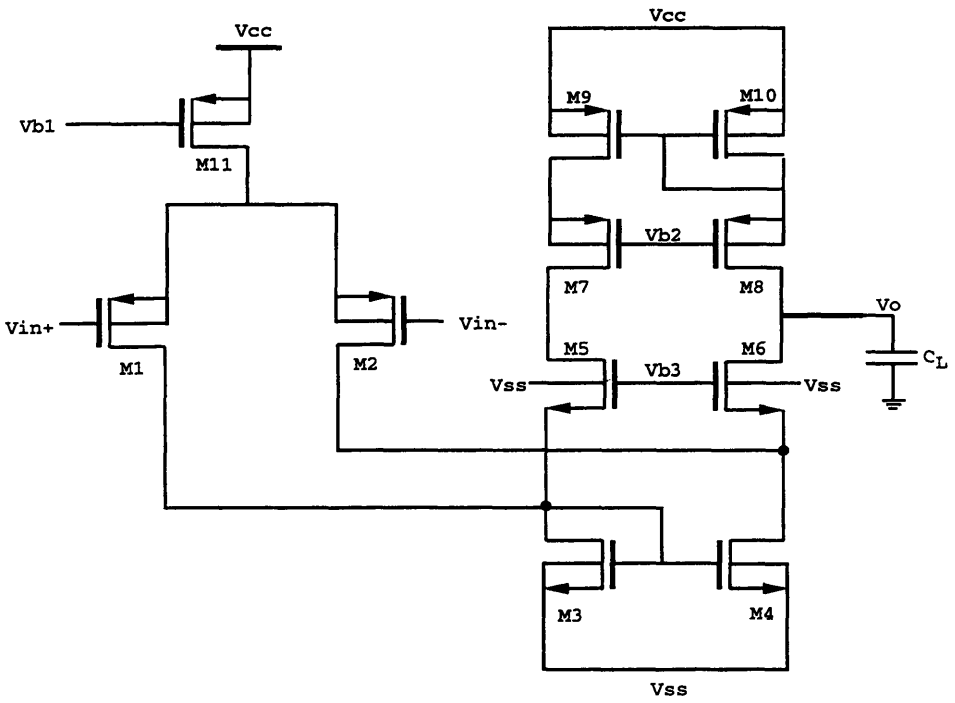

Figure 6.4: The Folded Cascode Amplifier for High Bandwidth Performance

6.5 A Low Noise Preamplifier Design

Figure 6.5 shows the schematic of a CMOS preamplifier circuit designed to be fabricated using the Orbit 1.2um process. The circuit consists of 3 stages. The first stage is a differential pair consisting of M1 through M6, with large P-channel input devices for low noise. M3 and M4 are used to improve the power supply rejection ratio by providing more DC gain to the first stage. Assume that M3 and M4 were not in the design. The output impedance of M6 (r_{o6}=150K ohms) is many times larger that the output impedance of M2, so the output impedance at node V7 is dominated by r_{o2}, which is about 12K ohms. By adding the p-channel devices M3 and M4 the output impedance r_{o2} of M2 is multiplied by $g_{m4}r_{o4}$. M3 and M4 increases the output impedance at node V7. M5 and M6 are the current mirror load. Their lengths are made long in order to minimize their transconductance and reduce the flicker noise. This load also provides the differential-ended to single-ended

conversion. The second stage is a class A gain stage. The gain is achieved by multiplying the transconductance of M10 with the output impedance of the stage at V10. Transistor M11 was used to give an output voltage at V10 that was closer to the middle of the rails. The last stage (M14 and M15) is a follower, or a level shifter. The output voltage of this stage was kept near MID. This stage also provides a low output impedance because of the source of M15. The inclusion of this stage will allow for a larger range of capacitive loading without degrading the phase margin (thus maintaining high stability).

Table 6.1 shows some performance figures obtained through Spice simulations.

v_{ein} thermal only (27kHz)	2.18 nV/rtHz
v_{ein} with Flicker (27kHz)	9.33 nV/rtHz
Unity Gain Frequency	45 Meg Hz
DC Gain	26.8 K (or 88.6dB)
Phase Margin	45 degrees
Power Dissipation	14.7 mW
CMRR	112 dB
PSRR+ at DC	86dB
PSRR+ at 27kHz	82dB
PSRR- at DC	94 dB
PSRR- at 27kHz	66 dB
Input Voltage Offset	2 μV
Slew Rate	55V/μs

Table 6.1: Performance of the IC CMOS Preamplifier

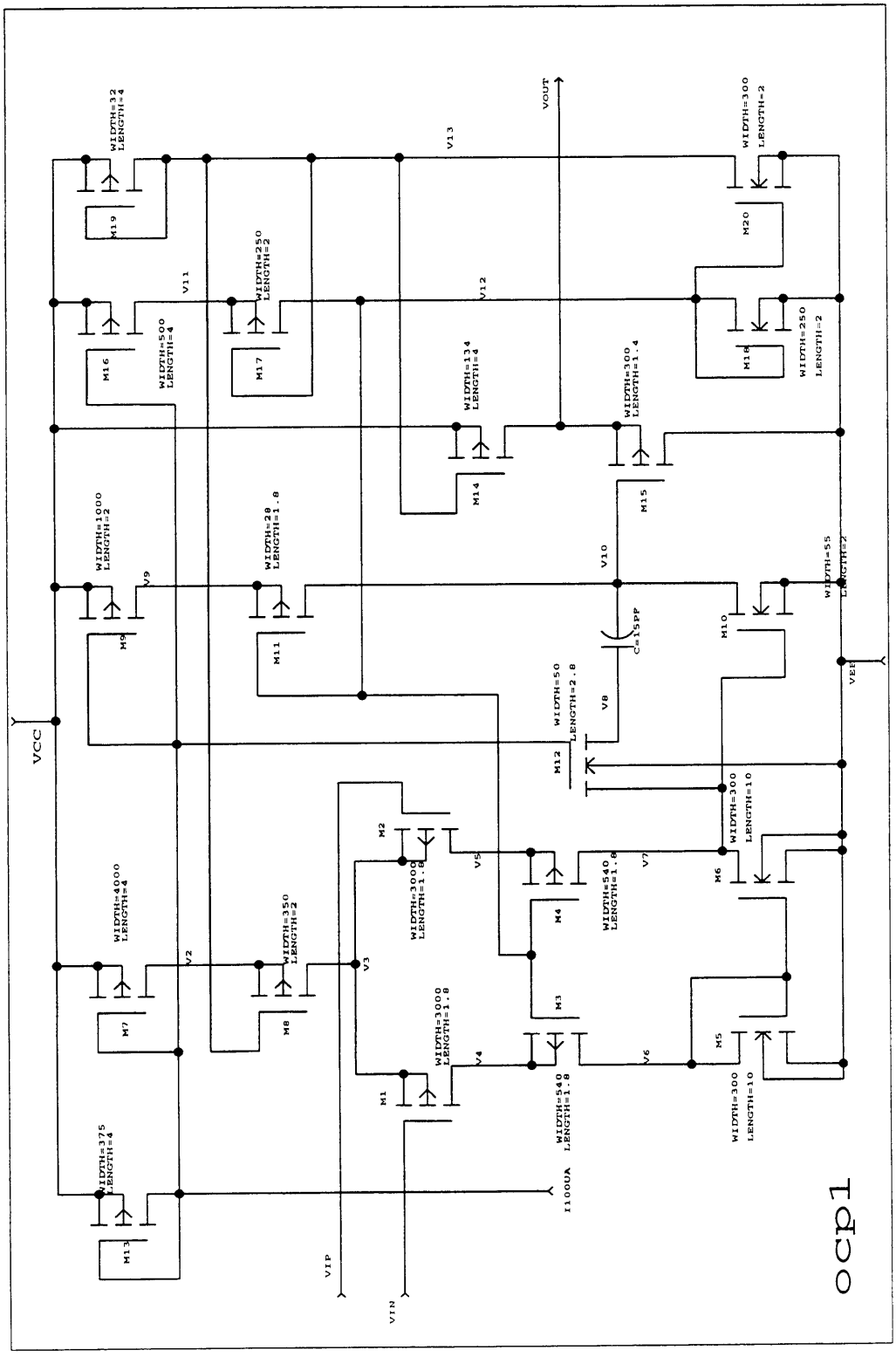

Figure 6.5: The IC CMOS Preamplifier Schematic

6.6 Noise Analysis

The Spice simulator was used to calculate the noise performance of this circuit. The flicker component could be added or removed by setting or omitting KF and AF in the transistor models. The rest of the noise was the result of thermal noise and noise coupled between the gate and drain (at high frequency). Spice uses the standard MOSFET noise equations below [10]:

$$I_{drain}^2 = 4kTg_m(\frac{2}{3}) + \frac{K_F I_{drain}^{AF}}{f(L_{eff})^2 C_{ox}} \tag{6.4}$$

where I_{drain} is the drain current, g_m the transconductance of the device, KF the flicker coefficient, and AF the flicker exponent. The exponential coefficient AF usually varies between 0.5 and 2, depending on the process used. The first noise term in Equation 6.4 is due to the thermal noise found in the resistive material of the channel, and the second component is the flicker noise.

The circuits below (Figures 6.6a and 6.6b) show the equivalent small-signal circuit of the preamplifier (one with internal noise sources and the other with equivalent input noise generators).

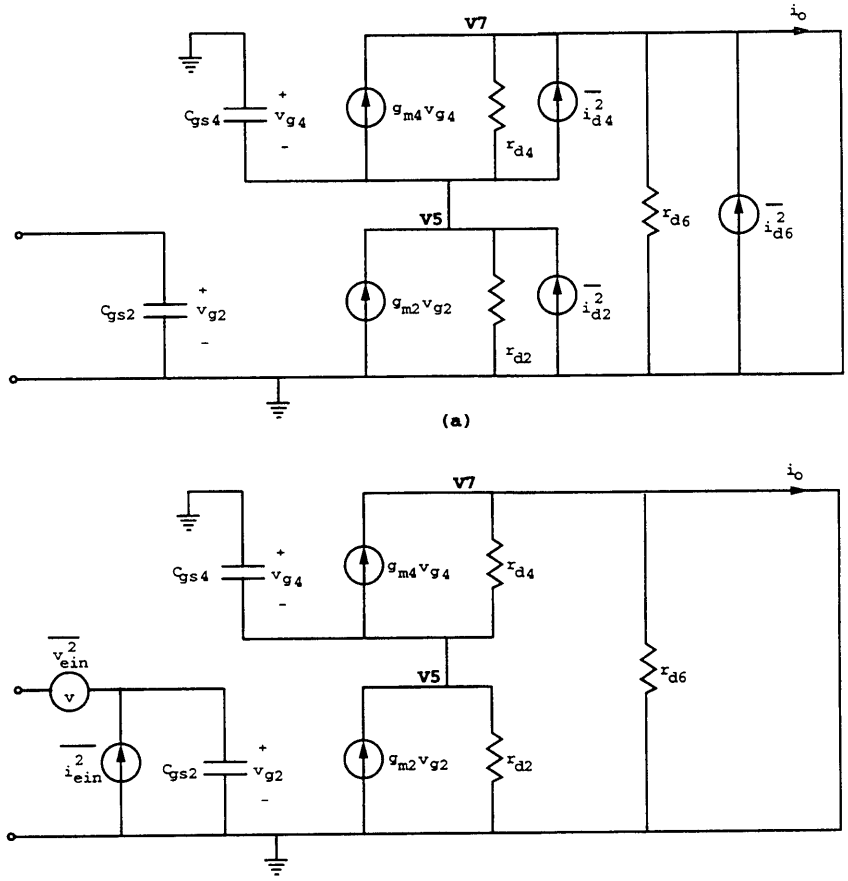

Figure 6.6: The IC CMOS Preamplifier's Noise Model

Using the transistor noise calculations technique described in Section 3.3, the equivalent input noise voltage $\overline{v_{ein}^2}$ and equivalent input noise current $\overline{i_{ein}^2}$ are

$$\frac{1}{2}\overline{v_{ein}^2} = \frac{\overline{i_{d2}^2}}{g_{m2}^2} + \frac{\overline{i_{d4}^2}}{g_{m2}^2}\left(\frac{1+sC_{gs4}r_{d4}}{(g_{m4}r_{d2}-1-r_{d2})-sC_{gs4}r_{d2}}\right)^2 + \frac{\overline{i_{d6}^2}}{g_{m2}^2} \tag{6.5}$$

$$i_{ein}^2 = i_{d2}^2\left(\frac{sC_{gs2}}{g_{m2}}\right)^2 + i_{d4}^2\left(\frac{1+sC_{gs4}r_{d4}}{(g_{m4}r_{d2}-1-r_{d2})-sC_{gs4}r_{d2}}\right)^2 + i_{d6}^2\left(\frac{sC_{gs2}}{g_{m2}}\right)^2 \tag{6.6}$$

where the noise current values are

$$\overline{i_{d2}^2} = \frac{8kT}{3}g_{m2} = \frac{8kT}{3}(5.71\times10^{-3}mho) = 63.0\times10^{-24}\frac{A^2}{Hz} \tag{6.7}$$

$$\overline{i_{d4}^2} = \frac{8kT}{3} g_{m4} = \frac{8kT}{3} (2.23\times10^{-3} mho) = 24.6\times10^{-24} \frac{A^2}{Hz} \tag{6.8}$$

$$\overline{d_{d6}^2} = \frac{8kT}{3} g_{m6} = \frac{8kT}{3} (1.26\times10^{-3} mho) = 13.9\times10^{-24} \frac{A^2}{Hz} \tag{6.9}$$

$$\left(\frac{1 + sC_{gs4} r_{d4}}{(g_{m4} r_{d2} - 1 - r_{d2}) - sC_{gs4} r_{d2}} \right)^2 \cong \left(\frac{1}{r_{d2}} \right)^2 = \left(\frac{1}{117 ohms} \right)^2 \tag{6.10}$$

Values in Equations 6.7 to 6.10 were calculated at room temperature and at 27kHz. Flicker noise is omitted for simplicity. The noise of M3 and M4 have a different gain than the noise of M1,M2 and M5,M6.

Hand calculations of the equivalent input noise were compared to the Spice calculation to verify the proper analysis of the circuit topology. Spice calculated an input referred thermal noise of $2.18 \frac{nV}{\sqrt{Hz}}$ and a combined thermal and flicker noise of $9.33 \frac{nV}{\sqrt{Hz}}$. At 27kHz, calculation of v_{ein} (shown in Equations 6.11) resulted in a value of $2.17 \frac{nV}{\sqrt{Hz}}$, which matches very closely the Spice calculation. The noise current i_{ein} is $49.1\times10^{-21} \frac{A}{\sqrt{Hz}}$, an insignificant noise source.

$$\frac{1}{2} \overline{v_{ein}^2} = 1.93\times10^{-18} \frac{V^2}{Hz} + 55.16\times10^{-24} \frac{V^2}{Hz} + 426.6\times10^{-21} \frac{V^2}{Hz} = 2.36\times10^{-18} \frac{V^2}{Hz} \tag{6.11}$$

$$v_{ein} = 2.17 \frac{nV}{\sqrt{Hz}} \tag{6.12}$$

$$\overline{i_{ein}^2} = 1.98\times10^{-39} \frac{A^2}{Hz} + 56.4\times10^{-45} \frac{A^2}{Hz} + 436.4\times10^{-42} \frac{A^2}{Hz} = 2.41\times10^{-39} \frac{A^2}{Hz} \tag{6.13}$$

$$i_{ein} = 49.1\times10^{-21} \frac{A}{\sqrt{Hz}} \tag{6.14}$$

Figure 6.7 shows the simulation result of the open-loop equivalent input thermal noise versus frequency.

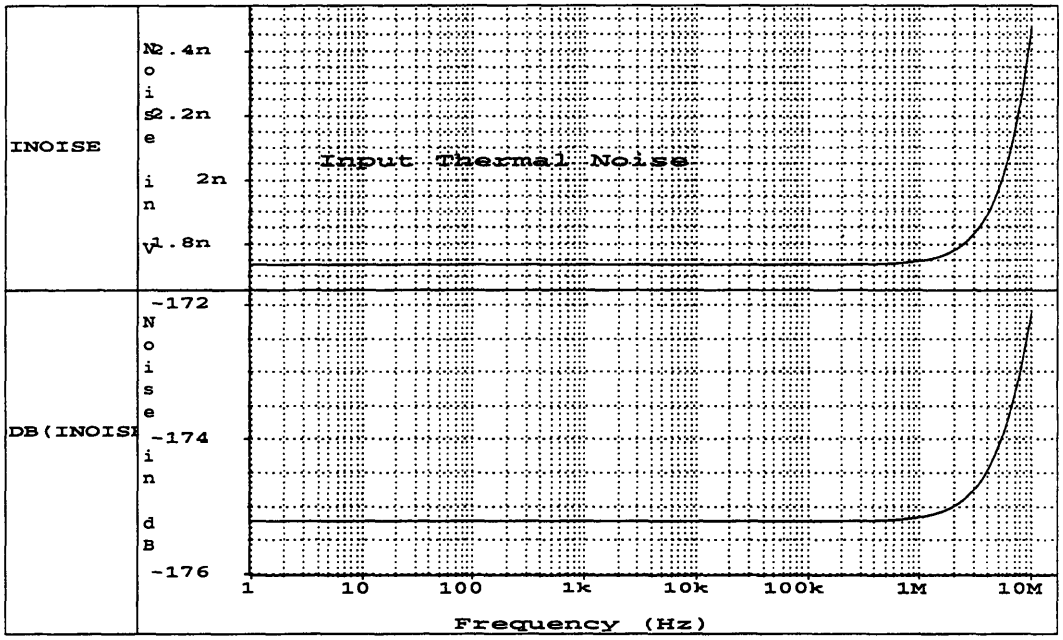

Figure 6.7: Equivalent Input Thermal Noise

Up until 1MegHz, v_{ein} has a flat spectral density. The increase of noise at high frequency is due to the coupling between the gate and the channel thermal noise through C_{gd}, as the capacitor's impedance decreases in addition to the decrease of the gain at high frequencies.

Figure 6.8 shows the input referred noise curve when the flicker component is included. As previously mentioned, the flicker noise dominates at low frequencies. The flicker dominates well into the 100's of kHz, so we have not cleared the flicker effect at the operating frequency of 27kHz.

In order to avoid flicker noise, the circuit should be operated beyond the flicker corner frequency, 100kHz. The lower frequency noise can be filtered out. Due to coupling through C_{gd} at high frequencies, this signal should not operate at too high a frequency. However, increasing the signal frequency to the MegaHz range is an unlikely option

because designing for such high frequency in CMOS is extremely challenging in meeting other specifications (such as keeping the phase integrity of the information signal).

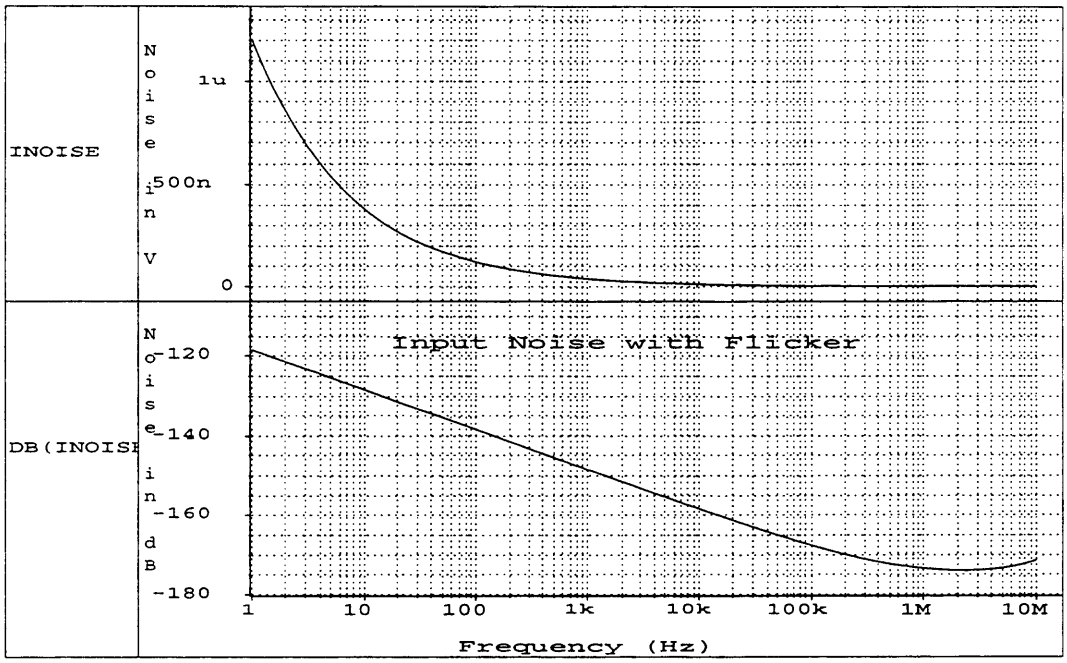

Figure 6.8: Equivalent Input Noise Including Flicker Noise

6.7 Gain and Phase Analysis

Figure 6.9 shows the small-signal equivalent circuit of the IC preamplifier. To simplify the low-frequency gain analysis, stray capacitances are neglected. The gain of the first stage is provided by the transconductance of the input device and the output impedance seen at node V7. The gain of the second stage is the product of the transconductance of M10 and the output impedance seen at node V10.

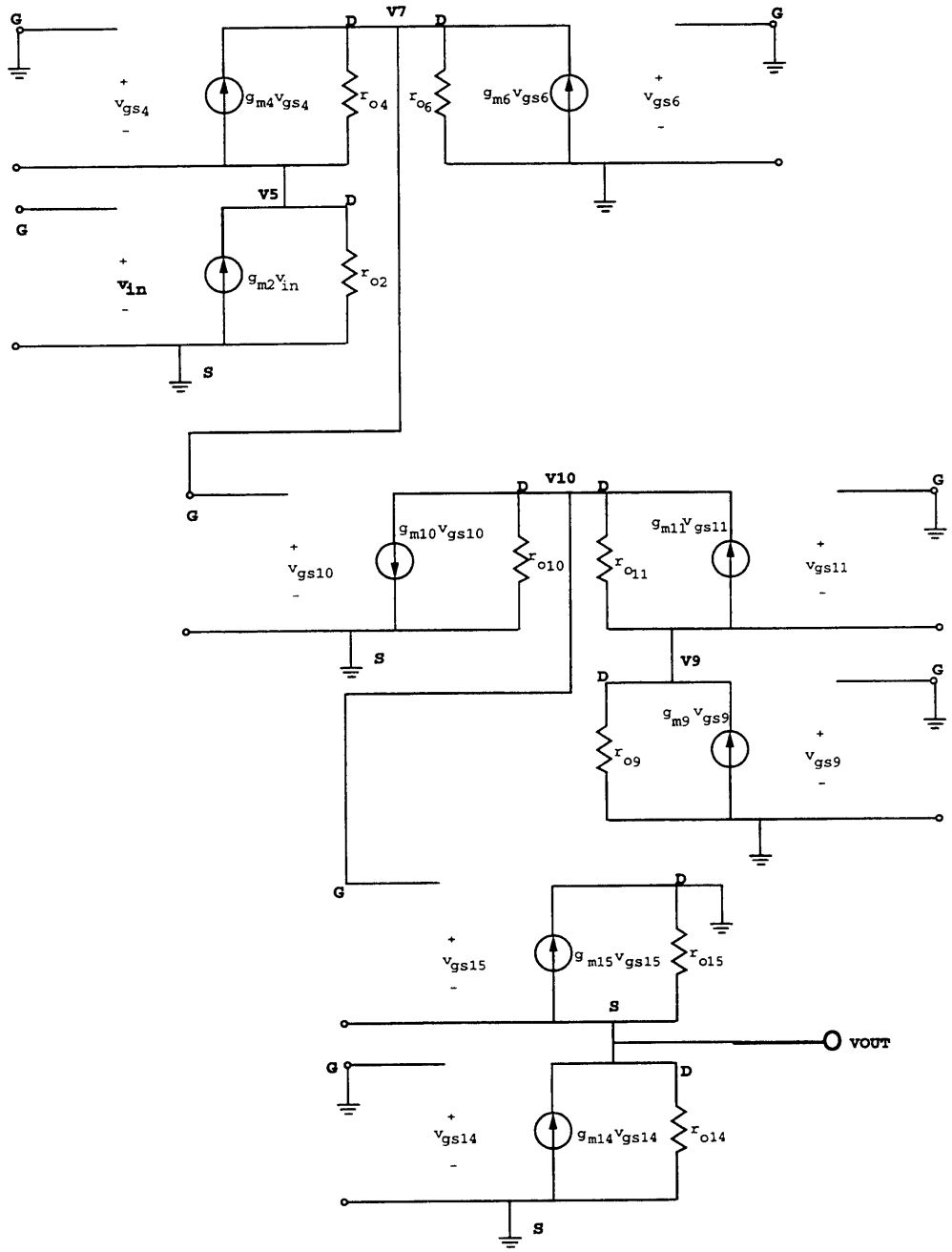

Figure 6.9: IC CMOS Preamplifier's Small-Signal Equivalent Circuit

The low-frequency gain of the circuit is

$$A_o = g_{m2}[(r_{o2} + r_{o4} + g_{m4}r_{o2}r_{o4}) \| r_{o6}]\, g_{m10}[(r_{o9} + r_{o11} + g_{m11}r_{o11}r_{o9}) \| r_{o10}] \tag{6.15}$$

We can simplify the circuit by modeling it as two stages with the following transconductance and output impedance:

$$G_{m1} = g_{m2} = 5.71\times10^{-3} mho \tag{6.16}$$

$$R_{o1} = (r_{o2} + r_{o4} + g_{m4} r_{o2} r_{o4}) \parallel r_{o6} = 148 Kohms \tag{6.17}$$

$$G_{m2} = g_{m10} = 1.43\times10^{-3} mho \tag{6.18}$$

$$R_{o2} = (r_{o9} + r_{o11} + g_{m11} r_{o11} r_{o9}) \parallel r_{o10} = 28.7 Kohms \tag{6.19}$$

$$G_{m3} = g_{m15} = 2.55\times10^{-3} mho \tag{6.20}$$

$$R_{o3} = \frac{1}{g_{m14} + g_{m15}} = 294 ohms \tag{6.21}$$

$$A_o = G_{m1} R_{o1} G_{m2} R_{o2} G_{m3} R_{o3} = 26,000 \tag{6.22}$$

The fact that the circuit is not perfectly symmetrical, due to the current mirror load transistors M5 and M6, makes the frequency response analysis (which accounts for parasitic capacitive) rather difficult. However, an approximation can be made. One way of obtaining the frequency response of the preamplifier is to use the circuit model shown below (Figure 6.10). Each stage is defined by a transconductance G_m and an output impedance R_o. For example, Gm1 is the transconductance of the first stage, R_{o1} is the output of the resistance seen at the output of the first stage, C_1 is the capacitance value seen at the output of the first stage. The parasitic capacitance seen at the output node will provide the poles that will degrade the frequency performance.

The frequency response of the preamplifier circuit in Figure 6.10 can be modeled as

$$A(f) = \frac{A_o}{(1 - \frac{s}{s_{p1}})(1 - \frac{s}{s_{p2}})(1 - \frac{s}{s_{p3}})} \tag{6.23}$$

$$s_{p1} = \frac{1}{R_{o1} C_1} = 3.69\times10^{6} \frac{rad}{s} \tag{6.24}$$

$$s_{p2} = \frac{1}{R_{o2} C_2} = 44.7\times10^{6} \frac{rad}{s} \tag{6.25}$$

$$s_{p3} = \frac{1}{R_{o3}C_3} = 2.42\times10^9 \frac{rad}{s} \tag{6.26}$$

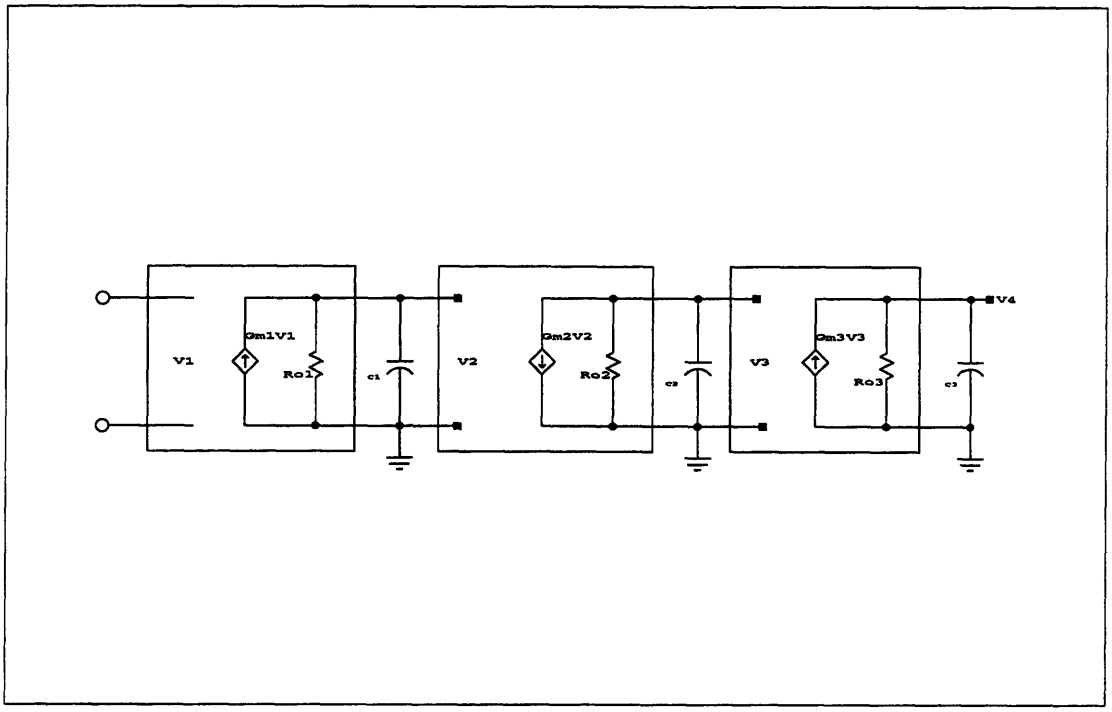

Figure 6.10: Op-Amp's Model of Frequency Response

The R_o's and G_m's are defined in Equation 6.14 to 6.19. The capacitances seen at the outputs of the three stages are

$$C_1 = C_{gd4} + C_{db4} + C_{db6} + C_{gd6} + C_{gs10} \cong 1.83pF \tag{6.27}$$

$$C_2 = C_{gd11} + C_{db10} + C_{db11} + C_{gs15} \cong 0.94pF \tag{6.28}$$

$$C_3 = C_{gd14} + C_{db14} + C_{sb15} + C_{gs15} \cong 1.41pF \tag{6.29}$$

Equations 6.21 through 6.23 predict the first three poles at 590kHz, 7.11MegHz, and 384MegHz, which correspond to the Spice calculation, shown in Figure 6.11

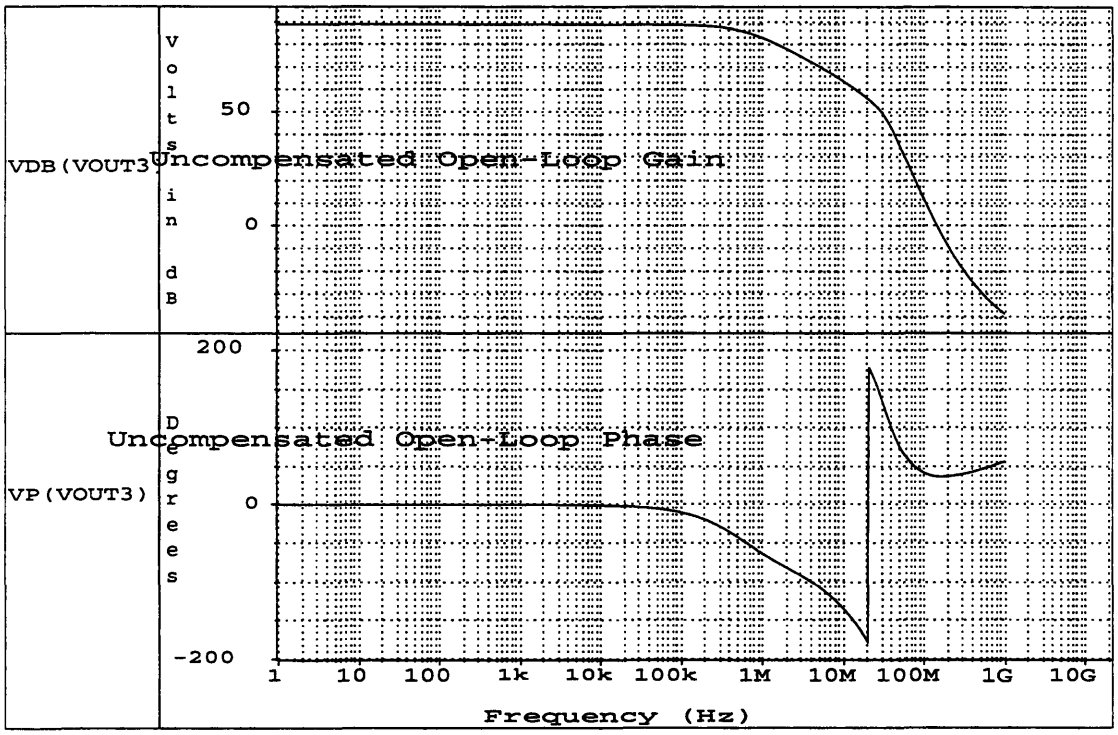

Figure 6.11: Uncompensated Open-Loop Frequency Response of the IC Preamplifier

This approximation gives a fairly accurate piciture of the circuit's frequency performance. The validation of this approximation as well as the insight of the circuit's frequency response can be obtained from analyzing the circuit using the open-circuit time constant technique. This method is described in [11].

The open-circuit time constant technique requires designers to understand how each component's capacitance contributes to the degradation of the circuit's frequency response. The impedance as seen by each capacitance is calculated to find a time constant for that capacitor/resistor combination. This technique gives an approximation of the -3dB frequency. The circuit in Figure 6.12 shows the locations of all the capacitors and where the impedances are being seen from. For example, R_{10} is the equivalent resistance seen

through the terminals of capacitor C_{gs2}. The time constants associated with C_{gs2} is $\tau_{10}=R_{10}C_{gs2}$.

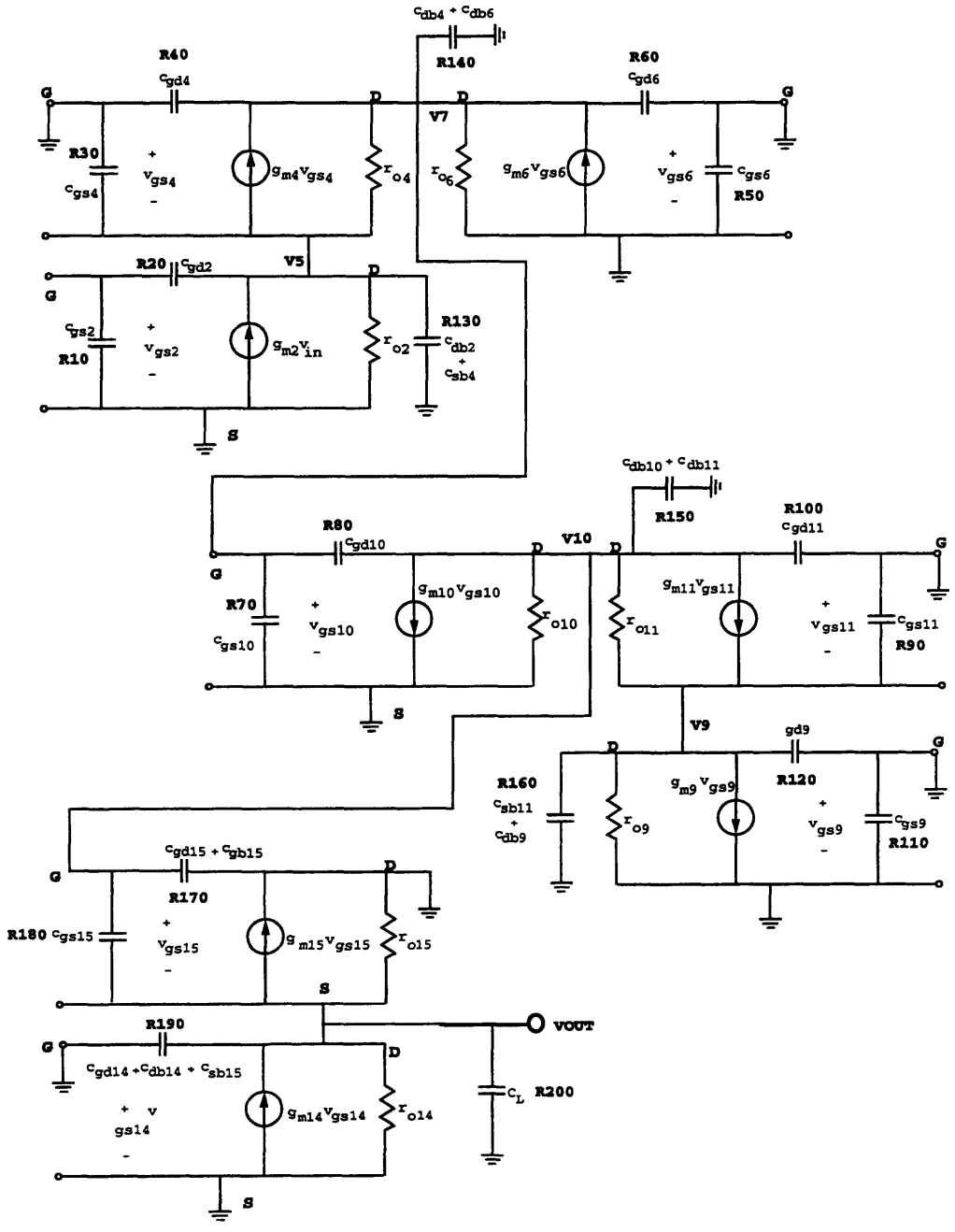

Figure 6.12: Open-Circuit Time Constants Technique

The following sections show the calculated impedance seen between the terminals of each capacitor followed by a table showing the time constants calculated.

$$R_{10} = 0 \tag{6.30}$$

$$R_{20} = r_{o2} \| \ (r_{o4} + r_{o6}) \ = 11.8 Kohms \tag{6.31}$$

$$R_{30} = r_{o2} \| \ \frac{r_{o4} + r_{o6}}{1 + g_{m4} r_{o4}} \ = 5.26 Kohms \tag{6.32}$$

$$R_{40} = (r_{o2} + r_{04}) \| \ r_{o6} \ = 22.6 Kohms \tag{6.33}$$

$$R_{50} = 0 \tag{6.34}$$

$$R_{60} = (r_{o2} + r_{04}) \| \ r_{o6} \ = 22.6 Kohms \tag{6.35}$$

$$R_{70} = (r_{o2} + r_{o4} + g_{m4} r_{o2} r_{o4}) \| \ r_{o6} \ = 148 Kohms \tag{6.36}$$

$$R_{80} = [r_{o2} + r_{o4} + g_{m4} r_{o4} r_{o2}] \| \ [r_{o10} \| \ (r_{o9} + r_{o11} + g_{m11} r_{o11} r_{o9})] \ = 20.5 Kohms \tag{6.37}$$

$$R_{90} = r_{o9} \| \left(\frac{r_{o10} + r_{o11}}{1 + gm11 r_{o11}} \right) = 2.83 Kohms \tag{6.38}$$

$$R_{100} = r_{o10} \| \ (r_{o9} + r_{o11} + g_{m11} r_{o11} r_{o9}) \ = 28.8 Kohms \tag{6.39}$$

$$R_{110} = 0 \tag{6.40}$$

$$R_{120} = r_{09} \| \left(\frac{r_{o10} + r_{o11}}{1 + g_{m11} r_{o11}} \right) = 2.83 Kohms \tag{6.41}$$

$$R_{130} = r_{o2} \| \left(\frac{r_{o4} + r_{o6}}{1 + g_{m4} r_{o4}} \right) = 5.26 Kohms \tag{6.42}$$

$$R_{140} = r_{o6} \| \ (r_{o2} + r_{o4} + g_{m4} r_{o4} r_{o2}) \ = 148 Kohms \tag{6.43}$$

$$R_{150} = r_{o10} \| \ (r_{o9} + r_{o11} + g_{m11} r_{o11} r_{o9}) \ = 28.8 Kohms \tag{6.44}$$

$$R_{160} = r_{o9} \| \left(\frac{r_{o11} + r_{o10}}{1 + g_{m11} r_{o11}} \right) = 2.84 Kohms \tag{6.45}$$

$$R_{170} = [r_{o10} \| \ (r_{o9} + r_{o11} + g_{m11} r_{o11} r_{o9})] \| \ [r_{o14} + r_{o15} + g_{m15} r_{o15} r_{o14}] \ = 23.45 Kohms \tag{6.46}$$

$$R_{180} = [r_{o10} \| \ (r_{o9} + r_{o11} + g_{m11} r_{o11} r_{o9})] \| \ (r_{o14} \| \ r_{o15}) \ = 10.09 Kohms \tag{6.47}$$

$$R_{190} = r_{o14} \| \ r_{o15} \ = 10.57 Kohms \tag{6.48}$$

$$R_{200} = r_{o14} \| \ r_{o15} \ = 10.57 Kohms \tag{6.49}$$

Impedance	Capacitor	Time Constant
R_{10}=0	C_{gs2}=5.09pF	τ_{10}=0
R_{20}=11.8K	C_{gd2}=0.837fF	τ_{20}=0.0099ns
R_{30}=5.3K	C_{gs4}=0.915pF	τ_{30}=4.85ns
R_{40}=22.6K	C_{gd4}=0.19fF	τ_{40}=0.0043ns
R_{50}=0	C_{gs6}=2.94pF	τ_{50}=0
R_{60}=22.6K	C_{dg6}=0.158fF	τ_{60}=0.0036ns
R_{70}=148K	C_{gs10}=89.0fF	τ_{70}=13.17ns
R_{80}=148K	C_{gd10}=.02fF* ($G_{m2}R_{o2}$)	τ_{80}=0.1211ns
R_{90}=2.83K	C_{gs11}=46.1fF	τ_{90}=0.130ns
R_{100}=28.8K	C_{gd11}=.008fF	τ_{100}=0.0002ns
R_{110}=0	C_{gs9}=1.90pF	τ_{110}=0
R_{120}=2.83K	C_{gd9}=0.31fF	τ_{120}=0.0009ns
R_{130} =5.26K	C_{db2} + C_{bs4}=7.21pF	τ_{130}=37.93ns
R_{140}=148K	C_{db4} + C_{db6}=1.74pF	τ_{140}=257.58ns
R_{150}=28.8K	C_{db10} + C_{db11}=0.550pF	τ_{150}=15.844ns
R_{160}=2.84K	C_{sb9}=2.71pF	τ_{160}=7.708ns
R_{170}=23.45K	C_{gd15}+C_{gb15} = 0.5fF	τ_{170}=0.012ns
R_{180}=10.09K	C_{gs15} = 0.385pF	τ_{180}=3.885ns
R_{190}=10.57K	C_{gd14} + C_{db14} + C_{sb15} = 1.03pF	τ_{190}=10.89ns
R_{200}=10.57K	C_L = 5pF	τ_{200}=52.85ns

Table 6.2: Open Circuit Time Constants

The approximated -3dB bandwidth is the reciprocal of the sum of all the time constants.

$$w_{3dB} \leq \frac{1}{\sum_{i=10}^{160} \tau_i} \tag{6.50}$$

The first pole is approximated to be 400KHz (where the gain is approximately 85dB), which is in agreement with the Spice results shown in Figure 6.11. This is the approximate location of the -3dB drop from the DC gain.

By inspecting the time constants in Table 6.2, we can see that most of the ω_{3dB} time constants come from capacitors seen at the output impedance of the first and second stages. This verifies our approximation of the circuit's frequency response represented by equation 6.21.

6.8 Compensation

The circuit has a very high unity-gain frequency, however its phase shift is far beyond the 180 degree stability limit (see Figure 6.11). To achieve acceptable phase margin, an extra Miller capacitance was used with a right-plane zero cancellation technique (R_c and C_c in Figure 6.13).

The frequency response of the circuit can be approximated as a third order system by the equation:

$$A_v(s) = \frac{A_o(1-\frac{s}{s_z})}{(1-\frac{s}{s_{p1}})(1-\frac{s}{s_{p2}})(1-\frac{s}{s_{p3}})} \tag{6.51}$$

where Ao is the low-frequency gain calculated in equation 6.13.

The equations below are the poles and zero in equation 6.45.

$$p_1 = -\frac{1}{R_{o1}(C_1 + C_c + G_{m2}R_{o2}C_c)} = 10.68\times10^3\frac{rad}{s} \tag{6.52}$$

$$p_2 = \frac{G_{m2}C_c}{C_1C_2 + C_c(C_1 + C_2)} = 495.7\times10^6\frac{rad}{s} \tag{6.53}$$

$$z = \frac{1}{C_c(\frac{1}{G_{m2}} - R_c)} = 190.1\times10^6\frac{rad}{s} \tag{6.54}$$

$$p_3 = \frac{1}{R_cC_1} = 520\times10^6\frac{rad}{s} \tag{6.55}$$

The first three poles in the compensated preamplifier are at 1.7kHz, 78.9MegHz, and 82.8MegHz. The zero is at 30.3MegHz.

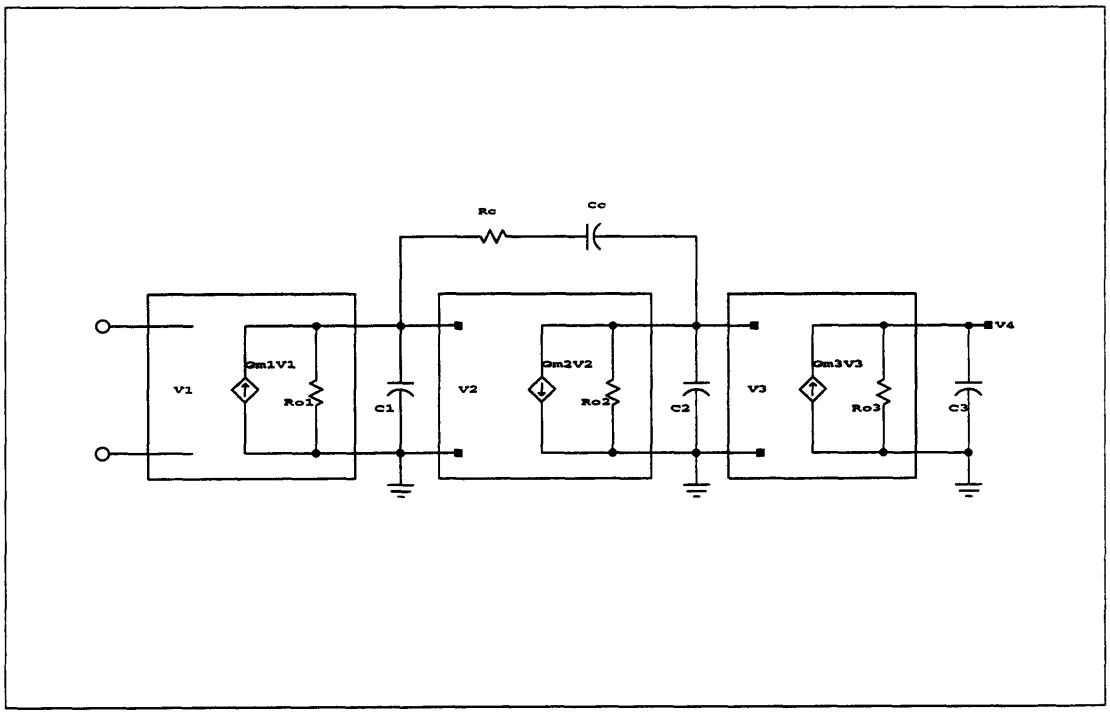

Figure 6.13: Model of Compensated Preamplifier

To prevent the zero from being in the right hand plane, Rc (which is approximaltely 1.05K Ω) must be kept larger than $\frac{1}{G_{m2}}$. Also instead of a resistor, a transistor (M12) operating in the triode region is used. Its output transconductance g_{ds} provides the necessary resistance. This option is superior to using a resistor since IC resistors have a large varia-

tion in their manufactured values (from the specified value). Using this transistor also allows the resistance to track the transconductance of M6.

Figure 6.14 shows the open-loop frequency response of the compensated preamplifier.

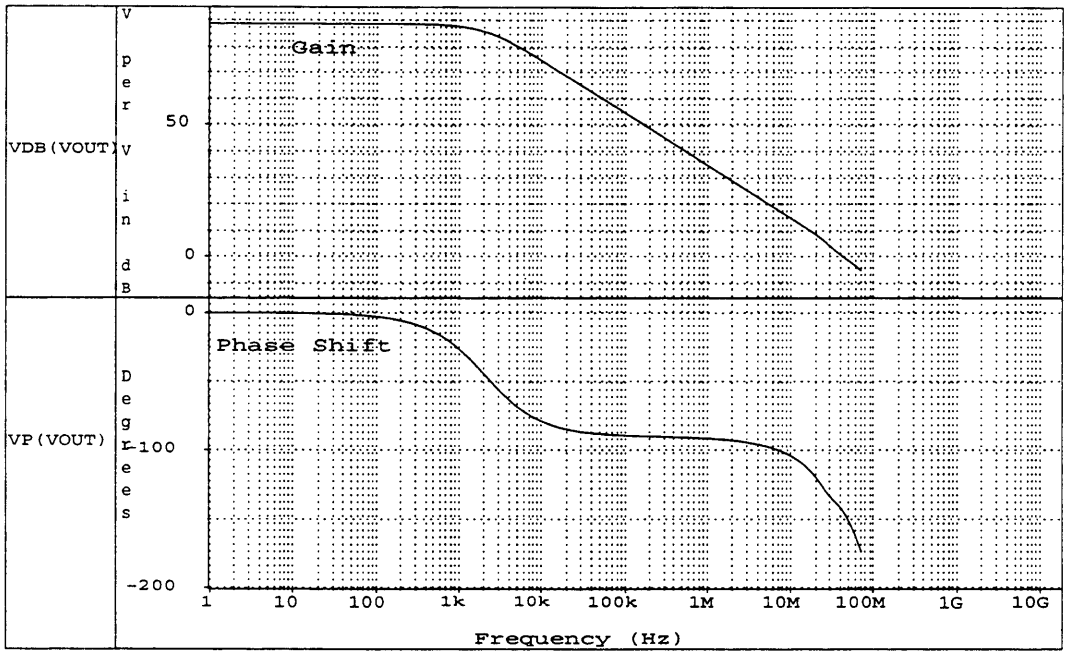

Figure 6.14: Circuit Open-Loop Gain and Phase of the Compensated Preamplifier

6.9 Common-Mode Rejection Ratio and Power Supply Rejection Ratio Analyses

These figures of merit are very important because the common-mode signal and the power supply ripples too are considered "noise" since they introduce an undesired signal superimposed over the information signal. Rejecting noise signals introduced by the common-mode signal and the power supplies will help maintain the integrity of the information.

A simplified circuit used to calculate the common-mode response is shown below (Figure 6.15). Transistors M2 and M4 are a cascode set, we can combine them to one transistor with a transconductance of G_{m1} (which equals to g_{m2}) and an output resistance of

$$(r_{o2} + r_{o4} + g_{m4} r_{o4} r_{o2}) = 367.7 Kohms \tag{6.56}$$

Because the voltage at V7 is approximately equal to V6 in Figure 6.5, we can split the current mirror as shown in Figure 6.15 to achieve a half circuit.

The common-mode voltage is placed at the input gate, and the output signal is measured at the output of the second stage. The current source output resistance of the half circuit is $2R_S$. The analysis can be simplified as follows.

$$v_x \equiv v_{ic} \tag{6.57}$$

$$i_s \equiv -\frac{v_{ic}}{2R_S} \tag{6.58}$$

$$i_D = i_S \tag{6.59}$$

$$v_1 = i_D \frac{1}{g_{m6}} = -\frac{v_{ic}}{2R_s g_{m6}} \tag{6.60}$$

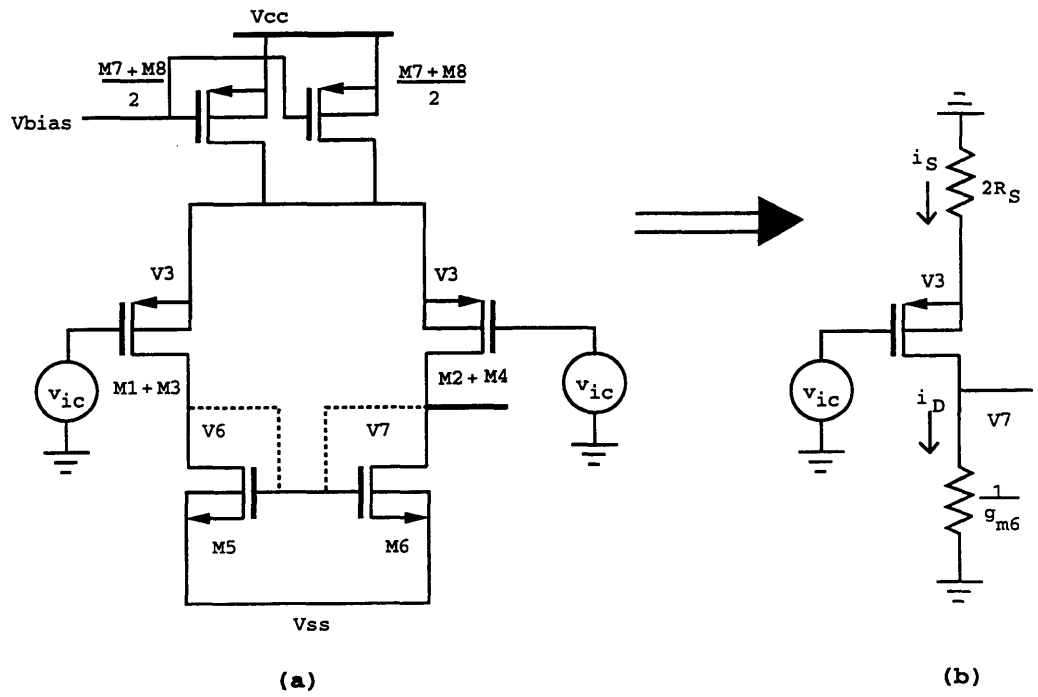

Figure 6.15: Modeling the Preamplifier's Response to the Common-Mode Signal

The output impedance of the cascode current source (M7 and M8) is:

$$R_s = r_{o7} + r_{o8} + g_{m8} r_{o8} r_{o7} = 80.4 Kohms \tag{6.61}$$

The second stage of the preamplifier must also be considered, and the third stage can be assumed to have a gain of 1. The output VOUT due to the common-mode input signal v_{ic} is

$$v_o = a_{v2} v_1 = \frac{a_{v2}}{2R_s g_{m6}} v_{ic} = \frac{G_{m2} R_{o2}}{2R_s g_{m6}} v_{ic} = a_{cm} v_{ic} = 0.203 v_{ic} \tag{6.62}$$

where a_{cm} is called the common-mode gain and a_{v2} is the gain of the second stage.

The node v_3 in Figure 6.15 is approximately equal to the ac signal v_{ic} because v_3 follows the gate signal. The current flowing through $2R_s$ (the resistance of the common current source) is i_S, which is approximately equal to i_D. The output VOUT is i_D times R_D. So the common-mode gain is the ratio of the load resistance over the common current source resistance. The CMRR is the ratio of the differential gain ($a_{vd} = A_v(s)$) to the common-mode gain (a_{cm}). Often times, the CMRR is expressed in decibels.

$$CMRR = \frac{a_{vd}}{a_{cm}} = \frac{a_{v1} a_{v2}}{1} \frac{2R_S g_{m6}}{a_{v2}} = 2a_{v1} g_{m6} R_S \tag{6.63}$$

Also, (in decibels):

$$CMRR = 20\log\left(\frac{a_{dm}}{a_{cm}}\right) = 20\log\left[2G_{m1} R_{o1} g_{m4} R_S\right] \tag{6.64}$$

As we can see, the common-mode rejection ratio can be improved by making the resistance of the current source (M7 and M8) as well as the first stage differential gain as large as possible. Large output resistance of the current source was obtained by cascoding the current source. The figure below (6.16) shows the common-mode gain of the preamplifier

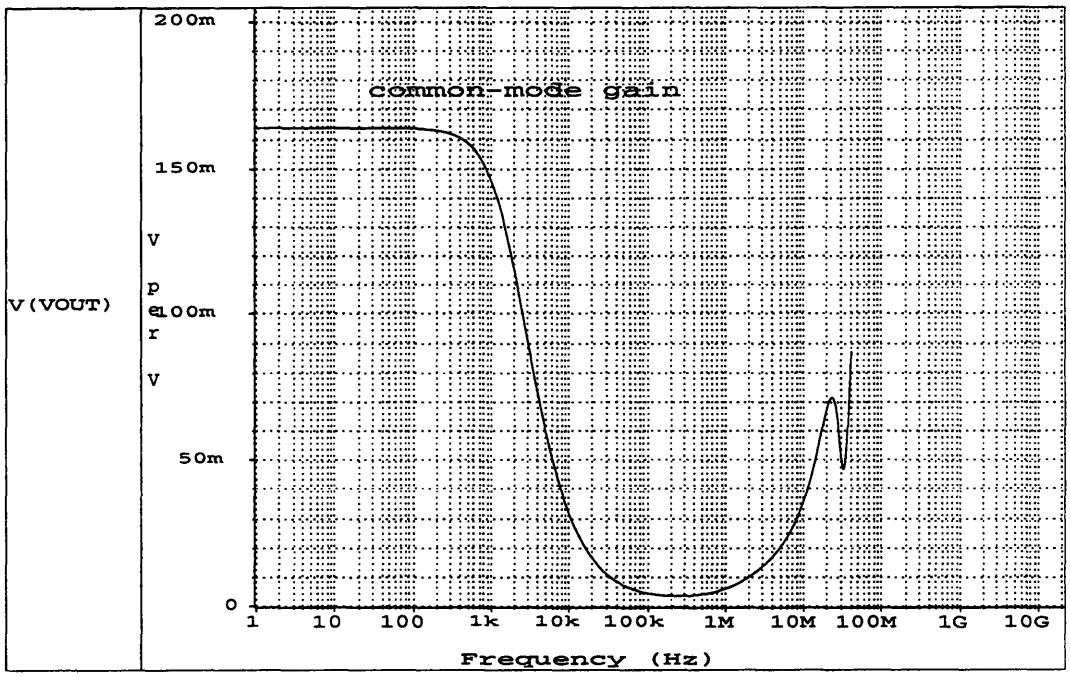

Figure 6.16: Common-Mode Gain of the Preamplifier

The circuit in Figure 6.17 is the small-signal equivalent circuit showing the effects of the circuit to changes in the positive power supply.

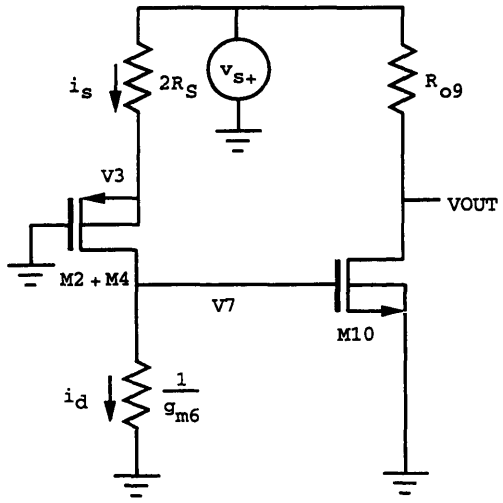

Figure 6.17: Small-Signal Circuit for PSRR+ Analysis

Because the gate of M2 is grounded, and V3 (the voltage at the source of M2) follows the gate voltage, we can consider V3 as a virtual ground. Notice that the circuit's response to V_{s+} is very similar to its response to the common-mode voltage. The current i_D is approximately equal to i_S. The output resistance of M10 is r_{o10} and R9 is the impedance of the cascoded M9 and M11 ($R_9 = r_{o9} + r_{011} + g_{m11} r_{o11} r_{o9} = 223 Kohms$).

$$i_S = -\frac{v_+}{2R_S} \tag{6.65}$$

$$v_3 = i_D \frac{1}{g_{m6}} = -\frac{v_+}{2R_S} \frac{1}{g_{m6}} \tag{6.66}$$

$$v_o = -\frac{a_{v2}}{2R_S g_{m6}} v_+ + \frac{r_{o10}}{r_{o10} + R_9} v_+ \tag{6.67}$$

$$a_+ = \frac{v_o}{v_+} = -\frac{a_{v2}}{2R_S g_{m6}} + \frac{r_{o10}}{r_{o10} + R_9} \tag{6.68}$$

$$PSRR+ = 20\log\left(\frac{a_{dm}}{a_+}\right) \cong 20\log\left(a_{vd}\right) = 82dB \tag{6.69}$$

The second term in equation 6.62 is close to unity. To improve the PSRR+, the differential gain must be made large.

The PSRR- is analyzed in the same manner. The circuit for the analysis is shown in Figure 6.18.

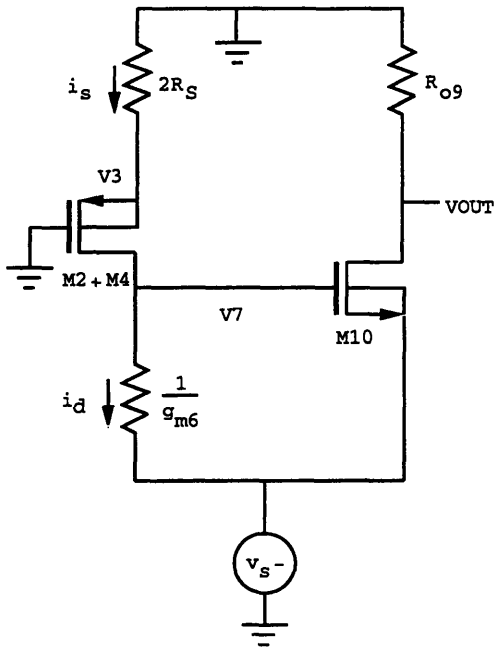

Figure 6.18: Small-Signal Circuit for PSRR- Analysis

$$v_o = \frac{R_{th}}{R_{th} + \frac{1}{g_{m6}}} v_{s^-} + \frac{R_9}{R_9 + r_{o10}} v_{s^-} \tag{6.70}$$

$$a^- = \frac{v_o}{v_{s^-}} = \frac{R_{th}}{R_{th} + \frac{1}{g_{m6}}} + \frac{R_9}{R_9 + r_{o10}} \cong 2 \tag{6.71}$$

$$R_{th} = r_{o4}[1 + g_{m4} r_{o2} (r_{o2}(1 + g_{m4} r_{o4} R_S) + R_S)] + [(r_{o2}(1 + g_{m2} r_{o2} R_S)) + R_S] \gg R_9 \tag{6.72}$$

$$PSRR^- = 20\log\left(\frac{a_{dm}}{a^-}\right) \tag{6.73}$$

The PSRR- can be maintained at acceptable values by keeping the output resistance of the circuit high. Noise due to power supplies can also be reduced by having a higher quality power supply or using a filter to eliminate the ripples. In most IC processes, the negative supply is not too critical an issue, so the PSRR specification can be relaxed a bit.

Figure 6.19 shows an example PSRR curve of the preamplifier.

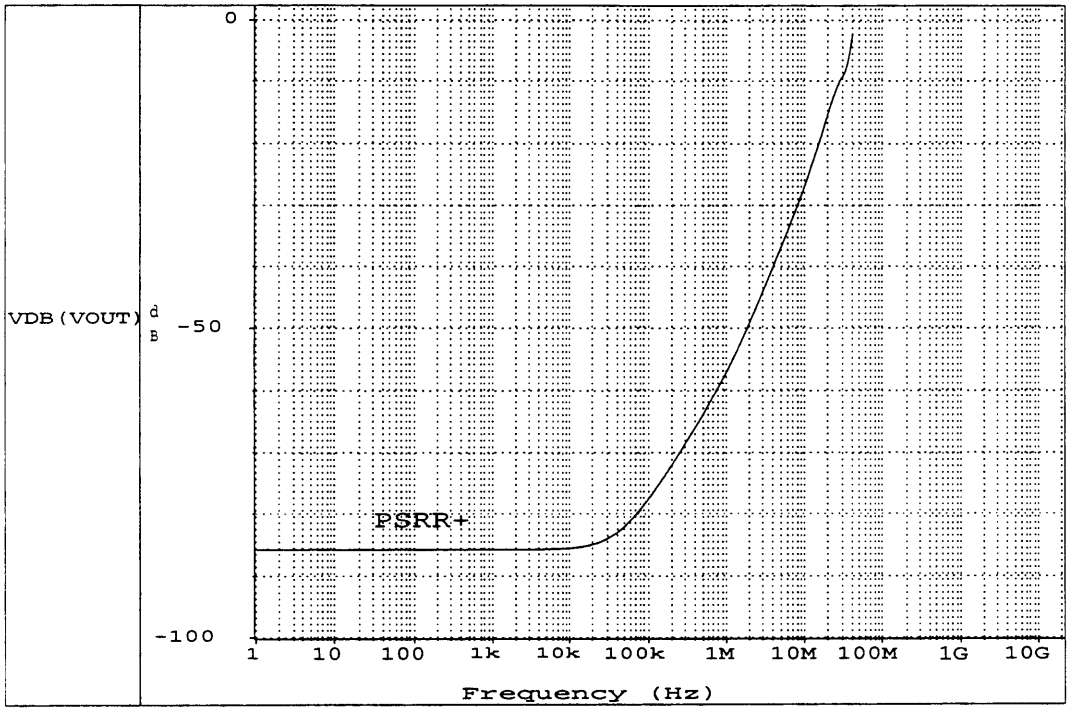

Figure 6.19: The Preamplifier's PSRR+ vs. Frequency

6.10 Closed-Loop Circuit Performance

So far we have been dealing with open-loop figures of merit. The preamplifier will be used in a closed-loop configuration. The closed loop topology that will be used with the sensor is shown in Figure 6.20 (where the source labeled AC is the input source).

The sensor is modeled by a 1pF nominal capacitance with a sinusoidal voltage source oscillating at 27kHz. The stray capacitance due to parasitics of the sensor system is C_p (4pF). The feedback network is a capacitor C_f of 2pF parallel to a resistor R_f of 3.9Gohm. The output will probably need to drive 5pF when connected to another circuit in the chip, and to about 18pF if the output node is probed for measurements. In this configuration, the input capacitance at the gate of the preamplifier will have a significant effect on the circuit's performance. The closed-loop frequency response is

$$\frac{V_{out}}{V_{in}}(s) = -\frac{C_s}{C_f + \dfrac{C_s + C_p + C_f + C_{inp}}{A(s)}} \tag{6.74}$$

Where $A_v(s)$ is the frequency response of the op-amp (Equation 6.45). Spice simulations resulted in a closed-loop gain of 0.5 and a phase shift of 0.11 degree at 27kHz. The closed loop frequency response is shown in Figure 6.21.

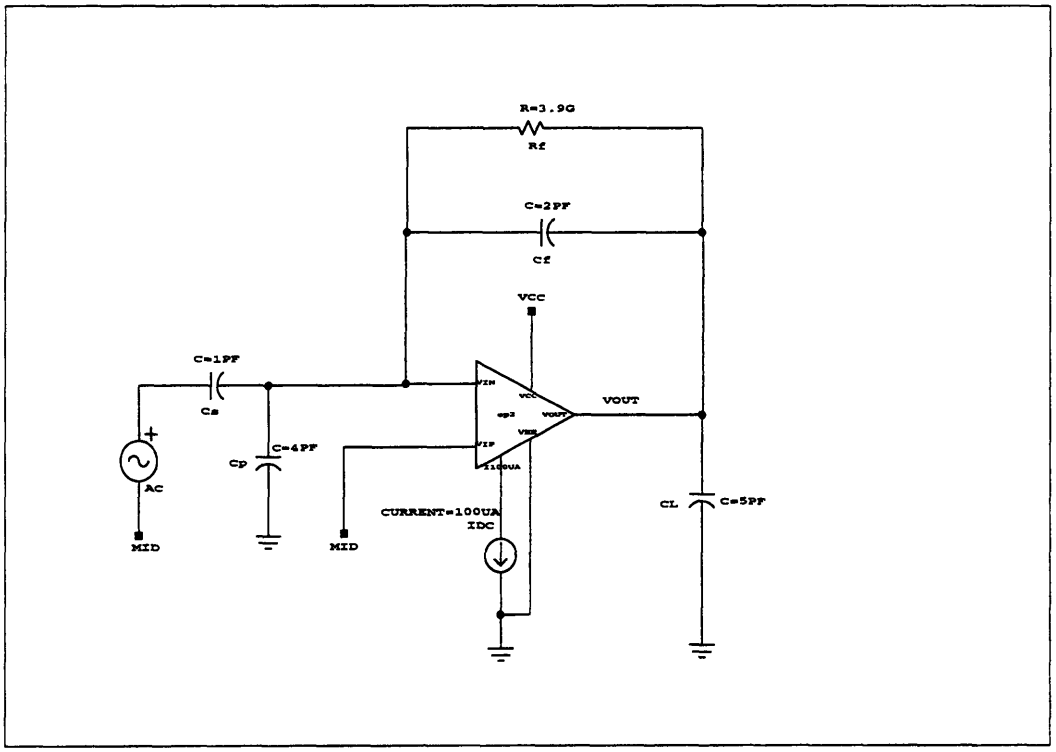

Figure 6.20: Closed-Loop Configuration of the Preamplifier

To measure the equivalent input noise of the preamplifier in a closed-loop configuration, the input voltage source is placed at the positive terminal of the amplifier. Spice will take the output noise, calculate the gain from the input source to the output node, and divide the output node by that gain. The circuit shown in Figure 6.22 was used to test the input referred noise.

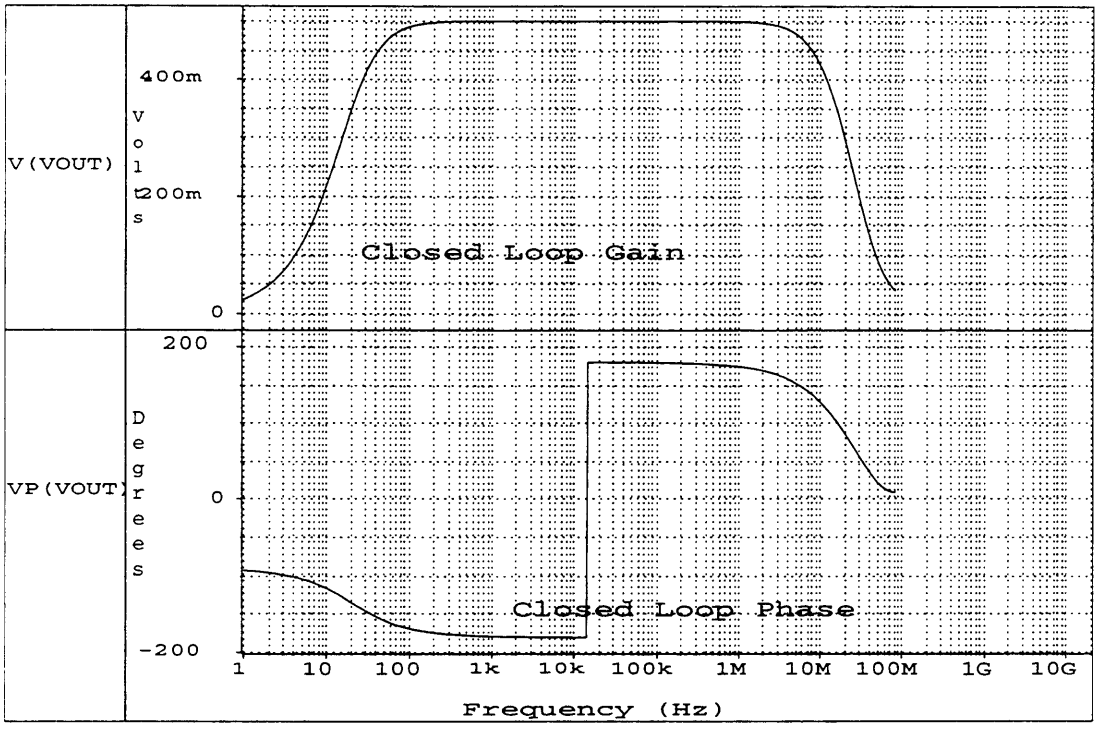

Figure 6.21: The Preamplifier's Closed-Loop Frequency Response

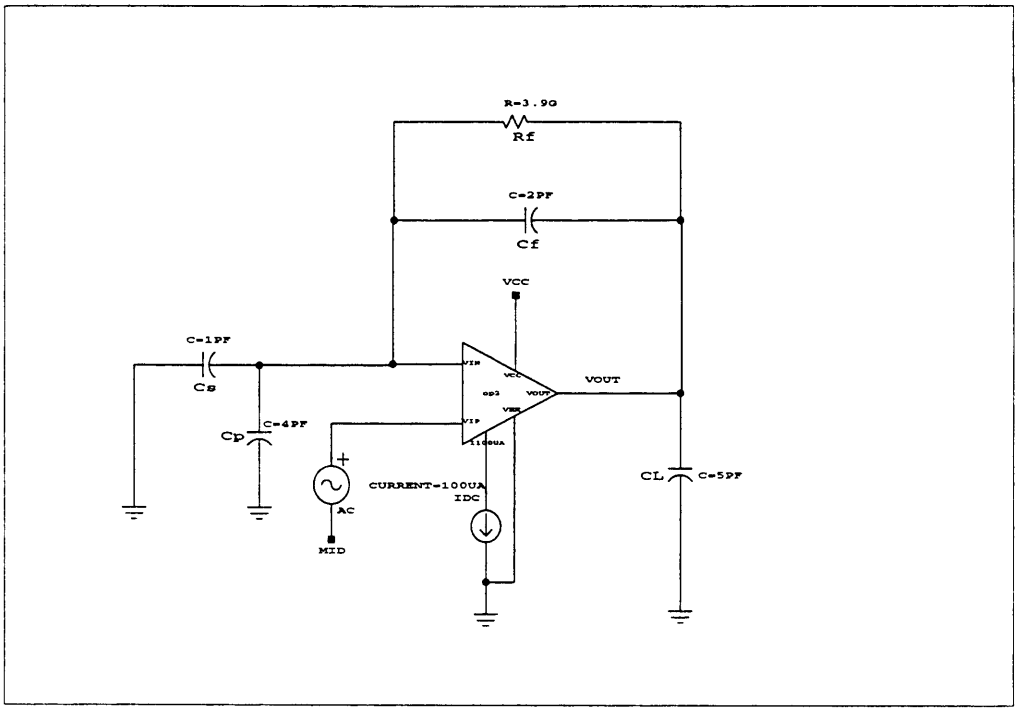

Figure 6.22: The Circuit Configuration Used to Measure Input Referred Noise

The noise gain can also be approximated by adding 1 to the gain of the signal. However, the approximation can be far from accurate if the parasitic capacitance C_p and the input capacitance of the op-amp (C_{inp}) are large compared to the sensor and the feedback capacitances.

The output thermal noise shown in Figure 6.23 is shown in linear scale (upper) and log scale (lower). The output noise is high at low frequency because the large noise voltage of the feedback resistor R_f is high at low frequencies. After the resistor noise is attenuated to a value smaller than the amplifier's noise, we see a leveling off of the noise at about 10kHz.

The output noise with flicker is shown in Figure 6.24. The output noise with flicker looks similar to that with only the thermal, except for the higher corner frequency. Once the resistor noise dies out, the flicker takes over, and then finally, we are left with the fundamental thermal noise of the op-amp.

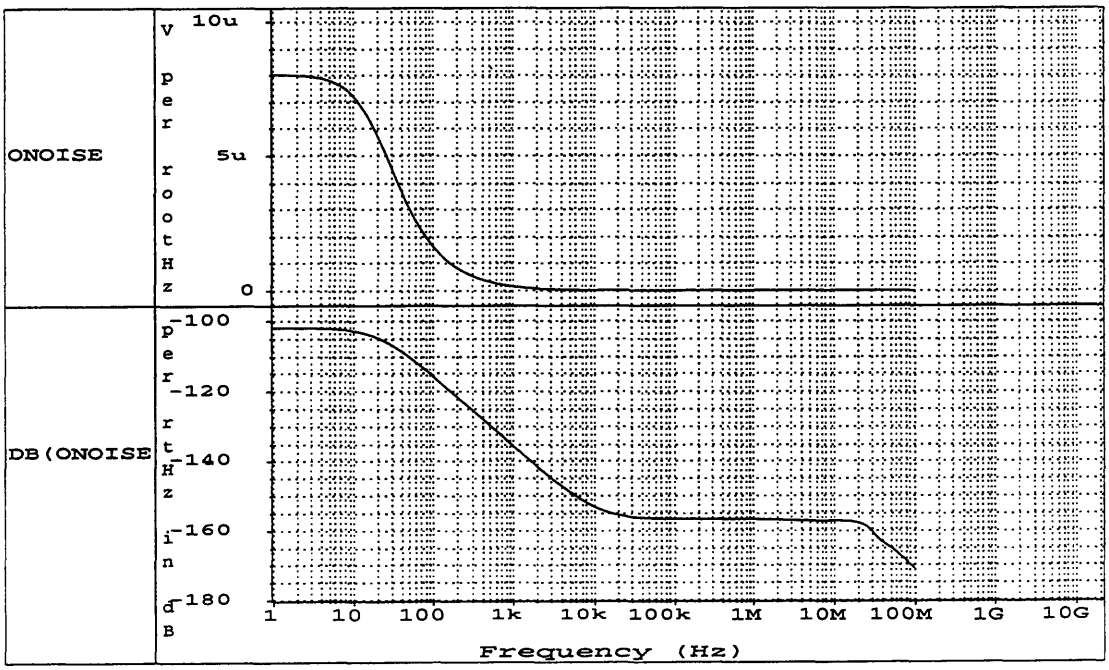

Figure 6.23: Closed-Loop Output Thermal Noise

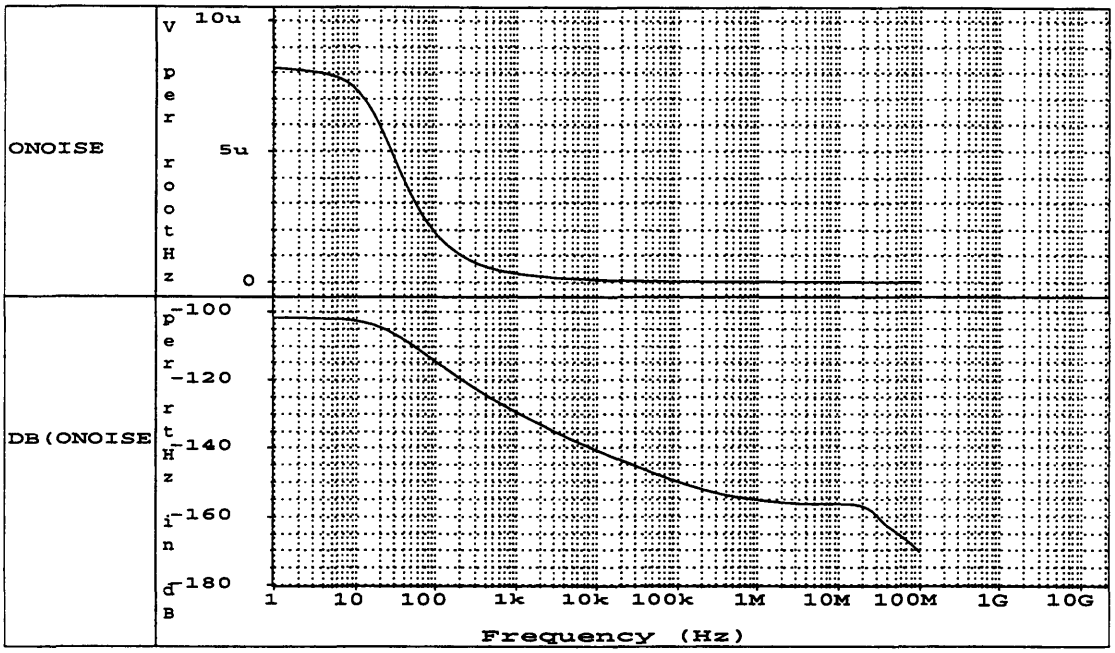

Figure 6.24: Closed-Loop Output Noise Including Flicker Noise

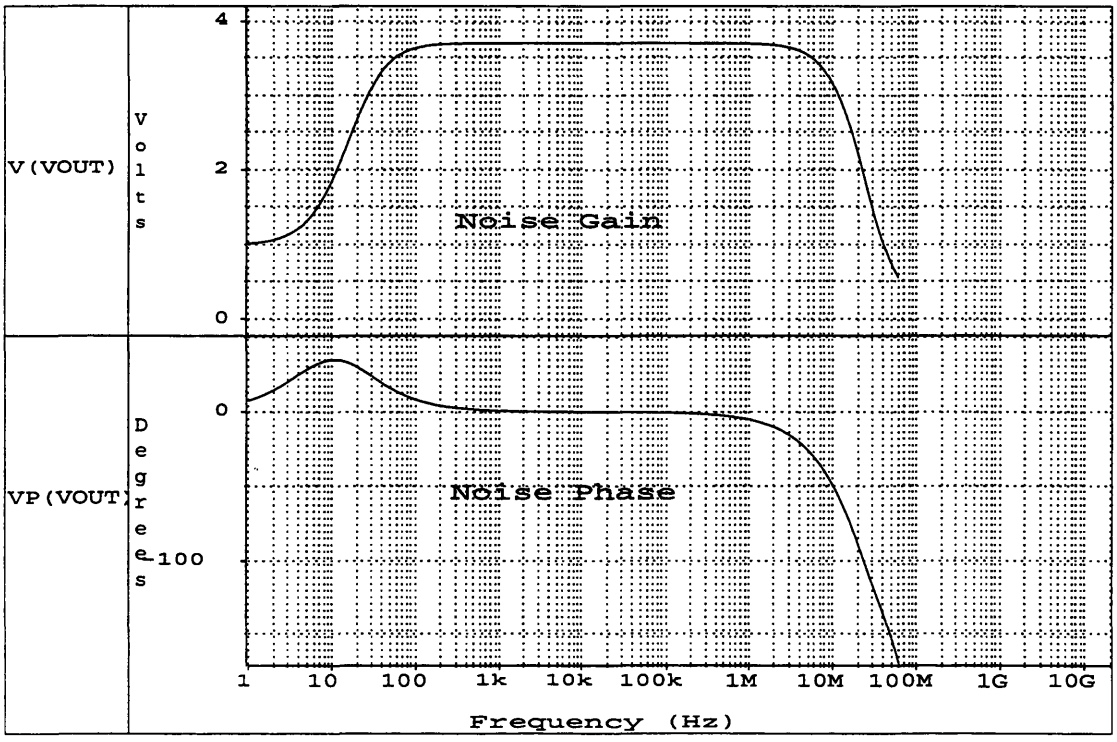

Figure 6.25: The Preamplifier's Closed-Loop Noise Gain

Spice calculated a noise gain of 3.7 (as shown in Figure 6.25) which is equivalent to $\frac{C_s + C_p}{C_f} + 1 = \frac{1pF + 4pF}{2pF} + 1 = 3.5$; however, the simulator did not take into account the input capacitance of the input device (C_{inp}=5pF). The actual noise measurement should be $\frac{C_s + C_p + C_{inp}}{C_f} + 1$, which comes to 6. This noise gain of 6 is consistent with the Spice calculations of the output noise.

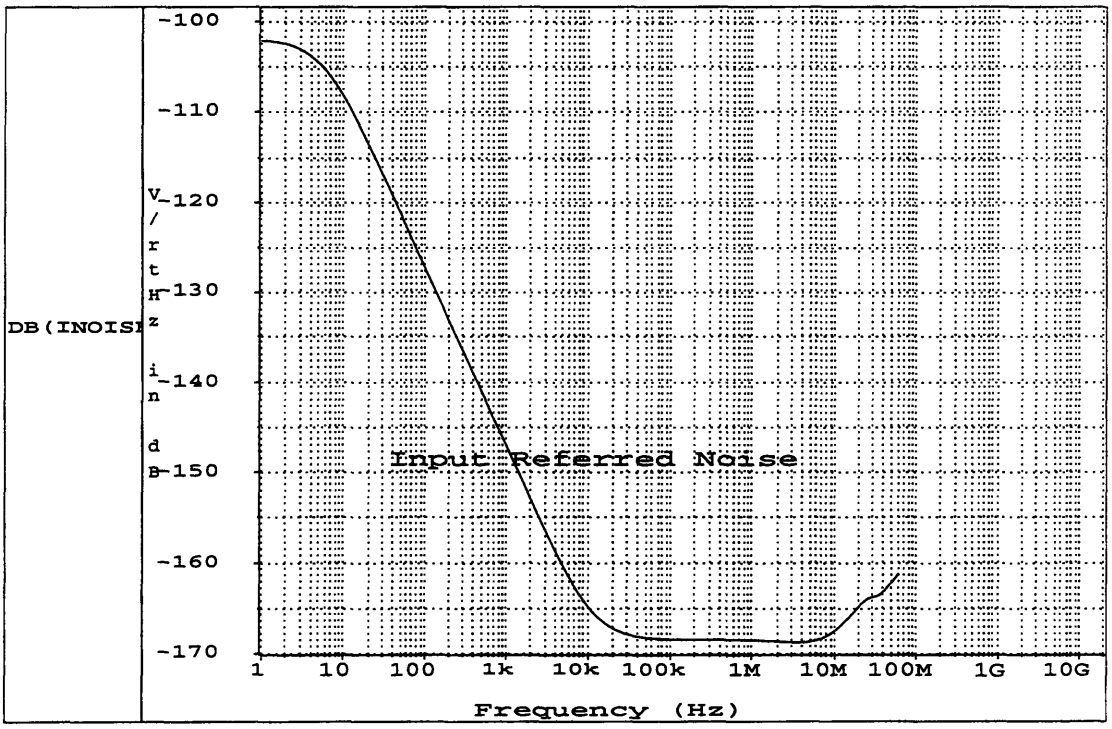

Figure 6.26: The Preamplifier's Closed-Loop Input Referred Thermal Noise

The input referred thermal noise at low frequency is high because of the decreasing gain as the frequency reaches DC as well as the high thermal noise from the resistor R_f at low frequency, (as shown in Figure 6.26). At 27kHz, the output noise breakdown is shown in Table 6.3.

	Rf	Preamplifier	Total	Spice Calculation
Output Noise	$6.07\frac{nV}{\sqrt{Hz}}$	$13.1\frac{nV}{\sqrt{Hz}}$	$14.4\frac{nV}{\sqrt{Hz}}$	$15.19\frac{nV}{\sqrt{Hz}}$
Input Noise	$1.01\frac{nV}{\sqrt{Hz}}$	$2.18\frac{nV}{\sqrt{Hz}}$	$2.40\frac{nV}{\sqrt{Hz}}$	$2.53\frac{nV}{\sqrt{Hz}}$

Table 6.3: Breakdown of Noise in Closed-Loop System

With flicker component added, the input referred noise curve looks as follows (in Figure 6.27).

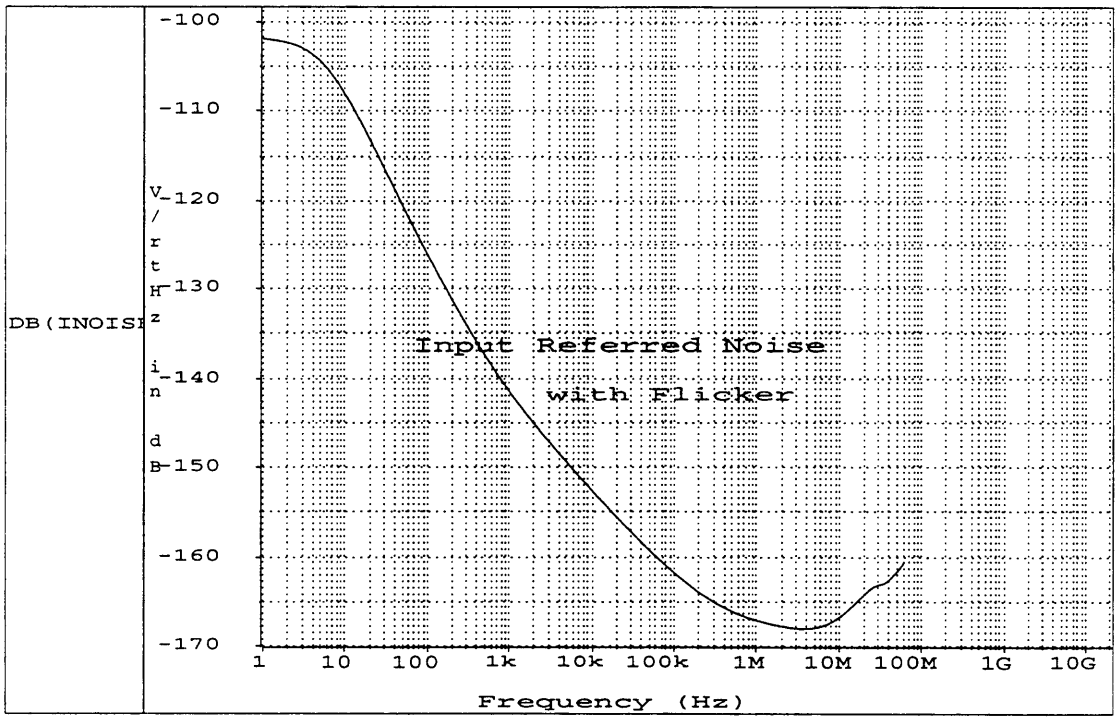

Figure 6.27: The Closed-Loop Input Referred Noise Including Flicker Noise

Closed-loop noise performance was also tested over the temperature range of -40C to 85C. The change in noise is due to the thermal noise in the channel and resistor R_f. Figure 6.28 shows the noise performance versus temperature.

In practice, any parasitic gate current will double every decade of temperature increases. This noise current will generate noise with the feedback network in the close loop configuration, so the noise variation with increasing temperature might be worse than predicted by Figure 6.28.

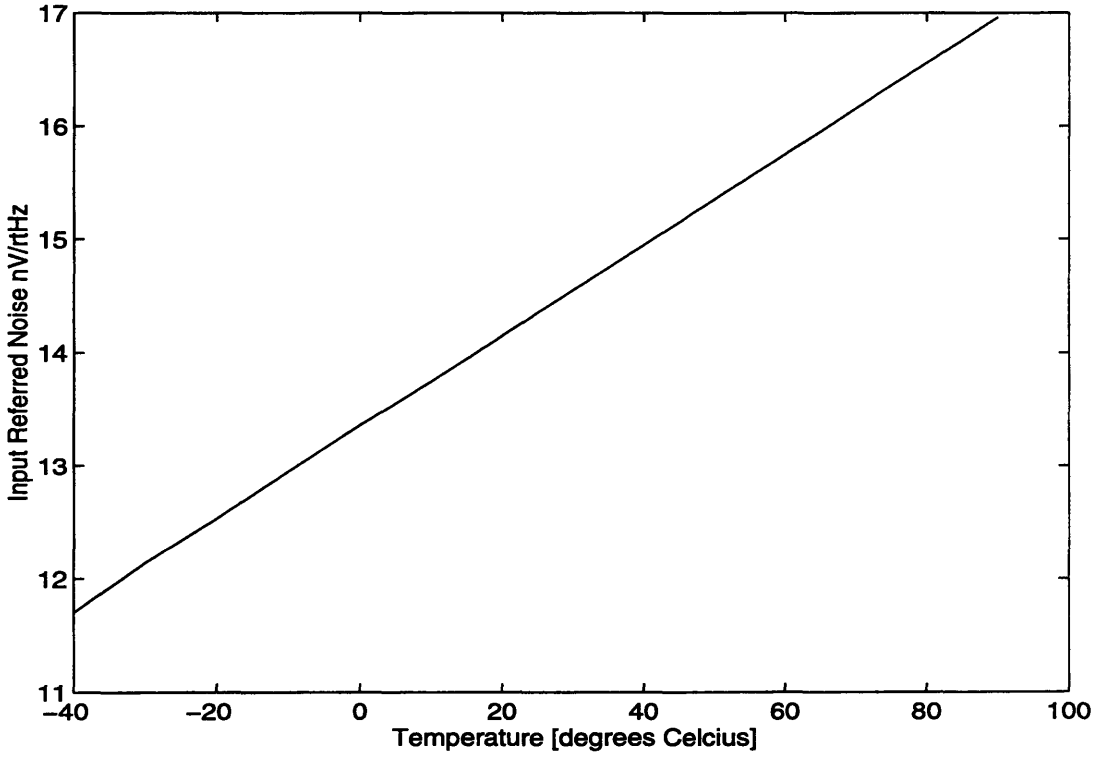

Figure 6.28: The Preamplifier's Noise versus Temperature (Including Flicker Noise)

Chapter 7

Conclusion

Exploiting the lower signal levels of today's micromechanical sensors require extremely low-noise preamplifiers. Two low-noise preamplifiers were constructed using (discrete) JFET front ends with the OP-27 as the next amplifying stage. One amplifier had a JFET differential pair front end; and the other had a JFET dual source follower front end. A third amplifier was designed to be fabricated in a CMOS process.

It is well known that front ends made of discrete components provide better noise performance than front ends made of integrated devices (whose process involves integration of other device types and components). Integration involves more processing steps as well as the inclusion of many more types of materials that contribute to significant level of impurities.

The discrete JFET front ends and the OP-27 offered excellent low-noise solution for capacitive sensing applications which tended to result in high source impedances due to the small size of the sensed capacitance. The U440 of Siliconix offered the necessary low noise voltage, low noise current, and low input capacitance necessary to provide a noise performance superior than the popular low-noise JFET input op-amp AD549 produced by Analog Device, Inc. The differential pair front end made of the U440 JFETs had an input referred noise of $9\frac{nV}{\sqrt{Hz}}$ and the dual source follower front end resulted in an input referred noise of $10\frac{nV}{\sqrt{Hz}}$. Both noise measurements were taken at 27kHz and room temperature.

The differential pair front end performed somewhat better than the dual source follower front end because of its larger gain. The noise of the OP-27 was reduced by the gain of the differential pair when referred to the input. In the case of the virtually unity-gain dual source follower, the noise contribution from the OP-27 is referred directly to the

input without any reduction from the front end stage. Although the differential pair has slightly better noise performance, the dual source follower was preferred over the differential pair because it did not introduce instability into the preamplifier system. The gain of the differential pair degraded the phase margin of the OP-27. The gain of the differential pair is $g_m R_D$, where g_m is the transconductance of the JFET and R_D is the load resistance. Because these discrete JFETs vary significantly in transconductance, so would the gain. The gain variation would make the system's stability unpredictable.

The IC solution offers the flexibility to optimize the size of the input devices. In general, large transconductance reduce the channel thermal noise and flicker noise. Thus devices are made large; however, their size increase create large input capacitances which result in a higher noise gain while the signal gain remains constant. An optimal device size can be obtained by keeping track of the noise gain increase versus the reduction of the device's noise.

Aside from the input devices, the active load devices were also specially sized. These were made to have large gate lengths to reduce their flicker noise and thermal noise contributions, when referred to the input of the preamplifier. Noise calculations show that the load's thermal noise contribution is a fraction of the thermal noise of the input device. This fraction is defined by the ratio of the load transistor's transconductance over the input device's transconductance ($\frac{g_{m\_load}}{g_{m\_in}}$). Making the gate lengths of the load transistors large keeps the load's transconductance small, thus reducing the load's thermal noise contribution. The input devices were made a little larger than the minimal length to reduce the channel length modulation effect as well as to reduce the flicker noise.

The CMOS preamplifier design offers a white input referred thermal noise of $2.18\frac{nV}{\sqrt{Hz}}$, and a total input referred noise of $9.33\frac{nV}{\sqrt{Hz}}$ at 27kHz when the process's predicted flicker coefficient was included in the simulation. However, there is no way of accurately predict-

ing the flicker's contribution. The presence of flicker noise makes it difficult to design for low-noise. The noise performance of the chip will depend on how close the predicted flicker contribution is to the actual flicker contribution.

In terms of noise performance, CMOS devices are better suited for applications with high operating frequencies (100kHz to 500kHz), where the effect of flicker noise is insignificant. However, higher frequency operation is not only demanding to the construction of the sensor but to other processing circuits as well.

It appears that using a front end made of discrete JFETs is the most promising solution to capacitive sensor applications. If the preamplifier is to be made in CMOS, the operating frequency should increase to 100kHz or somewhat higher to avoid flicker noise.

Appendix A

Circuit Configurations for Simulations

The following sections discuss simulation methods and circuit configurations used to make the various specifications for the preamplifier.

A.0.1 Operating Points

The table below (A.1) shows the important characteristics of the devices in the signal path. Table A.2 shows the capacitances of the devices. The device parasitic capacitances C_{gd} and C_{gb} are negligibly small. The values in Tables A.1 and A.2 are necessary to calculate the AC performance of the circuit.

Device	W (μm)	L (μm)	I_d (μA)	g_m (mmho)	r_o (Ω)
M1, M2	3000	1.8	527	5.71	12.38K
M3, M4	540	1.8	527	2.23	12.42K
M5, M6	300	10	527	1.26	249.76K
M14	134	4	1050	5.70	17.82K
M15	300	1.4	1050	1.95	1.75K
M9	1000	2	656	3.27	13.193K
M10	55	2	656	1.43	26.67K
M11	28	1.8	656	0.515	26.95K
M14	134	4	801	0.856	46.73K
M15	300	1.4	801	2.55	13.66K

Table A.1: Operating Points Information

Device	Cgs	Cdb	Csb
M1, M2	5.09pF	5.74pF	8.13pF
M3, M4	0.915pF	1.18pF	1.47pF
M5, M6	2.94pF	0.558pF	0.893pF
M9	1.90pF	2.07pF	2.71pF
M10	89fF	0.117pF	0.165pF
M11	46.1fF	0.433pF	0.780pF
M14	0.526pF	0.214pF	0.365pF
M15	0.385pF	0.476pF	0.815pF

Table A.2: Device Capacitances

A.0.2 The Input Offset

The input offset was measured by configuring the preamplifier in a unity gain configuration.

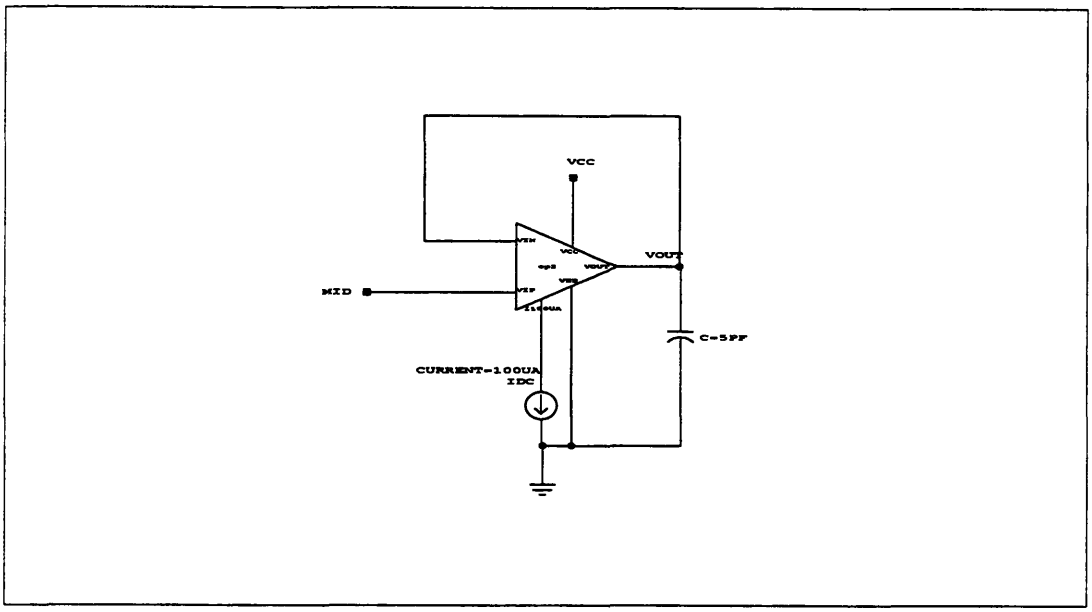

Figure A.1: Circuit Configuration for Measuring Input Offset

From simulation results, the input offset of this preamplifier is 2.0uV at room temperature.

A.0.3 Open Loop Gain and Phase vs. Frequency

Testing the circuit in an open-loop configuration is different than testing it in a closed-loop configuration. When set up in a closed-loop configuration with a resistor in the feedback, the output usually goes to a potential close to the reference terminal (the non-inverting terminal) and the offset appears at the summing node of the closed-loop configuration. This balancing act is possible through the feedback resistor R_f. However, in the open-loop configuration, there is no path for the output to control the input and the op-amp's output saturates. This offset must be placed at one of the input terminals to balance the output bias.

Once the input offset is determined, the negative of the input offset voltage can be inserted at the non-inverting terminal of the op-amp to balance the biasing. Such biasing correction by the input offset gives the best open-loop circuit performance. The circuit below shows the open-loop configuration used in the simulations.

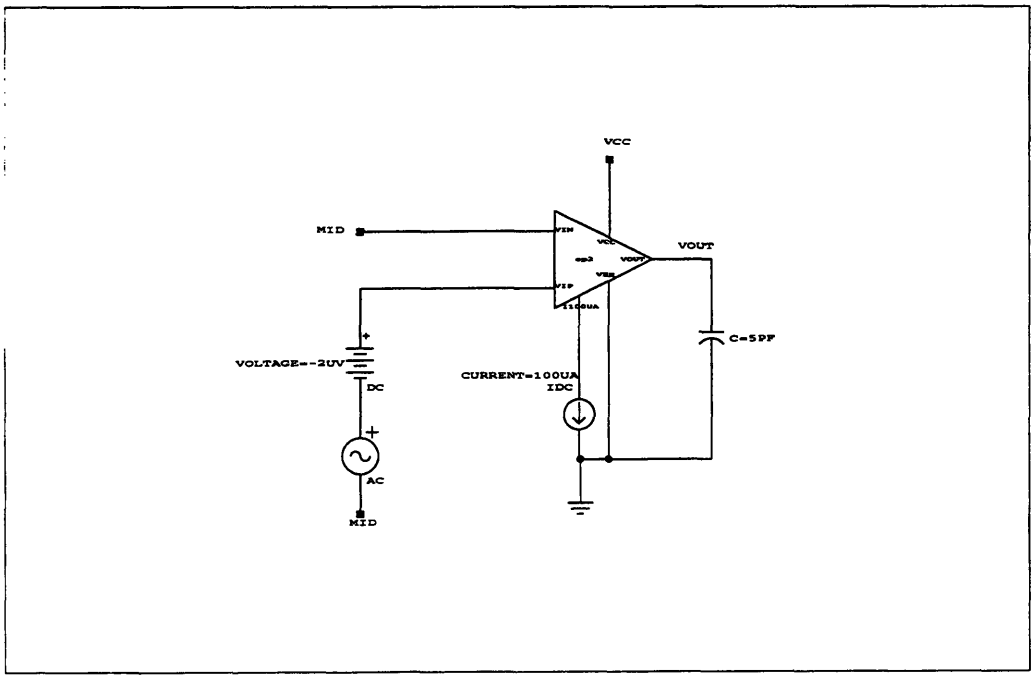

Figure A.2: Circuit Configuration for Measuring Open-Loop Gain

A.0.4 PSRR's

The circuit topology used to simulate the PSRR+ is shown in Figure A.3. The preamplifier is in a unity-gain configuration..

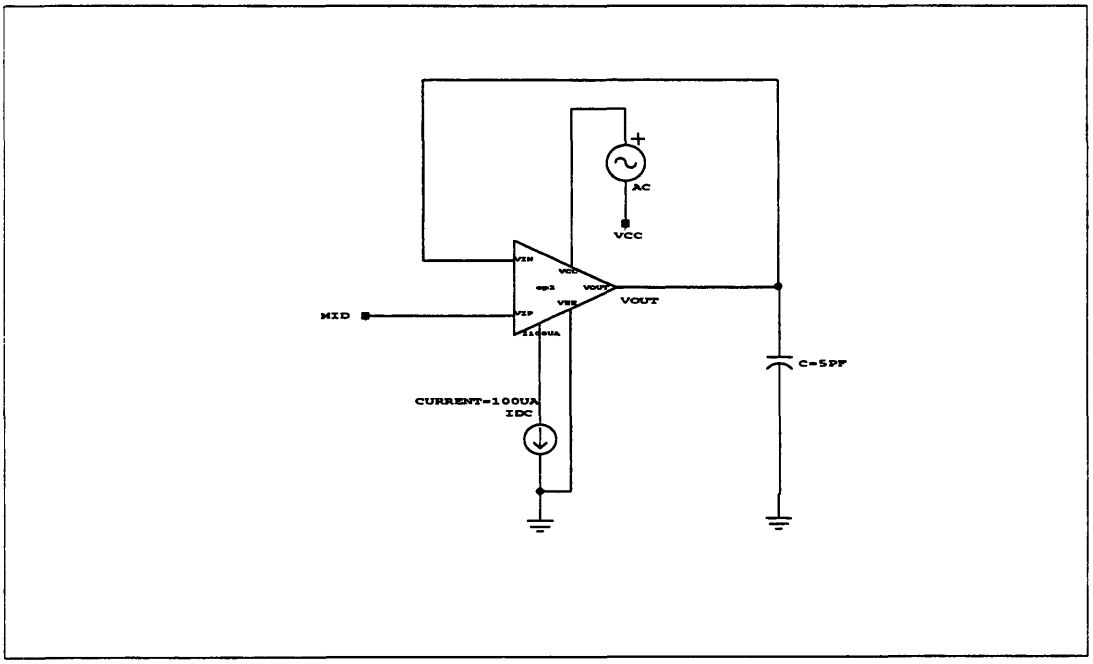

Figure A.3: Circuit Configuration Used to Find the PSRR+

A.0.5 CMRR

The common-mode gain was measured by tying the inverting terminal and the non-inverting terminal of the op-amp together and connecting to a common AC source. Because the AC signal's amplitude was set to unity, the output signal VOUT also represents the common-mode gain. This gain is then divided by the differential-mode gain to obtain the CMRR. The common-mode gain at 27kHz was divided by the differential gain at 27kHz to get the CMRR of the op-amp at 27kHz. Note that this configuration can only be accomplished in simulations because in practical use, we cannot easily insert an offset voltage as shown in Figure A.4.

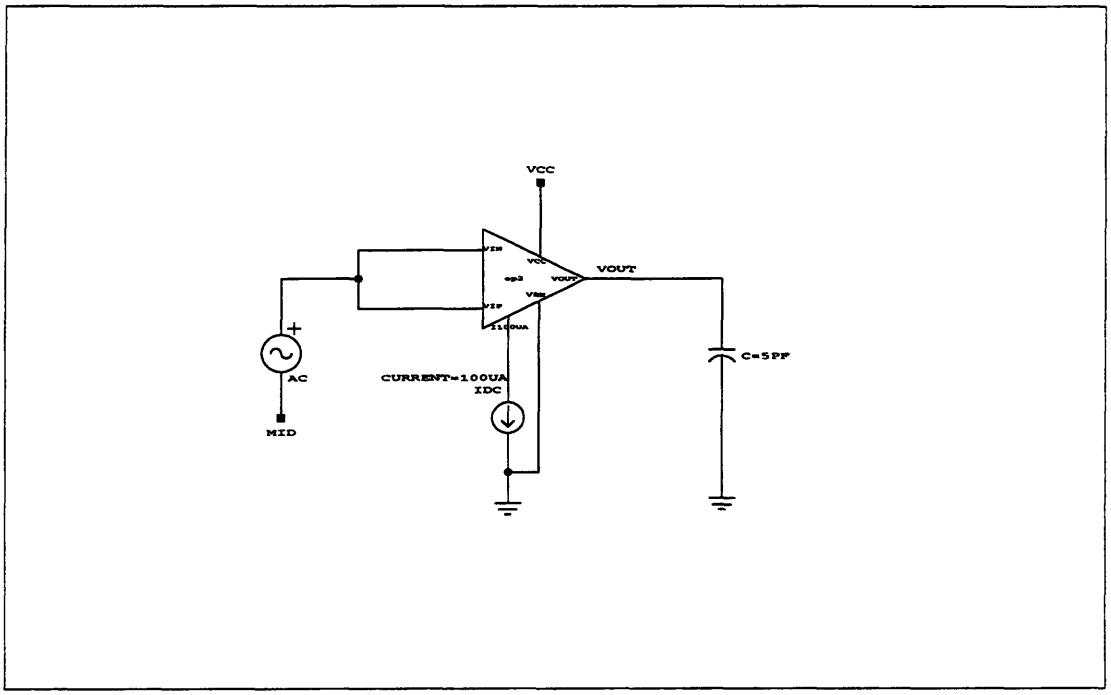

Figure A.4: Circuit Configuration for Measuring Common-Mode Gain

A.0.6 Step Response

It is important to test the step response of the circuit because the circuit needs to respond quickly to fast-edged signals. The best way to test the response of the preamplifier is to set it up in a unit gain configuration. If other capacitor or resistor components are used to close the loop around the circuit, then the response will be dominated by these resistor-capacitor networks.

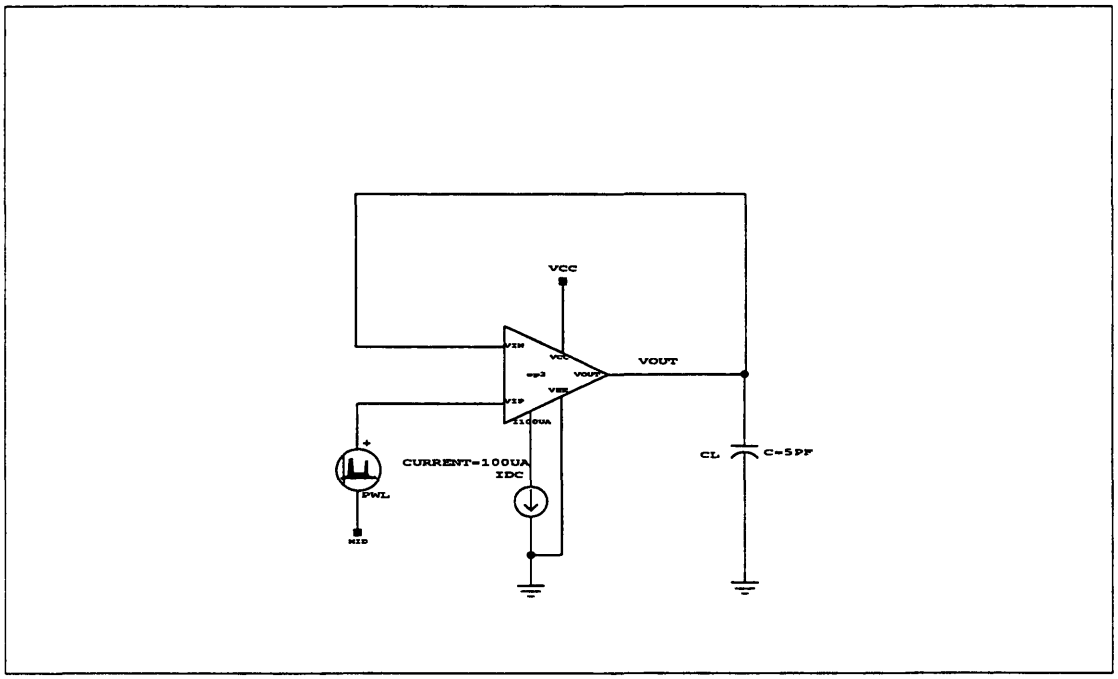

Figure A.5: Circuit Used to Measure Step Response

The large-signal step response is shown in Figure A.6. It took the circuit 170ns to settle to 0.1% of the settled value.

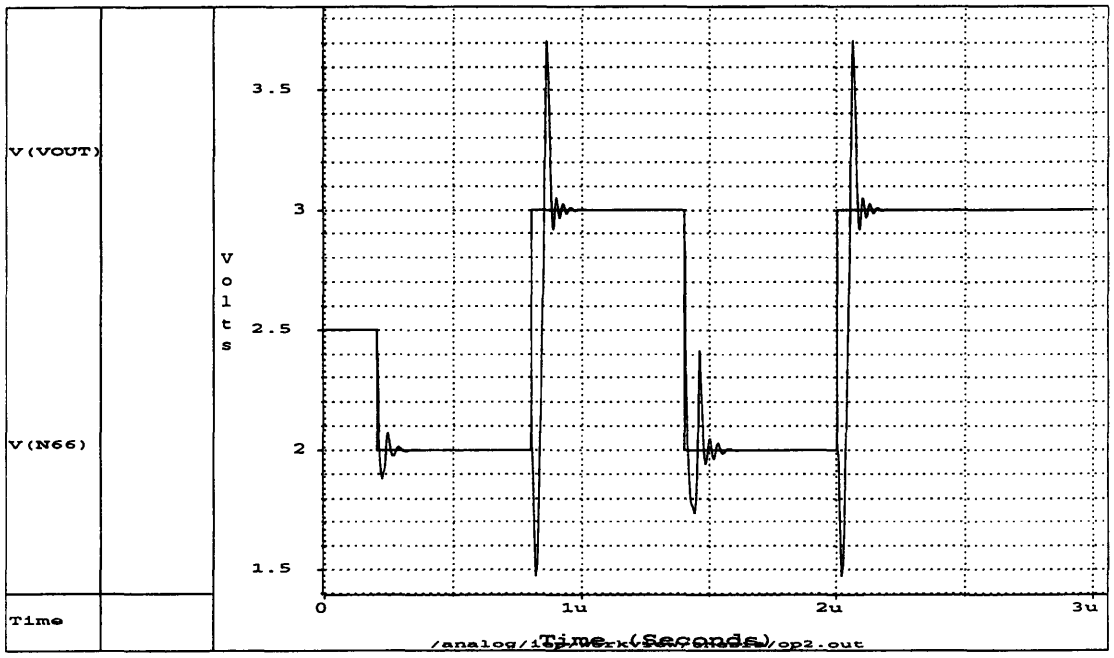

Figure A.6: Large-Signal Step Response

The small-signal step response is better than the large-step response. It took 100ns to reach 0.1% of the settled value.

Figure A.7: Small-Signal Step Response

A.0.7 Slew Rate

The slew rate is an indication of how quickly the amplifier can respond to a fast input signal. The output of the step response can be used to measure the slew rate. It appears to be about $55\frac{V}{\mu s}$. The slew rate is also very dependent on the load capacitance. In general, maximum slew rate is approximated to be $\frac{I_o}{C_L}$, where I_o is the biasing current at the output stage and C_L is the load capacitance.

A.0.8 Common-Mode Input Range

The op-amp can operate with excellent gain for an input biasing value $\pm 500mV$ from the midpoint between the positive and negative rails (2.5V in our case).

A.0.9 Output Swing

The circuit used to check the output swing is shown in section A.6. The output is shown below.

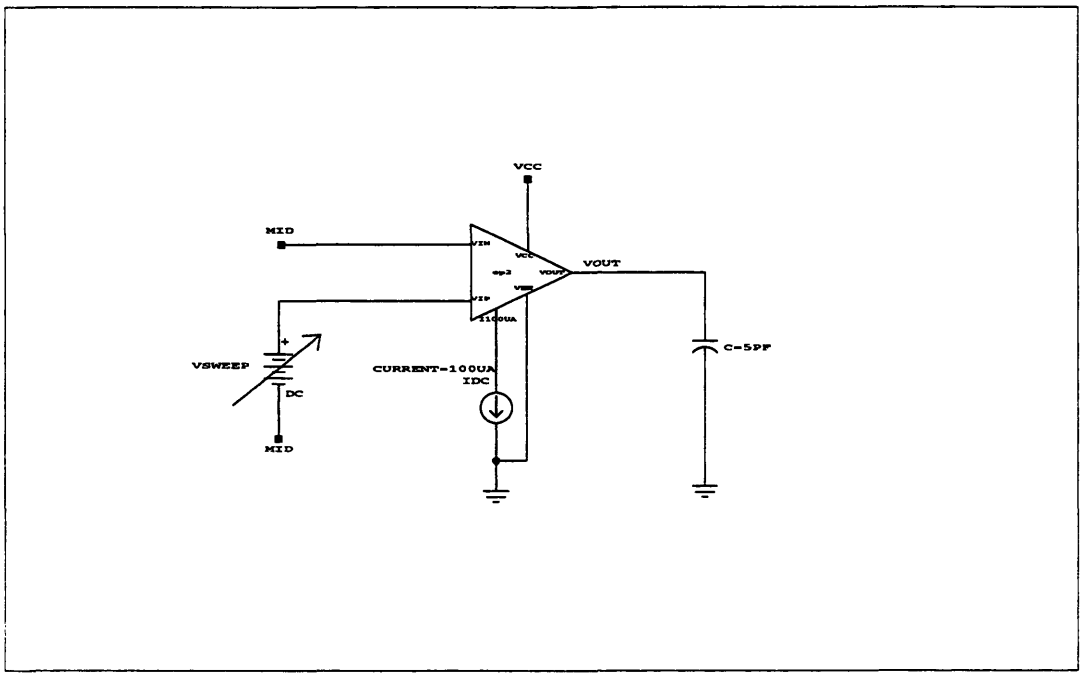

Figure A.8: Circuit Configuration for Testing Output Range

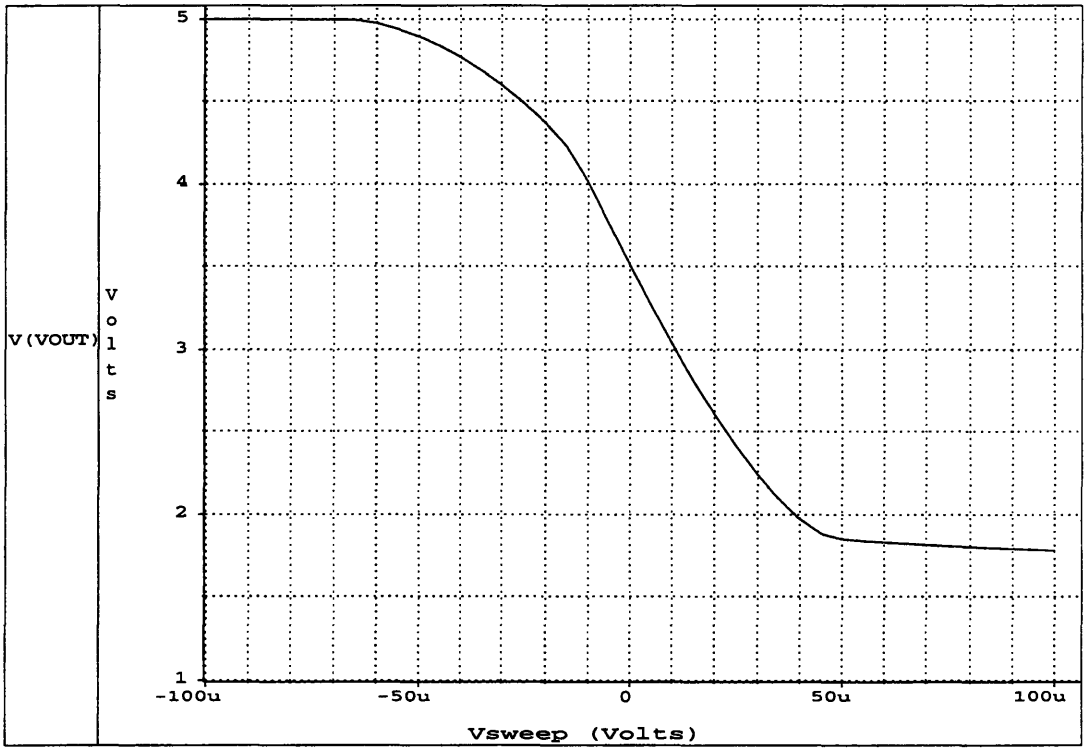

Figure A.9: Output Swing

We can see that the amplifier has more room for the upswing. The down swing is limited by the source follower.

References

[1] Weinberg, Marc; Bernstein, Jonathan; Cho, Steven; King, A. Thomas; Kourepenis, Anthony; Marcel, Paul. *Micromachined Comb-Drive Tuning Fork Rate Gyroscope.* Proceedings of the Annual Meeting - Institude of Navigation 1993. p. 595-602.

[2] Motchenbacher, C.D.; Connelly, J. A. *Low-Noise Electronic System Design.* John Wiley & Sons, New York, New York, 1993.

[3] Gray, Paul R.; Meyer, Robert G. *Analysis and Design of Analog Integrated Circuits.* John Wiley and Sons, Inc. New York, New York, Thrid Edition. 1993.

[4] Gregorian, Roubik; Temes, Gabor C. *Analog MOS Integrated Circuits for Signal Processing.* John Wiley & Sons, Reading, Massachusetts, Second Edition, 1973.

[5] *Siliconix Low-Power Discretes Databook.* 1994.

[6] Sze, S. M. *Physics of Semiconductor Devices.* John Wiley and Sons, Inc. New York, New York, Second Edition. 1981.

[7] Netzer, Yishay. The Design of Low-Noise Amplifiers. In Gupta, Madhu S., editor, *Selected Papers on Noise in Circuits and Systems*, in Advances in Circuits and Systems, pages 19-32. IEEE Press, New York, 1988.

[8] Horowitz, Paul; Hill, Winfield. *The Art of Electronics.* Cambridge University Press, Cambridge, Massachusetts, Second Edition, 1989.

[9] Allen, Phillip E.; Holdberg, Douglas R. *CMOS Analog Circuit Design.* Harcourt Brace Jovanovich College Publishers. New York, New York, 1987.

[10] MicroSim Corporation. *Pspice.* Irvin, California, 1989.

[11] Gray, Paul E.; Searle, Campbell L. *Electronic Princlipes: Physics, Models, and Circuits.* John Wiley and Sons, Inc. New York, New York, 1969.