

# A 20 dBm 5-14 GHz Power Amplifier with Integrated Planar Transformers in SiGe

by

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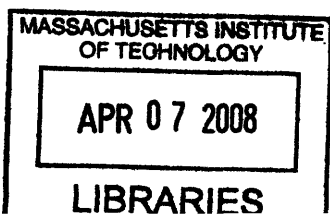
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## Abstract

The integration of radar systems has taken a long journey into the modern world. Advances in signal processing technology and integrated circuit technology have lead the way for smaller, more integrated radar systems. Specific to the hardware side of a radar, the RF generation and detection once done in one location in the radar is now being replaced by small sub-elements which combine RF generation and detection at the element level. This work describes a power amplifier that can be used at the element level. The design methodology for a single stage amplifier in a Silicon Germanium Bipolar process covering 5-14 GHz is discussed. Simulation results and measurement results closely match and show peak power outputs of 25 dBm and peak power-added efficiencies (PAE) of approximately 32 %.

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# Chapter 1

## Introduction

The microwave frequency spectrum is home to numerous application areas, a few of which include communication links, radar and other remote sensing activities. X-band, covering 7-12.5 GHz is the microwave frequency spectrum of interest in this work. Inherent to X-band systems is the generation and amplification of RF energy. X-band signals are generated by a microwave oscillator, however the output level is typically not high enough to be of practical use alone, and thus there is a need for a power amplifier.

Modern trends in system design have moved to the design of powerful digital circuits in CMOS and SiGe BiCMOS processes. However, analog, radio-frequency (RF) and microwave circuits have not followed the same trend as fast. Traditionally microwave power amplifiers have been designed in Gallium Arsenide (GaAs), Indium Phosphide (InP) and recently Gallium Nitride (GaN) which benefit from transistors that can handle high peak current densities, high voltage swings and semi-insulating substrates aimed at microwave circuit designs. The desire to integrate system-on-a-chip (SOC) solutions has been pushing the development of microwave circuits to silicon processes, however the power amplifier is typically one of the most difficult things to integrate due to its physical size, high power consumption and relatively high power dissipation. This thesis looks at the design of a power amplifier covering all of X-band with at least 20 dBm of output power in a SiGe BiCMOS process.

Chapter one describes previous amplifiers designed in CMOS and BiCMOS for the microwave and millimeter wave bands.

Chapter two looks at the operation of power amplifiers and the tradeoffs between different amplifier classes and topologies. Additionally, design metrics used for the classification of power amplifiers are also discussed.

Chapter three looks at the design of a class AB power amplifier for X-band. The topology and circuit design are discussed along with the sizing considerations for the design.

Chapter four looks at the design of the planar transformers for the input and output matching networks, along with the simulated results.

Chapter five contains the circuit simulation and measurement results of the amplifier. Large signal and small signal S-parameters, power added efficiency, power output and stability are shown.

Chapter six gives a small summary of the power amplifier work with a summary of the results.

## **1.1 X-Band Applications**

The main application areas that will be examined within X-band are radar systems and communication links. Both of these applications typically require a power amplifier to meet the criteria of a given link budget. Radar systems are used to estimate the range and speed of targets, and in some cases identify the targets through microwave imaging. Communications systems are used for transferring information from a source to a destination.

### **1.1.1 Radar**

Modern digital phased array radar systems are beginning to push the boundary between the RF and digital domain to array or sub-array elements. Each sub-array system must have a full transmitter and receiver including the high speed analog to digital converters (ADC) and digital to analog converters (DAC). Data from each of



the elements is converted to the digital domain and is processed at a central data processor to implement digital beamforming. Figure 1-1 shows a typical radar transmit receive element containing a double conversion receiver and transmitter architecture. The PA is located closest to the antenna before the transmit-receive switch.

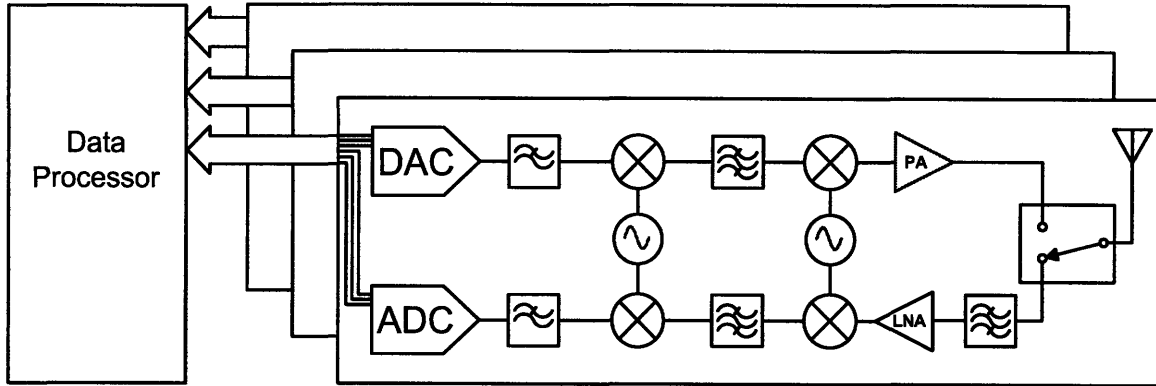


Figure 1-1: A phased array radar system with transmitter and receiver at the subarray level.

Transmitted radar waveforms are typically constant envelope, such as chirped frequency modulation (FM), or phased coded, and thus do not require a linear amplifier. Therefore, a linear or non-linear class of amplifier can be chosen for this application.

### 1.1.2 Communication Systems

Communication systems carry information from transmitter to receiver and can carry a given amount of information depending on the modulation and allowed bandwidth. These modulations come in all flavors - linear (envelope varying) and constant envelope type. Thus, in order to support all possible modulations it is would be necessary to use a linear power amplifier. However, if the use of a non-linear amplifier is desired, envelope elimination and restoration (EER) developed by Kahn [1], can be used in a polar loop transmitter. Originally developed in the early 1950's for adapting class C amplifiers for use with single-sideband, an EER system works as follows: The signal is split into two paths; one path is hard-limited so only the phase information remains, and the other is AM detected to isolate the envelope of the signal. The phase information drives the input of the amplifier, while the envelope information is used to

drive a modulator which modulates the power supply rail of the amplifier. By doing this, the output is a linearly amplified copy of the input.

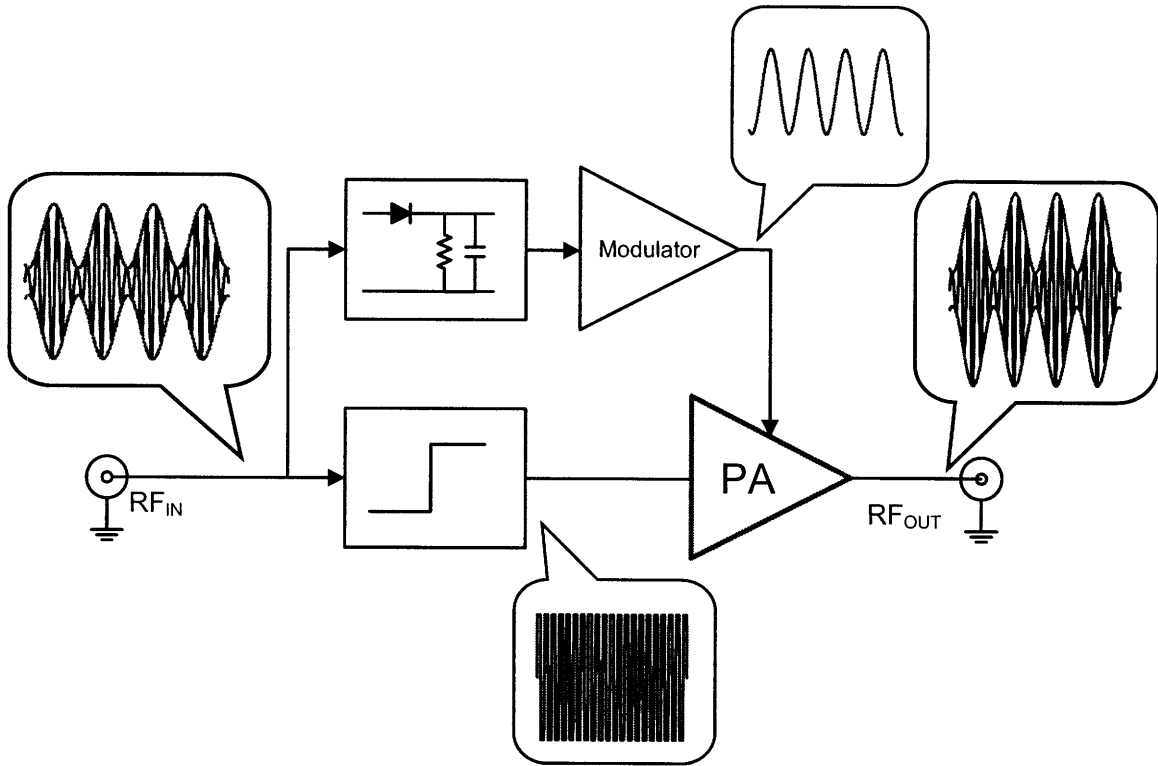


Figure 1-2: An simplified diagram of an envelope elimination and restoration system.

When used with a non-linear amplifier, using an EER system in effect linearizes the output. When used with a linear type of amplifier, modulating the power supply rail improves the efficiency of the amplifier at the low end of the range of output power.

## 1.2 Previous Work

Microwave and millimeter-wave design of power amplifiers is a well establish field, and numerous designs exist ranging from multi-kilowatt klystron designs [2] to high performance solid state amplifiers in III-V materials such as Indium Phosphide (InP) [3] and Gallium Arsenide (GaAs) [4]. However, in the X-band frequency spectrum and above, SiGe BiCMOS designs have not been widely explored. Designs in the

past can be put into two distinct groups for discussion - single ended designs and differential (balanced) designs.

### 1.2.1 Single Ended Amplifier Designs

Andrews et al [5], presented a two stage single-ended amplifier covering 8.5 to 10.5 GHz in a 200 GHz  $f_T$  process. The design utilized a two stage cascoded design to overcome the devices breakdown voltage of 3 volts. The power amplifier achieved a gain of 41 dB, maximum PAE of 26 % and saturated output power of 21.4 dBm. Impedance matching was accomplished using a combination of lumped capacitors and inductors along with transmission line structures. Total die size is 1.1 mm x 1.2 mm.

Komijani and Hajimiri [6] presented a four stage amplifier for 77 GHz applications in a SiGe process with an  $f_T$  of 200 GHz. The design made use of microstrip matching sections along with lumped capacitors for impedance matching. The transmission line consisted of side shields and a ground plane which shielded the microstrip from the lossy substrate in an attempt to prevent lossy substrate coupling. All stages are common emitter types biased for class AB operation. The devices exhibit a collector emitter breakdown voltage,  $BV_{CEO}$  of approximately 1.7 volts which is a limiting factor in selecting the power supply voltage. To get around this, a base resistance of 300 Ohms was used which raises the effective breakdown voltage closer to  $BV_{CER}$ , approximately 4 volts. The amplifier achieved a power gain of 17 dB, saturated output power of 17 dBm, peak PAE of 12.8 % and a 3 dB bandwidth of 15 GHz. Total die size is 1.35 mm x 0.45 mm.

### 1.2.2 Differential Amplifier Designs

Bakalski et al [7], presented a two stage differential amplifier covering 7-18 GHz. The SiGe based design utilized a 0.35 um process with an  $f_T$  of 75 GHz. Planar transformers were employed at the input to the amplifier and at the interstage match. The output matching network consisted of a LC-balun constructed with lumped inductors and capacitors. The balun and one additional inductor formed the collector

DC feed network. Each stage consisted of push-pull devices, in a common emitter configuration. The matching transformers were multi-turn designs, with the primary and secondary interwound on adjacent metal layers. The input transformer achieved a reported coupling coefficient of  $k = 0.45$ . The interstage matching transformer has a reported coupling coefficient of  $k = 0.6$ . At 2.4 volts, the amplifier delivered 17.5 dBm, has a PAE of 11 % and a gain of approximately 9 dB. Total die size is 0.8 mm x 0.9 mm.

Walling and Allstot [8] presented a similar amplifier to Bakalski. The two stage design covered 7-12 GHz while using cascoded push-pull pair for each of the stages. Input and interstage matching was accomplished using planar transformers, while the output matching network was implemented using an on chip LC-balun. Somewhat different than the design by Bakalski, the LC-balun used here did not serve as part of the DC collector feed network to the devices. Instead, the LC-balun is DC isolated using blocking capacitors, and microstrip lines were used on each collector for DC biasing. The driver stage is biased at the base and collector using the center tap from the input and interstage transformer respectively. At a power supply voltage of 3.8 volts the amplifier achieved a power output of 25.5 dBm, power gain of 20 dB and a peak PAE of 35 %. Total die size is 1.5 mm x 1.0 mm.

Haldi et al [9], presented a 5.8 GHz differential amplifier in a 90 nm CMOS process. The design utilized 4 differential stages arranged in a distributed active transformer topology (DAT). In this structure all of the 4 amplifiers are excited at the same level, and the outputs combined in a transformer which effectively sums the voltage from each amplifier. At the center frequency, the combining transformer achieved a maximum efficiency of 75 %. The transformer is unique in that the primary winding is present on both sides of the secondary winding. This results in a uniform current distribution on the secondary winding, causing lower loss than traditional designs. The amplifier achieved a maximum output power of 24.3 dBm, a power gain of 8 dB and peak drain efficiency of 27 %. Total die size is 0.9 mm x 0.9 mm.

Pfeiffer et al [10], presented a single stage class AB power amplifier for 60 GHz. The SiGe based design was fabricated in a 0.12  $\mu\text{m}$  process with an  $f_T$  of 200 GHz.

Table 1.1: Previous Work Summary

Authors	Freq (GHz)	Psat (dBm)	Gain (dB)	Peak PAE (%)	Size (mm <sup>2</sup> )
Andrews et al. [5]	8.5-10	21.4	41	26	1.32
Komijani et al. [6]	77	17	17	12.8	0.61
Bakalski et al. [7]	7-18	17.5	9	11	0.72
Walling et al. [8]	7-12	25.5	20	35	1.5
Haldi et al. [9]	5.8	24.3	8	23	0.81
Pfeiffer et al. [10]	60	14	12	4.2	0.625
Chang et al. [11]	26-40	19.4	13	11.2	1.82

The amplifier utilized transmission line matching at the input circuit, while a planar transformer is used at the output. The transformer was made using overlapping slabs on adjacent metal layers and employed a ground-shield to prevent excessive substrate loss. The transformer achieved a coupling coefficient of  $k = 0.8$ . The amplifier was characterized in a differential manner using ground signal ground signal ground (GSGSG) probes at  $100 \Omega$  differential impedance. Utilizing a power supply voltage of 4 volts, the amplifier achieved a power gain of 12 dB, saturated output power of 14 dBm and a peak PAE of 4.2 %. Total die size is 0.5 mm x 1.25 mm.

Chang and Rebeiz [11] presented a two stage class AB amplifier for 26 GHz to 40 GHz. The SiGe design was fabricated in a 0.13 um process with an  $f_T$  of 200 GHz. The amplifier utilizes microstrip transmission lines and lumped capacitors for input, interstage and output matching. To overcome the low  $BV_{CEO}$  of the process, the bases of the devices in the two common emitter stages were presented with  $40 \Omega$  at DC and lower than  $20 \Omega$  from 26 to 40 GHz. The amplifier is measured in a fully differential mode using GSGSG probes and was powered from a 1.4 volt power supply. The amplifier has a peak saturated output power of 19.4 dBm, peak small signal gain of 13 dB, and peak PAE of 11.2 %. Total die size is 0.75 mm x 2.43 mm.



# Chapter 2

## Power Amplifier Operation

The design of power amplifiers is not a straight forward process. A specific design criteria will largely shape the topology and methods used to form the power amplifier. Depending on the application that the amplifier is being designed for, different criteria will be weighed more heavily. It is common that some design criteria will oppose each other, necessitating the need for compromise.

This section first looks at design metrics used to classify power amplifiers. Next, single ended and differential amplifier operation are examined along with benefits and tradeoffs associated with each. Lastly linear classes of power amplifiers are examined, and the effects of bias point on different amplifier parameters.

### 2.1 Power Amplifier Design Criteria

#### 2.1.1 Scattering Parameters

In order to be classified as a amplifier, the device under question must be able to take in a signal of some amplitude and output a amplified replica of the signal. When classifying the gain of an amplifier it is common to refer to this in terms of the amplifier's S-parameters. For a given black box, with some internal structure and N ports, we can define the relationship between each of the terminals when an excitation source is applied to one terminal. For example, taking a two port network

and applying an excitation source at port one, and measuring the outward traveling component at port 2,  $S_{21}$ , also know as forward transmission would be obtained.

$$S_{11} = V_1^-/V_1^+, V_2^+ = 0 \quad (2.1)$$

$$S_{12} = V_1^-/V_2^+, V_1^+ = 0 \quad (2.2)$$

$$S_{22} = V_2^-/V_2^+, V_1^+ = 0 \quad (2.3)$$

$$S_{21} = V_2^-/V_1^+, V_2^+ = 0 \quad (2.4)$$

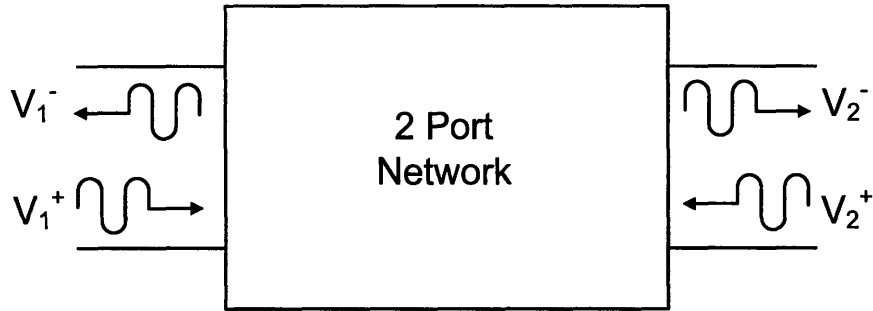


Figure 2-1: A two port network with incident and reflected waves.

While we have limited our discussion to two port networks, S-parameters can be applied to any network with up to N ports. In the context of power amplifiers, scattering parameters can be measured under two conditions: small-signal and large-signal. Small signal S-parameters are measured when the amplifier is operating in a small signal linear region. In this mode the devices are not being excited with a large amplitude. When the input power is increased, the output power increases which typically causes the output impedance of amplifier to decrease. Therefore, it is common to measure  $S_{22}$  under “hot” conditions. By this, we mean the output impedance of the amplifier is measured while an excitation signal is applied to the input of the amplifier. Under large signal conditions the active devices start to operate in a non-linear region, and thus S-parameters become a function of input power.



## 2.1.2 Measurements of Efficiency

Since an amplifier is nothing more than an energy conversion device, metrics exist to classify how well an amplifier can convert DC power to radio frequency energy. A simple measurement efficiency is simply collector efficiency (Bipolar Designs) or drain efficiency (for designs with FET's). This is simply the ratio of output power to DC input power.

$$\eta = \frac{P_{OUT}}{P_{DC}} \quad (2.5)$$

While this is informative, it is possible that we can have an amplifier with a very small gain with exceptionally high collector efficiency. Thus, a means to take into account the gain of the amplifier is desirable when comparing efficiencies of different amplifiers. A measurement off efficiency which also takes into account the input power is power added efficiency (PAE).

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} \quad (2.6)$$

For the example above, an amplifier with relatively low gain, but high collector efficiency would have relatively low PAE. At the other extreme, as gain grows large relative to output power, PAE approaches collector efficiency.

## 2.1.3 Measurements of Bandwidth

The operational bandwidth of an amplifier is also an important parameter to consider in the design process. Several metrics exist to quantify bandwidth. The simplest, 3 dB bandwidth, is the difference of the frequencies in which the power gain of an amplifier is down 3 dB from its peak value. Similar to S-parameters and efficiency, bandwidth is highly dependant on excitation level especially when driving an amplifier into a non-linear region of operation. Thus, measurements are typically made under small-signal, and large-signal conditions.

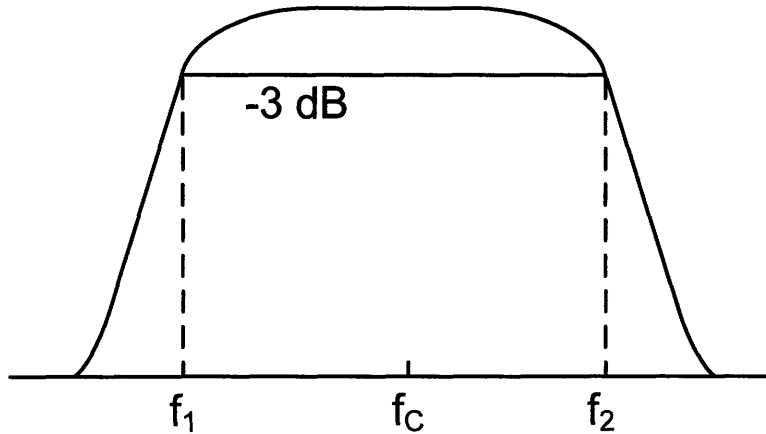


Figure 2-2: Amplifier gain response with 3 dB points.

The other metric that is often referenced when talking about bandwidth is fractional bandwidth. If we consider two different amplifiers with different center frequencies, they may have the same absolute (3 dB) bandwidth. However, when comparing the two we need some way to normalize the bandwidth with respect to its center frequency. Thus, fractional bandwidth is defined as the absolute bandwidth (3 dB) divided by its center frequency.

$$\text{Fractional BW} = \frac{f_2 - f_1}{f_c} \quad (2.7)$$

### 2.1.4 Measurements of Linearity

In the case of a system where we have signals with time-varying envelopes, the linearity of the power amplifier is important. Linearity is a measure of the ability of the amplifier to take an input signal and produce an amplified replica as closely as possible. Inherent to any power amplifier, due to circuit and device constraints, only a finite amount of power can be produced before a limit is reached. At this limit, the amplifier is said to be “saturated.” Around the region of saturation the behavior of the amplifier can best be described as still having usable gain, but this gain is decreasing with increasing input power. To model this behavior, a simple polynomial can be fit to the curve describing an amplifiers transfer characteristic from input to output.

$$V_{OUT} = AV_{IN} + BV_{IN}^2 + CV_{IN}^3 + DV_{IN}^4 + \dots \quad (2.8)$$

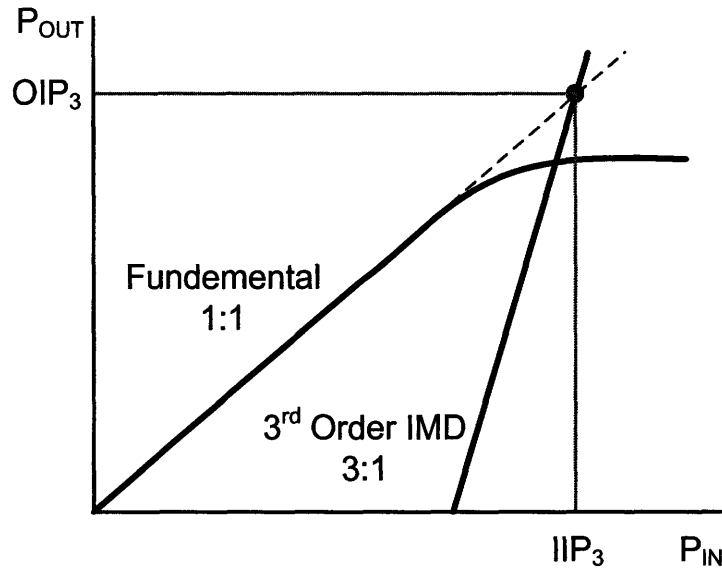


Figure 2-3: Amplifier input to output transfer characteristic for fundamental tones and 3rd order IMD tones.

The coefficients on the independent variable are determined by the level of non-linearity in the amplifier. In the case of a single-tone, the output of the amplifier will consist of the fundamental tone in addition to harmonics of the fundamental at lower amplitudes. To quantify this, the amplitude of the harmonic is compared to the fundamental tone and is expressed in units of dBc, decibels relative to the fundamental carrier.

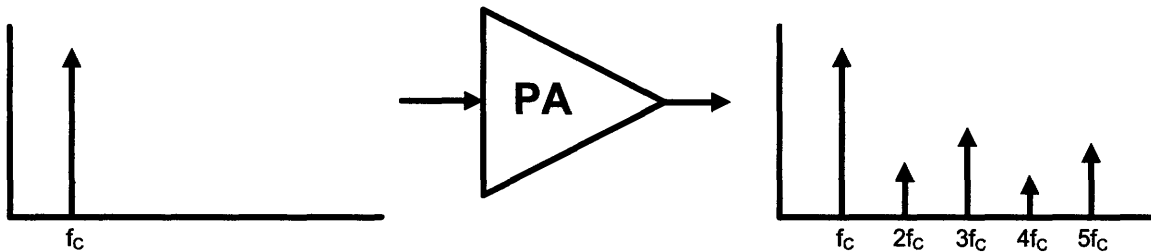


Figure 2-4: Amplifier input and output spectrum for the case of a single tone input.

When a multi-tone signal is used to excite an amplifier, intermodulation products are formed as a result of the odd ordered terms in the polynomial expansion describing

the amplifiers transfer characteristic. Assuming two equal input tones of  $f_1$  and  $f_2$ , the output signal in the region of the fundamental consists of the two original tones in addition to new tones spaced on each side of the fundamentals by  $|f_2 - f_1|$ . Similar to the single tone case, with a multi-tone input replicas of the signal in the fundamental region are also contained at integer multiples of the input center frequency.

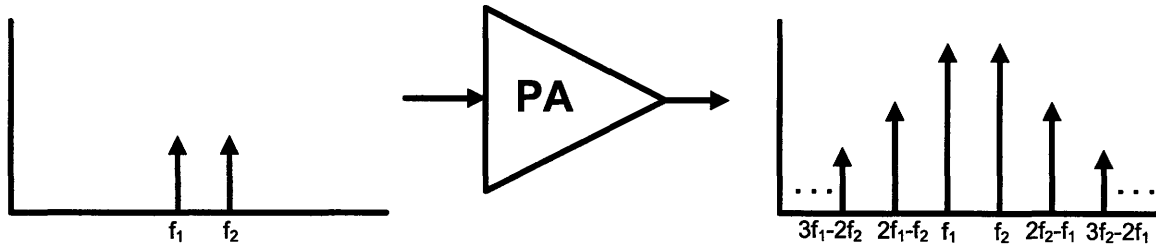


Figure 2-5: Amplifier input and output spectrum for the case of a multi-tone input signal.

Typically the degree of the non-linearity is characterized by the 3rd order intermodulation products amplitude relative to the fundamental input tones. This measurement is typically taken with the output level of the fundamental tones set to approximately six dB below the peak output level for the single tone case so as to keep the peak value of the RF time domain signal the same. In theory, for every one dB increase in the fundamental tones, the magnitude of the 3rd order intermodulation products will increase by 3 dB. Theoretically, though physically impossible, at some output level the 3rd order intermodulation products will be the same amplitude as the fundamental tones. This point is referred to as the output 3rd order intercept point and is commonly used to compare the relative linearity of different amplifiers.

### 2.1.5 Stability Concerns

The stability of an amplifier is a measure of its ability to resist oscillation. The combination of a high gain element and several parasitic feedback paths produce the potential for an amplifier to oscillate. There are three general terms to aid in describing an amplifiers stability: Unconditionally stable, conditionally stable and unstable. For an amplifier to be unconditionally stable, when presented with any

combination of source and load impedance, the amplifier must not oscillate. For conditional stability, the amplifier is stable for most load and source impedances however it may oscillate for certain load or source impedances. An unstable amplifier oscillates for all source and load impedances and it better refereed to as an oscillator. Using S-parameters it is possible to put bounds on the criteria necessary for stability.

$$\begin{vmatrix} V_1^- \\ V_2^- \end{vmatrix} = \begin{vmatrix} S_{11}S_{12} \\ S_{21}S_{22} \end{vmatrix} \begin{vmatrix} V_1^+ \\ V_2^+ \end{vmatrix}$$

Using the first two rows of the S matrix, we can write the input and output reflection coefficients as a function of the S matrix and the source and load reflection coefficients. For stability, each of these quantities must be less than one to assure that for a given input signal to any port, the reflected signal from that same port is smaller in magnitude. Following the analysis found in [12] we get:

$$|\Gamma_{IN}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \quad (2.9)$$

$$|\Gamma_{OUT}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \quad (2.10)$$

Where  $\Gamma_L$  and  $\Gamma_S$ , the load and source reflection coefficients are defined as:

$$\Gamma_L = \frac{Z_L - Z_O}{Z_L + Z_O} \quad (2.11)$$

$$\Gamma_S = \frac{Z_S - Z_O}{Z_S + Z_O} \quad (2.12)$$

Using the conditions above, it can shown as in [12], the following condition must hold true for unconditional stability.

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \quad (2.13)$$

Where  $\Delta$  is the determinant of the S-matrix.

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (2.14)$$

## 2.2 Single Ended vs. Differential

There are several different ways to break power amplifiers into different hierarchies. One classification is that of single ended versus differential. This designation refers to the terminals and internal construction of the amplifier. A single ended device uses ground as a reference point in which to reference all potentials. In contrast, a differential device always refers to potentials as the difference in voltage between two points that are elevated from ground by some amount which can in theory be an arbitrary value.

Within the context of power amplifiers the difference in single ended and differential topologies may seem subtle at first, but they have many ramifications on the design process and performance of the amplifier both in simulation and measurement.

### 2.2.1 Single Ended Topologies

For simplicity consider one method of constructing a single ended amplifier stage. It should be noted that this is not the only way to construct a single ended RF amplifier, nor is it the best way. The single ended amplifier can be broken down into three main parts - input matching, device selection, and output matching.

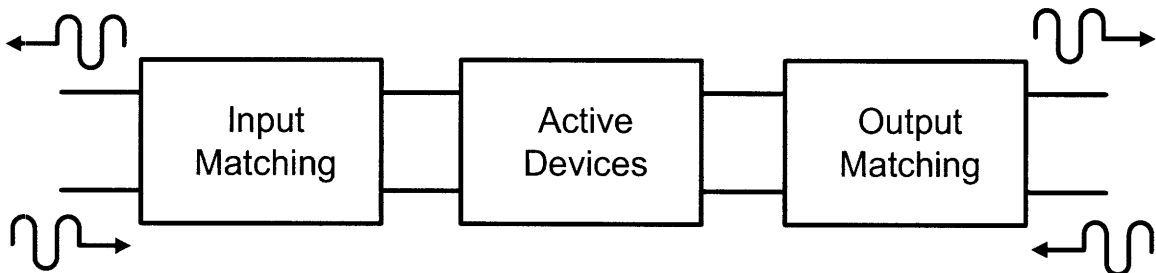


Figure 2-6: The major parts of an amplifier: input matching, active devices, and output matching.

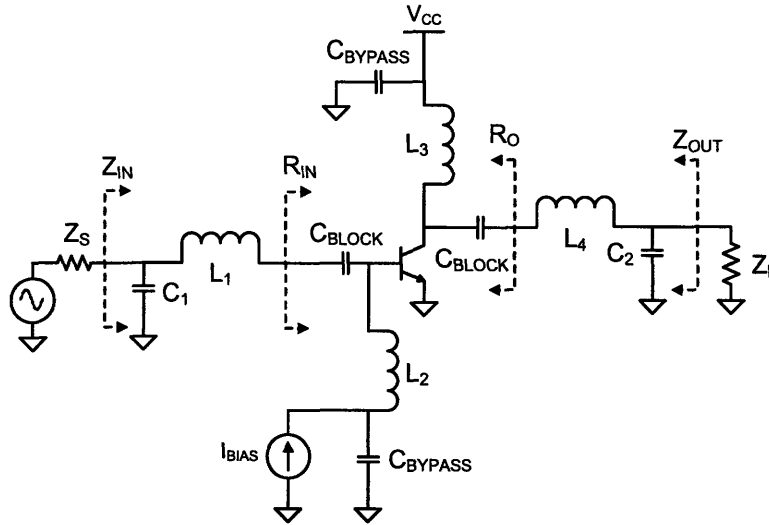


Figure 2-7: A single ended common emitter bipolar amplifier topology.

The operation of the single ended amplifier can be analyzed as follows: Assuming a sinusoidal input to the base of the transistor, the device will start to conduct. If we make the assumption that the transistor can turn on with zero voltage drop across its collector emitter junction, the output voltage will sinusoidally drop to zero at the collector of the device. As the input starts to decrease and go negative, the device conducts less, and the voltage at the collector starts to rise. Since the average voltage across the inductor during one cycle must be zero (assuming the magnitude of its inductive reactance is large compared to  $R_O$ ), on the crest of the sinusoidal output, the voltage reaches  $2V_{CC}$ . We now know the peak voltage across the collector emitter junction, and with this knowledge we can compute the real part of the impedance looking into the collector  $R_O$  for a given power level,  $P_O$ .

By definition, the power across some resistance R is defined as:

$$P_O = \frac{V_{RMS}^2}{R} \quad (2.15)$$

Using the peak to peak value of the sinusoid at the collector of  $2V_{CC}$ , we get the power output as a function of the voltage and resistance:

$$P_O = \frac{V_{CC}^2}{2R_O} \implies R_O = \frac{V_{CC}^2}{2P_O} \quad (2.16)$$

Knowing the peak voltage, the peak current can be written as:

$$I_{PEAK} = \frac{2V_{CC}}{R_O} = \frac{4P_O}{V_{CC}} \quad (2.17)$$

Thus, the devices must be sized such that the collector emitter junction can handle at least  $2V_{CC}$  without breaking down, and be capable of supporting at least the peak current. In practice these values are slightly lower due to the finite forward drop across the collector emitter junction while conducting.

The other main parts of a simple single ended design include the blocking capacitors, used for keeping DC current from flowing into the source and load from the bias network and DC feed respectively. The other main components include lumped elements  $L_1$ ,  $C_2$ , and  $L_4$ ,  $C_2$ . These each form impedance matching networks for matching the relatively low impedance of the base and collector nodes to a nominal source and load impedance (usually  $50 \Omega$ ). Operation of the L network is readily evident by examining the Smith chart. Starting at the load side,  $Z_L$ , capacitor  $C_2$  decreases the magnitude of the impedance until the real part is equal to  $R_O$ . Series inductor  $L_4$  then cancels out the capacitive reactance caused by the shunt capacitor.

Evident from the Q-arcs plotted on the smith chart, the loaded Quality factor of the network is entirely dependant on the impedance of the source and load. Thus as the impedance ratio increases, the bandwidth of the amplifier decreases with increasing loaded Q. Another negative effect of the high Q network is the sensitivity to component values. A small relative shift in component value will have a very large effect on the center frequency of the amplifier.

While the design of the single ended stage looks simple, several caveats exist. First, if a large quantity of power is desired from a single ended stage, the output impedance of the device will be extremely low, making matching very difficult over a wide frequency range. Secondly, the operational parameters of the single ended amplifier are highly influenced by the layout of the amplifier. Since the RF current flows directly through the ground path connecting the active device, matching network and output load, care needs to be taken to either insure that the ground path is as



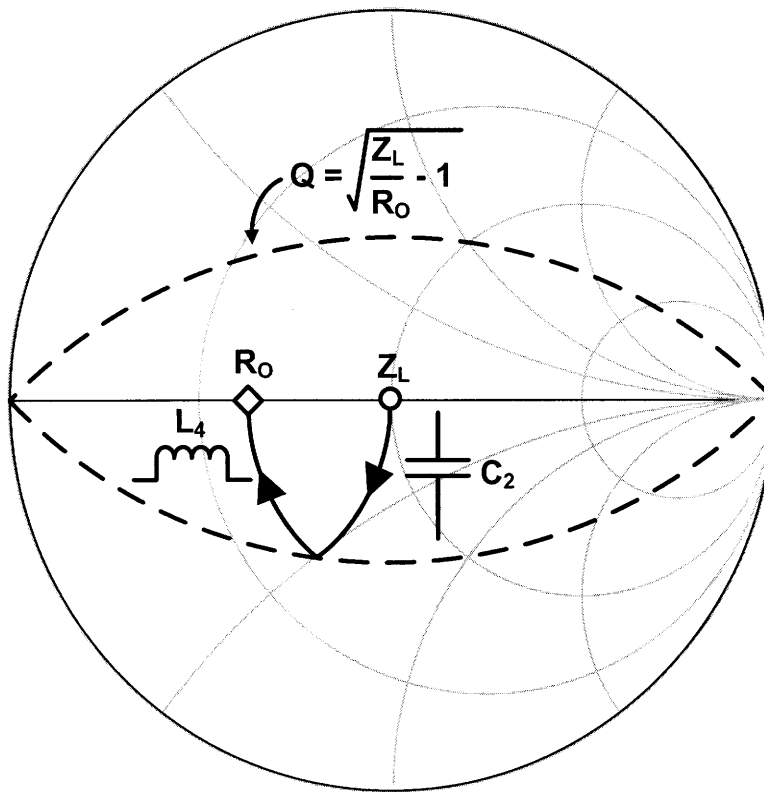


Figure 2-8: Smith chart showing a low pass step down network.

small as possible, or spend time characterizing the ground interconnect. This is unlike the differential topology discussed in the next section which is inherently free off grounding since none of the RF signal current flows through the common DC ground, (excluding even order harmonic distortion).

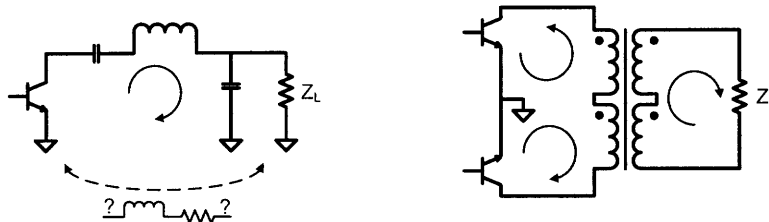


Figure 2-9: Single ended and differential amplifier topologies showing the flow of RF signal current.

## 2.2.2 Differential Topologies

The basic differential amplifier can be thought of as two single ended amplifiers that are excited 180 degrees out of phase and their outputs combined together. By symmetry, the center taps of the transformer are always at zero volts RF potential, and thus from an RF perspective they are virtual grounds. This aids in the bias network and DC feed of the amplifier. Unlike the single-ended amplifier which requires a bias choke at the base of the devices, the differential amplifier can be biased directly at the center-tap of the input transformer without the need for any choke. At the collector side, the same thing can be done with the output transformer.

Examining the operation of the differential amplifier found in Figure 2-10, and assuming class B operation (described later in section 2.3), only one of the devices is conducting for each RF half cycle. If a sinusoidal excitation is applied to the bases of the transistors, the top device first turns on and places  $V_{CC}$  across the top primary winding of the output transformer. By transformer action,  $-V_{CC}$  is also inductively coupled into the lower primary winding of the transformer with respect to ground. On the negative half of the RF cycle when the lower device conducts, the polarity of voltage across the transformer is now reversed while the magnitude is the same.

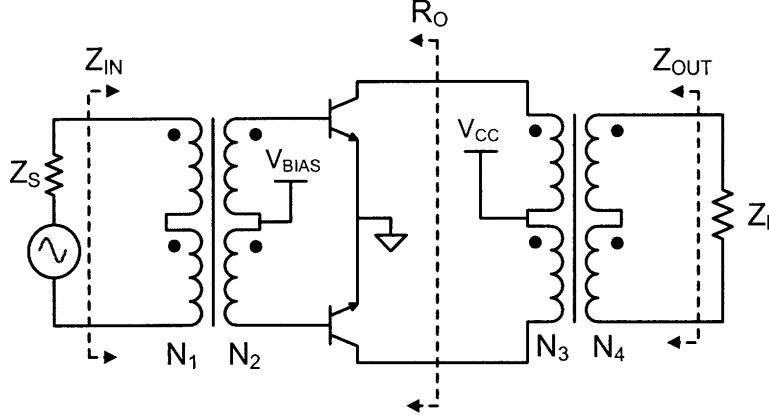


Figure 2-10: A transformer coupled differential amplifier.

Thus, for a full RF cycle the voltage across the primary of the transformer has a peak to peak value of  $4V_{CC}$ . From this, the power  $P_O$  and the output resistance  $R_O$  can be related.

$$P_O = \frac{2V_{CC}^2}{R_O} \implies R_O = \frac{2V_{CC}^2}{P_O} \quad (2.18)$$

Knowing the peak voltage and resistance, we can write the peak current (per device):

$$I_{PEAK} = \frac{2V_{CC}}{R_O} = \frac{P_O}{V_{CC}} \quad (2.19)$$

Comparing this to 2.16, for a given voltage and power output, a differential topology has 4 times the output resistance as compared to a single-ended stage. This is a very important element to keep in mind when considering the impedance matching network. Comparing the peak current from 2.17 of the single ended amplifier, the peak current for a single device in the differential pair is 4 times lower.

Now that the output resistance looking into the collectors is known, values for the number of turns in the transformer windings,  $N_3$  and  $N_4$  can be selected. Making the very crude assumption that the power lost through the transformer is minimal, and that the power is proportional to voltage squared, the impedance ratio of the transformer,  $N_4 : N_3$ , can be written as:

$$N_4 : N_3 = \sqrt{\frac{Z_L}{R_O}} \quad (2.20)$$

Equation (2.20) assumes the transformer has a coupling coefficient ( $k$ ) of 1, which at microwave frequencies is not realistic. Chapter 4 will further address the design of transformers at microwave frequencies.

## 2.3 Linear Classes of Operation : Your Basic ABC's

In the family of linear amplifiers, there exist 4 main distinct operational classes: A, AB, B, and C. The main distinction that separates each of the devices is the fraction of the RF input cycle which the active devices conduct. Starting with class A, the device conducts for the full RF cycle, and decreases as we go towards class C. As we decrease the conduction angle, linearity and gain decrease while efficiency increases.

Table 2.1: Linear Amplifier Classes

Amplifier Class	Conduction Angle ( $\theta$ )	Max Efficiency (%)	Gain
A	$360^\circ$	50	Highest
AB	$180^\circ < \theta < 360^\circ$	$50 < \theta < 78.5$	High
B	$180^\circ$	78.5	Medium
C	$\theta < 180^\circ$	100	Low

In general for linear amplifier classes operating in class A, AB, B or C, the efficiency and overall power output can be written as a function of the conduction angle,  $\theta$  as given in [13].

$$\eta = \frac{\theta - \sin\theta}{4\sin(\frac{\theta}{2}) - 2\theta\cos(\frac{\theta}{2})} \quad (2.21)$$

$$P_O = \frac{V_{CC}I_{MAX}}{4\pi} \frac{\theta - \sin\theta}{1 - \cos(\frac{\theta}{2})} \quad (2.22)$$

Figure 2-11 shows a graphical representation of Equations (2.21) and (2.22). Equations (2.21) and (2.22) assume that the device and matching networks are ideal. This

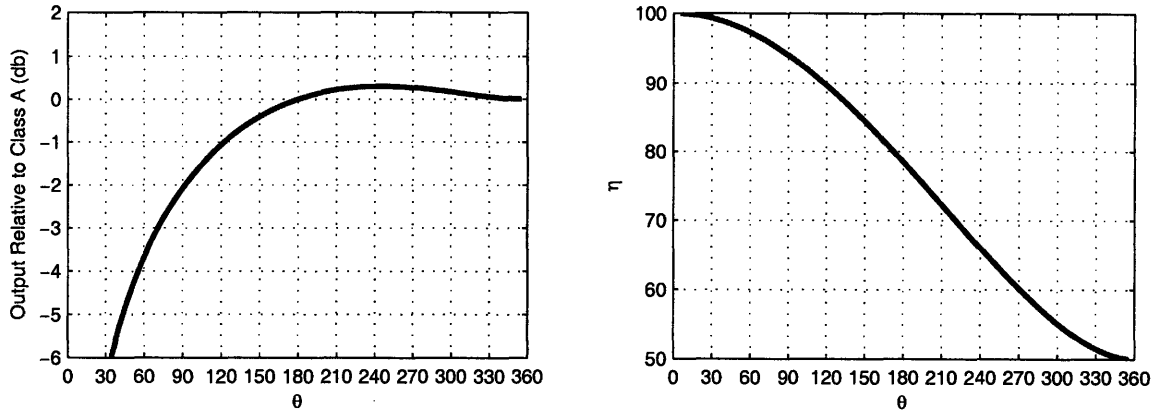


Figure 2-11: The effects of conduction angle on efficiency and power output for linear amplifier classes.

is hardly the case, devices do not operate in a perfectly linear and efficient manner, nor are matching networks lossless. Thus, power outputs and efficiencies are typically much lower in practice.



# Chapter 3

## Class AB Amplifier Design

### 3.0.1 Design Specifications

A set of specifications for the amplifier were required as part of the intended application. The system was to use constant envelope signals, so no requirements were set on the linearity of the amplifier, making it possible to set a high goal for the amplifiers PAE. A summary of the performance requirements can be found in Table 3.1.

Table 3.1: Power Amplifier Design Objectives

Parameter	Goal	Units
Frequency Range	7 - 12	GHz
Power Gain	12	dB
Full-Scale Input Power	10	dBm
Full-Scale Output Power	22	dBm
Power Supply Voltage	1.8	Volts
Power Added Efficiency (PAE)	30	%
Input and Output Interface	Differential	-

### 3.0.2 Circuit Topology Selection

The choice of the circuit topology rested on the required amount of gain and the center frequency that the amplifier was to operate at. The intended application for the amplifier dictated that the amplifier have differential inputs and outputs. By

selecting a fully differential topology the need for critical modeling of the ground interconnect was eased. Additionally, as described in Chapter 2, for a given amount of output power, a differential structure has 4 times the output impedance to that of a single-ended amplifier. Thus, impedance matching over a wide-frequency range is much easier to accomplish.

The second design choice was whether to use a common emitter gain stage or a cascoded stage (common emitter and common source tied together). Using the common emitter would be the simplest method, however tuning would be somewhat of a challenge due to the non-unilateral nature of the device, caused by the feedback capacitance from collector to base. This causes the input and output matching to affect each other, making tuning an iterative process. The cascode configuration is approximately unilateral allowing the input and output network to be tuned independently. On the other hand, with the cascode the output collector of the cascode transistor cannot swing as close to ground, making the optimal load impedance lower than that of a common emitter stage for a given output power.

With these considerations in mind and the design requirements, it was decided to initially start with the common emitter topology. Had this not worked out, or the gain requirement not been met, the cascode would have been the next option to explore.

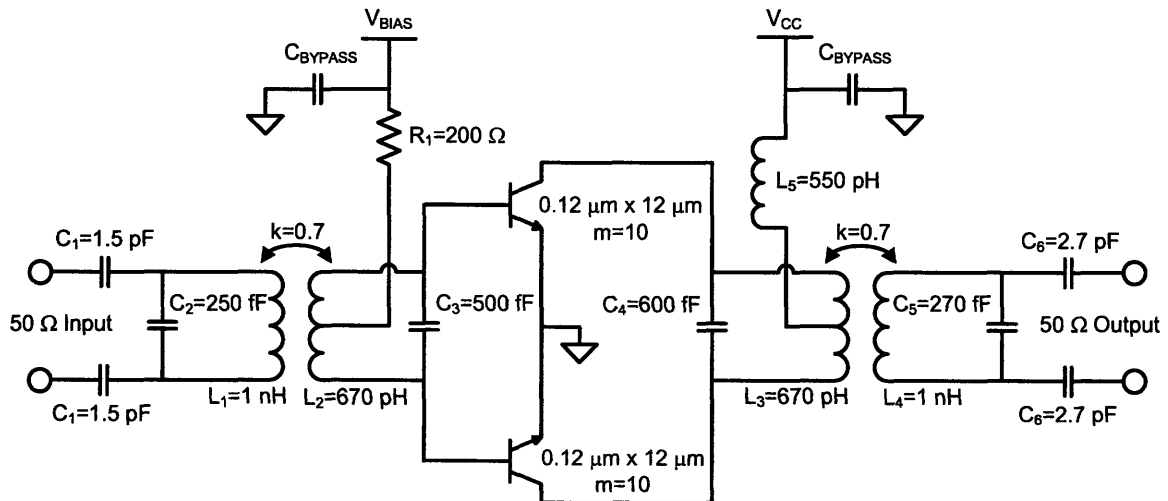


Figure 3-1: Schematic Diagram of the X-band power amplifier.



### 3.0.3 Active Device Sizing

The process technology used for the design has both bipolar transistors and FETs available to designers. Bipolar transistors were chosen over FETs for several reasons. First, for a given process the  $f_T$  of a bipolar transistor is much higher than a FET. For this process the  $f_T$  of the bipolar devices is 200 GHz while it is approximately 100 GHz for the FETs. Secondly, bipolars are more resistant to damage from breakdown voltage constraints and over current than FET devices. With FETs you must pay attention to the drain swing since there is the risk of puncturing the gate-oxide. As described in [14] and [15] the breakdown of a bipolar does not lead to permanent damage, and can be raised from  $BV_{CEO}$  closer to  $BV_{CBO}$  by providing a low impedance path to ground at the base of the device. To accomplish this, a resistance of 200  $\Omega$  was used at the base of the devices.

To pick the size and number of devices, several parametric sweeps were performed with different device sizes and load impedances to see what the maximum output power and efficiency were. In essence a quasi load-pull was performed, except the results were not plotted on Smith chart, but rather a regular two axes plot. These device size values are constrained by the requirement that the maximum current density of the devices cannot be exceeded.

Several device sizes, and finger numbers were tested into load impedances of 10  $\Omega$ , 15  $\Omega$ , 20  $\Omega$ , and 25  $\Omega$ . Results of these sweeps are shown in Figures 3-3, 3-4, 3-5 and 3-6. A negative capacitor was placed in parallel with the push-pull devices collector to find the optimal termination impedance. The input looking into the devices alone is the load line resistance with a slight amount of capacitive reactance. Sweeping the negative capacitor rotates the impedance coordinates about an arc of constant admittance on the Smith chart. Figure 3-2 shows a simplified schematic of the device selection simulation setup.

Plotted on a two axes plot - a plot of power out and efficiency versus capacitor values and power out versus efficiency are obtained. Points along the line represent different values of capacitance.

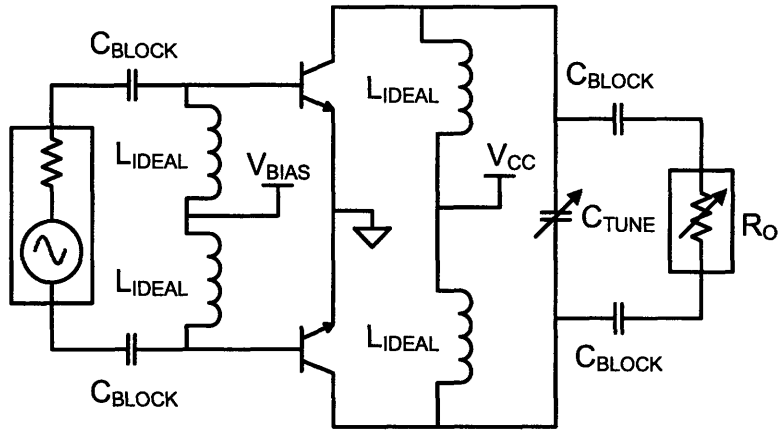


Figure 3-2: Schematic view of the simulation setup used to characterize the efficiency and output power of different devices.

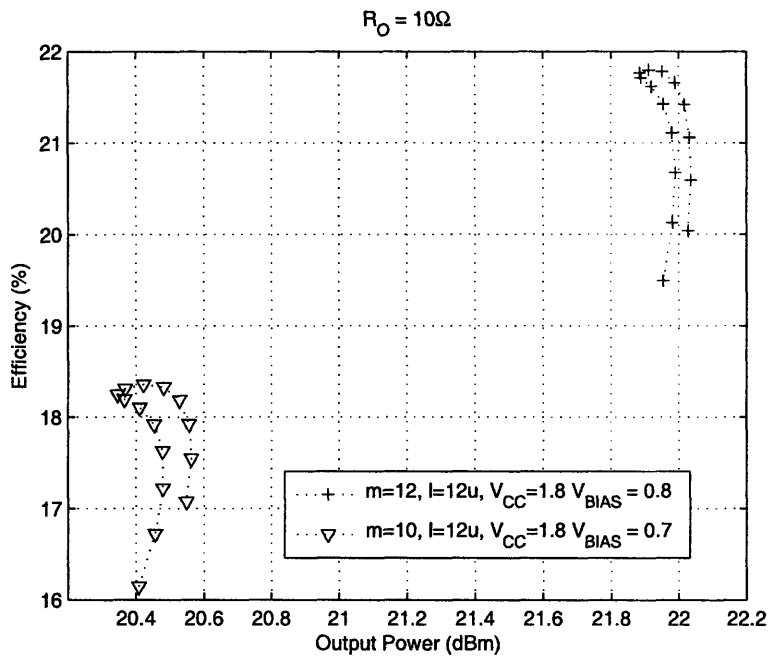


Figure 3-3: Efficiency and power output for various devices terminated into  $10 \Omega$ . The capacitor value varies from  $-1000 \text{ fF}$  to  $600 \text{ fF}$ .

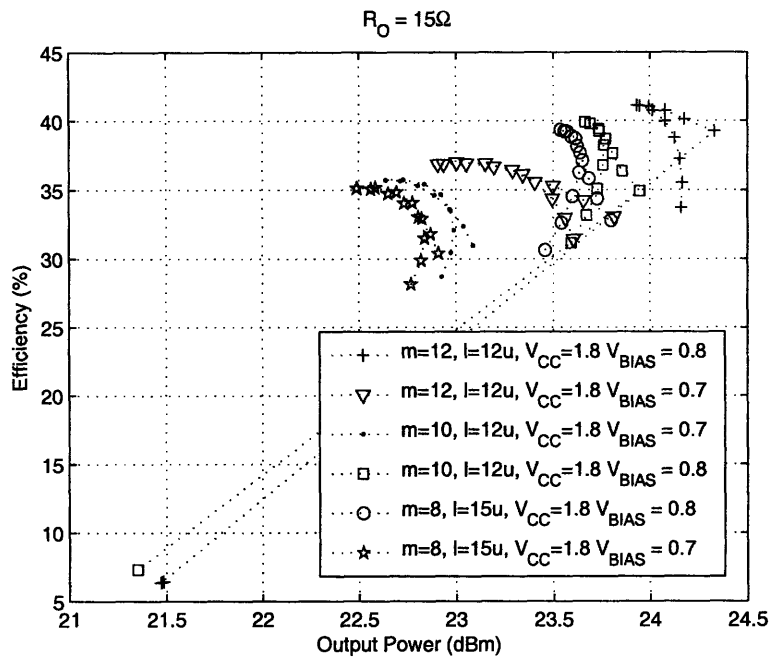


Figure 3-4: Efficiency and power output for various devices terminated into  $15\ \Omega$ . The capacitor value varies from  $-1000\ \text{fF}$  to  $600\ \text{fF}$ .

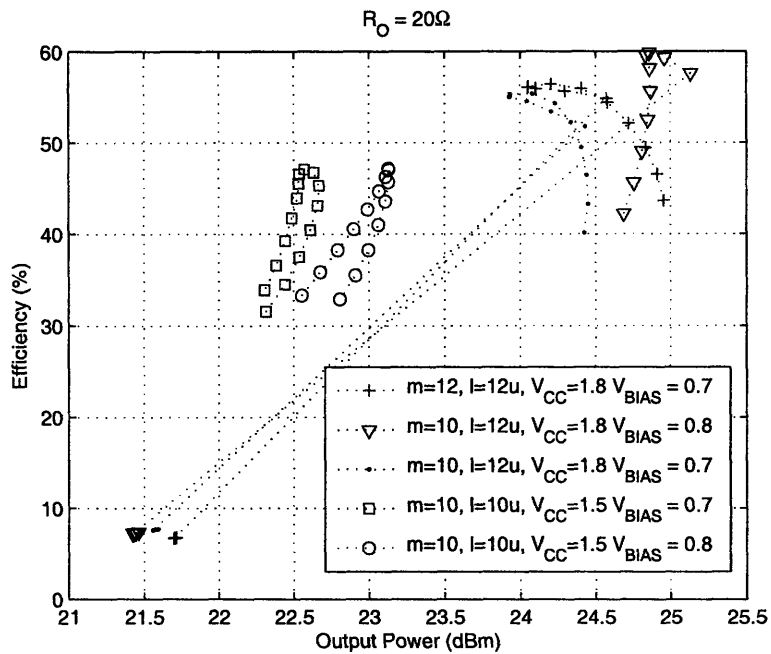


Figure 3-5: Efficiency and power output for various devices terminated into  $20\ \Omega$ . The capacitor value varies from  $-1000\ \text{fF}$  to  $600\ \text{fF}$ .

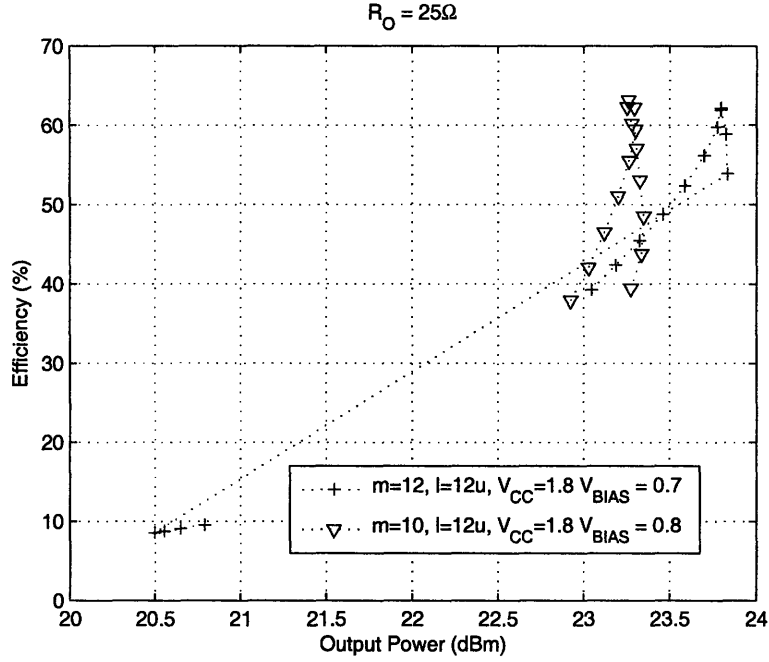


Figure 3-6: Efficiency and power output for various devices terminated into  $25 \Omega$ . The capacitor value varies from  $-1000 \text{ fF}$  to  $600 \text{ fF}$ .

For high efficiency and power output above  $20 \text{ dBm}$ , an emitter length of  $12 \text{ microns}$  was chosen, at power supply voltage of  $1.8 \text{ volts}$  and bias of  $0.8 \text{ volts}$ . Each side of the push pull pair has  $10$  of these devices in parallel to achieve the desired output power and current handling capability. The optimal impedance presented at the collectors was found to be approximately  $20 \Omega$ , while the capacitance was selected to be in the range of  $-300 \text{ fF}$  to  $0 \text{ fF}$ . This range yields suitable output power and efficiency while not being too sensitive to minor changes in capacitance. A more detailed plot of efficiency and power output of the selected device sizes can be seen in Figure 3-7.

Using Equation (2.18) from Chapter 2 we can also find a value of terminating resistance. In practice it is important to take into account the voltage drop across the collector emitter junction since it cannot swing all the way down the ground. Rewriting Equation (2.18) we get:

$$R_O = \frac{2(V_{CC} - V_{SAT})^2}{P_O} \quad (3.1)$$

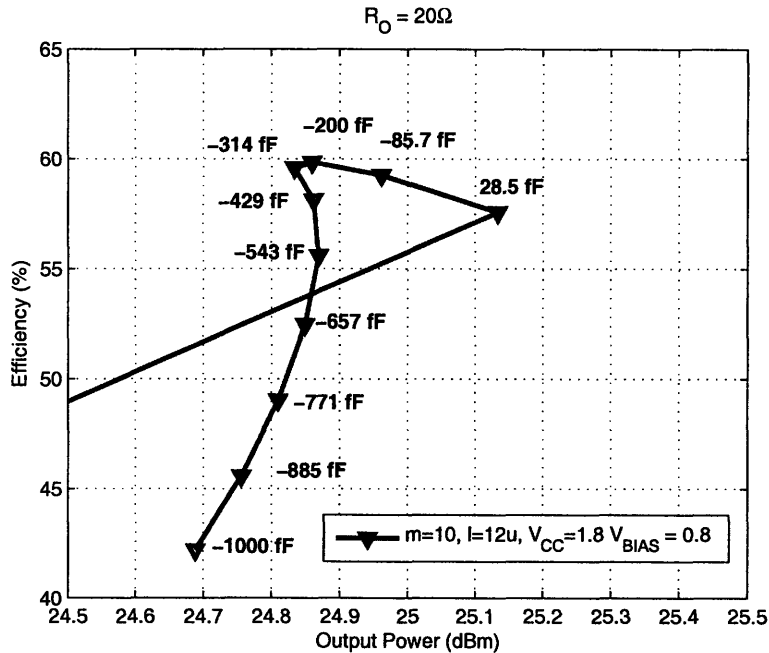


Figure 3-7: Efficiency and power output for the selected devices.

Assuming a supply voltage of 1.8 volts, saturated collector emitter voltage of 0.4 volts and 23 dBm output power we get a output resistance,  $R_O$  of  $19.6 \Omega$ , very close to that found by simulation.

### 3.0.4 Layout Considerations

The layout of the power amplifier is highly symmetric, simplifying things greatly. Redundant pads are used for the connection of power and ground. The power supply is supported by 5 separate pads while the grounding for DC current return is supported by 4 pads. Base bias voltage is brought in through a single pad.

A ground bus connects all of the interface pads and also surrounds a good part of the chip. While not affecting the performance of the amplifier at the fundamental, even harmonics of the amplifier are aided by the common grounding structure. A image of the amplifier from the layout editor can be seen in Figure 3-8.

Great care was also taken to assure that metal lines carrying high currents were sized appropriately. The power supply must support currents on the order of hundreds

of milliamperes, making it necessary to sandwich several layers of metal together to meet electromigration rules at 100° C.

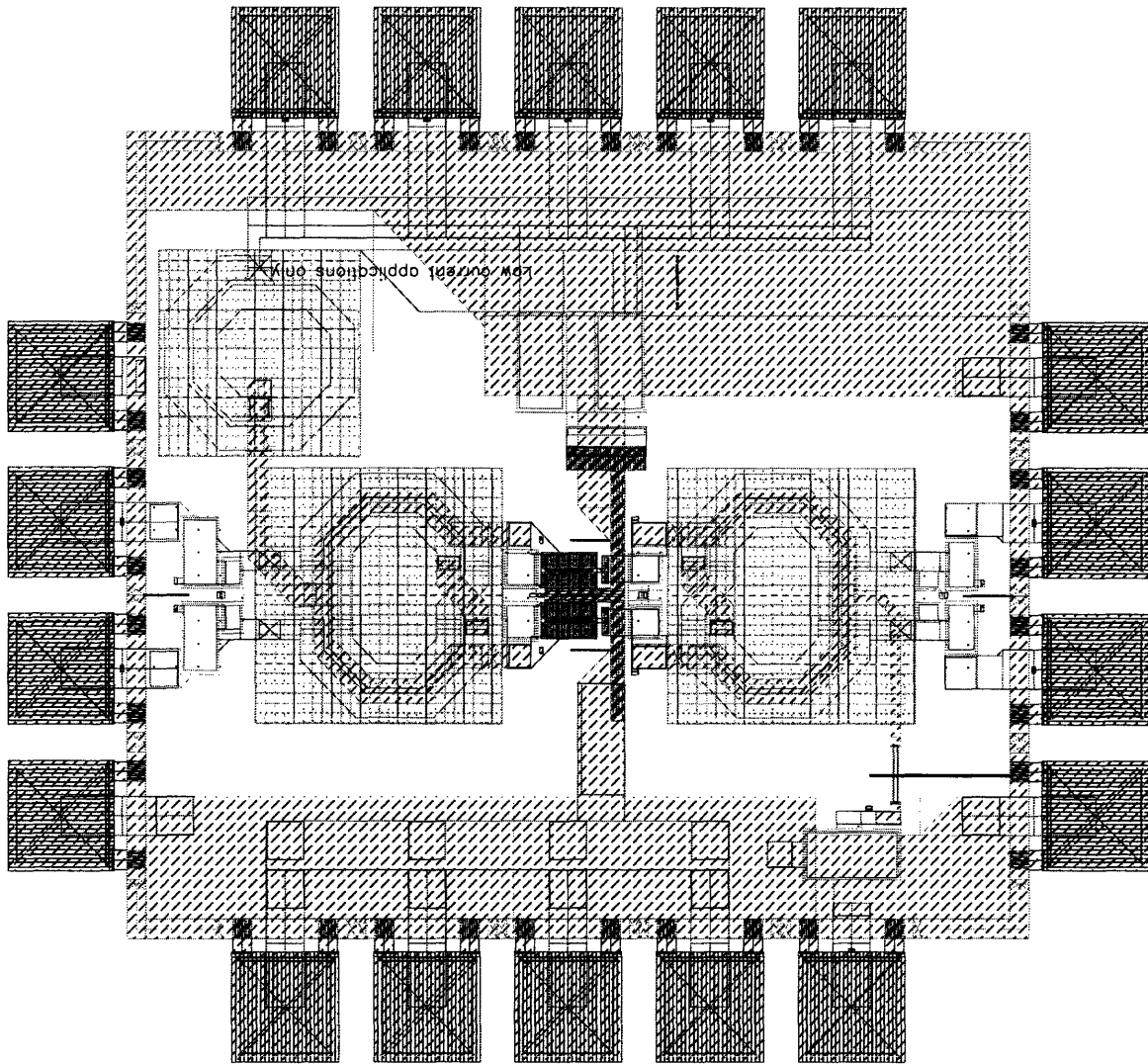


Figure 3-8: Cadence Virtuoso layout image of the power amplifier.

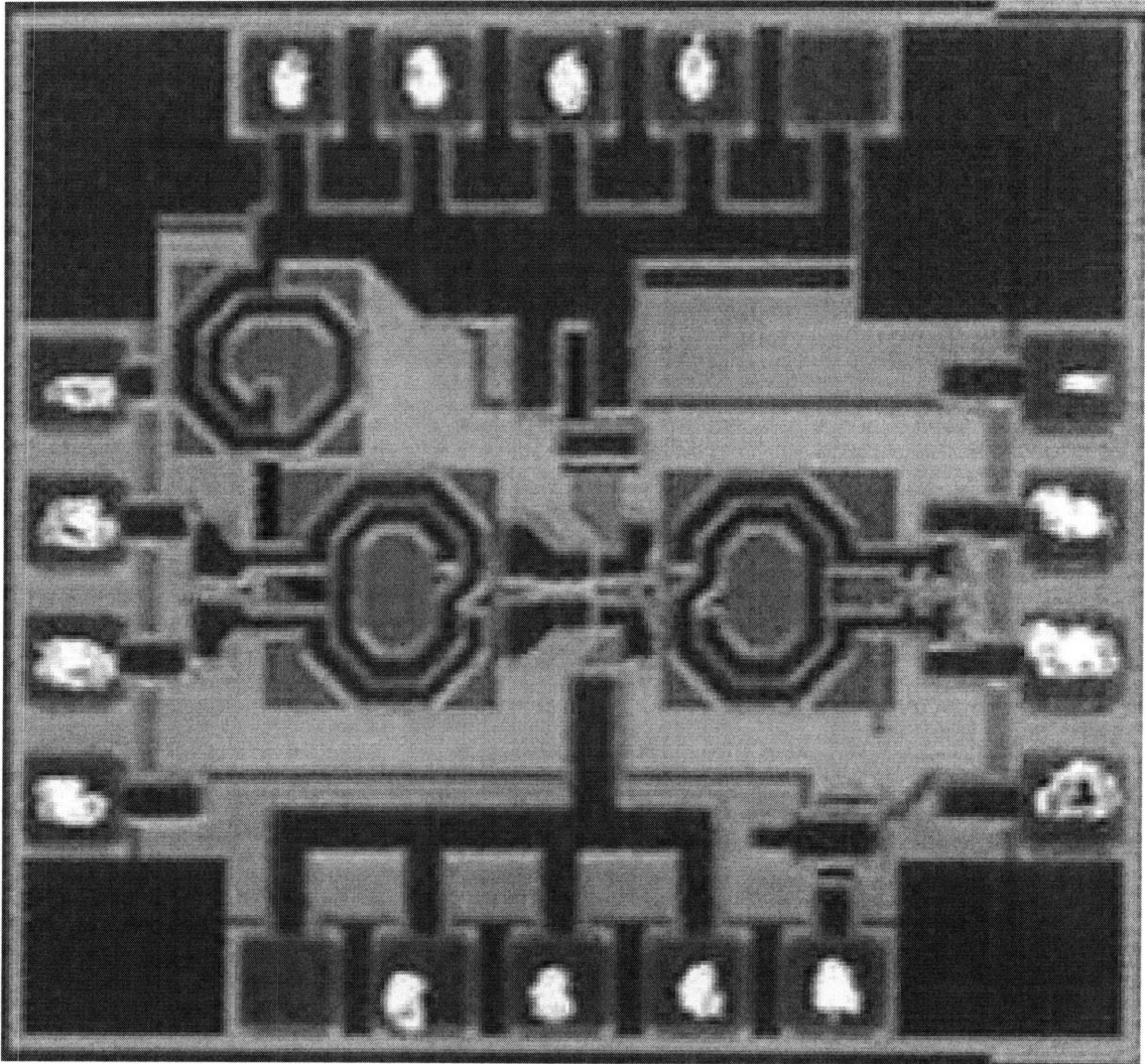


Figure 3-9: Die photograph of the X-band amplifier.





# Chapter 4

## Planar Transformer Design

To match the relatively low impedance of  $20\ \Omega$  seen looking into the collectors of the transistors to a nominal  $50\ \Omega$ , an impedance matching network is needed. To achieve this impedance transformation over a wide bandwidth, a transformer was chosen for the task. This chapter will look at circuit models of transformers, double-tuned transformers and the design of the planar transformer for the X-band amplifier.

### 4.0.5 Lossless Transformer Circuit Models

The basic structure of a transformer is essentially two inductors that are coupled together by the same magnetic flux linkage. In this discussion we will limit ourselves to transformers with a single primary and secondary winding, however the number of windings can easily exceed this. The extent to which the two inductors are coupled together is reflected directly by the coupling coefficient,  $k$ , which ranges from 0 to 1 with 1 being the most tightly coupled.

While a simple model with two coupling inductors  $L_1$  and  $L_2$  is good for general discussion, it is not so useful when trying to optimize a transformer design. As described in [16], the T-model breaks the simple coupled inductor model into three lumped inductors. The inductor  $m$  in the model represents the mutual inductance between the windings while the series inductors represent the leakage inductance

which does not contribute to the transformer action. The mutual inductance  $m$  can be written as function of  $k$ ,  $L_1$  and  $L_2$  from the simple coupled inductor model.

$$m = k\sqrt{L_1 L_2} \quad (4.1)$$

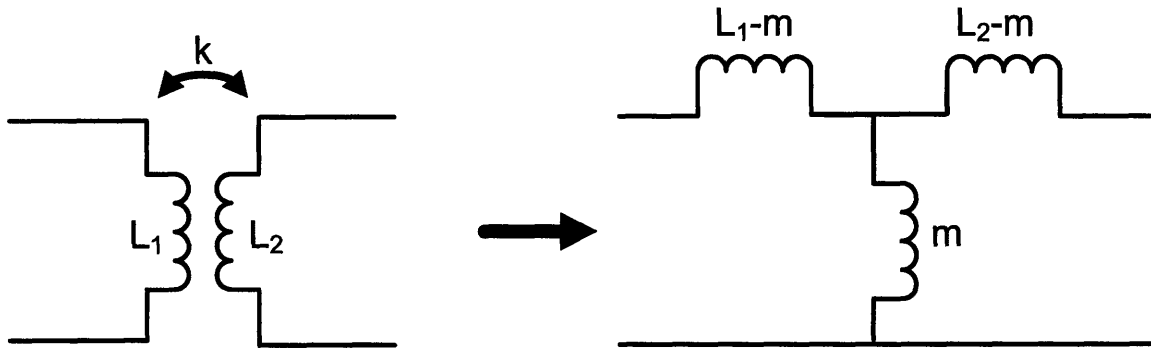


Figure 4-1: Lossless transformer T-model.

Another model that is useful for analyzing transformers found in [16] is shown in Figure 4-2. In this model there is an ideal transformer with winding ratio  $n$ , along with inductors  $L_P$  and  $L_M$ . Inductor  $L_P$  represents the portion of the magnetic flux that does not contribute to the transformer action while  $L_M$  represents the portion of the primary inductance  $L_1$  that does contribute to the transformer action.

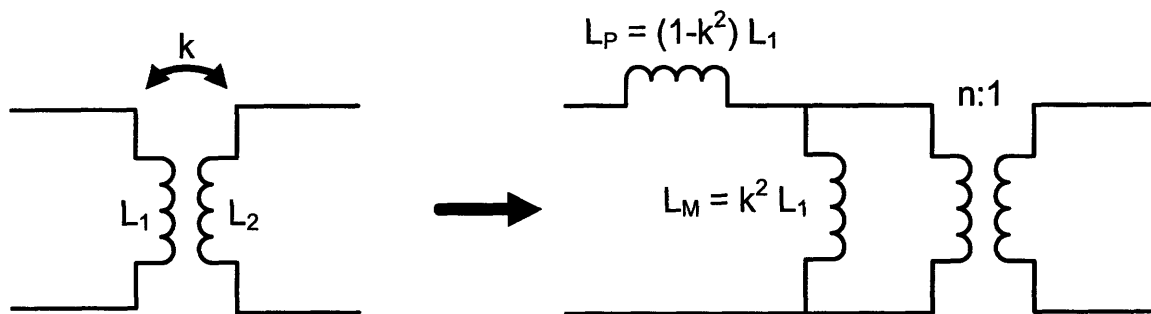


Figure 4-2: Lossless transformer model with ideal transformer, leakage inductance and primary magnetizing inductance.

The one piece missing from this model is the relationship between the ideal transformer's turns ratio  $n$  and the parameters  $k$ ,  $L_1$  and  $L_2$ . This relationship is given in 4.2.

$$n = k\sqrt{\frac{L_1}{L_2}} \quad (4.2)$$

### 4.0.6 Lossy Transformer Circuit Models

Lossless models are great for analytical calculation, however several loss mechanisms exist in real world transformers. A lossy transformer model similar to that in [17] can be seen in Figure 4-3. Planar transformers fabricated in modern IC processes suffer from loss mainly due to lossy substrate coupling ( $Z_{SUB1}$ - $Z_{SUB4}$ ) and thin metal layers causing the windings to have finite Q ( $R_P$  and  $R_S$ ). Since the primary and secondary winding are a finite distance away from each other, interwinding parasitic capacitance exists ( $C_{W1}$ - $C_{W4}$ ).

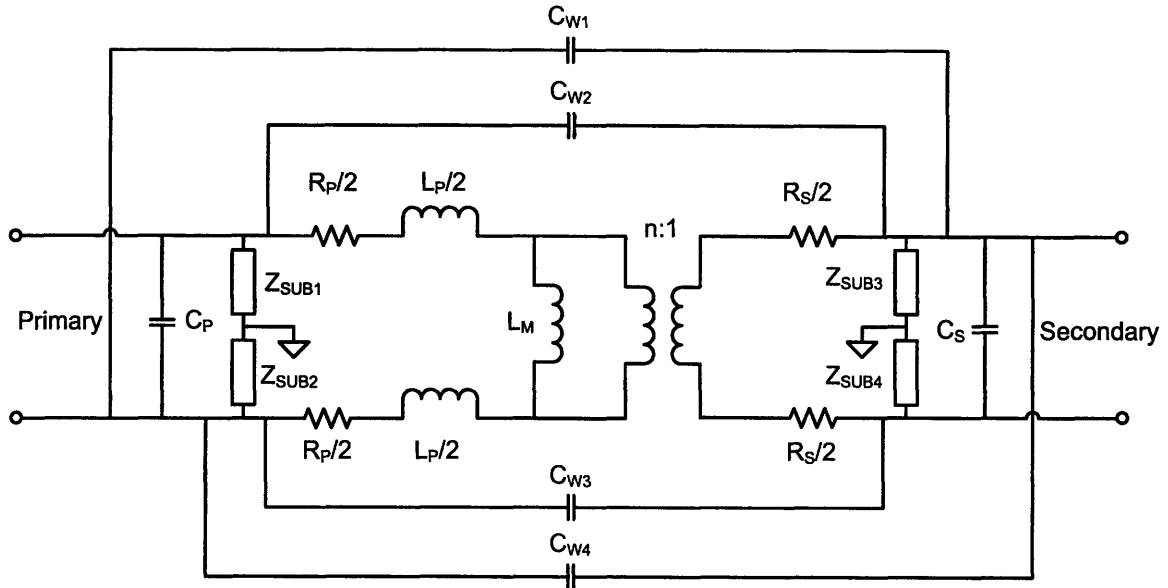


Figure 4-3: Planar transformer circuit model with loss.

### 4.0.7 Double Tuned-Transformers

It is often the case that that when realized alone, the transformer cannot easily match two real impedances over a large frequency range. To get around this limitation it is possible to use coupled resonant circuits consisting of the primary and secondary

winding inductance of the transformer in addition to resonating capacitors placed in parallel with the terminals.

Operation of the double tuned transformer can be analyzed by using the transformer model with ideal  $n : 1$  transformer along with leakage inductance and magnetizing inductance.

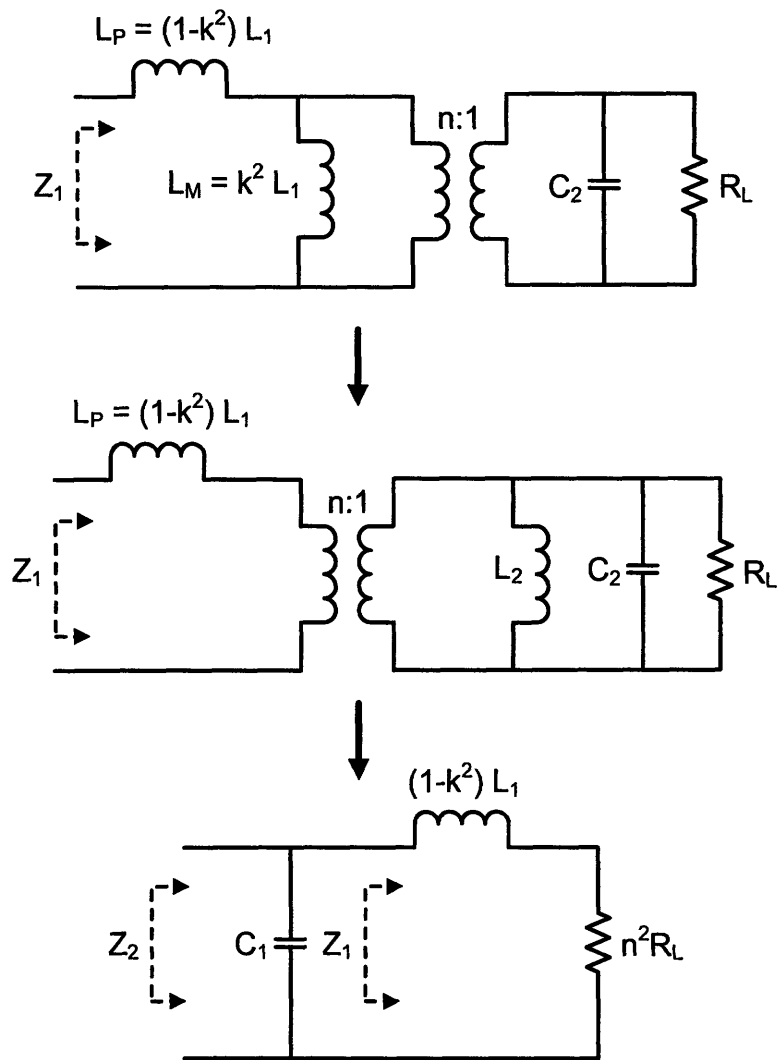


Figure 4-4: Equivalent circuit models of the double tuned transformer.

The following analysis is described in [18]. The magnetizing inductance  $L_M$  on the primary side of the transformer can be moved to the secondary side and by use of Equation (4.2) can be rewritten simply as  $L_2$ . At the resonant frequency  $\omega_o$ , capacitor  $C_2$  and magnetizing inductance  $L_2$  are parallel resonant, leaving only  $R_L$

on the secondary side of the ideal transformer. The resonant frequency  $\omega_o$  is defined as:

$$\omega_o = \frac{1}{\sqrt{L_2 C_2}} \quad (4.3)$$

Analyzing the input impedance  $Z_1$  at the resonant frequency of the secondary yields:

$$Z_1(\omega_o) = j\omega_o(1 - k^2)L_1 + n^2 R_L \quad (4.4)$$

Converting the above impedance to its equivalent admittance yields:

$$Y_1(\omega_o) = \frac{n^2 R_L}{(n^2 R_L)^2 + [\omega_o L_1(1 - k^2)]^2} - j \frac{\omega_o L_1(1 - k^2)}{(n^2 R_L)^2 + [\omega_o L_1(1 - k^2)]^2} \quad (4.5)$$

The capacitive susceptance of 4.5 can be canceled by a shunt capacitor of appropriate value to make the impedance  $Z_2$  purely resistive at  $\omega_o$ . The value of this capacitor  $C_1$  is found to be the following:

$$C_1 = \frac{L_1(1 - k^2)}{(n^2 R_L)^2 + [\omega_o L_1(1 - k^2)]^2} \quad (4.6)$$

The input impedance  $Z_2$  can now be written as:

$$Z_2 = n^2 R_L + \frac{[\omega_o L_1(1 - k^2)]^2}{n^2 R_L} \quad (4.7)$$

Assuming that  $Z_2$  is equal to  $R_S$  (a nominal 50  $\Omega$ ), we can write the value of  $L_1$  as:

$$L_1 = \frac{n}{\omega_o(1 - k^2)} \sqrt{R_L R_S - n^2 R_L^2} \quad (4.8)$$

Making the assumption that the equivalent shunt resistance of the primary and secondary winding are much larger than the source and load impedance, we can write the loaded Q of the primary and secondary as:

$$Q_1 = R_S \sqrt{\frac{C_1}{L_1}} \quad (4.9)$$

$$Q_2 = R_L \sqrt{\frac{C_2}{L_2}} \quad (4.10)$$

The critical coupling factor can be found to be:

$$k_c = \frac{1}{\sqrt{Q_1 Q_2}} \quad (4.11)$$

Typically critical coupling factors are typically near 0.9 to 1 for the impedances inductances involved in planar transformer design. However, physically realizable  $k$ 's are much lower. To estimate the bandwidth of the transformer, universal selectivity curves for double tuned circuits found in [19] are used. Selectivity curves are plotted for various values of  $b$  where  $b$  is defined as:

$$b = \frac{k}{k_c} \quad (4.12)$$

Where  $k$  is the maximum physically realizable  $k$  of the transformer.

#### 4.0.8 X-Band Double Tuned Transformer

The design of the double tuned transformer started by finding the required value of  $L_1$ . Using Equation (4.8) and assuming a source and load impedance of 20  $\Omega$  and 50  $\Omega$ ,  $L_1$  was found to be 821 pH. Resonating, this inductance at 9.5 GHz yields a value for  $C_1$  of 342 fF. Using Equation (4.2) and assuming a value of  $k = 0.7$ , the value of  $L_2$  was found to be 328 pH. Completing the design, resonating  $L_2$  at 9.5 GHz yielded a value of 855 fF for  $C_2$ . Using Equation (4.11) and (4.12),  $b$  was found to be approximately 0.7. Estimating the 3 dB bandwidth from the universal selectivity curves in [19], a value of 18 GHz was obtained. The component values were entered into an S-parameter simulation in ADS and were tuned to obtain maximum bandwidth with good input and output return loss. A summary of the component values can be found in 4.1.

Table 4.1: Planar Transformer Value Summary

Parameter	Analytic	Circuit Simulation	EM Simulation	Units
$L_1$	820	970	950	pH
$C_1$	340	328	306	fF
$L_2$	328	314	650	pH
$C_2$	854	1140	1140	fF
$k$	0.7	0.7	0.65-0.75	-
$3dB\text{Bandwidth}$	18	13.5	13.5	GHz

The transformer was designed and simulated using Momentum. With the values of the resonating capacitors found from the S-parameter tuning simulation, the EM simulation S-parameter data was tested. The results are shown in Figure 4-5.

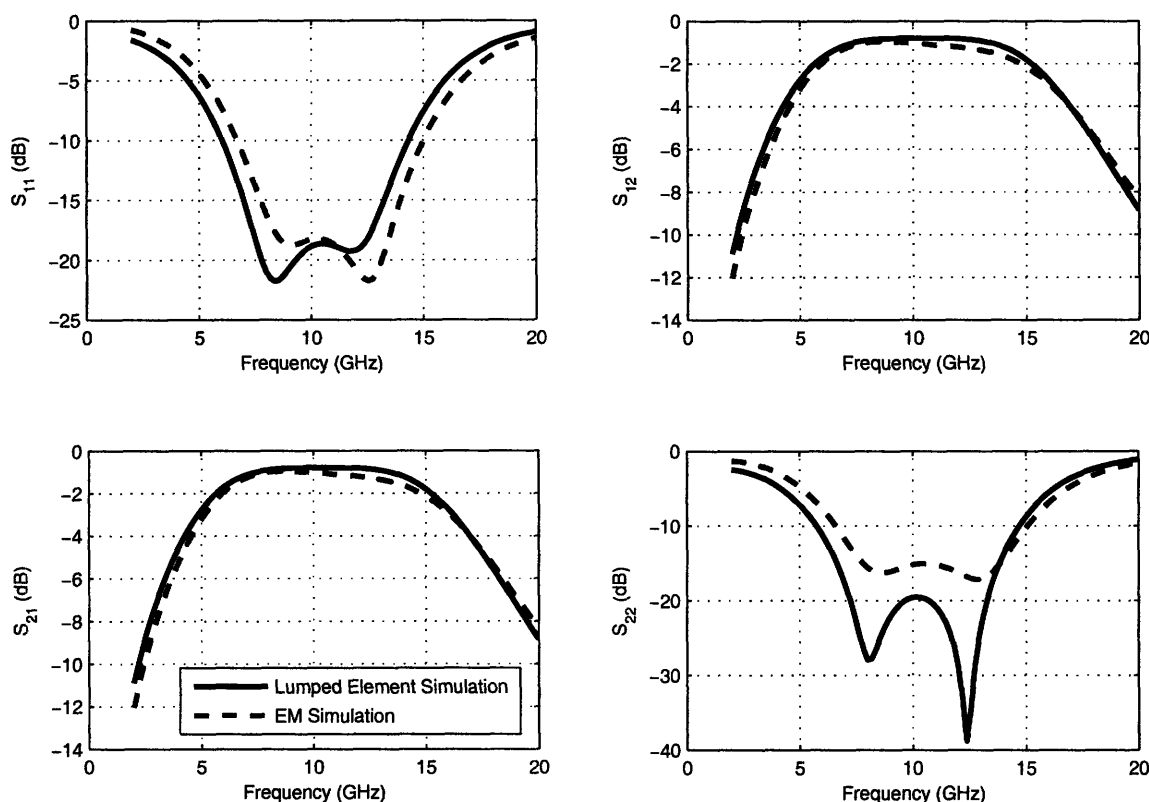


Figure 4-5: Lumped element and electromagnetic simulation results of the double tuned transformer.

Adjusting the capacitor values on the EM simulation slightly, the results were more closely matched to the initial S-parameter tuning simulation. The only value

changed was  $C_1$ , changing from 328 fF to 306 fF. The modified results are shown in Figure 4-6.

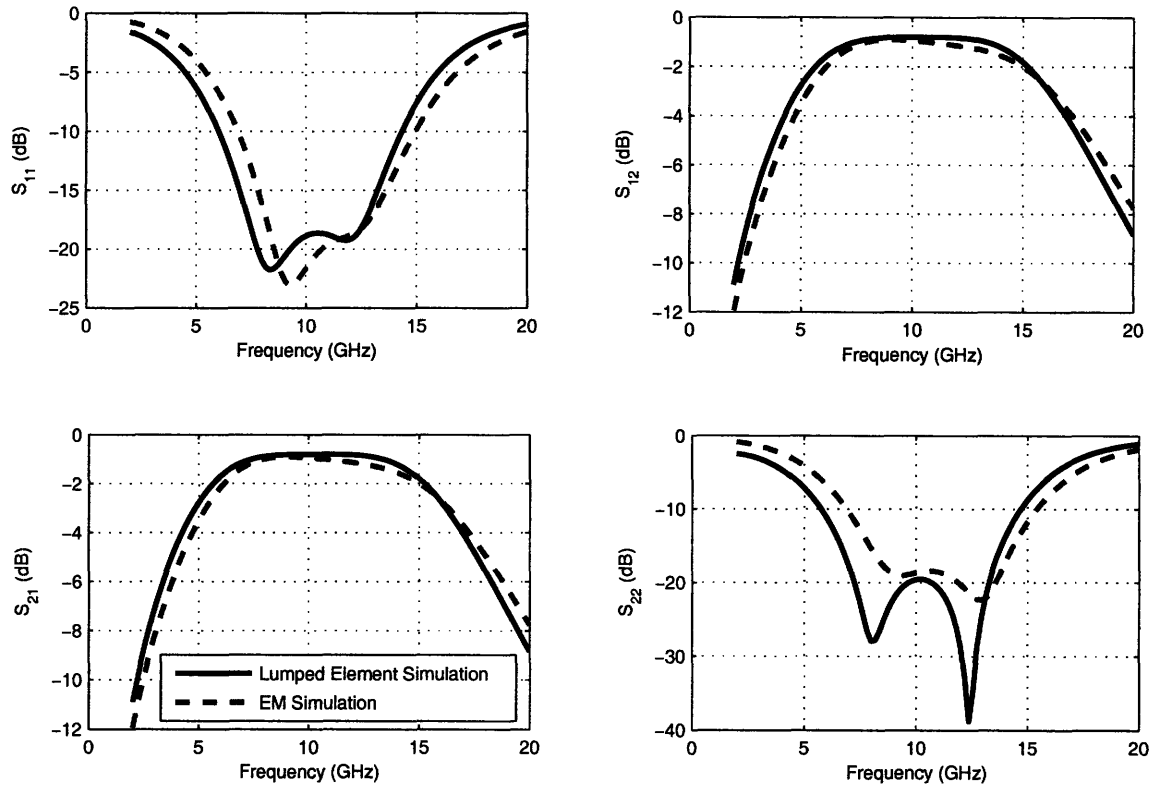


Figure 4-6: Lumped element and electromagnetic simulation results of the double tuned transformer with adjusted capacitor values.

From the EM simulation the critical parameters of the transformer were extracted. The value of  $k$ ,  $Q_1$ ,  $Q_2$ ,  $L_1$  and  $L_2$  can be seen in Figures 4-7, 4-8, and 4-9 respectively.

The final transformer has the primary winding  $L_1$  on the top metal layer, while the secondary winding  $L_2$  is contained on the next 2 lower metal levels. These two levels were used together in order to achieve the desired amount of inductance for the secondary winding. An image of the transformer can be seen in figure 4-10.



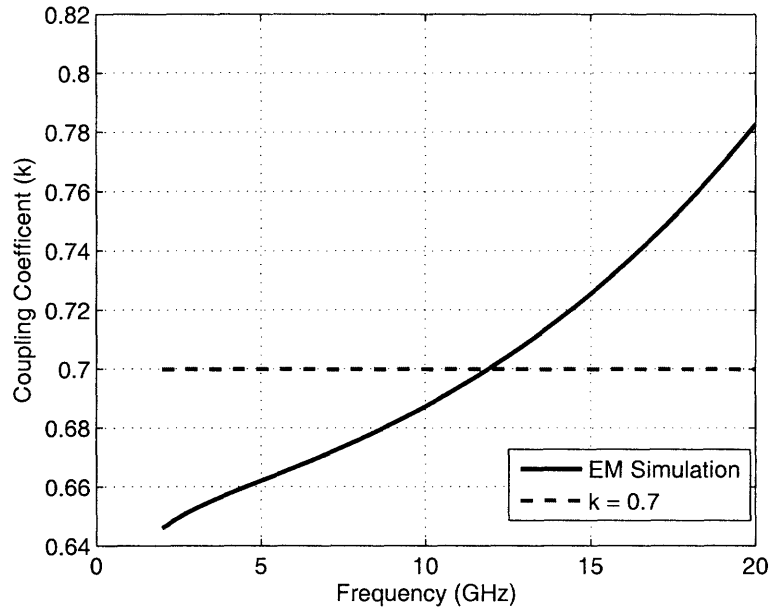


Figure 4-7: Coupling coefficient of the double tuned transformer.

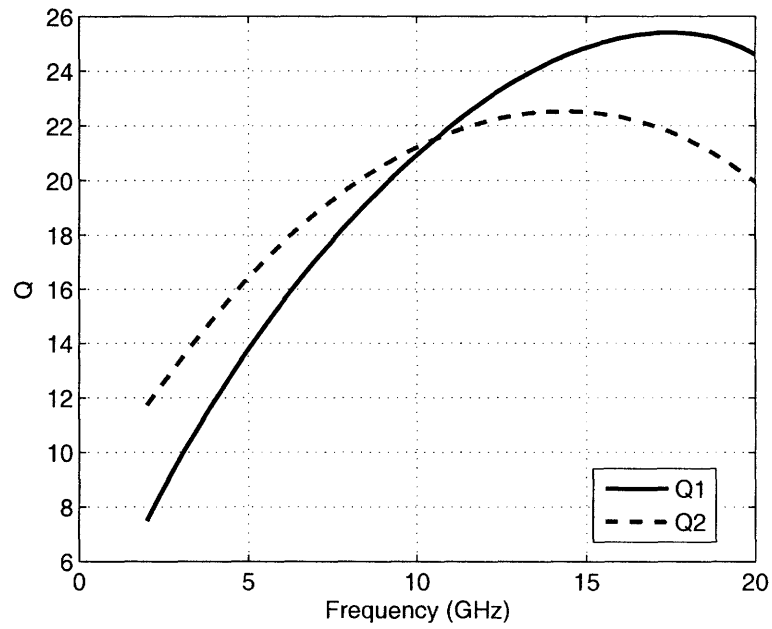


Figure 4-8: Quality factor of the primary and secondary windings obtained from EM Simulations.

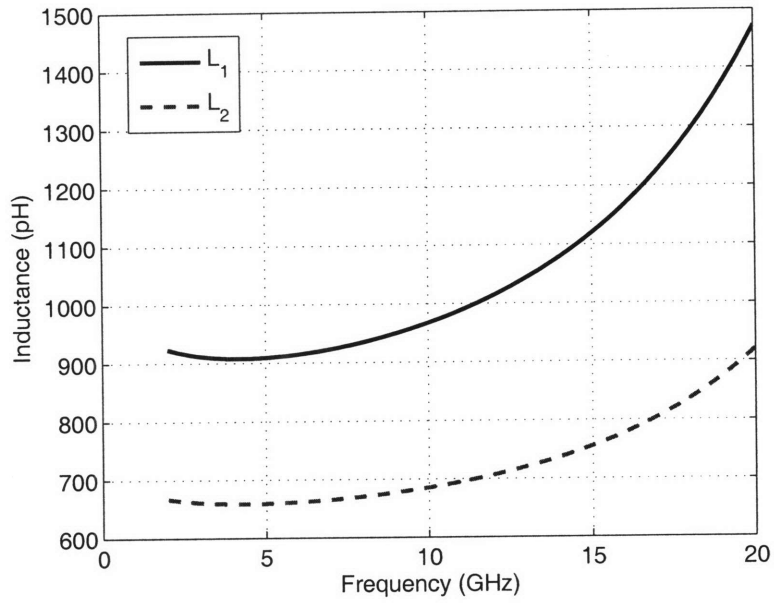


Figure 4-9: Inductance of the primary and secondary windings obtained from EM Simulations.

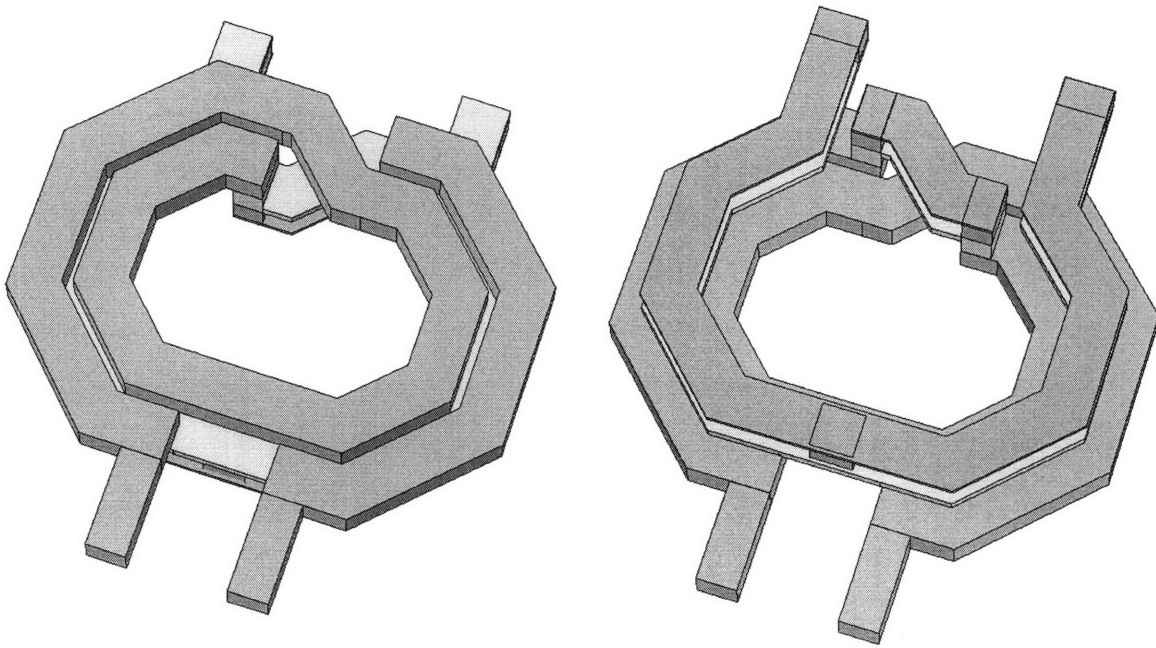


Figure 4-10: Top and bottom view of the planar transformer.

# Chapter 5

## Simulation and Measurement

### Results

This chapter presents simulation and measurement results of the single stage class AB amplifier. Simulation results and measurement results are plotted on the same graphs to compare and contrast the similarities and differences of the two. Simulations were done at a power supply voltage of 1.8 volts, however the measurements were done at a power supply voltage of 2 volts. This was done to account for the DC resistance of the power supply choke which was not accurately modeled in simulation. The choke has a DC resistance of approximately  $0.5\Omega$ , and thus with several hundred milliamperes flowing through it, the voltage drops several tenths of a volt. In simulation the power amplifier was powered through two ideal chokes since DC current could not be easily be used with the S-parameter blocks. A schematic view of the amplifier used in simulation can be seen in Figure 5-1.

#### 5.0.9 Large Signal Amplifier Measurements

The amplifier was designed to operate at an input power of 10 dBm, with an output power over 20 dBm expected. Simulations of the large signal gain were done in Agilent RFDE using the large signal S-parameter simulation (LSSP) tool. This is a harmonic balance simulator that uses VBIC transistor models. The planar transformers were

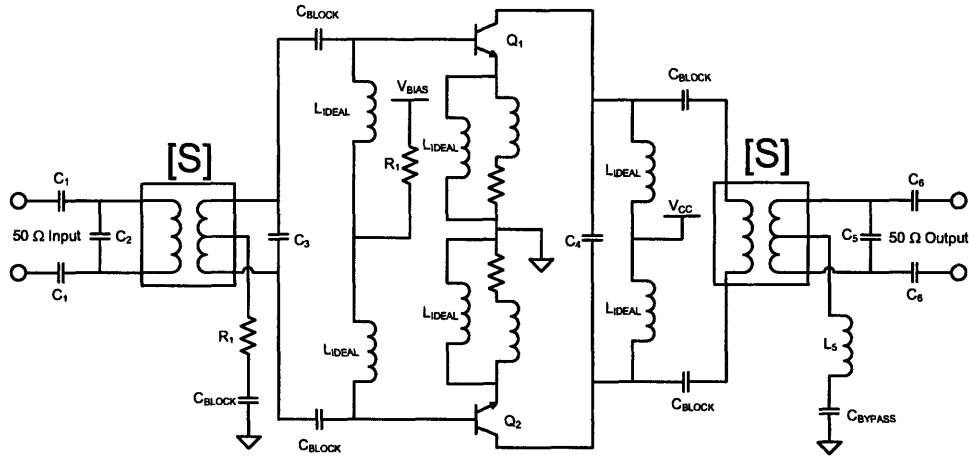


Figure 5-1: Schematic of the power amplifier used for circuit simulation.

implemented as 5 port S-parameter blocks, with ideal chokes used for the DC feed network. The ideal chokes were used since Momentum (a 2D planar EM simulator) cannot simulate a point at DC, but will try to extract a value from data in the kilohertz range. This causes a slight problem - ports that should be isolated at DC have finite resistance that is not low enough to neglect - often effecting the DC bias point of the simulator.

Measurements were done on wafer using ground signal (GS) probes and DC probes to provide DC power and bias. GS probes offer a method of testing a circuit differentially without using ground signal ground signal ground (GSGSG) probes and a full multi-mode calibration procedure [20].

The large signal gain of the amplifier was measured 2 different ways. An Agilent precision network analyzer (PNA) was first used, however as the results show, the source power was not leveled across frequency, nor was it able to achieve the desired input power of 10 dBm to drive the amplifier. The second method utilized a signal generator, and a calorimetric power meter. For this measurement everything was referenced to the accuracy of the power meter, which was assumed to be accurate within several tenths of a dB of its actual reading. First the output power of the signal generator was verified across the range of input powers. Secondly, all of the interfacing cables, connectors, and probes were measured using the power meter and calibrated signal generator. Once all the losses were established, it was possible to

set the power at the tips of the probes to exactly to the desired excitation power. A pictorial representation of the measurement setup is shown in Figure 5-2.

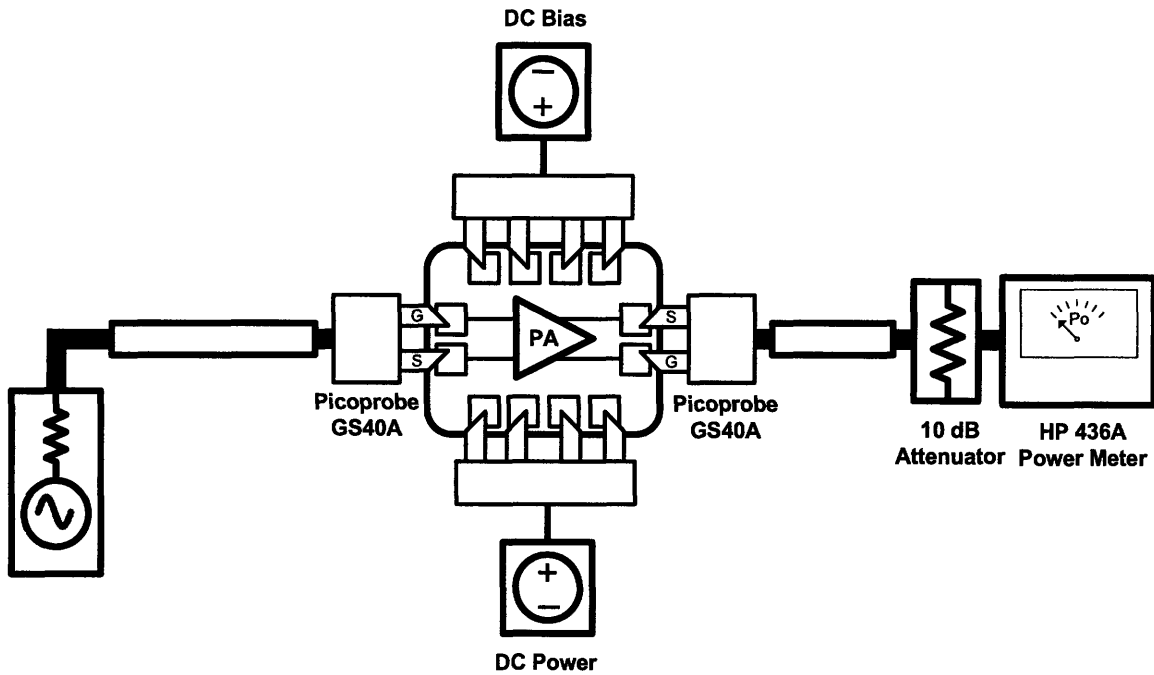


Figure 5-2: Test setup used to measure the large signal gain of the amplifier.

At the design input power of 10 dBm, the amplifier has a simulated gain of at least 10 dB from 4.5 to 14 GHz. The measured results exhibit the same trend as the simulated response with the gain within  $\pm 1.5$  dB over the band of interest. Within the passband of the amplifier, the maximum simulated gain is approximately 12 dB at a frequency of 11 GHz, while measurement shows a maximum gain of approximately 13 dB at 7.5 GHz.

In addition to measuring the large signal gain, the large signal output characteristics were also simulated and measured as a function of input power. As expected, as the input power is increased, the output power starts to compress as the power starts to reach its maximum output. While the power gain decreases, the power added efficiency peaks in the region of compressed output power and then starts to slightly decrease due to the rapidly falling gain. Plots of the amplifier's power output and PAE can be seen in Figures 5-4, 5-5, 5-6, 5-7, 5-8 and 5-9.

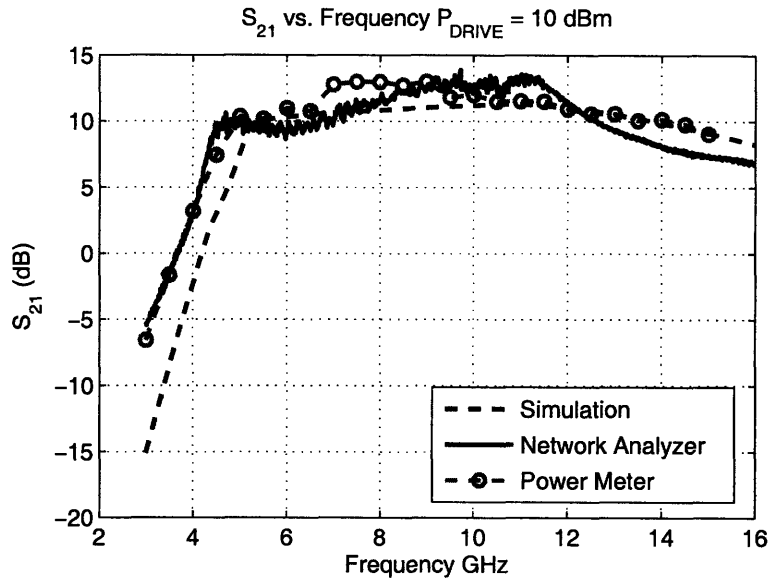


Figure 5-3: Simulated and measured large signal gain of the amplifier versus frequency. The input power is 10 dBm.

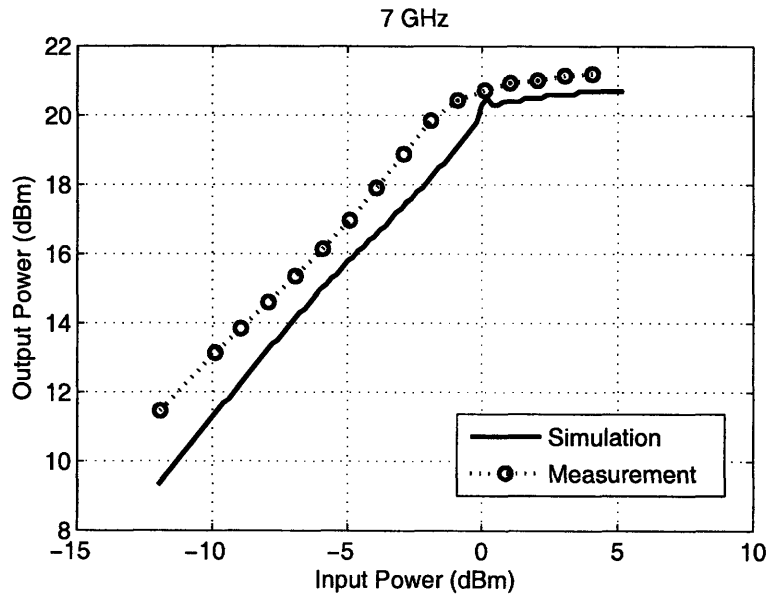


Figure 5-4: Simulated and measured large signal characteristics of the amplifier at 7 GHz.

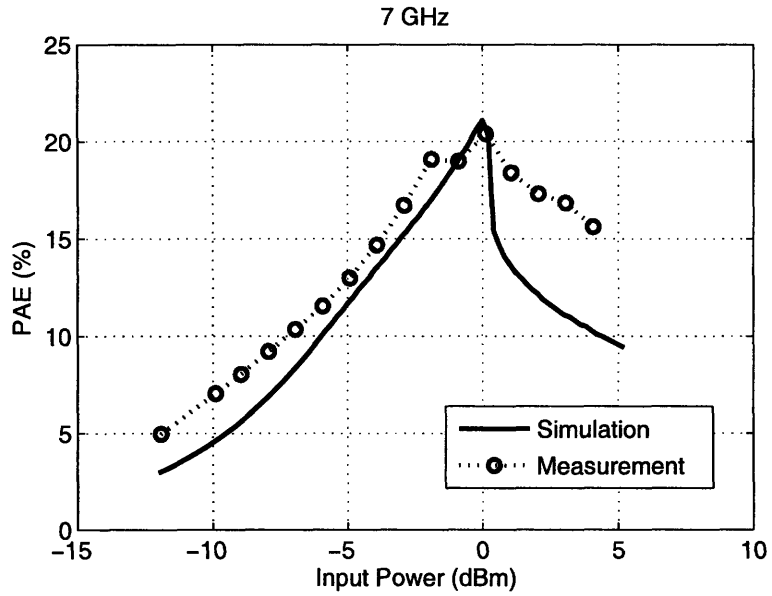


Figure 5-5: Simulated and measured power added efficiency as a function of input power at 7 GHz.

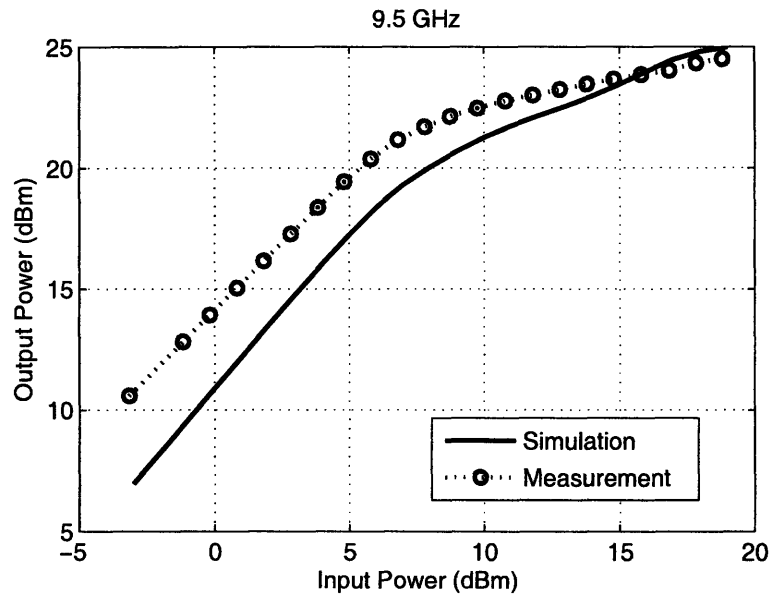


Figure 5-6: Simulated and measured large signal characteristics of the amplifier at 9.5 GHz.

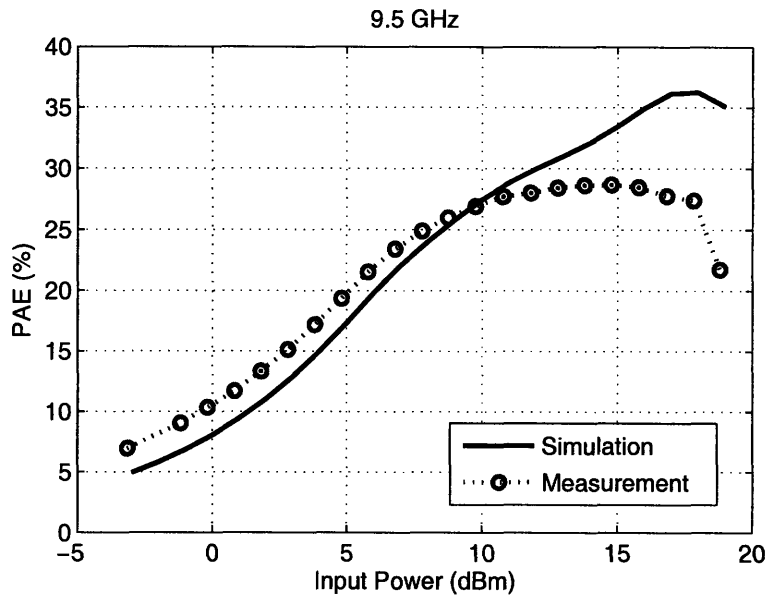


Figure 5-7: Simulated and measured power added efficiency as a function of input power at 9.5 GHz.

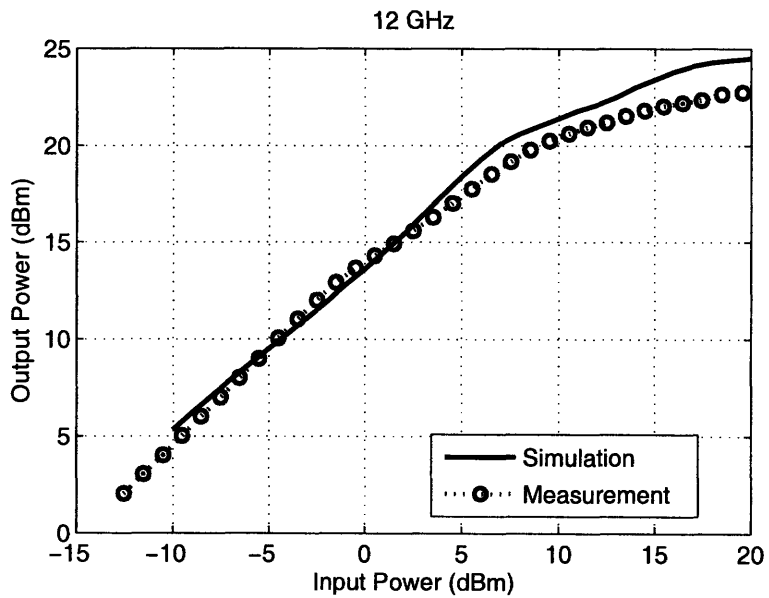


Figure 5-8: Simulated and measured large signal characteristics of the amplifier at 12 GHz.



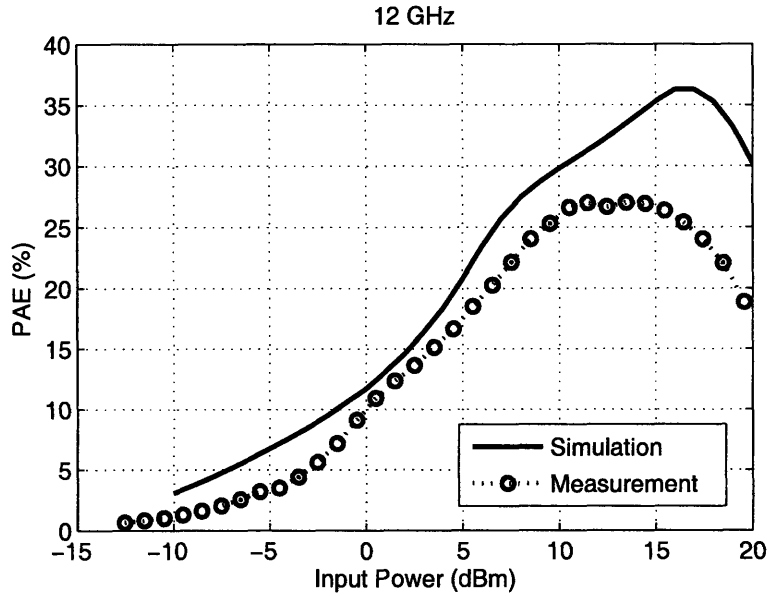


Figure 5-9: Simulated and measured power added efficiency as a function of input power at 12 GHz.

The PAE of the amplifier was also measured as a function of frequency with a fixed input power of 10 dBm. Within the X-band frequency spectrum of 7-12.5 GHz, the amplifier maintains a PAE of at least 22.7 %.

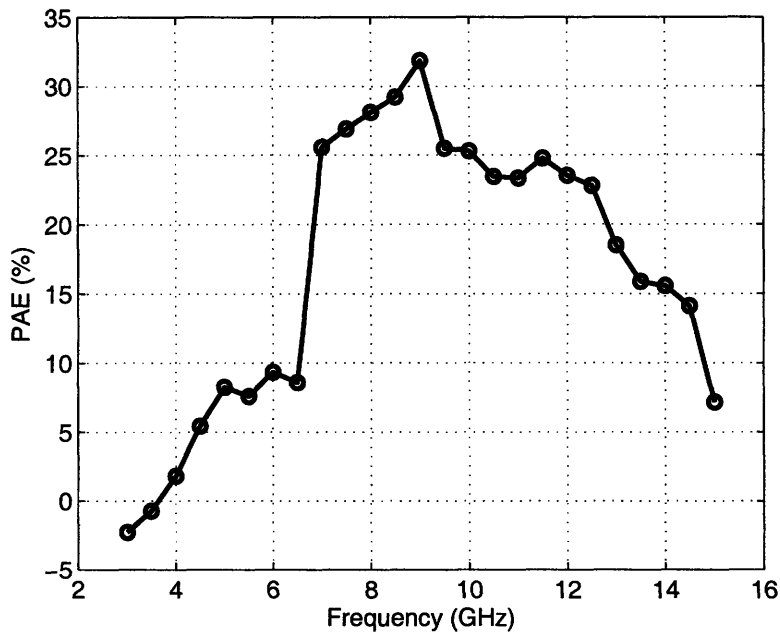


Figure 5-10: Measured PAE of the power amplifier at an input power of 10 dBm.

### 5.0.10 Small Signal S-Parameters

At lower power levels, the source power of a typical network analyzer is adequate enough to make small-signal measurements of active and passive devices. Even though the source power of the network analyzer is not guaranteed to be leveled (constant) across frequency, the resulting gain of the device under test should not change. Measurements of the small signal S-parameters were made using an Agilent N5238 Precision Network Analyzer with a source power of approximately -18 dBm. Calibration to the probe tip level was accomplished by way of a short-open-load-through (SOLT) calibration.

Simulations of the amplifiers small signal S-parameters were done using the large signal S-parameter simulation in Agilent RFDE with the source power set to -18 dBm.

The simulated small signal gain,  $S_{21}$ , has a peak value of about 23 dBm, while measurements show a peak value of 21 dB. Input return loss shows a null of approximately -24 dB at 12 GHz, while measurement indicates only about -13 dB. Possible sources for this error include small pieces of interconnecting metal that were not fully simulated. Additionally, coupling from the transformers to the surrounding ground shield may slightly effect the measured results.

Reverse isolation of the amplifier is somewhat low at only -23 dB due to the single stage common emitter topology, however the amplifier is quite stable and does not oscillate into the designed load impedance of 50  $\Omega$ . Simulated output return loss has a dip of -35 dB at 14 GHz, while measurements indicate approximately -23 dB. While this seems significantly different when analyzing data in terms of decibels, if we looked to the corresponding values in simple ratios, we would see the difference is very small.

### 5.0.11 Stability

At small signal levels the k-factor stability was simulated and measured. The k-factor was computed using small-signal S-parameter data and equation (2.1.5) from Chapter 2. Plots of the k-factor can be seen in Figures 5-12 and 5-13. At large signal-levels

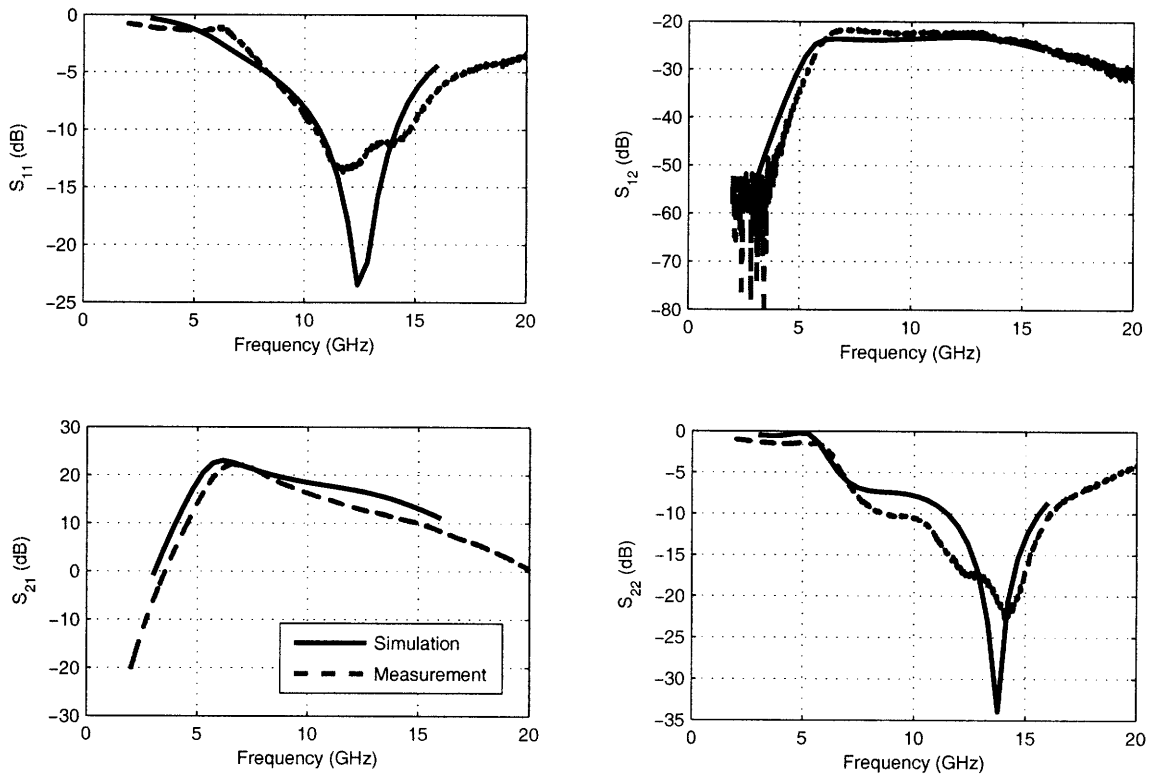


Figure 5-11: Simulated and measured small signal S-parameters. The measurements were taken at an input power of -18 dBm.

where the power amplifier is operated in a non-linear region, k-factor analysis is not valid since it assumes a linear two port network for its derivation.

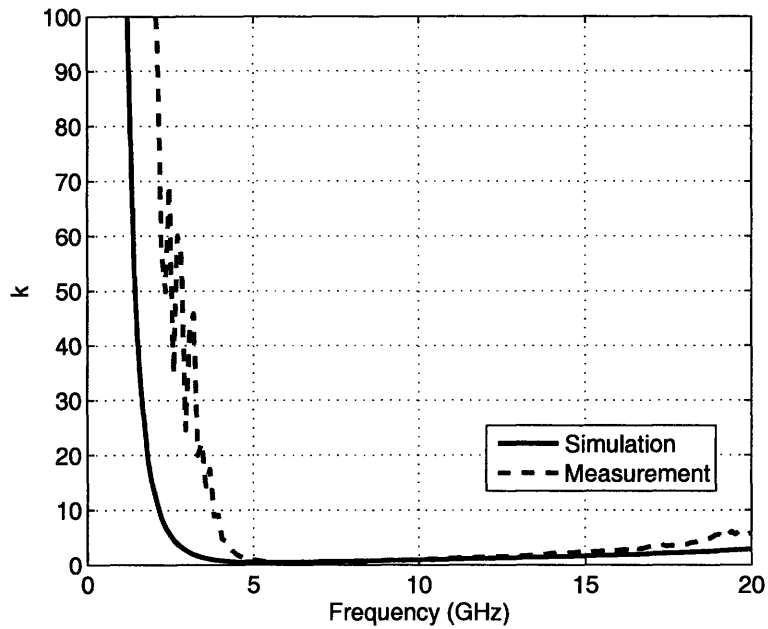


Figure 5-12: Simulated and measured k-factor stability plot taken from small signal S-parameter data.

Although k must be greater than one for unconditional stability, conditional stability is acceptable for this application. The measured and simulated  $S_{11}$  and  $S_{22}$  were clearly less than unity when properly terminated and no oscillations were observed during the measurements.

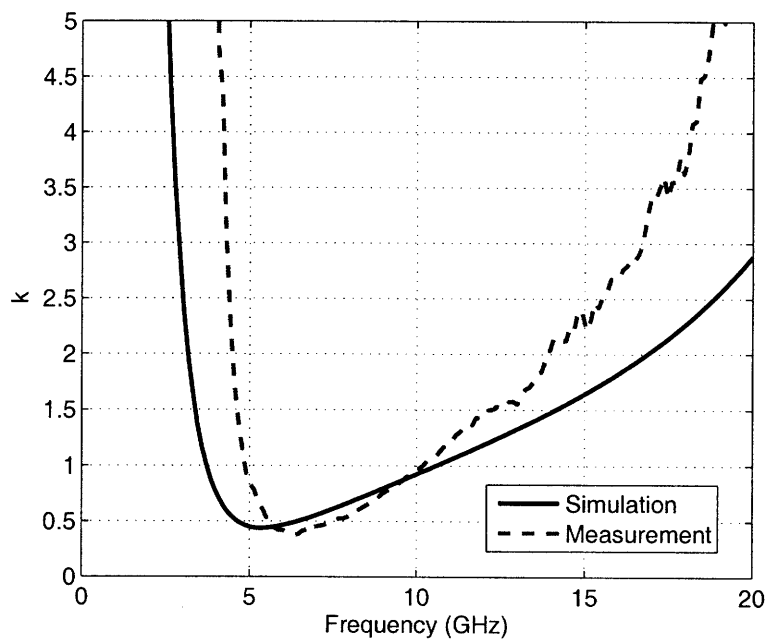


Figure 5-13: Simulated and measured k-factor stability plot, zoomed in view.



# Chapter 6

## Conclusion

This thesis explored the design, fabrication and measurement of a high power amplifier covering 5-14 GHz. The amplifier has at least 10 dB of gain from 5-14 GHz and maintains a PAE of 22.7 % from 7-12.5 GHz (X-band). The amplifier takes up a small amount of space, occupying 1.21 mm x 1.08 mm. This small size and high-bandwidth are achieved using double-tuned transformers as matching networks at the input and output of the amplifier.

In the future, improvements will be made to increase the stability of the design and increase the PAE over frequency. This will most likely be done by decreasing the gain of the amplifier at low frequencies, and improving the RF grounding and bypassing throughout the chip.

A summary of the amplifiers measured performance is shown in Table 6.1.

Table 6.1: Power Amplifier Performance Summary

Parameter	Value	Units
Maximum Large Signal Gain	13	dB
3 dB Bandwidth (Large Signal)	5-14	GHz
Maximum Small Signal Gain	23	dB
Maximum Output Power ( $P_{SAT}$ )	24.5	dBm
Minimum PAE (7-12.5 GHz)	22.7	%
Maximum PAE	32	%
Power Consumption (0 dBm drive)	200	mW
Power Consumption (10 dBm drive)	530	mW



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