Advanced Technologies for Improving High Frequency Performance of AlGaN/GaN High Electron Mobility Transistors

by

Jinwook W. Chung

B.S. Electrical Engineering and Computer Science
Korea Advanced Institute of Science and Technology, 2006

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of

Master of Science in Electrical Engineering

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ABSTRACT

In this thesis, we have used a combination of physical analysis, numerical simulation and experimental work to identify and overcome some of the main challenges in AlGaN/GaN high electron mobility transistors (HEMTs) for high frequency applications. In spite of their excellent material properties, GaN-based HEMTs are still below the theoretical predictions in their high frequency performance. If the frequency performance could be improved, the superior breakdown characteristics of nitride semiconductors would make these devices the best option for power amplifiers at any frequency. To achieve this goal, we have first identified some critical parameters that limit the high frequency performance of AlGaN/GaN HEMTs and then we have demonstrated several new technologies to increase the performance. Some of these technologies include advanced drain delay engineering, charge control in the channel and new N-face GaN HEMTs. Although more work is needed in the future to combine all these new technologies, the initial results are extremely promising.

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May 2008

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- "New devices based on Si/Nitride structures". Inventor: T. Palacios and J. W. Chung. Patent pending (2007).

PAPERS IN INTERNATIONAL JOURNALS

- J. W. Chung, E. L. Piner, and T. Palacios, "*N-face GaN transistors through wafer removal*", to be submitted to IEEE Electron Device Lett. (May. 2008.)

- J. W. Chung, J. C. Roberts, E. L. Piner, and T. Palacios, "*Effect of Gate Leakage in the Subthreshold Characteristics of AlGaN/GaN HEMTs*", submitted to IEEE Electron Device Lett. (May. 2008.)

- J. W. Chung, X. Zhao, Y. Wu, J. Singh and T. Palacios, "*Effect of image charges in the drain delay of AlGaN/GaN high electron mobility transistors*", Appl. Phys. Lett., vol. 92, 093502, Mar. 2008.

- J. M. Tirado, F. Miéville, J. W. Chung, T. Palacios and J. L. Sánchez-Rojas, "*Origin of the Increasing Access Resistance in AlGaN/GaN HEMTs*", submitted to IEEE Trans. Electron Devices. (May. 2008.)

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- J. W. Chung, X. Zhao, and T. Palacios, "*Estimation of Trap Density in AlGaN/GaN HEMTs from Subthreshold Slope Study*", 65th Device Research Conference, University of Notre Dame, June 18-20, 2007.

- X. Zhao, J. W. Chung, and T. Palacios, "*Atomic Layer Etching of AlGaN/GaN Structures*", International Conference on Nitride Semiconductors, Las Vegas, NV, Sept. 17-21, 2007.

- X. Zhao, J. W. Chung, and T. Palacios, "Increase of Electron Velocity in GaN HEMTs by Electric Field Engineering", International Conference on Nitride Semiconductors, Las Vegas, NV, Sept. 17-21, 2007.

- X. Zhao, J. W. Chung, H. Tang, and T. Palacios, "Schottky Drain AlGaN/GaN HEMTs for mm-wave Applications", 65th Device Research Conference, University of Notre Dame, June 18-20, 2007.

- T. Palacios, X. Zhao, J. W. Chung, "*Drain Delay: The Ultimate Limit for the Frequency Performance of AlGaN/GaN HEMTs*", 12th Advanced Heterostructure Workshop, Kohala Coast, Big Island of Hawai'i, December 3-8, 2006.

- J. M. Tirado, F. Miéville, X. Zhao, J. W. Chung, T. Palacios, and J. Sánchez-Rojas, "*Origin of the Increasing Access Resistance in AlGaN/GaN HEMTs*", 66th Device Research Conference, University of California, Santa Barbara, June 23-25, 2008. (accepted).

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Chapter 1. Introduction

1.1. Nitride semiconductors

In only 15 years, nitride semiconductors have evolved remarkably from the first materials grown by molecular-beam epitaxy (MBE) and metal-organic chemical vapour deposition (MOCVD) with very high dislocation densities to commercial applications. Nitride semiconductors have a unique combination of properties that make them the most complete semiconductor family and especially suitable for many of the new challenges and applications in the 21st century. Some of these properties are a direct bandgap tunable from 6.2 eV (AlN) down to 0.7 eV (InN) (Figure 1-1.), piezoelectricity, polarization, large breakdown voltage, biocompatibility, high chemical and thermal stability, etc. Moreover, even superconductivity and ferromagnetism have been proposed by some researchers. These outstanding properties allow many new optoelectronics, electronics, and biomedical applications such as LEDs and lasers, photodetectors, transistors, piezoelectric filters, biosensors, etc as shown in Figure 1-2.

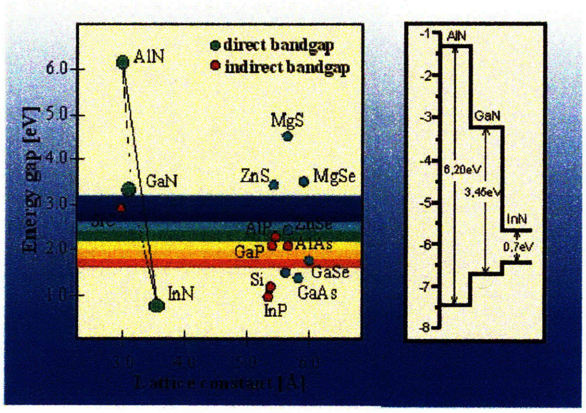


Figure 1-1. The wide tunable bandgap of nitride semiconductors (0.6~6.2eV) covers the spectral range from UV to visible and, even, infrared.

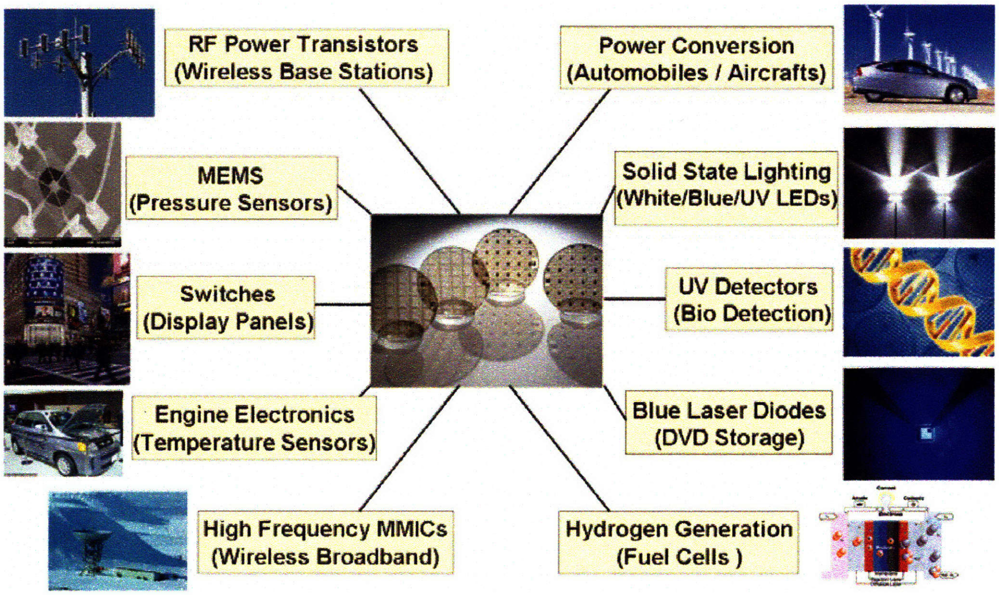

RF Power Transistors
(Wireless Base Stations)
Power Conversion
(Automobiles / Aircrafts)
MEMS
(Pressure Sensors)
Solid State Lighting
(White/Blue/UV LEDs)
Switches
(Display Panels)
UV Detectors
(Bio Detection)
Engine Electronics
(Temperature Sensors)
Blue Laser Diodes
(DVD Storage)
High Frequency MMICs
(Wireless Broadband)
Hydrogen Generation
(Fuel Cells)

Figure 1-2. Some of the many applications of nitride semiconductors.

1.2. GaN HEMTs

One of the most promising and widely used electronic devices in nitride semiconductors are the AlGaN/GaN high electron mobility transistors (HEMTs). These devices attracted considerable attention soon after they were first reported in the early 1990s [1] due to their unique and superior properties, such as large sheet charge density (~1×10^{13} cm^{-2}), high peak electron velocity (~2.1×10^{7} cm/s), high breakdown field strength (~3 MV/cm) and good thermal conductivity (>1.5 W/cm·K) as shown in Table 1-1. All these properties make them the best option for the fabrication of power amplifiers with unprecedented output power levels at GHz frequencies. In only 15 years, AlGaN/GaN HEMTs have evolved tremendously from the initial devices with less than 40 mA/mm of output current and virtually no high frequency performance [1], to world-wide commercialization as power amplifiers in S- and X-band [2]. AlGaN/GaN HEMTs have already been demonstrated an output power density of 32.2 W/mm at 4 GHz [3] and recently have also expanded their frequency range to a power density of 2.1 W/mm at 80.5 GHz [4].

Characteristic	Silicon	AlGaAs/ InGaAs	InAlAs/ InGaAs	SiC	AlGaN/ GaN
Bandgap (eV)	1.1	1.42	1.35	3.26	**3.49**
Electron mobility at 300K (cm^2/V·s)	1500	8500	5400	700	**1500-2200**
Saturated (peak) electron velocity (×10^7 cm/s)	1.0 (1.0)	1.3 (2.1)	1.0 (2.3)	2.0 (2.0)	**1.3** **(2.1)**
Critical breakdown field (MV/cm)	0.3	0.4	0.5	3.0	**3.0**
Thermal conductivity (W/cm·K)	1.5	0.5	0.7	4.5	**>1.5**

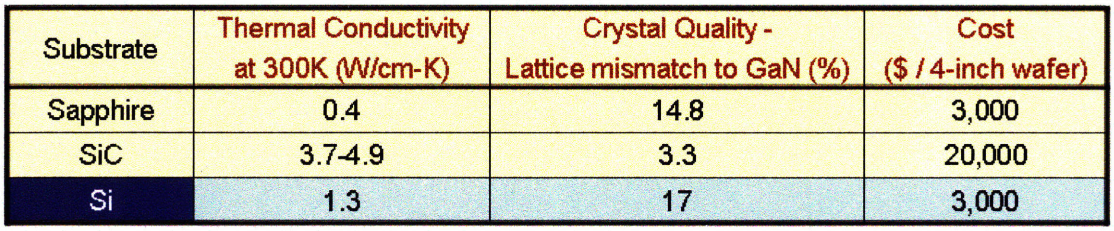
Table 1-1. Some of the outstrip material properties of GaN compared to other semiconductor families.

Although these results are excellent, GaN transistors are not ubiquitous yet. Mass production and wide commercialization of GaN devices are hindered by their high cost, which is dominated by the expensive SiC substrates on which they are fabricated. The following section will describe GaN HEMTs grown on different substrates and analyze Si substrate as the best option for achieving both excellent performance and broad commercialization of GaN.

1.3. GaN on Si substrate

Traditionally, due to the lack of bulk GaN substrates that would allow homoepitaxy, state-of-the-art GaN HEMTs have been grown on semi-insulating SiC substrates. Due to the lower cost, the first AlGaN/GaN HEMT was grown on sapphire substrates [1]. However, SiC substrates has become more popular because its better thermal conductivity and smaller lattice mismatch to GaN render superior electrical performance to the GaN HEMTs.

In spite of the good lattice match between SiC substrates and GaN, the commercialization of these devices is severely hindered by the high cost of SiC wafers (more than $2,000 for a 2" SiC wafer, compared to less than $100 for a 3" Si wafer). To solve this problem, GaN transistors have also been studied to grow on Si substrates and Chumbes *et al.* [5] reported the first successful growth of AlGaN/GaN HEMT structures on Si substrates in 1999. However, the performance of these devices was limited by the high electrical conductivity and poor thermal conductivity of the Si substrate (Table 1-2). For example, the maximum current gain cut-off frequency (f_T) of GaN-on-Si HEMTs is 18 GHz for a gate length of 0.7 µm, while in SiC grown AlGaN/GaN HEMTs values of 20 GHz are common. The difference is more important in maximum oscillation frequency (f_{max}). While GaN-on-Si devices show an f_{max} of 30-35 GHz for a gate length of 0.7 µm, values of 50-60 GHz are standard in GaN-on-SiC [6].



Substrate	Thermal Conductivity at 300K (W/cm-K)	Crystal Quality - Lattice mismatch to GaN (%)	Cost ($ / 4-inch wafer)
Sapphire	0.4	14.8	3,000
SiC	3.7-4.9	3.3	20,000
Si	1.3	17	3,000

Table 1-2. Main properties of some typical substrates for the heteroepitsxy of GaN layers.

Although GaN-on-Si HEMTs have shown inferior performance than GaN-on-SiC HEMTs, the Si substrate could still be the best alternative for future GaN devices. While the cost of SiC is intrinsically limited by material scarcity itself, the performance of GaN-on-Si HEMTs could significantly be improved with new device designs and proper optimization. Moreover, the flexibility given by the Si substrate allows for GaN to be integrated with state-of-the-art Si VLSI and even inspires completely new device schemes (i.e. double gated devices or GaN-Si hybrid circuits) with potentially unprecedented performance levels. Therefore, the optimized trade-off between the cost and the performance will pave the way for GaN-on-Si to become a competitive solution for next-generation HEMT power devices (Figure 1-3).

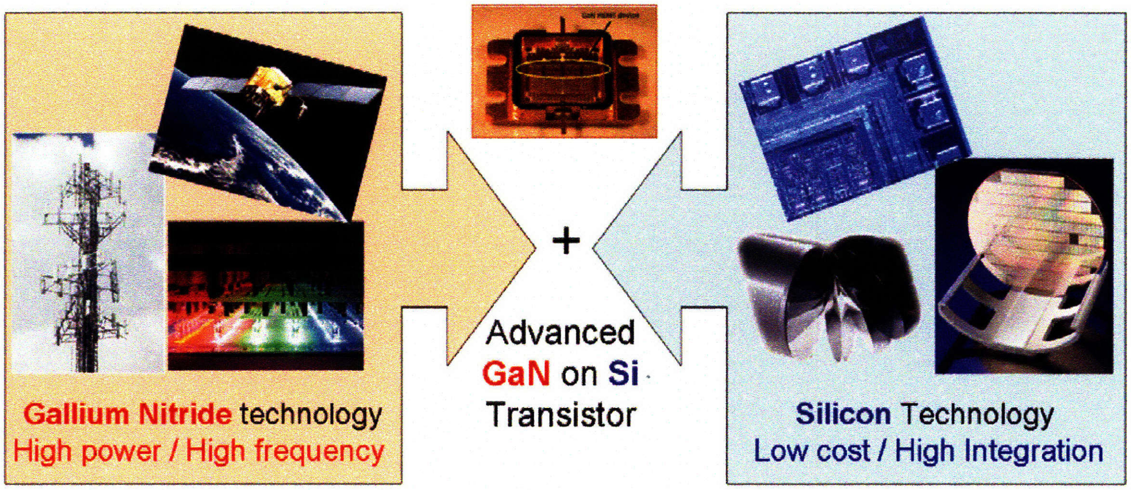

+
Advanced
GaN on Si
Transistor
Gallium Nitride technology
High power / High frequency
Silicon Technology
Low cost / High Integration

Figure 1-3. GaN-on-Si transistor is one of the best options for satisfying both low cost and maximum performance of GaN electronic products.

1.4. High Frequency Performance

When compared to other semiconductor families, nitrides have outstanding properties for the fabrication of high-frequency transistors (Table 1-1). Its excellent material properties in conjunction with a novel fabrication technology allowed very fast progress in high frequency performance of GaN. In 1994, Khan et al. [7] reported the first small-signal high frequency performance of an AlGaN/GaN transistor with 0.25 μm gate length. This transistor showed a current gain cut-off frequency (f_T) of 11 GHz and a power gain cut-off frequency (f_{max}) of 35 GHz. In 1997, Wu *et al.* [8] demonstrated and f_T of 50 GHz and an f_{max} of 92 GHz in a device with a gate length of 0.2 μm. In 2000, Micovic *et al.* [9] demonstrated AlGaN/GaN HEMTs with an extrinsic f_T of 110 GHz and f_{max} over 140 GHz with 0.15 μm gate length. In 2006, Palacios *et al.* [10] reported f_T of 153 GHz and f_{max} of 198 GHz with a gate length of 0.1 μm using InGaN back-barrier. Finally in 2007, Higashiwaki *et al.* [11] fabricated 30 nm gate AlGaN/GaN MIS-HFET and demonstrated f_T of 180 and f_{max} of 189 GHz.

Although these results are excellent, they are still below the theoretical predictions for this material system. Through this thesis, we will mainly focus on developing advanced technologies for improving high frequency operation of AlGaN/GaN HEMTs on either Si or SiC substrate. As seen in Figure 1-4, if the frequency performance of nitride transistors could be improved, its superior breakdown characteristics would make it the best option for power amplifiers at any frequency.

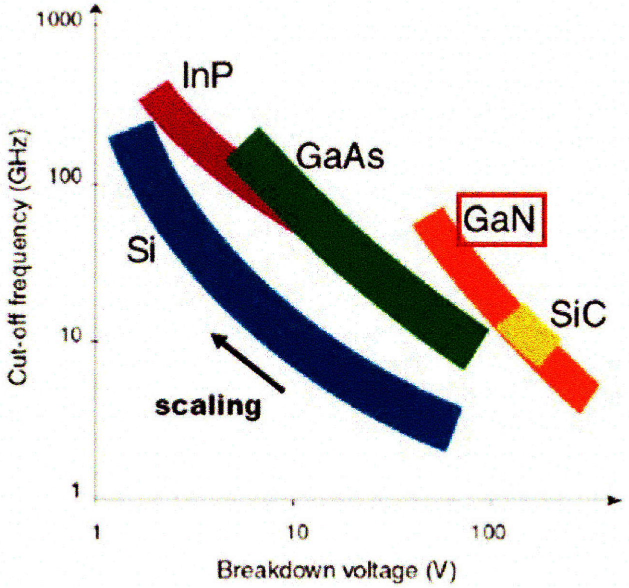


Figure 1-4. Curoff frequency and breakdown voltage curve for different semiconductor systems [12]. Although GaN is excellent for high power application, its high frequency performance is not fully explored yet.

1.5. Synopsis of the thesis

The main goal of this thesis is to identify, understand, and propose solutions to overcome the problems that limit the high frequency performance of GaN transistors. In order to achieve this goal, we performed a combination of theoretical studies, simulations and experimental work as will be seen in the following chapters.

Chapter 2 describes the basic process developed during this thesis to fabricate the first GaN transistors at MIT. Some of the steps that had to be developed include ohmic contact, mesa-isolation, and submicron T-gate processes. This chapter also described the DC and RF measurements used during this thesis to evaluate the performance of the standard and improved GaN transistors.

Chapter 3 discusses the effect of drain delay in the frequency performance of AlGaN/GaN HEMTs. Contrary to previous belief, we found that the effect of image charges in the drain delay of HEMT structures is different from that of HBT structure. Through theoretical analysis and 2-dimensional simulations, we have quantified for the first time the effect of image charges in a HEMT. This has been confirmed experimentally through the coupling of Monte Carlo simulations and drain delay measurements. Based on understanding of the image charge effect, we also propose a new device design for reducing drain delay.

Chapter 4 presents new techniques to improve charge control in 2DEG in high frequency operation of AlGaN/GaN HEMTs. Traditional equation of modulation efficiency is reexamined and we highlight importance of gate leakage current and gate-modulated traps on it. We show O_2 plasma treatment significantly reduces the gate leakage current. At the same time, we also find a strong correlation between gate leakage current and subthreshold characteristics in these devices. To estimate gate-modulated trap density we introduce a simple technique based on the temperature dependence of subthreshold slope.

Chapter 5 studies the use of N-face GaN/AlGaN HEMTs to increase the frequency performance of these devices. For the fabrication of these new devices, we developed a novel substrate removal and transfer technology. Two key steps of this technology are wafer bonding and GaN thinning processes. Initial results show a very promising performance improvement.

Finally in Chapter 6, summary and conclusions are presented. We will also discuss some future work that will allow us to expand the operating frequency of AlGaN/GaN HEMTs beyond mm-wave frequencies.

Chapter 2. Standard AlGaN/GaN HEMTs

The fabrication of nitride semiconductor devices at the Massachusetts Institute of Technology (MIT) was first started by Prof Tomás Palacios's group in 2006. In this project, we developed the entire deep-submicron AlGaN/GaN HEMTs fabrication technology. Some of the steps that had to be designed and optimized include photo-lithography, ohmic contact metallization, mesa-isolation, e-beam gate lithography, etc. In this chapter, we describe the optimization of three of the most important technological steps for achieving good high frequency performance; ohmic contact metallization, mesa-isolation, and submicron T-gate fabrication. Finally, we will show DC and RF performance of the first AlGaN/GaN HEMTs fabricated at MIT.

2.1. Nitride Technology

Because nitride-based semiconductors are thermally and chemically stable, it is attractive for many applications in harsh conditions such as high temperature and high pressure environment. However, due to their extremely high stability, every step of the fabrication of transistors in this material system is challenging. For example, the resistance of the ohmic contacts largely depends on the combination of different metal stacks (e.g. Ti, Al, Ni, Au, Mo, etc) and it is also very sensitive to the thickness of each layer. Also, the lack of a reproducible wet etching technique forces the use of dry etching such as chlorine-based plasma etching. However, dry etching is well known to create surface damage and degradation of the electrical properties of nitride-based semiconductors. Finally, the large bandgap and high electron scattering of nitride compounds reduces the resolution of the e-beam lithography technology, which increases the difficulty for defining deep-submicron gates in these materials.

In order to obtain excellent high frequency performance, it is imperative to fabricate transistors with low ohmic contact resistances, good pinch-off, and very short gate-length. From the processing point of view, these device parameters are related to ohmic contact metallization, mesa-isolation, and submicron T-gate fabrication, respectively. They are some of the most fundamental and important steps to ensure reliable and excellent operation of the device. More advanced techniques to further improve high frequency performance (i.e. gate recess, implantation, fluorine treatment, etc) are currently under development

2.2. Processing Optimization

In this section we will describe the main steps of the first generation of AlGaN/GaN HEMTs fabrication technology at MIT. All the devices described in this section were processed on AlGaN/GaN epilayers grown on Si (111) substrates at Nitronex Corporation [13] by metalorganic chemical vapor deposition (MOCVD). The layer-structure and cross-sectional SEM image of these samples are shown in Figure 2-1 and Figure 2-2, respectively.

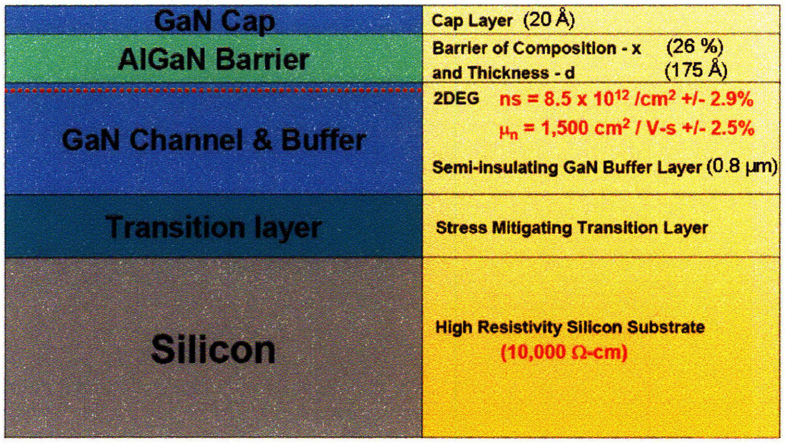

GaN Cap
AlGaN Barrier
GaN Channel & Buffer
Transition layer
Silicon
Cap Layer (20 Å)
Barrier of Composition - x (26 %)
and Thickness - d (175 Å)
2DEG ns = 8.5 x 10^12 /cm^2 +/- 2.9%
μn = 1,500 cm^2 / V-s +/- 2.5%
Semi-insulating GaN Buffer Layer (0.8 μm)
Stress Mitigating Transition Layer
High Resistivity Silicon Substrate
(10,000 Ω-cm)

Figure 2-1. Layer structure and profile of the AlGaN/GaN HEMT [14].

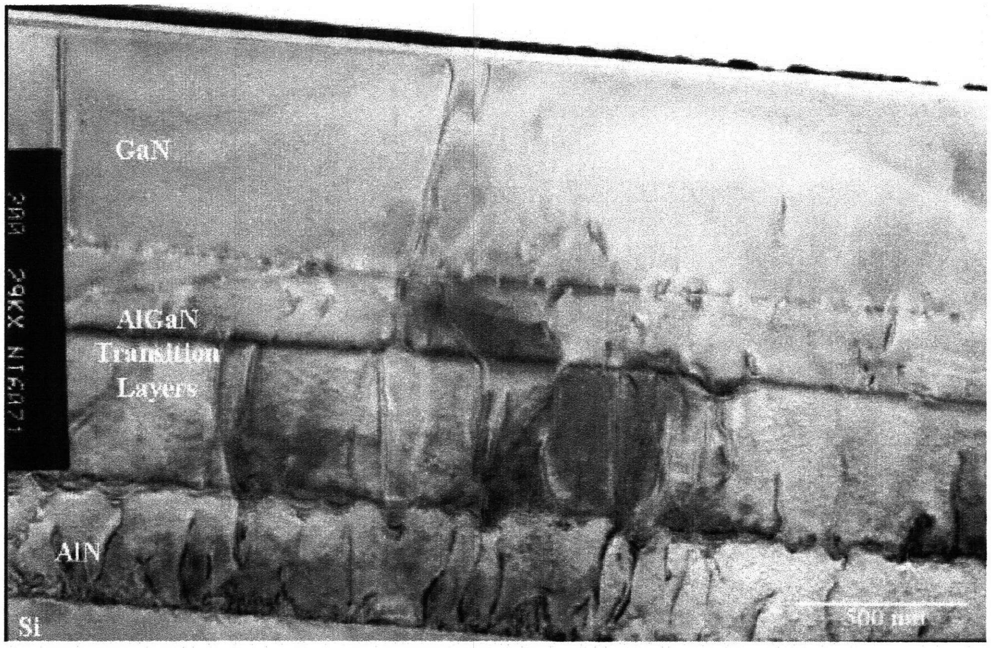


Figure 2-2. Cross-sectional SEM image of as-grown AlGaN/GaN heterostructure on Si (111) substrate [14].

2.2.1. Ohmic Contacts

Ohmic contacts need to have the lowest resistances possible to maximize efficiency and frequency performance. It is also important to get high thermal stability and smooth surface morphology to ensure high temperature operation and to facilitate sharp edge acuity for short channel devices, respectively. Among the many contact metallization schemes reported in the literature, the Ti/Al-based contacts are the most widely utilized. In this work, we utilize Ti/Al/Ni/Au scheme.

Titanium (Ti) is a key metal in the metallization scheme of III-nitride devices. After annealing it at high temperatures (800~900 °C) in the contact of a nitride semiconductors, it forms TiN, a semi-metallic compound with a work function of 3.74 eV [15]. The TiN layer creates N vacancies in the AlGaN/GaN structure which effectively dope the material. The resultant n^+-GaN interface and the conductive TiN constitute the necessary components for a tunneling contact. In addition, the formation of high melting point $TiAl_x$ inter-metallic layers stabilizes the contacts and prevents the contact structure from balling up. The Ni/Au bilayer cap is necessary to prevent diffusion and oxidation of Ti/Al at the annealing condition, respectively. Ni is a thermally stable metal (melting point >1400 °C), therefore it acts as a barrier against the out-diffusion of Ti/Al and the in-diffusion of Au. The Au overcoat is believed to have the effect of minimizing or preventing the oxidation of the underlying metallic layers, and also improving the conductivity of the contacts.

In this project, we performed systematic analysis of the effect of different Al and Ni thicknesses on the Ti/Al/Ni/Au contacts quality. Twenty different ohmic schemes were deposited on the same sample (Figure 2-3) and electrically measured through transfer length method (TLM) structures. All layers were defined by photo-lithography. Different Ti/Al/Ni/Au (200 / x / y / 500 Å) ohmics were deposited by e-beam evaporation, and annealed at 870 °C for 30s in N_2 ambient. Nominal Al thicknesses were 500, 1000, 1500, and 2000 Å and nominal Ni thicknesses were 0, 250, 500, 750, 1000 Å. A two-dimensional grid scheme was used and all possible Al/Ni thicknesses combinations were tested. To minimize the number of metallization steps, the 200 Å Ti layer was deposited first and then the different Al thicknesses were reached by sequential 500 Å depositions, progressively covering columns of the sample with a hard mask. The same procedure was applied by rows during Ni deposition. A 500 Å Au layer completed the structure. Base pressure during the metallization was always below 1×10^{-6} Torr. Mesa-isolation was obtained by ECR-RIE etch (it will be discussed in the next section). Plasma conditions were ECR=100 W, RF=25 W, 10 mtorr pressure, 20 sccm BCl_3 flow rate, and 5 sccm Cl_2 flow rate, corresponding to an etch rate of 3.7 Å/s. TLM contact spacings were 5, 10, 15, 20, and 25 μm and the width of the TLM patterns were 100 μm.

As shown in Figure 2-3 and Figure 2-4, not all compositions resulted in ohmic contacts. The lowest ohmic contact resistances were obtained for an Al/Ni=1000/250 Å and Al/Ni=500/0 Å. However, metal surface morphology was poor for Ti/Al/Au alloys and surface roughness was improved by the addition of a thin layer of Ni. Based on this result, the Ti/Al/Ni/Au alloy (200/1000/250/500 Å) was chosen as the standard metallization scheme in our GaN technology. It should be noted that the values obtained by this systematic study do not give the best ohmic contact resistances. Breaking the vacuum condition each time to progressively cover columns and rows of the sample contaminates metal interfaces and therefore degrades contact resistance. In the past six months, many samples have been processed with this technology and contact resistances in the range of 0.4-0.5 Ω·mm has been routinely obtained (Figure 2-5).

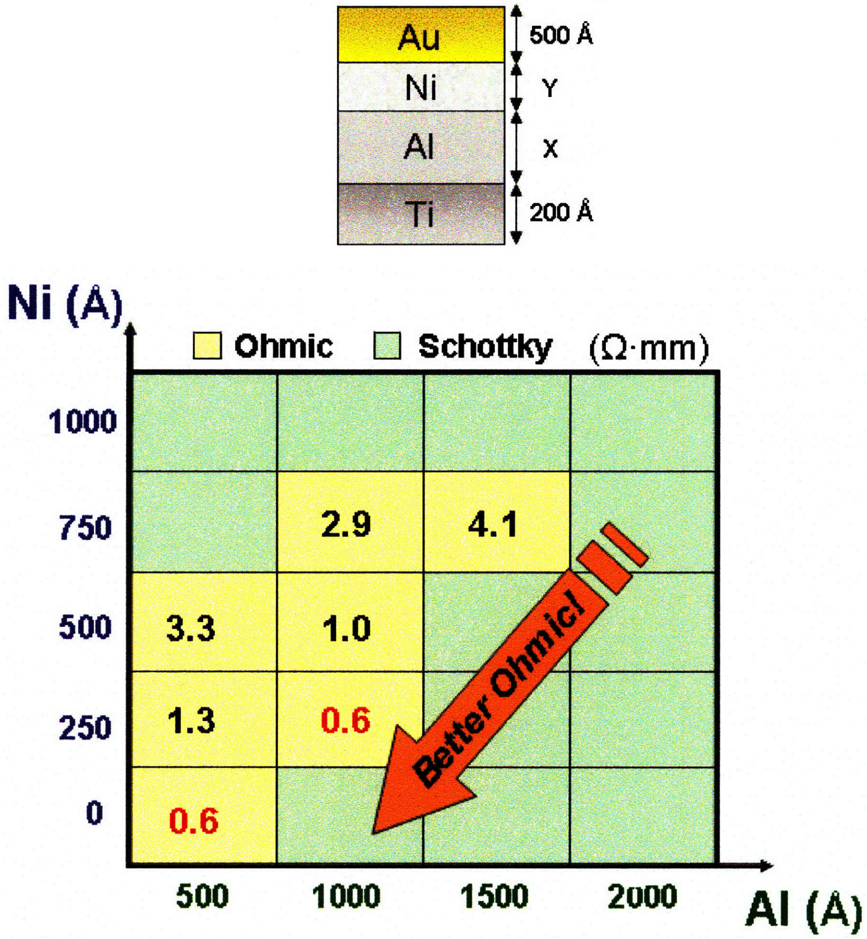


Figure 2-3. Measured contact resistance as function of metal layers thicknesses.

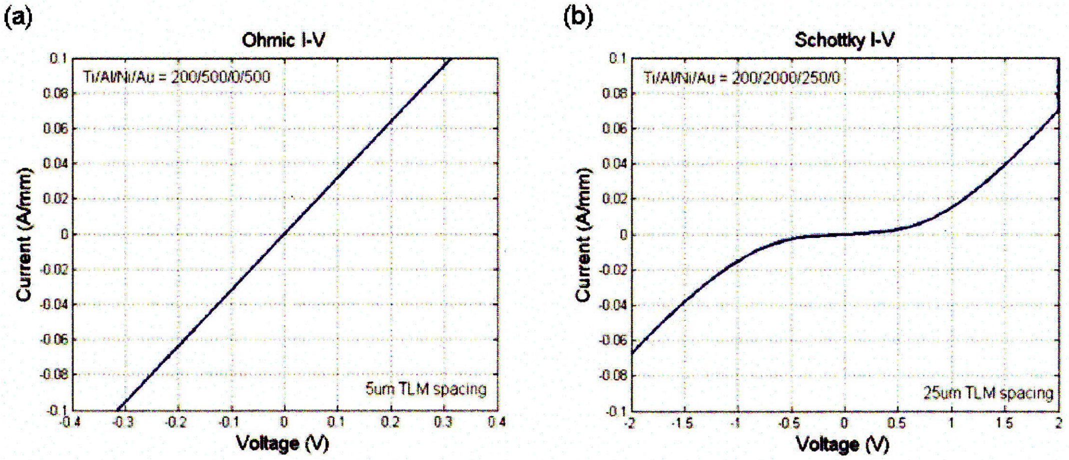


Figure 2-4. Comparison between (a) truly ohmic and (b) slightly rectifying contacts depending on different Ti/Al/Ni/Au metal thicknesses.

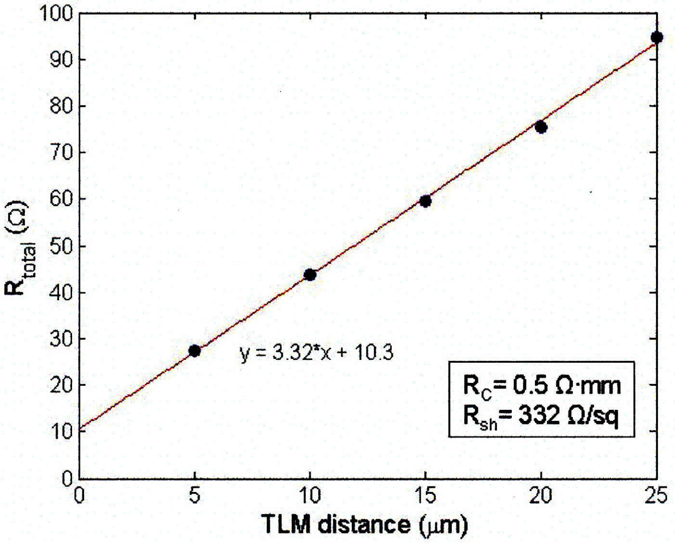


Figure 2-5. TLM measurement of typical ohmic contacts on AlGaN/GaN HEMTs (Ti/Al/Ni/Au=200/1000/250/500 Å).

2.2.2. Mesa-Isolation

After the formation of ohmic contacts, adjacent devices (or active regions) must be isolated by etching through the conducting channel as shown in Figure 2-6. Poorly isolated devices have large leakage current which results on bad pinch-off and poor frequency performance and efficiency. For the complete isolation, the etch depth should be around 1500~1800 Å in order to fully remove 2DEG between active regions.

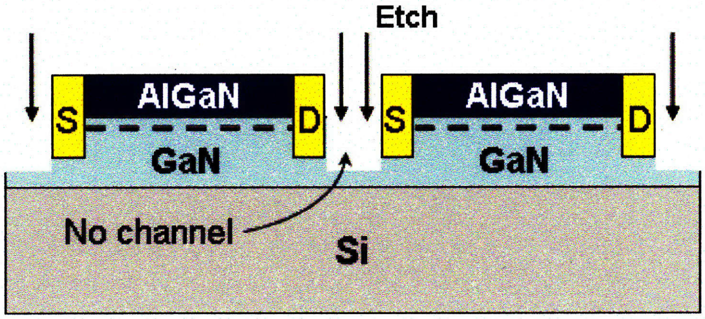


Figure 2-6. Schematic illustration of mesa-isolation.

Owing to the chemical inertness of GaN and AlGaN, there is not yet a suitable wet etching method for either mesa-isolation or gate recess. Therefore, we use a dry etching technology based on electron cyclotron resonance reactive ion etching (ECR-RIE) with Cl_2/BCl_3 gas mixture, which is one of the most popular methods to etch GaN. Figure 2-7 shows two different recipes we developed. The recipe (a) etches GaN faster than the recipe (b) due to its two times higher ECR power. However, increased power damages surface more severely, so the surface roughness was worse in the case of recipe (a). From this result, the recipe (a) can be used for mesa-isolation and the recipe (b) is suitable for gate-recess.

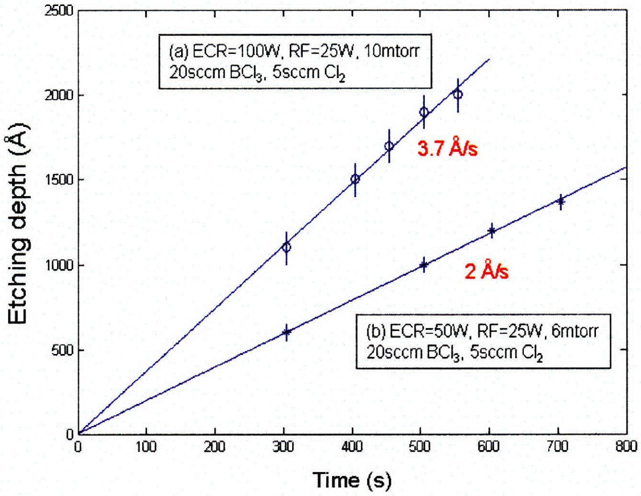


Figure 2-7. Two recipes developed for etching GaN. There is a trade-off between etch rate and surface roughness [16].

2.2.3. Deep submicron T-gate technology

After active regions are defined by mesa-isolation, deep-submicron T-gates (less than 100 nm) are fabricated by e-beam lithography. Typically, sub-micron gates are fabricated with T-shape cross section to reduce their resistance when compared to a standard rectangular gate. Low gate resistances are critical to maximize the gain and noise performance of the device [17].

During the development of the deep-submicron gate technology, we used a tri-layer resist structure of the LO/HI/LO (low resolution/high resolution/low resolution) system based on Polymethylmethacrylate (PMMA) and its methacrylic acid copolymer (PMMA/MAA). The tri-layer scheme offers much more robust lift-off processes than the bi-layer scheme. Each resist was spin-coated as shown in Figure 2-8(a) (PMMA/Copolymer/PMMA) and the thickness of each layer was 200/500/200 nm, respectively.

Gate mask exposure was performed by Raith 150 e-beam lithography system. Figure 2-8 shows the whole exposure and development procedure for fabricating submicron T-gate. It involves two exposure and two development steps. The amount of exposure dose and development time was optimized through the use of an exposure array. The optimized exposure doses for the head and the foot of the gate were 125 and 700 $\mu As/cm^2$, respectively. After the first exposure (head exposure), pure methyl-isobutyl-ketone (MIBK) was used for 60s to develop the top PMMA and subsequently the sample was dipped in methanol:isopropanol (IPA)=1:1 mixture for 20s to develop copolymer layer. The excellent selectivity of this chemical avoids the development of the bottom PMMA. After the second exposure (foot exposure), MIBK: IPA=1:3 mixture (diluted MIBK) was used for 60s at 21 °C to develop the bottom PMMA. It is noted that making MIBK: IPA mixture is an endothermic reaction, so if both solvents are at 21 °C before mixing them the resultant mixture is about 15 °C. It is important to wait until the temperature of the mixture reaches at 21 °C. The use of a 1:3 ratio is also important in order not to overdevelop narrowly defined (less than 70 nm) gate foot. Finally, Ni/Au/Ni (200/2000/500 Å) multilayer was deposited for the Schottky contact. Figure 2-9 shows SEM image of successfully fabricated

50 nm T-gate. Using this technology, it is possible to fabricate gate lengths even below 50 nm, however 70 nm gate length is the shortest gate length that can be reproducibly achieved.

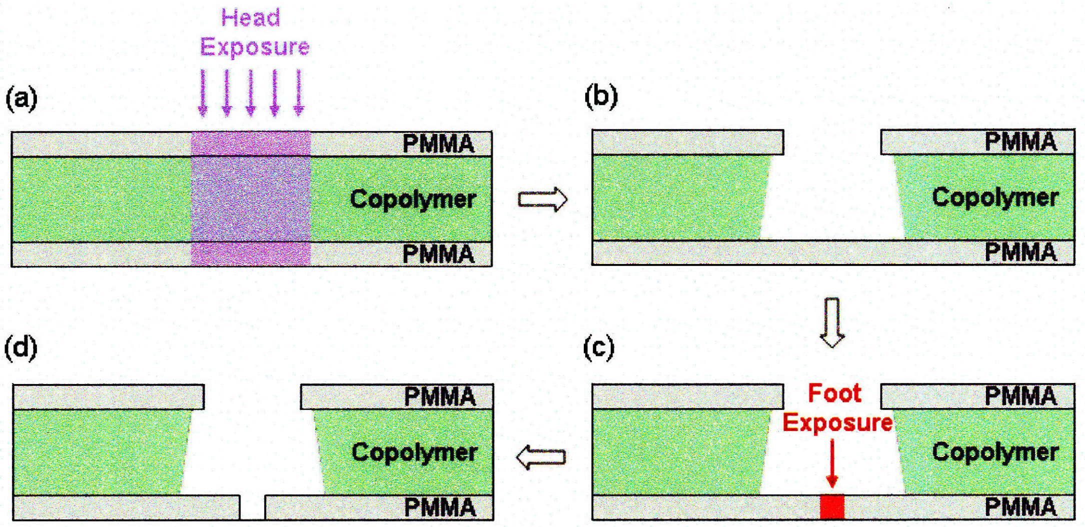

Head
Exposure
(a)
PMMA
Copolymer
PMMA
(b)
PMMA
Copolymer
PMMA
(d)
PMMA
Copolymer
PMMA
(c)
Foot
Exposure
PMMA
Copolymer
PMMA

Figure 2-8. E-beam lithography process for submicron T-gate fabrication. (a) 1st head exposure (dose= 125 μAs/cm^2), (b) 1st development (60s in pure MIBK, followed by 20s in methanol:IPA=1:1), (c) 2nd foot exposure (dose= 700 μAs/cm^2), (d) 2nd development (60s in MIBK:IPA=1:3)

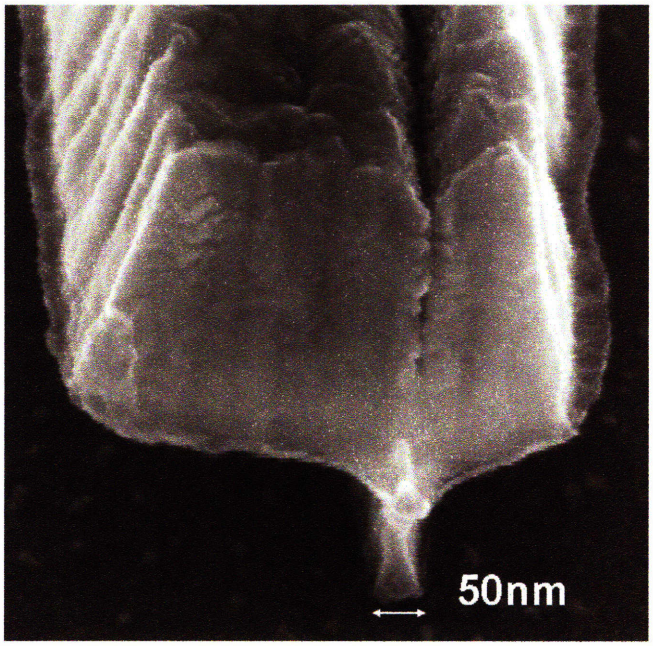


Figure 2-9. SEM image of fabricated 50 nm T-gate.

2.3. Device Characterization

By combining all these optimized technologies, we fabricated our first AlGaN/GaN HEMTs on Si substrate at MIT.

2.3.1. DC performance

Figure 2-10 through Figure 2-12 show DC characteristics of a typical 0.5 μm gate-length AlGaN/GaN HEMT. It should be noted that in these transistors, an O_2 plasma treatment was applied to reduce gate leakage current and improve subthreshold slope (this surface treatment will be discussed in chapter 4).

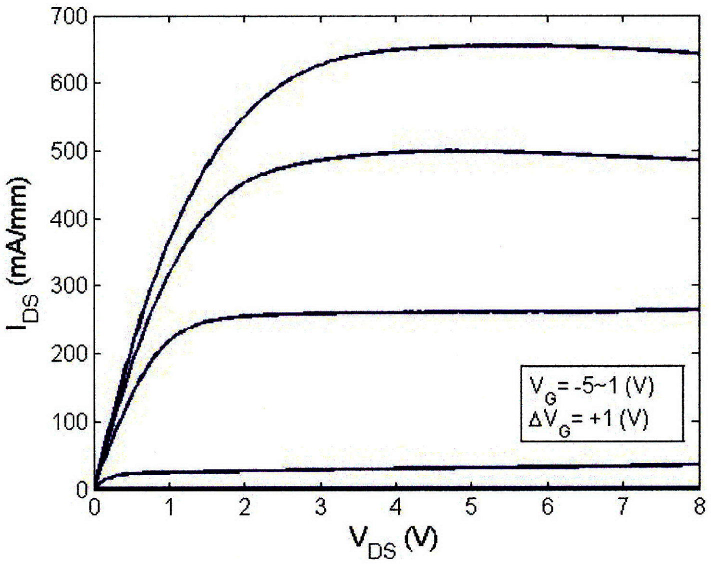


Figure 2-10. DC current-voltage characteristics of a 0.5μm gate-length AlGaN/GaN HEMT.

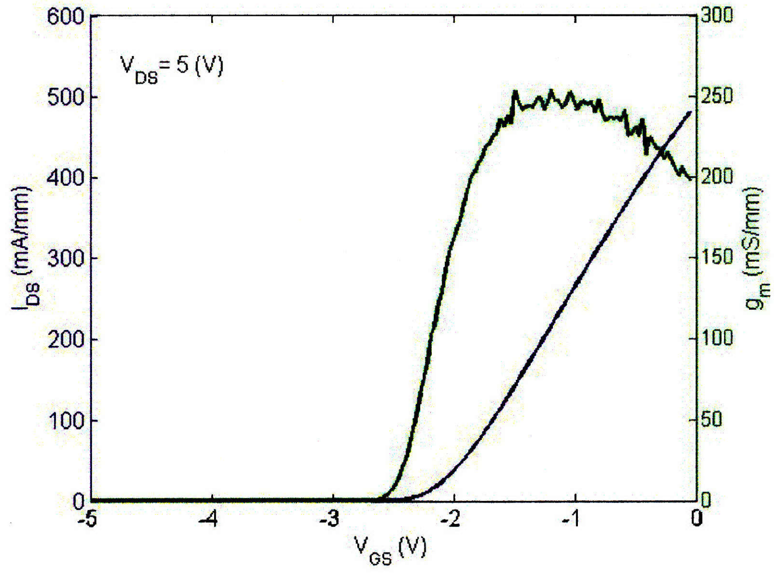


Figure 2-11. Transconductance (g_m) characteristics of a 0.5µm gate-length AlGaN/GaN HEMT.

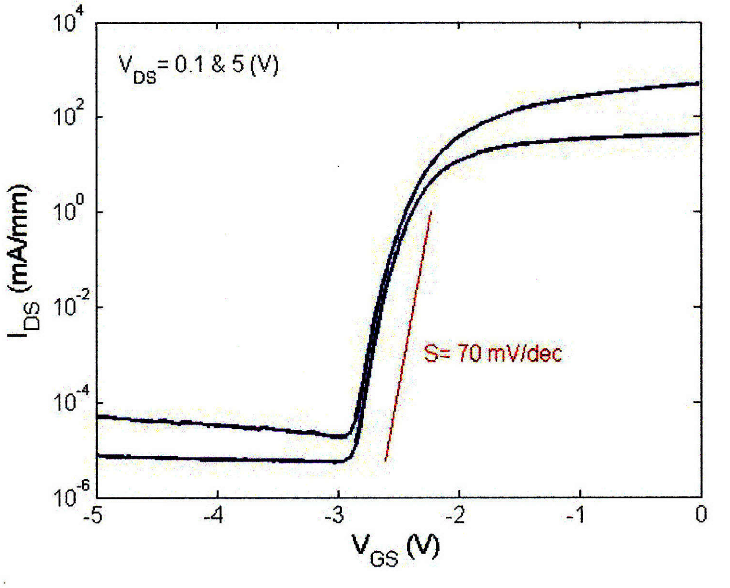
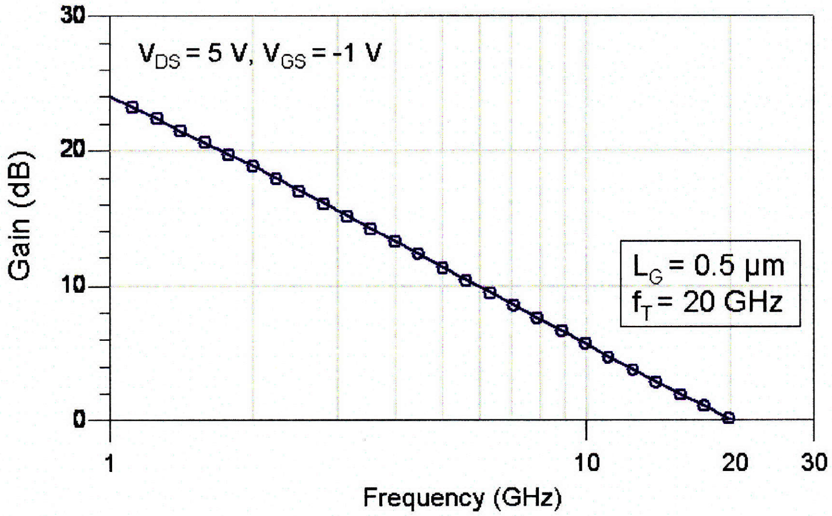


Figure 2-12. Subthreshold characteristics of a 0.5µm gate-length AlGaN/GaN HEMT at V_{DS}=0.1 and 5 V. Subthreshold slope is 70 mV/decade at V_{DS}=5 V.

2.3.2. RF Performance

The cutoff frequency f_T and maximum frequency f_{max} are the most important figures of merit for the RF characteristics of microwave transistors. The f_T is the frequency at which the magnitude of short circuit current gain (h_{21}) equals unity and f_{max} is defined as the frequency at which the unilateral power gain U equals unity. From a physical point of view, f_T and f_{max} are the maximum frequency at which the transistor still provides a current gain and a power gain, respectively. Figure 2-13 shows f_T and f_{max} of our 0.5 × 70 μm (gate-length × gate-width) AlGaN/GaN HEMT biased for maximum transconductance (g_m) in Figure 2-11.



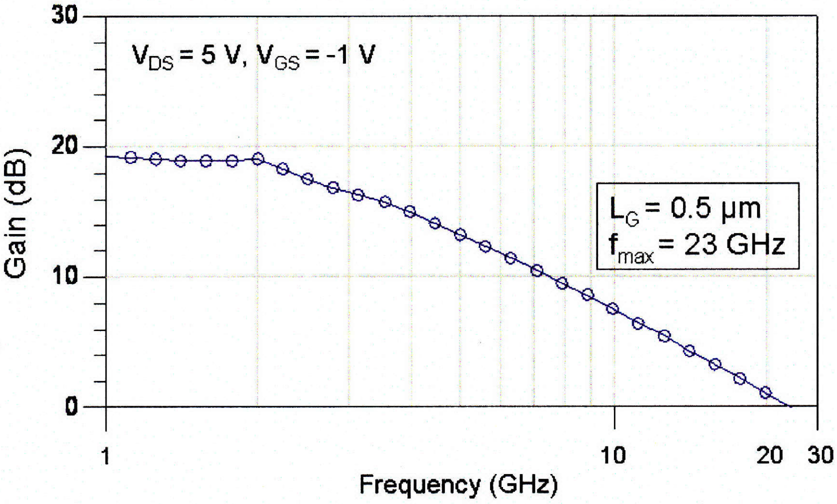


Figure 2-13. Small-signal performance of an unpassivated 0.5 μm gate-length AlGaN/GaN HEMT on Si substrate. f_T= 20 GHz and f_{max} = 23 GHz were achieved at the bias condition of V_{DS} = 5 V and V_{GS} = -1 V. The relatively low f_{max} value is due to the parasitic capacitance introduced by the Si substrate.

2.4. Summary

In this chapter, we have developed a basic submicron T-gate AlGaN/GaN HEMT fabrication technology. Ohmic contact, mesa-isolation, and submicron T-gate fabrication processes are optimized for a correct device operation. DC and RF characteristics are measured and the performance is adequate to apply the new advanced technologies described in future chapters to further improve high frequency performance in this device.

Chapter 3. Drain Delay Analysis

The drain delay in AlGaN/GaN deep submicron high electron mobility transistors (HEMTs) accounts for almost 25% of the total electron delay. This long delay significantly limits the maximum frequency performance and linearity of these devices. In this chapter, we study the origin of this important delay and how it is coupled to channel electrons imaging at the different contacts in the HEMT. Through analytical analysis and 2-dimensional simulations we have found that this coupling makes the drain delay three times shorter than previously thought. It has been confirmed experimentally through the coupling of Monte Carlo simulations and drain delay measurements.

3.1. High Frequency Operation

One of the new challenges in GaN electronics is to increase their frequency of operation to millimeter and sub-millimeter wave frequencies. To achieve this goal improved growth in combination with the introduction of new device structures such as InGaN [10] and AlGaN back-barriers [18] and Cat-CVD SiN gate-insulating and passivation layers [19] have been recently reported. These new structures have allowed devices with a current gain cut-off frequency (f_T) in excess of 150 GHz and a maximum oscillation frequency (f_{max}) of 230 GHz in AlGaN/GaN HEMTs with a gate length of 100 nm. However, in spite of these excellent results, nitride devices are still far from their theoretically expected maximum performance.

3.2. Time-Delay Factors; Drain Delay

The operating frequency of a HEMT is inversely proportional to the total delay of the carriers across the transistor (τ_{total}). Following Moll *et al.*'s analysis [20], τ_{total} can be divided in three different components: intrinsic delay (τ_{int}), channel charging delay ($\tau_{channel}$), and drain delay (τ_{drain}). τ_{int} is the time taken by the electrons to cross the channel region under the gate, $\tau_{channel}$ is the time needed to charge and discharge the parasitic capacitances, and τ_{drain} is the time required by the electrons to cross the depletion region induced at the drain side of the gate. Figure 3-1 shows each delay component in a standard AlGaN/GaN HEMT.

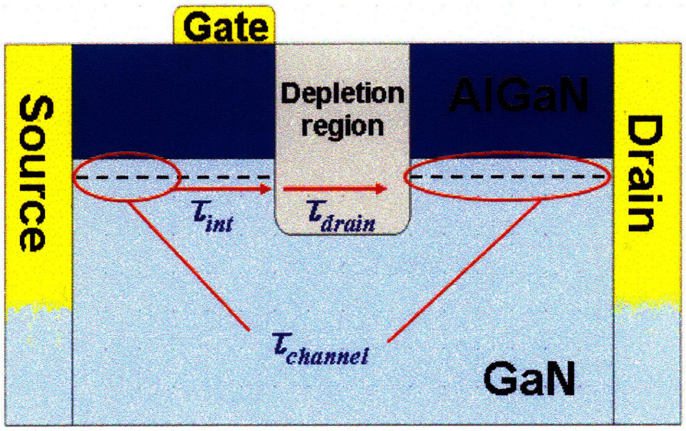


Figure 3-1. Schematic illustration of each delay factor, τ_{int}, $\tau_{channel}$, and τ_{drain} in a standard AlGaN/GaN HEMT.

Among the three different components of the electron delay, τ_{drain} is the most important as the geometry of AlGaN/GaN HEMTs is scaled down to sub-micrometer range (<100 nm). As shown in Figure 3-2, τ_{int} decreases when scaling down the devices dimensions, however τ_{drain} (and in less degree $\tau_{channel}$) remains constant and ultimately limits the maximum frequency performance of these transistors. This is because τ_{int} and $\tau_{channel}$ depend largely on the length of the gate and the source/drain access region, respectively, however τ_{drain} (or depletion region) is given by the applied voltage between the drain and gate contacts and the channel doping.

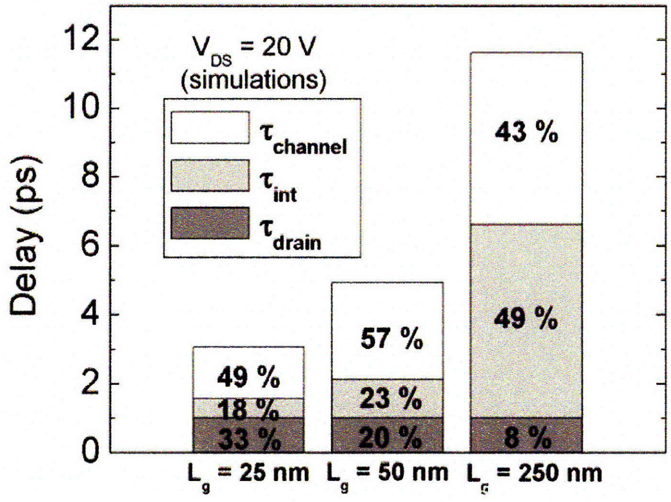


Figure 3-2. Effect of the different components of the electron delay in the performance of AlGaN/GaN HEMTs with several gate lengths.

Moreover, τ_{drain} also affects the linearity of f_T and f_{max} with drain voltage. As shown in Figure 3-3, the increase in drain voltage causes a reduction in f_T and f_{max} of more than 30 % at high drain voltages. This decrease severely limits the large signal linearity of the transistor due to the associated nonlinearity of the gain. The origin of this decrease with drain voltage is commonly associated to the increase in the width of the depletion region at the drain side of the gate and, therefore, drain delay as the drain voltage increases.

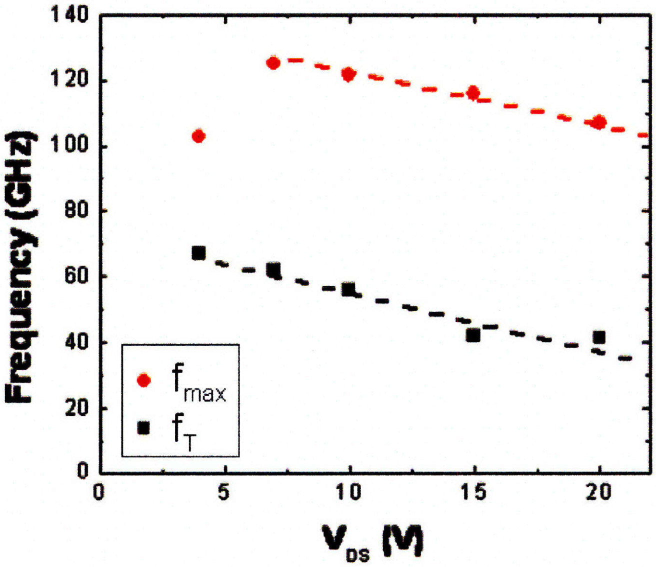


Figure 3-3. Variation of f_T and f_{max} with drain voltage in a typical AlGaN/GaN HEMT.

3.3. The Origin of Drain Delay

In spite of the great importance of the drain delay in the performance of deep-submicron devices, this delay has only been scarcely studied so far. In the following sections in this chapter, we will analyze the origin of drain delay in AlGaN/GaN HEMTs to understand its contribution to the high frequency performance and to be able to engineer it in future generation devices.

3.3.1. Effect of Image Charges

From a physical point of view, the drain delay in HEMTs is the time taken by the channel electrons to cross the depletion region induced at the drain side of the gate. The transport of the negative sheet of charge formed by the channel electrons across the depletion region induces image charges in the nearby contacts and highly conductive access regions (i.e. gate contact and source and drain access regions). This image charge modifies the electric field in the depletion region, which ultimately affects the carrier transport in that region. This mechanism is similar to that in the collector-base space charge region of heterojunction bipolar transistors (HBTs) which is responsible of the collector delay in these devices (τ_c). The collector delay in HBTs has been extensively studied in the past from the current transfer function [21] and charge-control analysis [22]. These previous work has shown that if v_e is the scattering-limited velocity of carriers traveling through the collector-base space charge region having width w, then $\tau_c = w/(2 \times v_e)$. The factor of 2 in the denominator of this expression accounts for the image charge induced at both sides of the space charge region when the carriers are crossing this region [23].

By analogy with HBTs, we define the drain delay (τ_{drain}) in HEMTs as

$$\tau_{drain} = \frac{w}{\alpha \times v_e} \tag{1}$$

where w is the width of the depletion region, v_e is the electron velocity and α is a constant given by the effect of image charges in the carrier transport. In HBTs, α is equal to 2 [21-

23]. However, the value of α has not been studied in detail in field effect transistors and several reports offer contradictory values. For example, some authors neglect the effect of image charges in the transport of electrons accross the drain depletion region and assume α equals to 1 [24-26]. Others texts, on the other hand, assume a behavior identical to the case of HBT devices and use a value of α equal to 2 [27]. In this section we have used a combination of charge control analysis and 2-dimensional simulations to calculate the value of α in HEMTs. From our work, α should have a value of 3 to accurately take into account the effect of image charges in the transport of electrons through the depletion region of a HEMT. This value has been confirmed experimentally through the coupling of Monte Carlo simulations and drain delay measurements.

Using charge control analysis in a way analog to the method used to calculate the collector delay in an HBT [22], τ_{drain} in a HEMT can be written as

$$\tau_{drain} = \frac{dQ_{inj}}{dJ} = \frac{dQ_{inj}}{d\rho}\frac{1}{v_e} = \frac{dq_{im,s}}{dq_{inj}}\frac{w}{v_e} \tag{2}$$

where Q_{inj} is the injected charge density (C/m^2) in the depletion region, J is the current density (A/m^2) in the transistor channel, w is the width of the depletion region, ρ is the volume charge density (C/m^3) in the source region moving to the depletion region, $q_{im,s}$ is the image charges induced in source access region and q_{inj} is the total charge of the injected carriers into the depletion region. By combining equation (1) and (2), we can express α as the ratio of injected charges in the depletion region to image charges in the source access region:

$$\alpha = \frac{dq_{inj}}{dq_{im,s}} \tag{3}$$

To calculate this ratio in AlGaN/GaN HEMTs, 2-dimensional simulations of the electric field in these devices have been performed using COMSOL Multiphysics 3.2 (formerly FEMLAB). The Electrostatics Application Mode of this simulation software can simulate the electrical properties (e.g. electric field, potential, image charge densities, etc) in dielectric materials with a fixed charge present. In this work, each contact or heavily doped access region (i.e. gate contact and source and drain access regions), two-dimensional electron gas (2DEG) channel and depletion region in a standard HEMT were defined with scaled conductive lines. After numerically solving the electrostatic equations, COMSOL calculates the amount of image charges at the source side of the channel ($dq_{im,s}$) when injecting dq_{inj} charges into the depletion region.

To validate our model and the simulation software, the case of an HBT was simulated as shown in Figure 3-4. In this 2-dimensional small signal analysis, the base and collector regions are grounded and 2×10^{-8} (C/m) of negative charges are uniformly distributed into a 2 μm length space charge region. After redistribution of image charges, the calculated image charge at the base region is 9.87×10^{-9} (C/m), which induces an α equal to 2.03, as expected in an HBT.

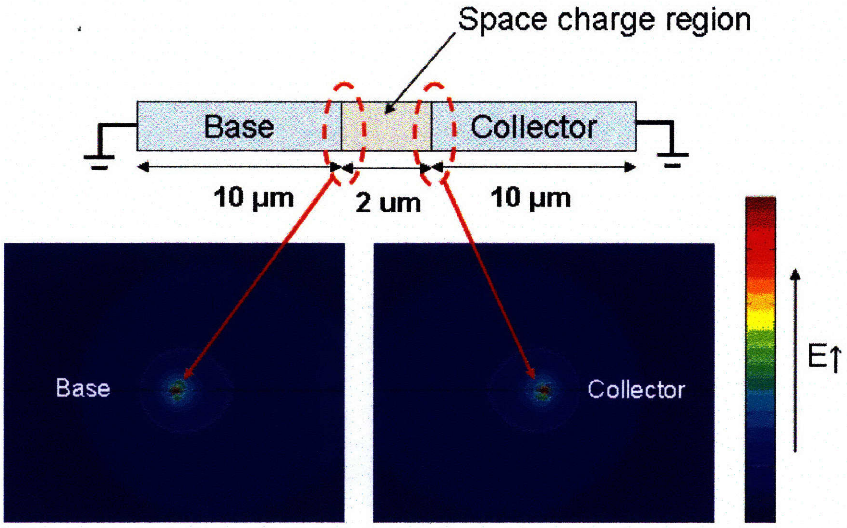


Figure 3-4. Schematic illustration of simulated HBT structure model and resulting electric field after redistribution of image charges. Actual horizontal dimensions are not critical to calculate the value of α.

Figure 3-5 shows the simulated model structure for an AlGaN/GaN HEMT. The main difference between the HEMT model and the HBT model of the depletion region is the addition of a 200 nm-long gate contact. The distance between this contact and the 2DEG is only 15 nm. In this structure, using a highly densified mesh, simulation results produce a $q_{im,s}$=6.65×10^{-9} (C/m) for a q_{inj}=2×10^{-8} (C/m), and thus α=3. Because in the HEMT structure the injected charges also image at the gate metal (only 15 nm above the channel), $q_{im,s}$ is about 33% less than in the HBT case (where the charges cannot image at the gate). It should be noted that no change was observed in the value of α for different widths of the depletion region. The value of α is also roughly independent (<1% change) of the distance between the gate metal and the 2DEG (5 nm ~ 30 nm), although it is expected to decrease for longer distances.

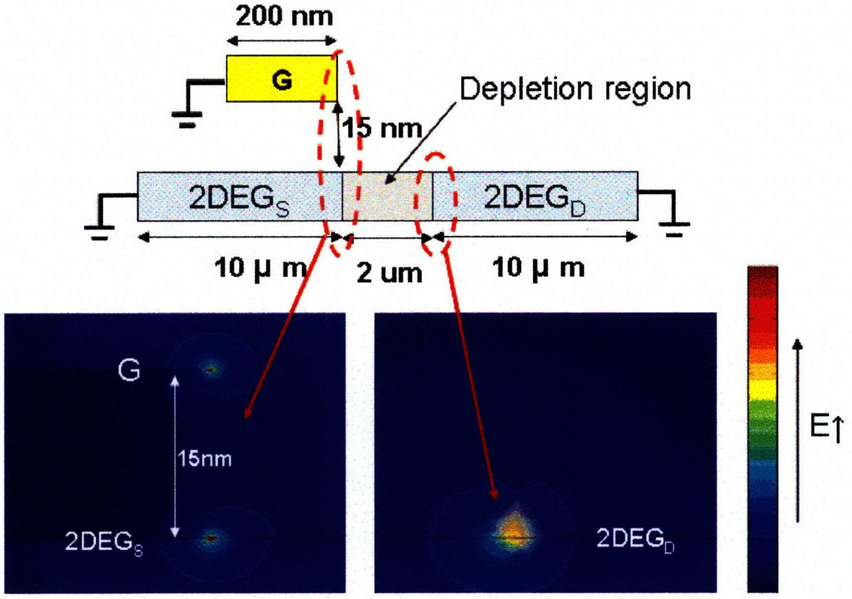


Figure 3-5. Schematic illustration of simulated HEMT structure model and resulting electric field after redistribution of image charges in the source, drain and gate contacts. 2DEG$_S$ and 2DEG$_D$ are 2-dimensional electron gases (2DEG) in the source access region and drain access region, respectively.

3.3.2. Experimental Verification

To verify the value of α=3, we have compared the value of the electron velocity given by equation (1) with the value predicted by Monte Carlo simulations in AlGaN/GaN HEMTs similar to the ones reported by Palacios *et al.* [28]. The devices used in this study have a gate length of 160 nm. When applying equation (1), the width of the depletion region is calculated from the change in effective gate length ($L_{G,eff}$) as a function of drain voltage (V_{DS}) given by simulations of the charge density in the channel (Figure 3-6) [29]. From these simulations, for every volt applied to the drain contact, the effective gate length increases 8.9 nm.

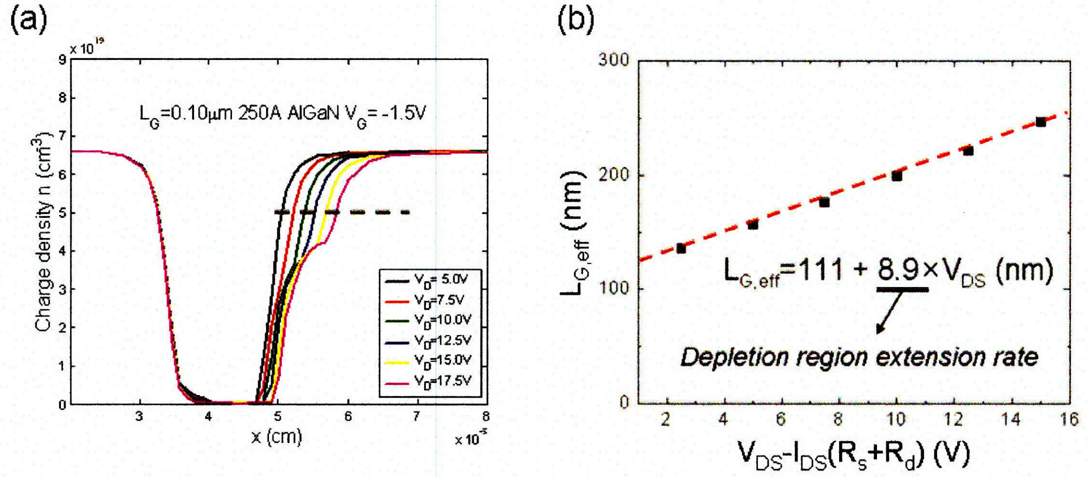


Figure 3-6 (a) Simulated charge density in the channel as a function of applied drain voltage and (b) effective gate length as a function of drain voltage extracted from (a).

On the other hand, the drain delay was measured applying Moll's analysis [20]. By measuring τ_{total} at different V_{DS} conditions, the drain delay at a given V_{DS} can be calculated as the difference between the actual measured delay and the extrapolated delay at V_{DS}=0 V. Figure 3-7 shows that the drain delay increases 0.03 ps per additional volt in drain voltage.

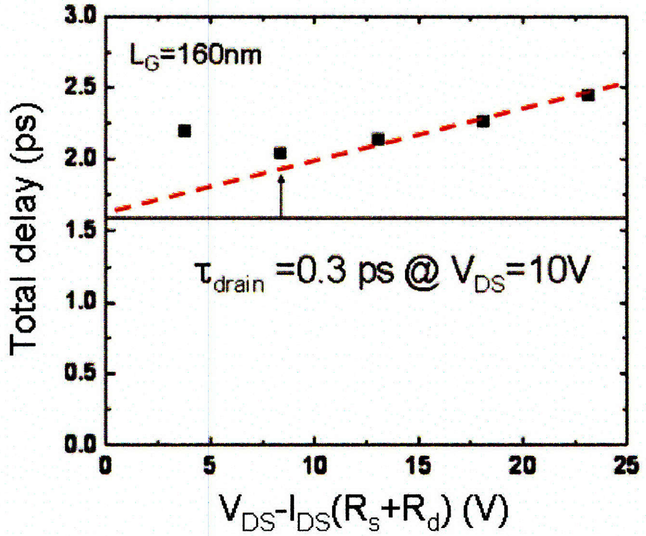


Figure 3-7. Measurement of drain delay in an AlGaN/GaN HEMT with 160 nm gate length.

Combining both the increase of the depletion region (8.9 nm/V) and the drain delay (0.03 ps/V) with drain voltage, the electron velocity in the depletion region can be calculated by applying equation (1) as:

$$v_e = \frac{w}{\alpha \times \tau_{drain}} = \frac{w}{3 \times \tau_{drain}} = \frac{8.9nm}{3 \times 0.03ps} \cong 1 \times 10^7 \quad \text{(cm/s)} \qquad (4)$$

Only α=3 allows a good agreement with the saturated electron velocity predicted by Monte Carlo simulations [29]. Typically, the electric fields in the depletion region at the drain side of the gate are very high, in excess of 200 (KV/cm). Under these values of electric field, the electron velocity is expected to saturate ($v_{e,sat} \sim 1 \times 10^7$ cm/s). This value is the same as predicted by equation (4). The use of α different from 3 (e.g. 1 or 2) would make the experimental value to differ more than 50% from the theoretically expected value.

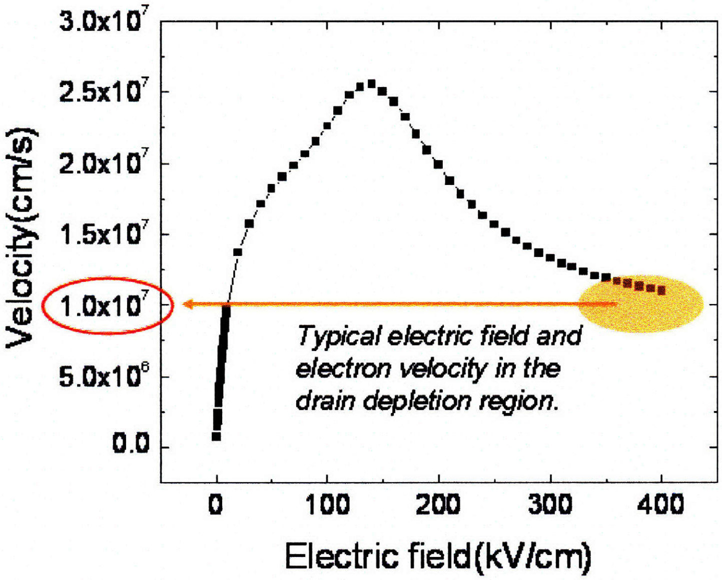


Figure 3-8. Monte Carlo simulation of the electron velocity in an AlGaN/GaN structure [].

3.4. New Transistor Designs to Reduce Drain Delay

It should be noted that the value of α depends on how the injected channel electrons image at the different contacts. Therefore, by changing the contact structure in these devices the drain delay in a HEMT can be engineered. This is the case of field-plated or Fin-FET structures. By adding a field plate structure and by varying its length and position, our simulation predicts at least a 2-fold improvement in the value of α; therefore improving the drain delay and linearity (Figure 3-9). These results agree with the improved linearity observed in field-plated devices [30]. The drawback of this approach is the introduction of additional gate capacitances which increase channel delay ($\tau_{channel}$). Therefore, it is necessary to optimize the structure of the device in order to achieve improved linearity and high speed performance.

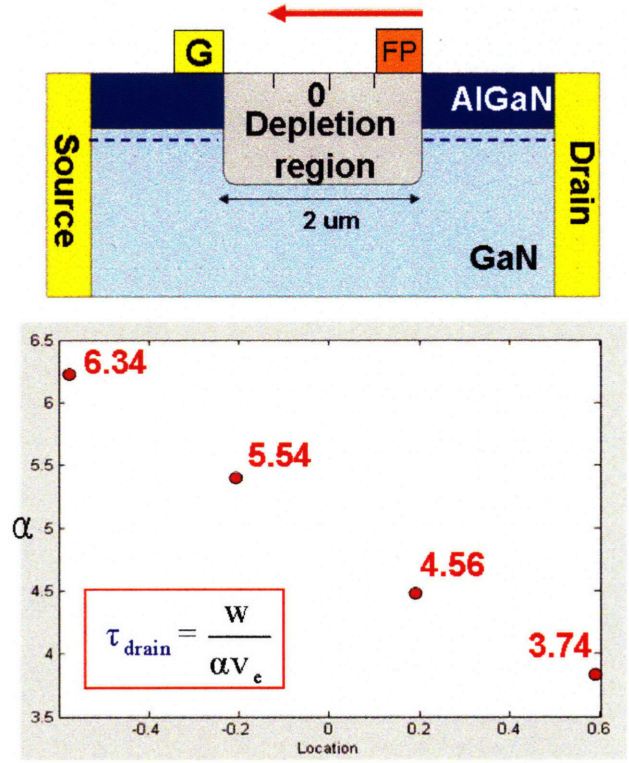


Figure 3-9. α increases (drain delay reduces) as field-plate(FP) approaches gate.

Another transistor design that can benefit from reduced drain delay is a nanowire FET. As shown in Figure 3-10, an AlGaN/GaN nanowire FET has all-around gate contact. Injected electrons to the depletion region (2μm) induce image charges at different contacts in a nanowire FET as in the case of a standard HEMT, however in nanowire FET more portions of injected electrons are imaged at the gate contact and increase the value of α to 26.6. Therefore the high frequency performance of a nanowire FET is less limited by the drain delay and this structure is very promising for beyond mm-wave applications.

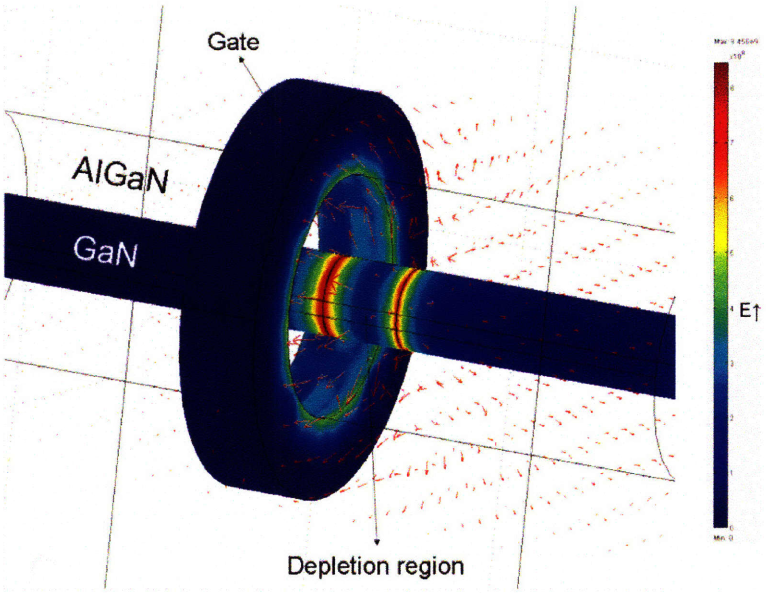


Figure 3-10. Schematic illustration of simulated AlGaN/GaN nanowire 3D structure model and resulting electric field after redistribution of image charges in the source, drain and gate contacts. α is calculated as 26.6.

3.5. Summary

In this chapter, we have studied the effect of image charges in the drain delay of AlGaN/GaN HEMTs. Although we have focused on HEMTs, the same analysis can be applied to any other kind of field effect transistor (FET). From our studies, in standard HEMTs, α (i.e. the proportionality factor between the drain delay and the drain depletion width) equals 3 and this value explains both theoretical predictions and experimental results of the value of the drain delay in these devices. Understanding the origin of drain delay is an important step to improve high frequency performance of AlGaN/GaN HEMTs and it opens the door to further improvements in the frequency performance of these devices by engineering how the injected channel charges image in the contacts.

Chapter 4. Charge Control in 2DEG

Traps (due to surface states, defects or dislocations) and gate leakage current severely degrade the high frequency performance of AlGaN/GaN HEMTs. They impede the gate control of 2DEG channel electrons and degrade modulation efficiency. Therefore, it is very important to quantify and minimize the effect of both traps and gate leakage current. In this chapter, we first introduce a modified concept of modulation efficiency which incorporated the effect of gate leakage current. Then, we study the effect of gate leakage in the subthreshold characteristics of GaN HEMTs. By using an O_2 plasma treatment, excellent gate leakage characteristics have been obtained and the devices show near-ideal subthreshold slope. Finally, we demonstrate a new method to estimate trap density underneath the gate based on the temperature dependence of the subthreshold slope.

4.1. Modulation Efficiency

The cutoff frequency f_T is one of the most important figures of merit for the frequency characteristics of microwave transistors. The cutoff frequency, often also designated as the gain-bandwidth product, is related to the short-circuit current gain h_{21}. This current gain is defined as the ratio of the small-signal output current to input current of the transistor with the output short-circuited. Such a current gain is frequency dependent, and its magnitude rolls off at high frequencies at a slope of -20 dB/decade. The cutoff frequency is the frequency at which the magnitude of h_{21} equals unity (or 0 dB).

From a physical point of view, the cutoff frequency can be also stated as the maximum frequency at which the channel current can be modulated by the gate voltage. Ideally, only the channel charges that contribute to the source to drain current need to be modulated. However, in real transistor operation, this modulation is degraded by other parasitic components (i.e. donor-trapped electrons, low-velocity electrons, gate leakage, etc) and therefore frequency performance of the device is reduced.

The concept of modulation efficiency was first introduced by Foisy *et al.* [31] in 1988. In the transistor, the drain-to-source current I_{DS} is modulated by varying the density of electrons in the conducting channel. Modulation of this charge produces a frequency-dependent displacement current through the gate terminal. f_T is defined as the frequency at which this current equals the ac drain current. Denoting the instantaneous gate-source voltage as V_{GS}, the small-signal gate-source voltage as v_{gs}, and the total charge modulated by the gate as Q_{TOT}, this equality may be expressed as

$$\left(2\pi f_T \frac{\partial Q_{TOT}}{\partial V_{GS}}\right) v_{gs} = \left(\frac{\partial I_{DS}}{\partial V_{GS}}\right) v_{gs} \tag{1}$$

Solving for f_T,

$$f_T = \frac{1}{2\pi} \frac{\partial I_{DS}}{\partial Q_{TOT}} \tag{2}$$

As previously shown in Figure 3-8, 2DEG electrons in deep submicron AlGaN/GaN HEMTs travel at their saturated velocity (v_{sat}) over the entire length of the gate, therefore I_{DS} would be

$$I_{DS} = I_D - I_G = \frac{v_{sat}}{L_G} n_D - \frac{3v_{sat}}{X_{dep}} n_G \tag{3}$$

where L_G is the gate length, n_D is the charge that contribute to the drain current, X_{dep} is length of the depletion region at the drain side of the gate, and n_G is the charge that contribute to the gate leakage current. The factor of 3 comes from the effect of image charges discussed in Chapter 3. In this expression, it is assume that the gate leakage current coming from the source is negligible since the voltage difference between gate and drain is much higher than between gate and source. Compared to Foisy's original equations, n_G is added to account for the gate leakage current (I_G). It should be noted that I_D represents not the drain-to-source current (I_{DS}) but the drain current (I_D) which is the sum of I_{DS} and I_G. Now, the total charge under the gate becomes $Q_{TOT} = n_D + n_{parasitic}$. $\mathrm{n_{parasitic}}$ includes any parasitic charge in the channel that is immobile and do not contribute to the drain current such as donor-trapped electrons, low-velocity electrons, etc.

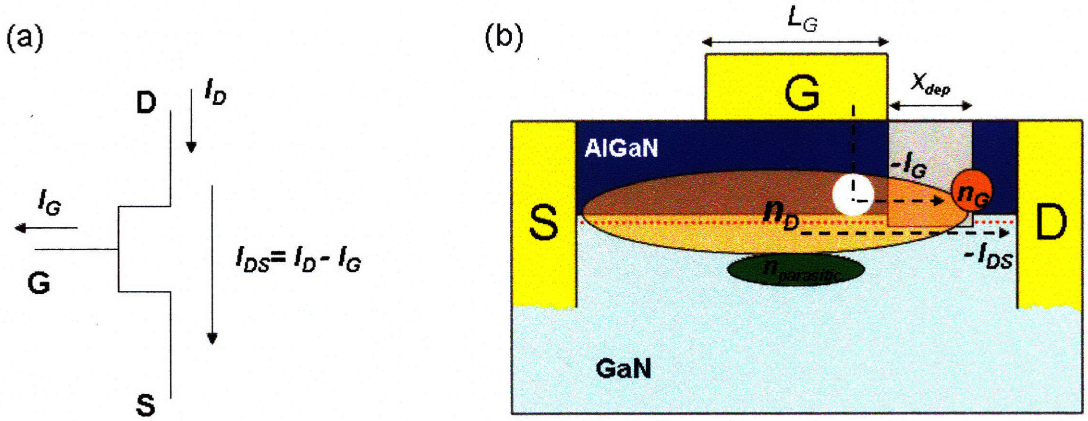


Figure 4-1. (a) Schematic illustration of the difference between I_D and I_{DS}. (b) Different charges that contribute to different currents in a HEMT. Note that I_{DS} is given by (n_D-n_G), not by just n_D.

By substituting (3) into (2), commonly applied equation $f_T = v_{sat}/(2\pi L_G)$ can be replaced by the more physically informative relationship,

$$f_T = \left(\frac{v_{sat}}{2\pi L_G}\right)\left(\frac{\partial(n_D - \frac{3L_G}{X_{dep}} n_G)}{\partial(n_D + n_{parasitic})}\right) \tag{4}$$

This formulation allows us to isolate a term dependent on the saturation velocity and a term dependent on charge utilization. We define the second term in (4) as the modulation efficiency of the device,

$$\eta = \frac{\partial(n_D - \frac{3L_G}{X_{dep}} n_G)}{\partial(n_D + n_{parasitic})} \tag{5}$$

At a fixed bias condition X_{dep} is a constant. Thus, the reduction in charge modulation due to gate leakage current (numerator) in addition to the excess charge modulation by traps underneath the gate (denominator) reduce the f_T by a factor equal to η. Experimental measurements to verify this theoretical analysis are part of our on-going work.

4.2. Subthreshold Slope

As shown in Figure 4-2. in the subthreshold region of HEMTs operation, ln(I_D) versus V_G is almost a straight line and its reciprocal slope determines the gate swing needed to change the drain current by one decade. This line is called subthreshold slope (or swing) and it is briefly stated as a gate voltage (V_G), necessary to change the drain current (I_D) by one decade. As will be seen in the following sections, the subthreshold slope is strongly affected by both trap density and gate leakage current. The smaller the trap density and the lower the gate leakage current, the lower the subthreshold slope (ideally 60 mV/decade). Therefore, subthreshold slope is an excellent indicator to estimate gate modulation efficiency of the transistors.

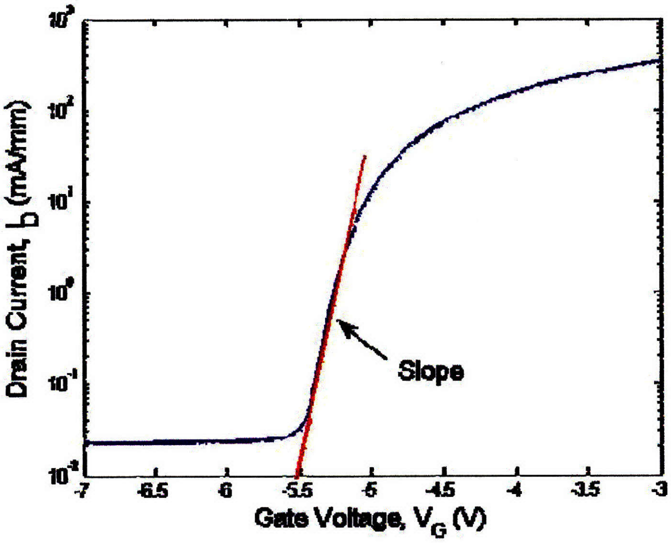


Figure 4-2. Typical transfer curve in AlGaN/GaN HEMTs. Subthreshold slope is an excellent indicator of traps and gate leakage current.

4.3. Gate Leakage Current

This section studies the effect of gate leakage on the subthreshold slope and ON/OFF current ratio of AlGaN/GaN HEMTs. We found a strong correlation between the gate leakage current and the transistor subthreshold characteristics: the lower the gate leakage, the higher the ON/OFF ratio and the steeper the subthreshold slope. To improve the subthreshold characteristics in GaN HEMTs, the gate leakage current was reduced with an O_2 plasma treatment prior to the gate metallization. The O_2 plasma treatment effectively reduces the gate leakage current by more than four orders of magnitude, it increases the ON/OFF ratio to more than seven orders of magnitude and the improved AlGaN/GaN HEMT shows a nearly ideal subthreshold slope of 64 mV/decade.

4.3.1. O_2 Plasma Treatment

The subthreshold characteristics of GaN devices have been only scarcely studied in the past in spite of their tremendous importance in high temperature digital electronics. They are also key to assure good power added efficiency, reliability, linearity and noise figure in power amplifiers [32]. The subthreshold slope in GaN HEMTs has traditionally been much higher (>300 mV/decade) than the theoretical limit of 60 mV/decade [33-34]. Also, no clear correlation between the ON/OFF drain current ratio and the transistor design parameters has been established.

The AlGaN/GaN transistor structures used in this work were grown on Si(111) substrates by metal-organic chemical vapor deposition (MOCVD) at Nitronex Corporation [13]. In these samples, the AlGaN barrier had a total thickness of 175 Å and an Al composition of 26 %, as determined by Hg-probe CV and photoluminescence, respectively. The structure is finished with a thin unintentionally doped GaN cap layer. A total charge density of 1.2×10^{13} /cm^2 and an electron mobility of 1000 cm^2/V·s were measured for unpassivated samples using van der Pauw's structures at room temperature.

AlGaN/GaN HEMTs and Schottky diodes were fabricated by first depositing a Ti/Al/Ni/Au metal stack for the ohmic contacts followed by annealing at 870 °C for 30 s in a N_2 atmosphere. Then Cl_2/BCl_3 plasma was used for the mesa isolation. Subsequently, Ni/Au/Ni Schottky contacts were defined in the transistors (2 μm gate length) and in circular Schottky diodes (90 μm-radius). Before the deposition of the Schottky metal, an O_2

plasma treatment was applied using a Branson IPC plasma asher in order to oxidize the GaN surface before metallization. The chamber was evacuated below 0.5 Torr pressure and an 800 W O_2 plasma was applied for 5 minutes. The O_2 plasma grows a self-limited Ga_2O_3 gate dielectric which reduces the gate leakage in the devices [35]. As a reference, in one sample the oxide layer was removed by etching the oxide for 2 minutes in HCl:DI (1:3). Finally, a Ni/Au/Ni multilayer was deposited for the gate (or Schottky) contact.

The use of Ga_2O_3 as gate dielectric has several advantages when compared to other approaches to reduce gate leakage. The high dielectric constant of Ga_2O_3 (~10) and its high quality allows the use of thinner layers than in the case of Si-based gate dielectrics (SiO_2 or Si_3N_4) [36-37]. Also, the growth of Ga_2O_3 does not degrade the transport properties of the two-dimensional electron gas. This degradation is an important trade-off when using fluorine-based plasma treatments to reduce gate leakage [38].

Figure 4-3 shows current-voltage (I-V) characteristics of AlGaN/GaN Schottky diodes with and without O_2 plasma treatment. The reverse-biased leakage current is reduced by more than two orders of magnitude in the case of the O_2 plasma-treated sample, while maintaining a forward-biased current level equivalent to the reference sample. This reduction in the leakage current is the result of the self-limited growth of a thin Ga_2O_3 gate dielectric during the O_2 plasma treatment [35]. The thickness of this dielectric is less than 4 nm according to capacitance-voltage measurements.

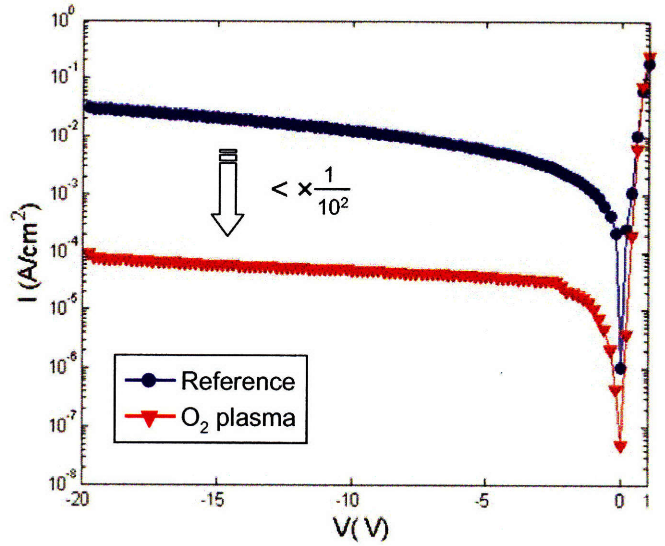


Figure 4-3. I-V characteristics of AlGaN/GaN Schottky diodes with and without O_2 plasma treatment. In transistors, the reduction in gate leakage due to O_2 plasma treatment exceeds four orders of magnitude.

4.3.2. Subthreshold Characteristics

Figure 4-4 shows the drain current characteristics of AlGaN/GaN HEMTs as a function of gate voltage in transistors with and without O_2 plasma treatment. The gate leakage current is also plotted in order to show its effect on subthreshold slope. When the device is pinched-off, the drain leakage current is dominated by reverse-biased gate current. As can be seen from Figure 4-4, in HEMTs the reduction of gate leakage current after O_2 plasma treatment exceeds four orders of magnitude, without degrading maximum drain saturation current. This reduction in the gate leakage increases the drain ON/OFF drain current ratio (I_{ON}/I_{OFF}) by the same amount as the gate leakage reduction and finally improves subthreshold slope to 64 mV/decade, very close to the theoretical limit of 60 mV/decade.

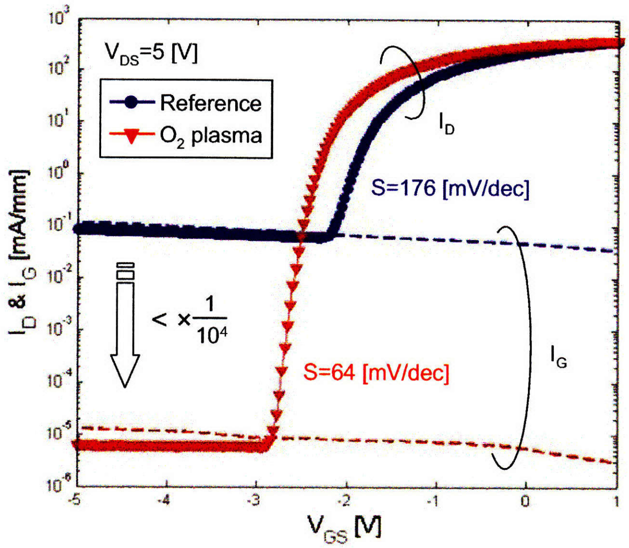


Figure 4-4. Transfer characteristics and gate leakage current of AlGaN/GaN HEMTs with and without O_2 plasma treatment at V_{DS}=5 V.

The effect of gate leakage (I_G) on I_{ON}/I_{OFF} of AlGaN/GaN HEMTs is shown in Figure 4-5. I_{OFF} and I_{ON} are measured at V_{GS} = -4 V and V_{GS} = 0 V, respectively at constant drain bias of V_{DS} = 5 V. I_G is measured at the same bias condition as I_{OFF}. There is a strong linear dependence between I_{ON}/I_{OFF} and I_G and the use of O_2 plasma treatment is very important to both lower I_G (< 10^{-2} mA/mm) and increase I_{ON}/I_{OFF} (> 10^7).

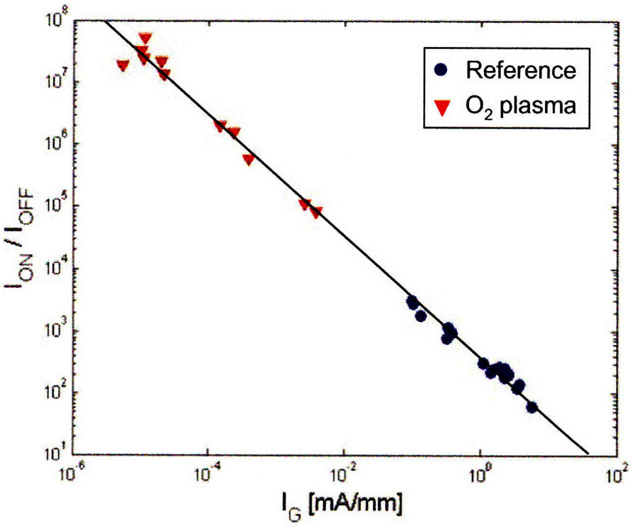


Figure 4-5. Linear dependence between the ON/OFF drain current ratio (I_{ON}/I_{OFF}) and the gate leakage current (I_G).

Figure 4-6 shows the correlation between subthreshold slope and the gate leakage current of AlGaN/GaN HEMTs for several samples with and without O_2 plasma treatment. In a logarithmic scale, the subthreshold slope has a clear linear dependence with the gate leakage in all the samples analyzed in this work. For the O_2 plasma treated samples, the subthreshold slope was well below 90 mV/decade in all the cases. However, reference (untreated) samples showed over 110 mV/decade and stronger dependence with the gate leakage current. The dispersion in the gate leakage characteristics within the same sample might be caused by different trap (or dislocation) densities underneath or near the gate [39] and it is the focus of our on-going work.

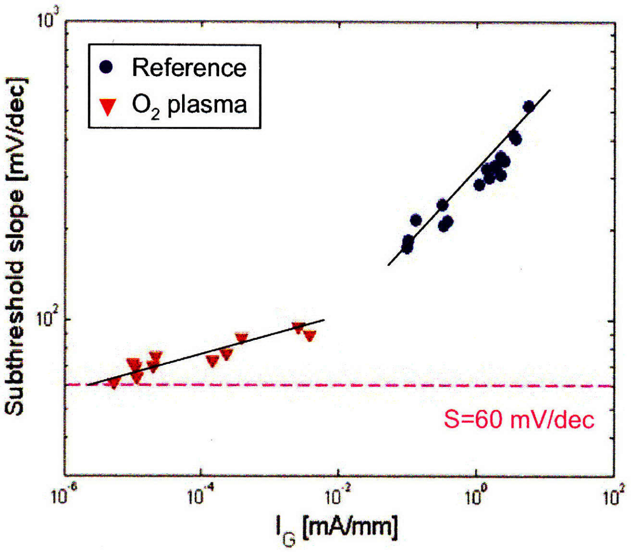


Figure 4-6. Linear dependence between subthreshold slope and the gate leakage current (I_G) with and without O_2 plasma treatment.

In summary, we have studied the effect of gate leakeage in the subthreshold slope of AlGaN/GaN HEMTs grown on Si substrates. A strong linear dependence of both subthreshold slope and I_{ON}/I_{OFF} to the gate leakage current has been observed. O_2 plasma treatment was used to reduce the gate leakage current by more than four orders of magnitude. As a result of the reduced gate leakage current, a near-ideal subthreshold slope of 64 mV/decade has been demonstrated. These results show the important effect of the gate leakage current in the performance of AlGaN/GaN HEMTs and the importance of using high quality gate dielectrics, such as Ga_2O_3, to reduce this gate leakage current and improve the subthreshold characteristics of nitride-based transistors.

4.4. Traps

Subthreshold slope is not only dependent on the gate leakage current, but also closely related to the trap density in AlGaN/GaN HEMTs. The presence of traps in the gate modulated region of these devices degrades gate modulation efficiency which is linked to the subthreshold slope and ultimately to high frequency performance. Therefore, it is very important to quantify trap density in the device. Several methods to quantify the trap density include low-frequency noise data [40] or gate-drain conductance and capacitance dispersion studies [41]. In this section we will show that subthreshold slope can also be used to easily quantify trap density in the gate modulated region of AlGaN/GaN HEMTs. First we demonstrate the effects of thermal annealing on subthreshold slope in AlGaN/GaN HEMTs. Then, based on the temperature dependence of subthreshold slope, we introduce a new method to estimate gate-modulated trap density in these devices.

4.4.1. Thermal Annealing

All the samples used in this work were standard AlGaN/GaN HEMTs with 0.6 μm gate length and 150 μm gate width. Layers consist of 25 nm $Al_{0.33}Ga_{0.67}N$ followed by 7 Å AIN interlayer and 1.8 μm GaN buffer and they are all grown by metal organic chemical vapor deposition (MOCVD) on SiC substrates and passivated. Initially, we measured subthreshold slope of each device in different dies in the same wafer to see the variations of subthreshold slope. As shown in Figure 4-7, subthreshold slope showed important variations from sample to sample and also within the same sample. This may be because of irregularly distributed traps (or dislocations) in GaN or non-uniformity of the fabrication process. To stabilize electrical properties of the device we performed post-thermal annealing [42]. Individual dies are cut from the sample and annealed from 25 °C to 200 °C and from 200 °C back to 25 °C 4 times using a Temptronic TP03010B Thermo Chuck System. Measurements are performed every 25 °C step. We performed all the current and voltage measurements using an Agilent 4155C Semiconductor Parameter Analyzer.

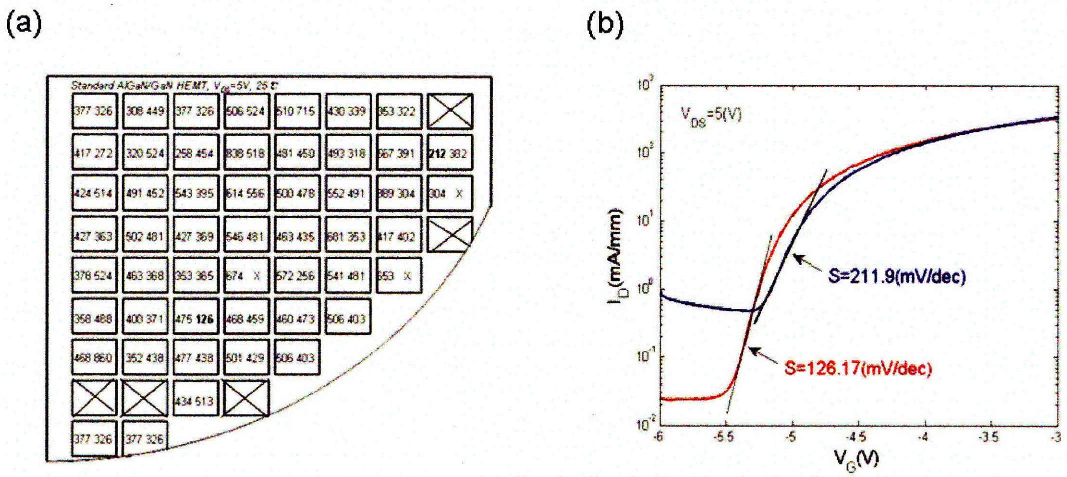


Figure 4-7. Variations of subthreshold slope in identically processed AlGaN/GaN HEMTs. (a) Subthreshold slope is measured by two transistors per die in quarter part of a 2-inch wafer. (b) Two separated transistors show different subthreshold slope values.

Figure 4-8 shows the temperature dependence of subthreshold slope (S) in two different transistors with different initial values of S. Notably, when the initial subthreshold slope is very high (typically in excess of 500 mV/dec, Figure 4-8(b)), reproducible results are only achieved after the first heating sequence.

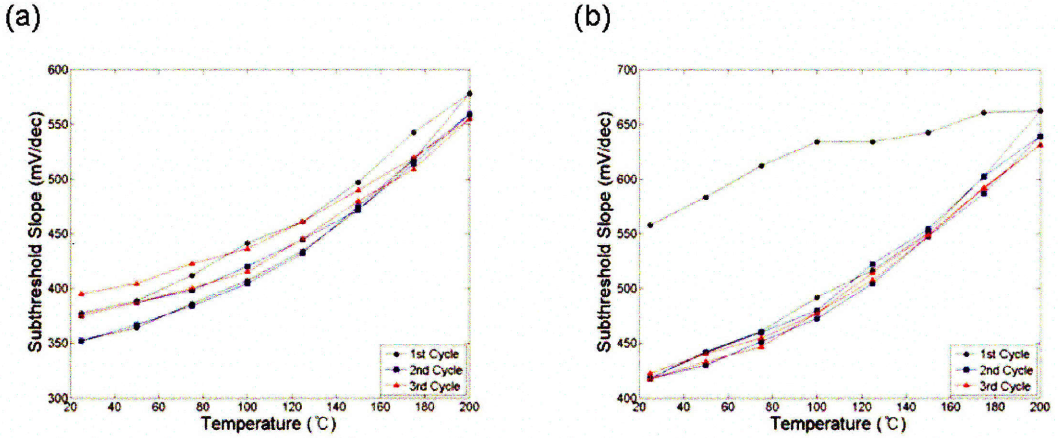


Figure 4-8. Dependence of subthreshold slope on temperature for two different transistors. (a) Transistors with an initial subthreshold slope below 500 mV/dec typically show a very reproducible linear dependence with temperature. (b) However, transistors with higher initial subthreshold slope reach stable operation only after the first heating sequence.

As we have shown in previous sections, the gate leakage has a strong effect on the subthreshold slope. Although this effect is not clear in un-annealed devices, we have measured a strong linear dependence after temperature annealing, as shown in Figure 4-9. Thermal annealing is believed to stabilize electrical performance of the device by removing possibly remained photo-resist or healing defects originated during the fabrication processing. By extrapolation from Figure 4-9(b), we can extract the expected subthreshold slope when the gate leakage current is zero (130 mV/dec). However, this value is still almost twice the value of the ideal subthreshold slope, 60 mV/dec, and we associated this difference to gate-modulated traps.

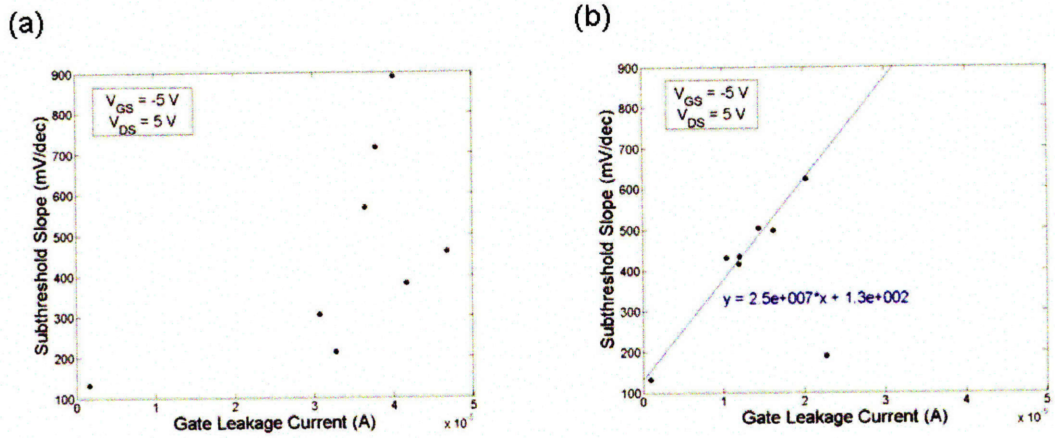


Figure 4-9. Dependence of subthreshold slope on gate leakage current before (a) and after (b) thermal annealing. After the annealing, the transistors showed a much more stable performance and the subthreshold slope is clearly proportional to the gate leakage current.

4.4.2. New Method to Estimate Trap Density

The gate-modulated trap density in these devices can be extracted from the change of S with temperature (T). By analogy with MOSFETs (Figure 4-10), the equation for subthreshold slope in HEMTs is given by,

$$S = \frac{kT}{q}\ln(10)\left(1+\frac{C_Q + C_{trap}}{C_{AlGaN}}\right) = \frac{kT}{q}\ln(10)(1+\varsigma) \qquad (6)$$

where C_{AlGaN} is AlGaN layer capacitance, C_Q is quantum capacitance, and C_{trap} is associated with the gate-modulated trap density. Here, ς is a non-ideality factor related to the gate-modulated trap density. The change rate of S with T can be calculated from the derivative of equation (6),

$$\frac{\partial S}{\partial T} = \frac{k}{q}\ln(10)(1+\varsigma) \tag{7}$$

ς can be calculated from the equation (7) after measuring the slope from the S vs. T curve (Figure 4-8).

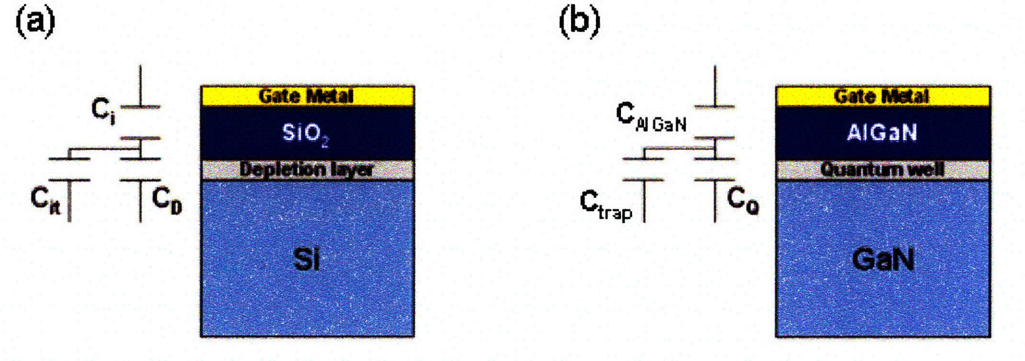

(a)
C_i
C_{it}
C_D
Gate Metal
SiO$_2$
Depletion layer
Si
(b)
C_{AlGaN}
C_{trap}
C_Q
Gate Metal
AlGaN
Quantum well
GaN

Figure 4-10. Analogy between (a) Si MOSFET and (b) AlGaN/GaN HEMT structure.

As shown in Figure 4-11, ς varies between 2 and 4. Slight variations of ς might be caused by differences in gate leakage current and its behavior with temperature. From the value of ς, we estimated a gate-modulated trap density of 3×10^{12}~ 8×10^{12} cm^{-2}eV^{-1}, assuming C_Q is negligible. This value is similar to previously reported data obtained from low-frequency noise data [40] or from gate-drain conductance and capacitance dispersion studies [41].

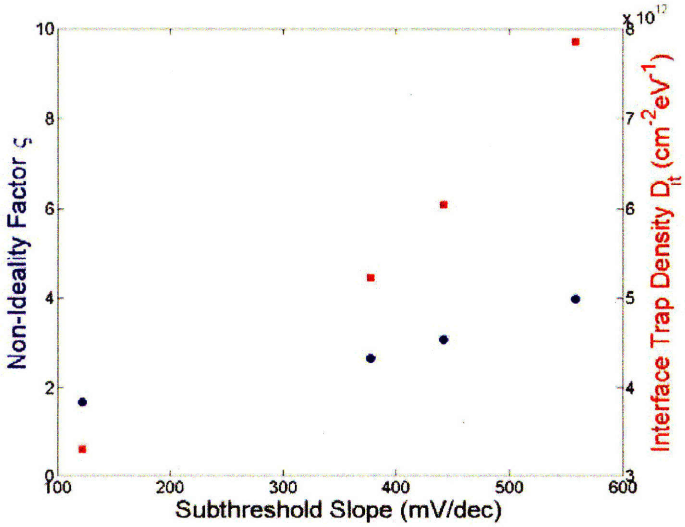


Figure 4-11. Calculated non-ideality factor and gate-modulated trap density.

In conclusion, we have studied the change in subthreshold slope in AlGaN/GaN HEMTs with temperature. From this experiment, we proposed for the first time a relatively simple way to estimate gate-modulated trap density. The understanding of this trap density is critical to optimize the gate modulation efficiency of GaN transistors and maximize their high frequency performance.

4.5. Summary

In this chapter we have studied two parasitic components, gate leakage current and traps that degrade modulation efficiency and ultimately high frequency performance of AlGaN/GaN HEMTs. We found that subthreshold slope is an excellent indicator of the effects of both gate leakage current and traps. Based on understanding of the effect of gate leakage current on the subthreshold characteristics, we have demonstrated a record subthreshold slope of 64 mV/decade in AlGaN/GaN HEMTs by using O_2 plasma treatment. From the close correlation between traps and subthreshold slope, we also proposed a new simple method to extract gate-modulated trap density in these devices by studying change of subthreshold slope with temperature.

Chapter 5. N-face GaN HEMTs

Nitride-based transistors are revolutionizing power electronics and high frequency amplifiers due to their combination of high current densities and large breakdown voltage. Although most of the reported GaN devices have been fabricated on nitride structures grown along the c-direction (i.e. Ga-face), N-face GaN/AlGaN transistors have the potential of higher electron confinement and lower contact resistances. These advantages are especially useful in high frequency devices. However, in spite of this promise, the performance of N-face devices is still much lower than in Ga-face devices due to the inferior material quality. Although N-face devices have been grown by molecular beam epitaxy and, recently, by metal-organic chemical vapor deposition (MOCVD), the growth of N-face nitrides is much more challenging than the growth of the more stable Ga-face structure, which degrades the final performance. In this chapter, we present a new method to fabricate N-face GaN/AlGaN HEMTs based on the substrate removal of a Ga-face AlGaN/GaN layer grown on Si.

5.1. N-face GaN

In electronic and optoelectronic applications of GaN, the most commonly used and stable crystal structure is wurtzite. The wurtzite material system has both a strain-independent spontaneous and a strain-induced piezoelectric polarizations [43]. The orientation of the spontaneous and piezoelectric polarization of GaN is determined by stacking properties of the Ga and N atomic layers (Ga-face or N-face) as shown in Figure 5-1. Due to these polarization effects, the band diagrams and electrostatics of device structures grown along the (0001) direction (Ga-face) and $(000\bar{1})$ direction (N-face) are very different.

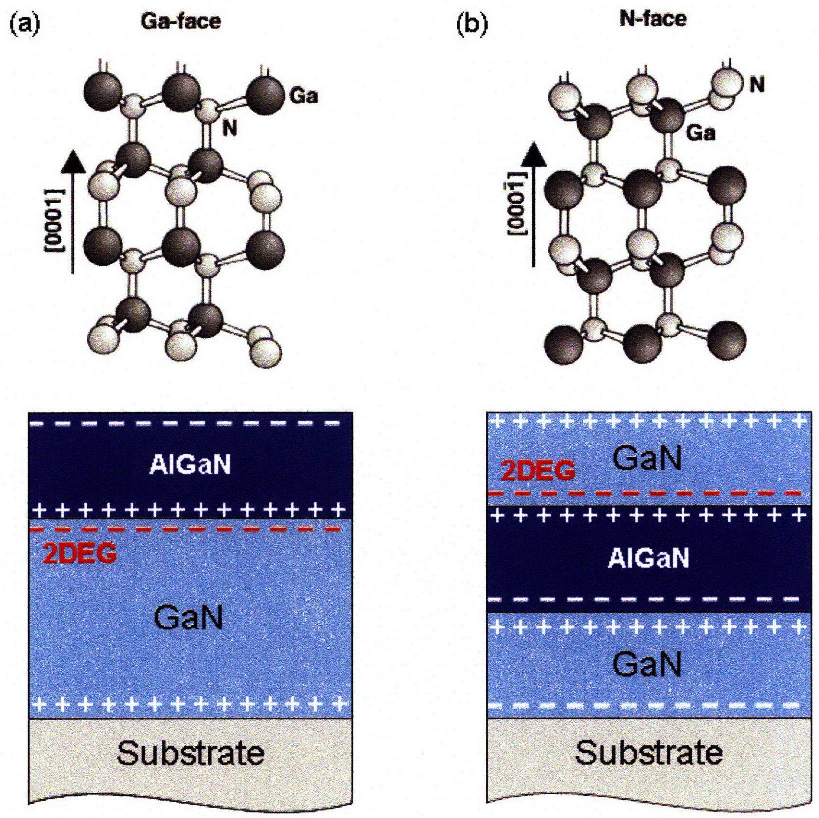


Figure 5-1. Schematic drawing of the crystal structure of wurtzite (a) Ga-face and (b) N-face GaN [44]. Polarization reverses direction with respect to the surface.

In the early stage of GaN research, both Ga- and N-face GaN were studied. However, after Dimitrov *et al.* [45] have shown better crystal qualities and electrical properties of Ga-face as well as difficulties to grow N-face, most research has focused on materials and heterostructures grown in the Ga-face. Recently, Rajan *et al.*[46] and Wong *et al.*[47] re-examined N-face GaN/AlGaN/GaN HEMTs grown by MBE, however their performance was still far from that of state-of-the-art Ga-face HEMTs and was not enough to promise N-face GaN HEMTs.

As will be shown in the following sections, in this project we have proposed N-face GaN/AlGaN HEMTs on Si(100) substrate through substrate removal technology. Figure 5-2 shows the schematic illustration of fabricated N-face GaN/AlGaN HEMTs. The AlGaN/GaN transistor structures grown along Ga-face is flipped and bonded to Si(100) substrate using HSQ as a interlayer. In this way, the exposed GaN surface is N-face and

2DEG channel is generated on top of the AlGaN layer. Detailed processing steps will be discussed in following sections.

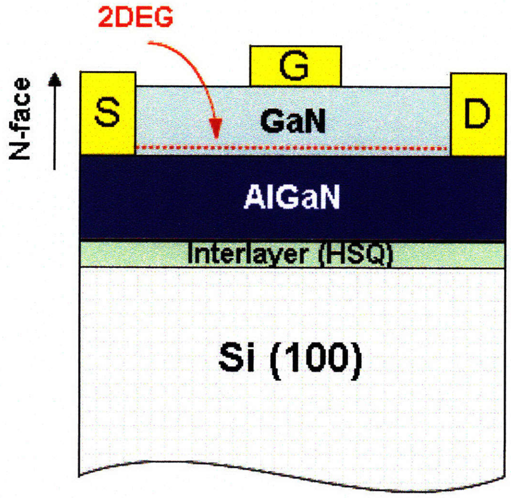


Figure 5-2. Schematic illustration of fabricated N-face GaN/AlGaN HEMTs on Si(100) substrate

Our N-face GaN/AlGaN HEMTs on Si(100) substrate have a great potential to solve many existing problems in Ga-face devices and further improve their frequency performance.

First of all, fabricating ohmic contacts on GaN layer instead of AlGaN layer may provide much lower contact resistances. In standard ohmic metal contacts fabricated on Ga-face AlGaN layer, a wide bandgap of AlGaN (3.4~6.2 eV) prevents tunneling current through the AlGaN layer and it is very challenging to reproducibly achieve contact resistances below 0.2 Ω·mm. However, in N-face devices, due to the narrower bandgap of GaN (3.4 eV) which reduces potential barriers to the electron flow, ohmic contacts fabricated on N-face GaN can have lower contact resistances.

Secondly, electron confinement in the channel is significantly improved. As mentioned earlier, the 2DEG in an N-face HEMT is induced on top of the AlGaN barrier, which is opposite to the case of Ga-face AlGaN/GaN HEMTs. Therefore, the AlGaN layer itself provides a strong back barrier for confinement of the 2DEG and this natural back barrier can also reduce short channel effects [46].

Another beneficial effect of N-face devices is the increase of the implantation yield. Si implantation is being investigated by several groups to reduce the access resistances in AlGaN/GaN HEMTs. However, it has only achieved a limited success due to the poor activation yield of implanted Si in the AlGaN cap layer. The direct implantation through the AlGaN-free N-face surface, most of the implanted atoms will be in GaN and the activation yield will be much higher than in standard devices. Moreover, in conjunction with the ohmic contacts, implantation will allow ultra low ohmic contacts.

Finally, the use of a Si(100) substrate bonded to AlGaN/GaN epilayer allows seamless integration of Si devices and GaN HEMTs in the same circuit. The standard orientation of Si wafers used in the microelectronics industry is (100), however the used in the growth of AlGaN/GaN epilayers is (111). As will be seen in the next sections, the substrate removal technology replaces Si(111) substrate with Si(100) substrate without affecting AlGaN/GaN epilayer. N-face GaN/AlGaN HEMTs on Si(100) substrate will allow the fabrication of world first hybrid GaN-Si circuits.

5.2. Processing Technology

5.2.1. Wafer Bonding

To fabricate N-face GaN/AlGaN HEMTs on Si(100), we have developed a new wafer bonding technique between GaN and Si wafers. Wafer-to-wafer bonding has been widely used in microstructure fabrication. The types of wafer bonding that are most commonly employed in microstructure fabrication can be placed in three categories: direct bonding, anodic bonding, and intermediate-layer bonding [48]. For our application, direct bonding and anodic bonding are not suitable for making a reliable bonding due to the large lattice mismatch between GaN and Si (17%) can cause bonding failure during the subsequent HEMT fabrication steps. For example, we observed high crack density during the rapid thermal annealing (RTA) due to the large mismatch in the thermal expansion coefficients between GaN and Si(100) (55%).

To relax strains coming from the GaN and Si lattice mismatch, we employed an intermediate bonding layer. A wide range of intermediate layers have been used for wafer-to-wafer bonding in microstructure fabrication. In this work, for the first time we used hydrogen silsesquioxane (HSQ), a flowable oxide with excellent thermal stability, which stands the high thermal budget required during the processing of GaN devices. Spin-coated HSQ also has a very uniform surface profile (surface roughness is less than 40 Å) which is necessary to avoid any void at the bonding interface. In addition, HSQ is a low dielectric material (dielectric constant = ~3) and can minimize the parasitic gate capacitances which is good for high frequency performance of the device.

Several different parameters had to be optimized to prevent bonding failure, including thickness of HSQ, bonding temperature and pressure, native particles, air gaps between two wafers, wafer bows, etc. Figure 5-3 shows some of those factors.

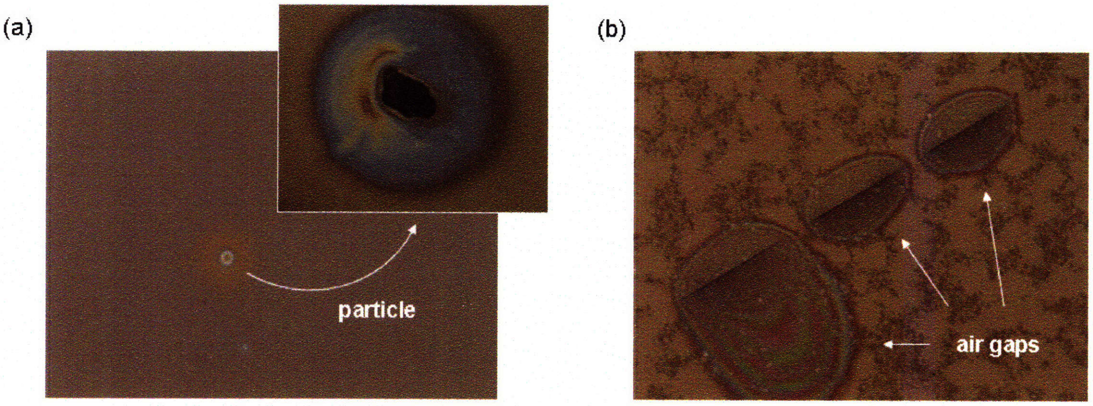


Figure 5-3. Some of the factors that cause bonding failure. (a) A small particle that resides on one of the wafer (b) air gaps between two bonded wafers make cracks.

5.2.2. GaN Thinning

Once we have GaN/AlGaN on Si(100) structure as shown in Figure 5-4, it is important to precisely control the thickness of GaN layer in order to have a good gate control over the 2DEG and to ensure sufficiently small distance (<100 nm) between the contacts and the channel to reduce the contact resistance.

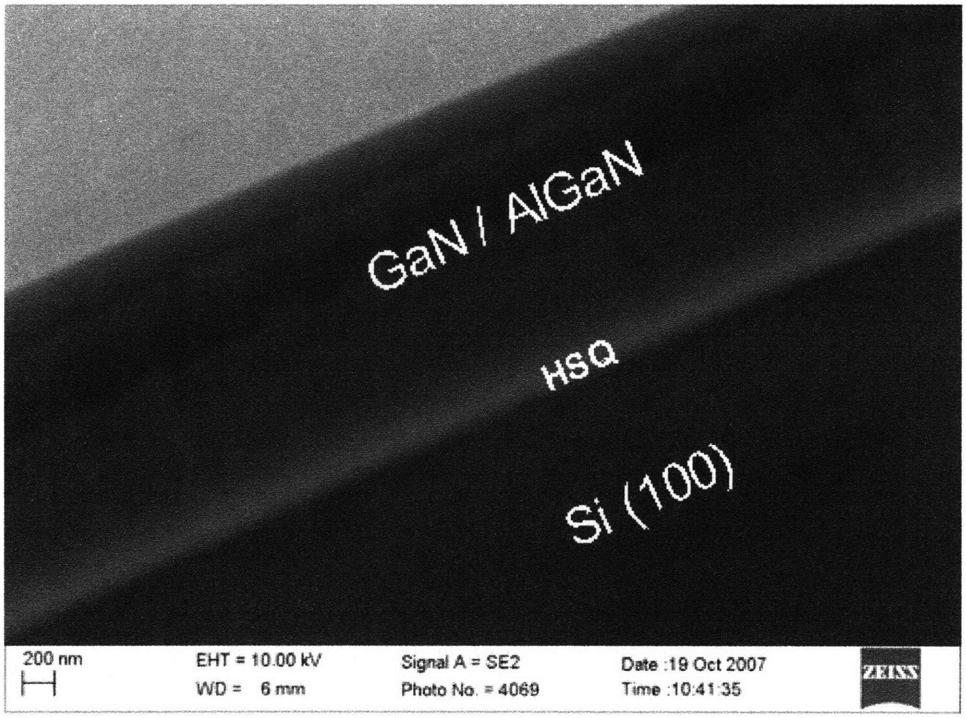


Figure 5-4. Cross-sectional SEM image of a free-standing AlGaN/GaN HEMT structure bonded to a Si(100) substrate through the use of a thin HSQ layer.

In general, there are two methods to etch GaN; dry etching and wet etching. However, due to the chemical stability of GaN, conventional wet etching is unsuitable for device processing [49]. Plasma or dry etching is more preferred way with a myriad of techniques including reactive ion etching (RIE), electron cyclotron resonance, chemical assisted ion-beam etching, magnetron RIE, and inductively coupled plasma (ICP). Among these techniques electron cyclotron resonance reactive ion etching (ECR-RIE) is the most popular because it provides high-density plasma and independently controlled substrate bias voltage. The chlorides of Ga and N are relatively volatile, making Cl_2, BCl_3, and $SiCl_4$ the primary reagents used to etch GaN.

In this work, ECR-RIE with Cl_2/BCl_3 gas mixture is used to etch GaN until the desired distance between the N-face GaN surface and the AlGaN/GaN interface is achieved. Figure 5-5 shows tilted cross-section SEM image of successively etched of GaN/AlGaN epilayer. ECR-RIE with Cl_2/BCl_3 gas mixture recipe (ECR=100W, RF=15W, DC bias=316 V, Temperature=80 °C) turned out to give reproducible and constant etch rate (1~1.5 Å/s), however poor surface roughness. Rough surface is not related to ion bombardment since lower RF power did not improve the surface roughness but to the higher chemical reactivity of N-face GaN. The improvement of the surface morphology is one of our on-going projects.

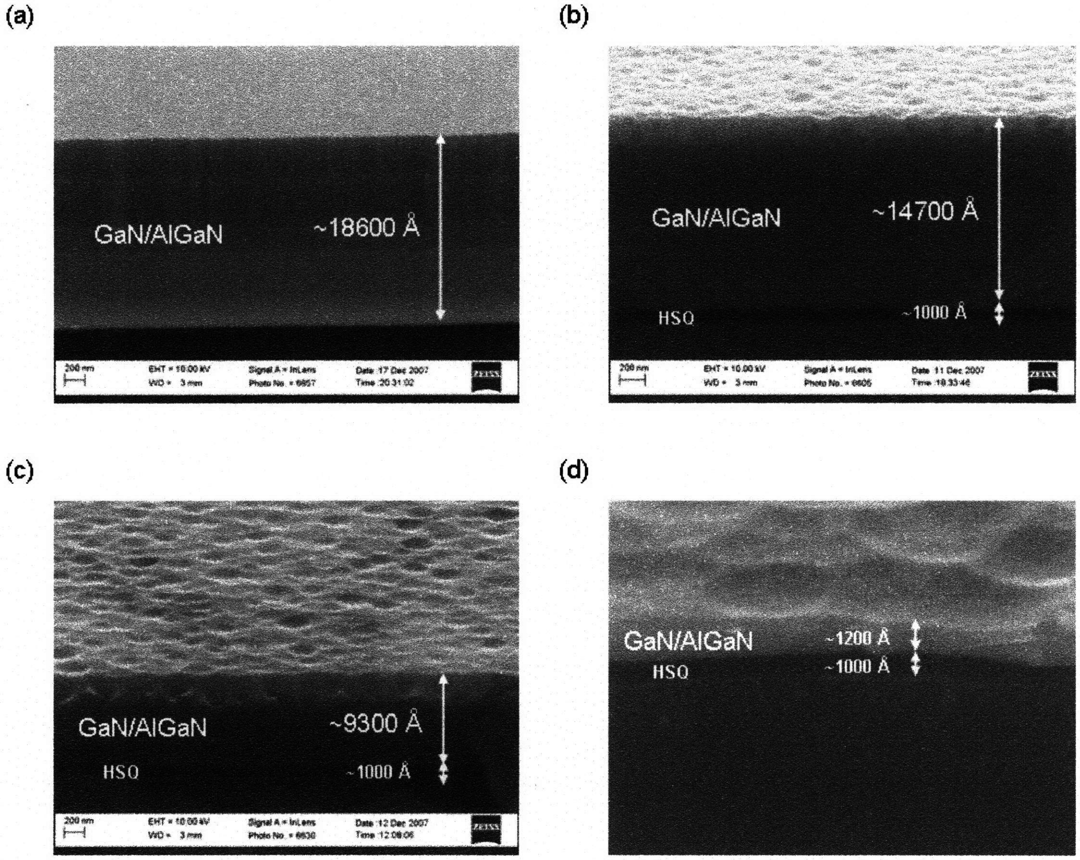


Figure 5-5. Tilted cross-section SEM image N-face GaN/AlGaN epilayer which is bonded to Si(100) substrate. (a) Before applying ECR-RIE, (b) 1 hr, (c) 2 hrs, (d) 4 hrs later.

5.3. N-face GaN/AlGaN HEMTs

The Ga-face AlGaN/GaN transistor structures used in this work were grown on Si(111) substrates by MOCVD at Nitronex Corporation [13]. In these samples, the AlGaN barrier had a total thickness of 175 Å and an Al composition of 26 %. To have access to the N-face of these samples, we have developed the substrate transfer technology shown in Figure 5-6.

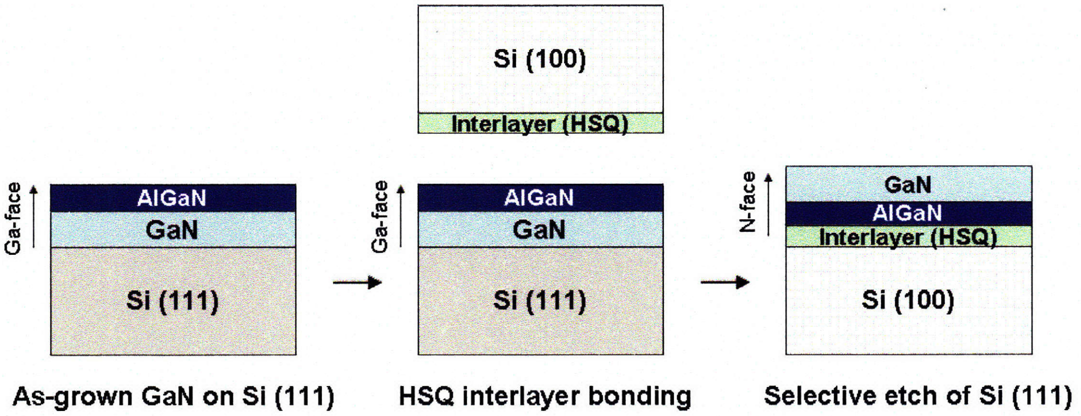


Figure 5-6. Main processing steps in the fabrication of N-face GaN on Si(100) substrate through substrate removal.

First, the Ga-face surface was bonded to a Si(100) carrier wafer by using a hydrogen silsesquioxane (HSQ) interlayer. The HSQ film is spin-coated on Si(100) to a thickness of about 1000 Å and baked sequentially on hot plates at 150 °C and 200 °C for 1 minute each. Then, the HSQ-coated Si(100) substrate is attached to the as-grown AlGaN/GaN layer and thermally compressed at 400 °C for an hour. The elevated temperature hardens the HSQ layer and forms an extremely stable bond between the GaN wafer and the Si carrier wafer. After the wafer bonding, the original Si(111) substrate is completely removed by dry etching using an SF_6-based plasma. The GaN buffer is an effective etch-stop layer for the SF_6 plasma etch and a smooth N-face GaN surface is obtained at the end of the etch. Figure 5-7 shows a scanning electron micrograph of the AlGaN/GaN layer transferred to the Si(100) substrate. After the substrate transfer, the N-face GaN buffer is etched by electron cyclotron resonance reactive ion etching (ECR-RIE) with Cl_2/BCl_3 gas mixture until the desired distance between the N-face GaN surface and the AlGaN/GaN interface is achieved.

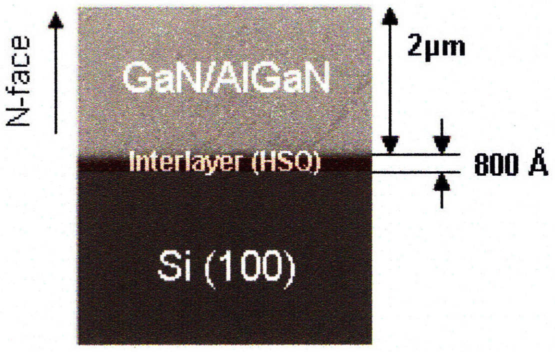


Figure 5-7. A cross-section scanning electron microscope (SEM) picture of the AlGaN/GaN layer transferred to the Si(100) substrate. False color has been added to highlight the HSQ interlayer in the structure.

The effect of the GaN buffer thickness on the electron transport was evaluated by four-point van der Pauw Hall measurements. The GaN buffer was etched as described in the previous section and the remaining GaN thickness was measured with an interferometer (NanoSpec). Figure 5-8 shows the measured values of mobility (μ), electron density (n_s) and sheet resistance (R_{sh}) at room temperature as a function of the remaining GaN buffer thickness. As shown in Figure 3, these electrical properties are almost constant with buffer thickness (μ=1670 cm^2/V·s, n_s=1.6×10^3 cm^{-2}, R_{sh}=240 Ω/sq). The sheet resistance is 50% lower than the sheet resistance measured in the Ga-face of the sample. This important reduction in the sheet resistance is due to an increase in the mobility and electron density during the substrate removal process. The change in the Fermi level pinning when the N-face surface is exposed after the substrate removal is believed to be partly responsible for this improvement although other causes are still under investigation.

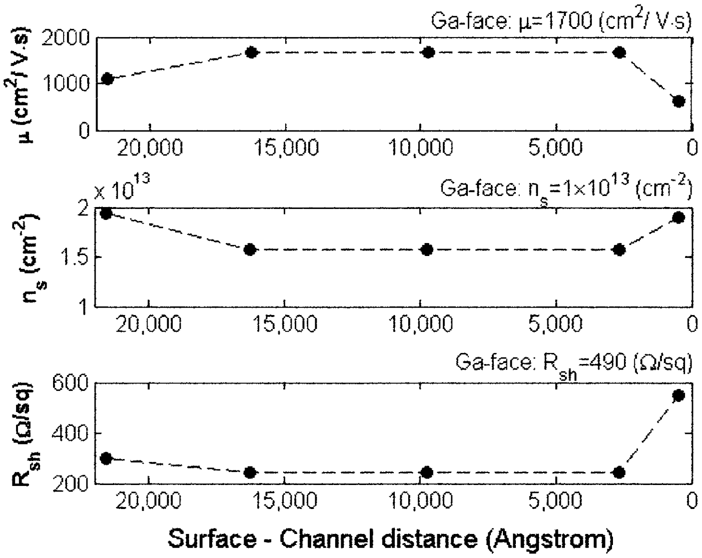


Figure 5-8. Electron mobility (μ), 2DEG density (n_s), and sheet resistance (R_{sh}) of N-face GaN as a function of the distance between N-face surface and 2DEG channel estimated by room temperature Hall measurement.

N-face GaN/AlGaN structures fabricated through the substrate removal process described before have been used in the fabrication of N-face high electron mobility transistors (HEMTs). In this samples, the distance between the N-face surface and the 2DEG was reduced to 1000 Å by ECR etch. A Ti/Al/Ni/Au multilayer was deposited for the ohmic contacts and annealed at 870°C for 30s in a N_2 atmosphere. Then Cl_2/BCl_3 plasma was used for the mesa isolation. Finally, a 2μm-length gate is defined by photolithography and a Ni/Au/Ni metallization was deposited for the Schottky contact. The drain current versus drain voltage characteristic of the N-face device is shown in Figure 5-9 and it is compared to a Ga-face HEMT used as a reference. For a gate voltage of 0 V, the maximum current in the N-face device is almost 70% higher than in the Ga-face device. This difference is mainly due to the higher charge density in the N-face device. The transconductance in the N-face device is low due to the gate-to-channel distance, as shown in Figure 5-10.

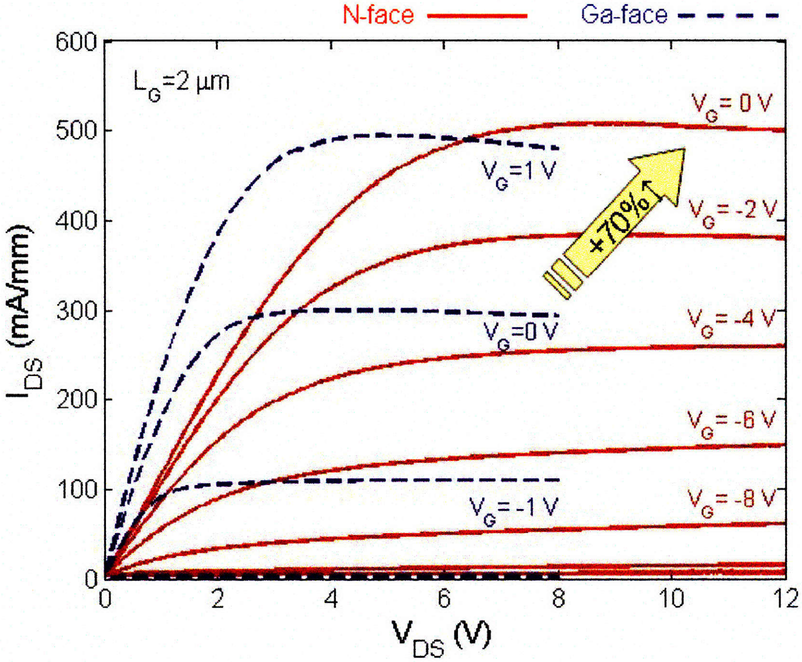


Figure 5-9. DC current-voltage characteristics of N-face (solid line) and Ga-face (dashed line) HEMTs with a gate length (L_G) of 2 μm. Almost 70% higher maximum current at V_G=0 V is achieved in N-face HEMTs. The higher on-resistance (R_{on}) in N-face HEMTs is due to unoptimized ohmic contacts.

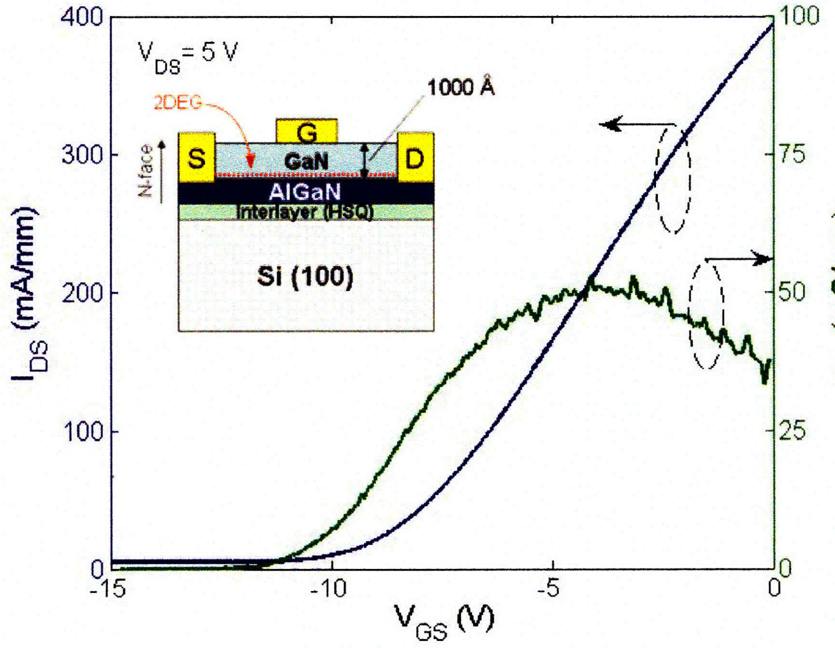


Figure 5-10. Transconductance (g_m) characteristics of 2 μm-length gate N-face HEMTs. The low g_m is due to the gate-to-channel distance (=1000Å).

5.4. Summary

In this chapter, we have demonstrated a new substrate removal and transfer technology with no degradation to the GaN active layer. This technology has allowed the fabrication of N-face GaN transistors with record sheet resistance values. Many other applications can be envisioned for the proposed substrate transfer technology including thermal management, integration with Si electronics and new approaches for high efficiency light emitting diodes.

Chapter 6. Conclusions and Future Work

In this thesis, we have identified some critical parameters that affect the high frequency performance of AlGaN/GaN HEMTs. We have also demonstrated several new technologies to improve these parameters and increase the frequency performance. Most efforts have focused on three different areas: drain delay, charge control in 2DEG, and N-face GaN. Although some of these ideas have been demonstrated only at the proof-of-concept level, initial results are very promising. In the following sections, we will summarize our key findings and remaining work in order to achieve maximum performance at beyond mm-wave frequencies.

6.1. Summary of Key findings

The low high frequency performance traditionally found in GaN-based devices is mainly due to the combination of:

- Unoptimized basic HEMT fabrication technology
- Drain delay, a non-scalable portion of electron delay
- Poor modulation efficiency caused by traps and gate leakage current
- High (contact + access) resistances

In order to study the potential of new ideas to solve these problems, it is necessary to have an optimized and reproducible device fabrication technology. During this project, we have developed the first prototype of AlGaN/GaN HEMT process on Si substrate at MIT, optimizing ohmic contacts, mesa-isolation, and submicron T-gate fabrication. Through systematic optimization, we achieved an excellent ohmic contact resistance of 0.4~0.5 Ω·mm through the ise of a Ti/Al/Ni/Au (200/1000/250/500 Å) metal stack annealed at 870 °C in N_2 ambient. Mesa-isolation by BCl_3/Cl_2 based ECR-RIE uniformly etched GaN at constant etch rate of 3.7 Å/s. By reducing ECR power, we have also developed a slower etching recipe (2 Å/s) suitable for the gate recess. By using advanced e-beam lithography and finding optimum development conditions, it has been possible to reduce the gate length to 70 nm while keeping a high fabrication yield. In longer gate length devices, L_g=0.5 μm, we have obtained reasonably good DC and RF performance with $g_{m,max}$=250 mS/mm, f_T=20 GHz and f_{max}=23 GHz.

Drain delay (τ_{drain}) becomes the most important delay as the geometry of AlGaN/GaN HEMTs is scaled down to sub-micrometer range (<70 nm). The drain delay is not scalable and ultimately limits the maximum frequency performance. From physical analysis and numerical simulation, we have found that the drain delay is inversely proportional to α, a parameter related to how injected channel electrons image at different contacts in the HEMT and α equals 3. Using this value we have successfully calculates saturated electron velocity in AlGaN/GaN HEMTs without contradiction between experimental measurement and Monte Carlo simulation.

The cutoff frequency (f_T) is defined as the maximum frequency at which the channel current can be modulated by the gate voltage. Unnecessary modulation of traps and gate leakage current lowers the modulation efficiency and finally degrade f_T. In this project, the traditional equation of modulation efficiency has been reexamined considering the effect of gate leakage current and we have proposed a new expression explicitly showing the effect of both traps and gate leakage current.

As mentioned before, the gate leakage significantly degrades the performance of GaN devices. To suppress the gate leakage current in AlGaN/GaN HEMTs we have applied an O_2 plasma treatment prior to the gate metallization. This plasma oxidation induced a self-limited growth of a thin (less than 4 nm) Ga_2O_3 gate dielectric and significantly reduced the gate leakage current by more than four orders of magnitude. As a beneficial side-effect, we have also found a strong correlation between the gate leakage current and the transistor subthreshold characteristics: the lower the gate leakage, the higher the ON/OFF ratio and the steeper the subthreshold slope. The O_2 plasma treatment turned out to be a very effective way for not only reducing the gate leakage current but also improving the ON/OFF ratio and subthreshold slope. Finally, we have demonstrated more than seven orders of magnitude ON/OFF ratio and a record nearly ideal subthreshold slope of 64 mV/decade in AlGaN/GaN HEMTs by the O_2 plasma treatment.

To identify and study the effect of gate-modulated traps, we have introduced a simple new technique to estimate these traps in AlGaN/GaN HEMTs based on the temperature dependence of subthreshold slope. By analogy with MOSFETs, the equation of subthreshold slope (S) in HEMTs is written as a function of temperature (T). Through the coupling of this equation and S vs. T measurements, we have obtained a level of trap density, $\sim 5\times10^{12}$ cm^{-2}eV^{-1} which well corresponds to the results in other groups.

Finally, an N-face GaN/AlGaN HEMT has been proposed to overcome high contact resistance and access resistance in Ga-face GaN HEMTs. This novel structure was fabricated by using substrate removal and transfer technology to the Ga-face AlGaN/GaN structure on Si (111) substrate. Wafer bonding and GaN thinning processes are optimized for this technology and the final structure is an N-face GaN/AlGaN structure on Si (100) substrate. Fabricating devices on N-face GaN has several advantages such as lower ohmic contact and access resistances, better electron confinement and higher implantation yield. Initial N-face GaN/AlGaN HEMTs have shown much lower access resistance than Ga-face GaN HEMTs, showing sheet resistance of 240 Ω/sq and 70% higher maximum drain current.

6.2. Future work

Although the results presented in this thesis have great potential, future work will have to show their effect on improving f_T and f_{max}, the high frequency performance of GaN HEMTs.

It is also important to optimize and combine each idea effectively to maximize high frequency performance. In addition, other technologies need to be investigated to overcome other existing problems limiting high frequency performance such as parasitic capacitances and low transconductance. There are many aspects that should be studied and here we suggest some of the most relevant ones for future research.

First of all, our ideas should be confirmed by measuring high frequency characteristics of the devices. Especially, f_T and f_{max} of the N-face GaN/AlGaN HEMTs or O_2 plasma treated samples should be compared to identically processed standard Ga-face AlGaN/GaN HEMTs. In parallel, the small signal circuit of the devices (C_{gs}, C_{gd}, R_{ds}, g_m, etc) should be considered to fully understand the effect of the new technology on the high frequency behavior.

Secondly, each proposed idea should be optimized and combined together in order to achieve maximum frequency performance. The drain delay can be engineered by optimizing the length and the shape of the field plates and the ohmic contacts on the N-face GaN/AlGaN HEMTs can be optimized by the same systematic method that we used in the standard Ga-face HEMTs. Once we have optimized technologies, it is important to combine all these technologies and take advantage of the minimized drain delay, high modulation efficiency, ultra-low ohmic contact and access resistances. These improvements will allow unprecedented high frequency performance of GaN HEMTs.

Finally, in spite of the recent progress, there are still other problems inhibiting high frequency performance of GaN HEMTs which should be addressed in the future. Gate capacitances, inversely proportional to f_T, are one of the most challenging parameters to control. One option to reduce some of the gate capacitances is to selectively remove the substrate wafer in the region underneath an AlGaN/GaN transistor. This will remove parasitic capacitances between gate and substrate. Another parameter that needs to be investigated is the transconductance which is proportional to f_T. Because the transconductance is improved by reducing the gate-to-channel distance, it is very important to develop reliable gate recess technology in the future.

In conclusion, it is a very exciting time for GaN-based transistors. Although these devices have already demonstrated excellent performance, we are still far from reaching their intrinsic maximum frequency performance. In the near future, the combination of advance technology and the amazing material properties of this semiconductor family will allow new breakthroughs and significant improvements in the frequency performance. We hope the different new technologies introduced in this thesis will be important steps in this direction and they will help to achieve the new performance levels required by the advanced wireless applications of the XXI century .

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