Commercialization of Low Temperature Copper Thermocompression Bonding for 3D Integrated Circuits

by

Raghavan Nagarajan

B.ENG. Electrical & Electronics Engineering
Nanyang Technological University, Singapore, 2007

SUBMITTED TO THE DEPARTMENT OF MATERIALS SCIENCE AND ENGINEERING IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

MASTER OF ENGINEERING IN MATERIALS SCIENCE AND ENGINEERING

AT THE

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

SEPTEMBER 2008

Signature of Author:.....
Department of Materials Science and Engineering
August 15th, 2008

Certified by: .....
Carl V. Thompson II
Stavros Salapatas Professor of Materials Science and Engineering
Thesis Co-Advisor

Certified by: .....
Chee Lip Gan
Assistant Professor, Nanyang Technological University (NTU), Singapore
Thesis Co-Advisor

Accepted by: .....
Samuel M. Allen
POSCO Professor of Physical Metallurgy
Chair, Departmental Committee on Graduate Students

Commercialization of Low Temperature Copper Thermocompression Bonding for 3D Integrated Circuits

by

Raghavan Nagarajan

Submitted to the Department of Materials Science and Engineering
on August 15th, 2008 in Partial Fulfillment of the Requirements for the Degree of
Master of Engineering in Materials Science and Engineering

ABSTRACT

Wafer bonding is a key process and enabling technology for realization of three-dimensional integrated circuits (3DIC) with reduced interconnect delay and correspondingly increased circuit speed and decreased power dissipation, along with an improved form factor and portability. One of the most recent novel and promising wafer bonding approaches to realizing 3DIC is Low Temperature Thermocompression (LTTC) bonding using copper (Cu) as the bonding interface material. This thesis investigates the LTTC bonding approach in terms of its technological implications in contrast to other conventional bonding approaches. The various technological aspects pertaining to LTTC are comprehensively explored and analyzed. In addition to this, the commercialization potential for this technology is also studied and the economic viability of this process in production is critically evaluated using suitable cost models. Based on the technological and economic outlook, the potential for commercialization of LTTC is gauged.

Thesis Supervisor: Carl V. Thompson II
Title: Stavros Salapatas Professor of Materials Science and Engineering

DEDICATION

This work is dedicated in memory of my beloved grandfather, ***Mr. S.N.Sivaramakrishnan***, who has been a great source of inspiration to me throughout my life. His divine blessings, compassion, unflagging support, good wishes and strong patronage have been a major driving force for me to achieve and fulfill all my endeavors in life successfully. I would like to take this opportunity to express my deepest gratitudes to him for everything he has bestowed me with.

ACKNOWLEDGEMENTS

First and foremost, I would like to convey my sincere gratitudes to both my supervisors ***Prof. Carl V. Thompson*** (MIT) and ***Dr. Gan Chee Lip*** (NTU, Singapore) for their timely guidance, useful advice, encouragement and support throughout the course of this work. I have gained a lot by interacting with them during the thesis discussion meetings and their suggestions have helped improve the quality of my work to a large extent. I have been greatly inspired by Prof. Thompson's courses in the Singapore-MIT Alliance (SMA) program and his teaching styles, his way of thinking and his approach to solving scientific problems have been fascinating. His courses have helped me look at semiconductors from a material science perspective in addition to the electronics perspective that I learnt during my undergraduate courses in Electronics Engineering at NTU. He is indeed one of my "role models" for my future ambition to join the academia. Thanks to Dr.Gan for organizing all the video conference sessions that I could use to update my thesis work to Prof.Thompson while I was here in Singapore.

Next, I would like to thank my parents *Mr.Narayanaswamy Nagarajan* and *Mrs.Srimathi Nagarajan* for the love and affection they have always showered at me. Without their psychological support, I would never have achieved what I intended to in life. The person I miss the most is my grandfather, *Mr.S.N.Sivaramakrishnan*, to whom I am dedicating this work. He has been instrumental in bringing me up since my childhood and propelling me to perform well in my research and has always stood by me during the course of my life. It is because of his constant encouragement and his divine blessings that I have been able to come up in life. Unfortunately, he is not with me today to share my happiness.

The greatest asset I have acquired through the SMA program are my friends who have become an integral part of my life. I have found some of the best friends of my life through the SMA program. They have been a major source of emotional support to me during my stay at MIT whenever I missed home and felt homesick. I have no words to express my gratitude to them. These are friends that will remain with me forever in my life and I am indeed very fortunate to have found them and I must thank the almighty for having given me such precious people. Let me take this opportunity to thank them individually. *Anay* (also nicknamed as "dumbass") and *Rajamouly* ("Raju") are two of the "coolest" friends I have ever had and by far, the ones with the best sense of humor. There have been many instances when I used to feel very dejected upon seeing my exam results at MIT. These two guys were the ones who comforted me all along and made me more sportive. *Kunal* (the one and only one who can challenge professors) has been a great advisor to me in all ways. I have benefited a lot from his advises and he is one of my true well-wishers. I know him since my undergrad days and we enjoy interacting with each other a lot. *Manik* (according to me the most handsome and "skeletony" Indians I have ever seen) is one of those soft characters whom I like talking to and making fun of very often. *Kwan Wee* (known as an "anti-social" person and the "grandfather" of our batch) has surprisingly been very social with me all along. He is according to me the most helpful person in our batch whom anyone could look up to when needed. He is one of those guys I admire a lot and like being scolded by him and we chat about interesting things for long hours every night disturbing each other's work. He is of a caring nature and along with *Yu Yan*, he helped organize various trips for our group both at MIT and in Singapore. *Yu Yan* and *Fidelia* (the youngest kid SMA has ever seen) are the two most cheerful and "enthu" girls in our batch who keep everyone around them excited and happy all the time. One thing I should admit I didn't like about *Yu Yan* was her desire to complete all her homework way before the deadline. *Qixun* ("Prof. Wee"), *Beng Sheng* (Mr. Handsome), "Uncle" *Song Yang*, *Zhoujia* (fatty boy), *Luo Jia* (the potential "rice-eater") *Man Yin* ("the rich i-Phone girl"), *Wardhana* (one with the smartest hairstyle), *Weimin* ("the future VIP of Singapore") and

Ha (always smiling as her name suggests) have all been great friends of mine and we have shared many interesting moments all along this journey. *Omkar* (CPE) (who is stuck with chemical reactions all the time and who ditches us for lunch and dinner whenever we call him) and *Priyanka* (MST) (who can give you facts and figures up to many decimal places which are totally irrelevant) were also part of our Indian gang and we had great fun going various places for dinner and cinema quite often while in Singapore. *Vivek*, my MIT roommate, is another guy who deserves mention. We had a good time as roommates at Tang Hall and enjoyed cooking delicious Indian food together.

As far as my thesis is concerned, I would like to thank *Wardhana* (SMA PhD) and *I Made Riko* (NTU PhD) who have helped me along the way with effective suggestions and provided useful reference materials for my study. The commercialization aspect of the technology investigated in this work has been largely possible because of the 3.207 module coordinated by *Prof. E.A.Fitzgerald.* I would like to thank him for the critical assessment of my work during the presentations for the 3.207 course.

Finally, let me extend my thanks to the SMA office at both the MIT and Singapore side for helping out in organizing the final thesis presentation. SMA was a great experience and its success stories will continue to unwind... It is the best example of how successful distance education programs can be.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

1. INTRODUCTION TO 3D INTEGRATED CIRCUITS

1.1 NEED FOR 3D INTEGRATED CIRCUITS

The electronics industry has been undergoing significant growth in the past four decades. This is spurred by the need for more sophisticated devices with higher computational power, increased data storage capacities, higher speed, lower power dissipation, increased portability and greater functionality. All these demands have led to rapid miniaturization of electronic devices all the way to the 45 nm technology that we have today. Further downscaling of devices has however become increasingly difficult given that we are approaching the lithographic limits[1] and the gate oxide layer[2] in the transistor has been reduced to just 1-2 monolayers of SiO_2. As a result, further downscaling, if attempted may cause very high tunneling currents across the gate oxide that may lead to high power dissipation which is undesirable from a circuit reliability viewpoint[2]. In addition to this, as interconnect widths shrink to the order of 1-10 nm, the effective resistivity of copper metallization has been increasing due to grain boundary and side wall surface scattering effects thereby nullifying the resistivity advantage that Cu earlier had[1]. Given this situation, researchers in the semiconductor industry have been looking into alternative ways of further miniaturization in the past few years. One of the effective ways is to fabricate ICs not just on a planar platform but to extend it to the +z direction. This vertical integration scheme is called *3D Integrated Circuits* (3DIC)[3].

Another motivation for research interest in 3DIC is the ability to integrate different heterogeneous device technologies together without making any modifications to the existing optimized processes for each of these technologies. Heterogeneous integration of devices[4] can be used to realize optoelectronic integrated circuits (OEICs) and System-on-Chip (SoC) architectures with adequate reliability as illustrated in Fig 1.1.

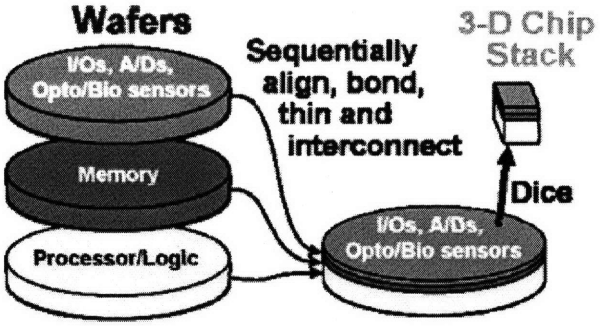


Fig 1.1: Heterogeneous integration of devices on a 3D IC layout platform to make SoC[4].

1.2 ADVANTAGES OF 3D INTEGRATED CIRCUITS

The advent of 3D integration offers many advantages compared to the conventional 2D platforms for device fabrication that was adopted in the past. Table 1.1 lists out the various advantages of a 3DIC platform[3, 5]. Fig 1.2 illustrates the reduced average distance between transistors due to the 3DIC architecture that helps enhance circuit speed and frequency of operation[5]. The logarithmic reduction in the number of interconnect segments for all lengths of interconnects is revealed by the graph[6].

Table 1.1: Various advantages due to implementation of 3D Integrated Circuits[3, 5].

ADVANTAGES of 3DIC
• Heterogeneous integration of devices to realize OEIC and SoC. • Reduced distance of global interconnects → Enhanced speed. • Higher integration density → more portable devices. • Higher form factor (capacity / volume ratio). • Cheaper than further downscaling beyond lithographic limits. • Faster access between memory and logic device modules. • Reduced overall resistance → lower joule heating and heat dissipation. • Reduced packaging cost. • Reduced power → fewer I/O pins to be driven. • Higher fault resistance.

1.3 APPROACHES TO 3D INTEGRATION

There are various approaches to realizing 3D integration. Each of these approaches has their own advantages and limitations. These have been highlighted in Table 1.2[7, 8, 9, 10, 11, 12] below. Based on the analysis presented in Table 1.2, the motivation for use of wafer bonding as a technique to 3D integration is clearly evident as it enables integration with a high density of interconnection and

does not disturb the existing optimized process technology sequence used for each of the individual wafers. Fig 1.3 illustrates the various wafer bonding techniques[13] mentioned in Table 1.2.

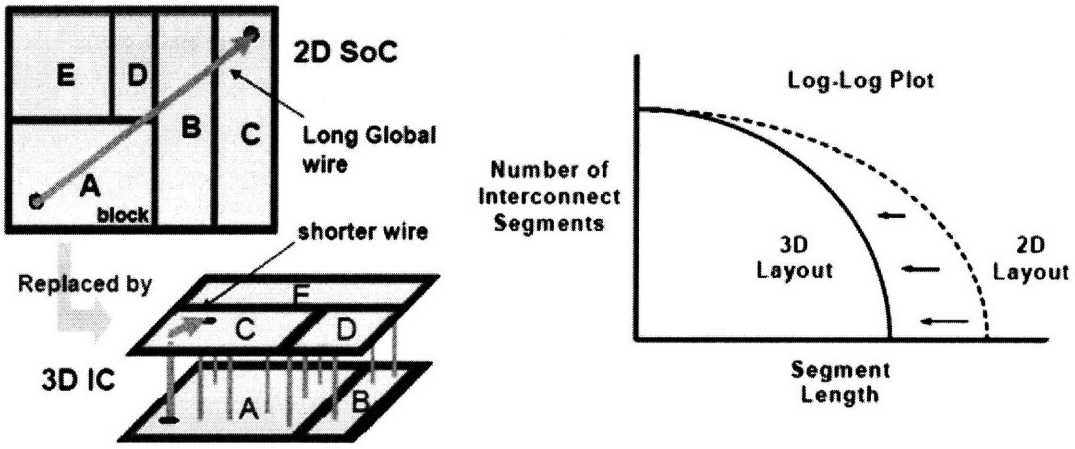


Fig 1.2: Reduction of global interconnect length and density of interconnects for 3D IC layout[5,6].

Table 1.2: Various techniques that may be used to realize 3D Integrated Circuits.

Technique	Advantages / Limitations
■ **BEAM RECRYSTALLIZATION**[7,8] Deposition of a second level polysilicon layer on top of an oxidized Si wafer in order to fabricate Si based thin film transistors on it. Need for intense electron or laser beam to induce recrystallization and remove grain boundaries in polysilicon.	(-) High temperature during melting of polysilicon (recrystallization) – cannot be sustained by 3D devices[7,8]. (-) Lack of control over grain size variations in polysilicon deposited, lower carrier mobility compared to single crystal silicon, effects of unintentional doping[7].
■ **SILICON EPITAXIAL GROWTH**[9] Etch a hole through a passivated Si wafer and epitaxially grow single crystal Si through the etched hole using the whole base Si as the seed layer. Si epitaxy involves vertical growth of Si through the etched hole followed by lateral overgrowth on the passivation dielectric.	(-) High temperature of epitaxy growth (1000^0C) affects device quality in lower Si device layers[9]. (-) Not suitable when metallization layers present under the dielectric since T = 1000^0C can cause Al metal lines to melt and Cu to substantially self-diffuse[9].

■ **SOLID PHASE CRYSTALLIZATION**[10, 11] Low temperature growth of amorphous silicon on oxidized Si substrate and subsequent lateral crystallization induced on the amorphous Si layer to form polysilicon using Ge seeding or Ni metal catalysts.	(+) Localized crystallization, low thermal budget (500 – 600^{0}C)[10]. (+) Lateral crystallization, dopant activation, minimal metal contamination, can be performed even when metallization layers are present[10, 11]. (-) Slow process.
■ **PACKAGE LEVEL 3D INTEGRATION**[12] Vertical stacking of dies or packaged chips using wire bonding or solder balls as interconnects to make multi-chip modules (MCM).	(+) Simple & high yield process. (-) Low density of interconnection. Wires could short each other in a large MCM.
■ **WAFER BONDING** Fabricate devices and interconnects on individual wafers and physically bond them after each wafer has been fully processed vertically for any level of stacking.	(+) Optimized processes for individual wafers remain undisturbed. (+) Higher density of interconnection. (-) Issues of bond adhesion quality due to thermal induced strain, patterned wafer alignment issues, wafer bowing and warping.

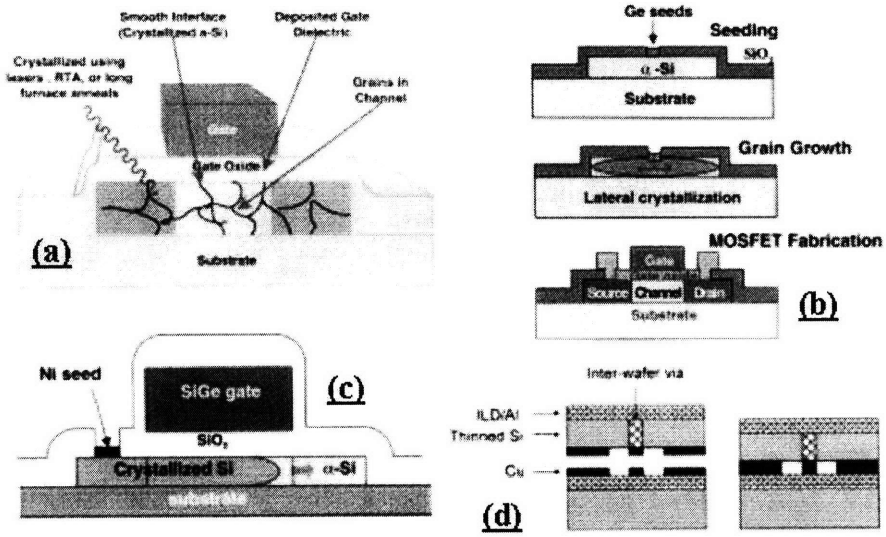


Fig 1.3: Various bonding techniques for 3D integration – (a) Beam recrystallization, (b) & (c) Solid phase crystallization, (d) Processed wafer bonding.[13]

CHAPTER 2

2. COPPER THERMOCOMPRESSION BONDING – OVERVIEW

2.1 TECHNIQUES OF WAFER BONDING

In order to stack wafers vertically on top of each other and bond them vertically, various bonding techniques have been explored in the past. Some of the more prominent techniques are listed in Table 2.1 along with a critical assessment of their advantages and limitations. Based on the analysis in Table 2.1, it is evident that *thermocompression bonding* (TCB) could be a good technique to adopt since the bonding metal layer serves the dual purpose of a mechanical as well as an electrical contact. In the other bonding techniques, further processing would be required for electrical interconnection thereby making the process more complex and reducing the yield.

Table 2.1: Various wafer bonding techniques and comparison of advantages (+) and limitations (-).

Bonding Technique	Advantages / Limitations
▪ **DIRECT BONDING** Bonding (fusion) of two contacting wafer surfaces at room temperature without any intermediate layer. Materials bonded: Si-Si[14], Si-SiO_2[15]. Formation of van der Waals or hydrogen bonds. Subsequent bond strengthening by annealing at elevated temperatures. Surface activation bonding (SAB)[16] – oxygen plasma pre-treatment for wafers before bonding + RCA wet clean to enhance bond quality.	(-) High annealing temperatures – (700 - 1000^{0}C) – cannot be sustained by metallization layers. Thermal expansion coefficient mismatch induced residual stresses[15]. (-) High annealing temperature may need to be compromised with ultra-high vacuum (UHV) levels and bonding duration → lower bonding throughput. (-) SAB increase surface roughness[17] degrading bond quality. High sensitivity to wafer bow, warpage and patterns. Bond only serves as a mechanical contact. (+) Best alignment accuracy among all bonding methods (since bonding done at room temperature)[18].

■ **SOLDER / EUTECTIC BONDING**[19] Use of a low melting temperature (eutectic temperature) alloy as an intermediate layer to facilitate bonding between wafers. Eutectic alloys used – Au-Si, Au-Ge, Au-Sn.	(+) Low temperature process (280 – 360^{0}C). Less sensitive to surface roughness, topology and particulates[20]. (+) Conductive eutectic alloys serve as mechanical and electrical contact for the bonded wafers. (-) Eutectic material may experience dewetting close to the eutectic temperature leading to low bond adhesion. Voids / non-uniformity at the bonding interface[19]. (-) Spontaneous oxide formation of Sn, Ge or Si under ambient condition hinders bonding[19].
■ **ANODIC BONDING**[21, 22] Application of an electric field (100 – 1000V) between an insulating substrate (e.g. glass) and conducting substrate to enhance bonding strength through electrostatic attraction. Materials - Silicon / metals with glass at T = 300 – 400^{0}C.	(+) Less sensitive to surface roughness and particulates[21, 22]. (-) Thermal expansion coefficient mismatch induced residual stresses. Outgassing of glass at room temperature[23].
■ **THERMOCOMPRESSION BONDING** Traditionally refers to application of an external high pressure load and high temperature in order to bond the wafers by plastic deformation. Materials – Si[24], glass, eutectic, Cu[25], Au[26].	(+) High temperature requirement may be relaxed through high applied load and plasma activation. Bond serves electrical and mechanical contact[25]. (+) For metallic TCB, high thermal conductivity of metals compared to polymers or oxides makes it a thermal conduit ensuring effective release of heat from joule heating[25]. (-) Thermal expansion coefficient mismatch induced residual stresses. Oxidation of bonding surfaces impedes good bond quality. Highly sensitive to surface cleanliness and roughness[25].

■ **ADHESIVE BONDING** Use of a polymer adhesive on one or both wafer surfaces and application of pressure to enforce wafer contact through the intermediate adhesive layer (Fig 2.1)[27]. Adhesive Material – Benzocyclobutene (BCB).	(+) Relatively low bonding temperature. Insensitive to the topology and surface contaminants on the wafer surface. Compatibility with standard CMOS process. Any two materials may be bonded[28]. (+) Simple, robust & low-cost process. No CMP, surface activation or wafer cleaning needed[28]. (-) Temperature instability of polymer (need for high glass transition temperature), mechanical instability, Outgassing of polymer during bonding could cause void formation. Low creep resistance and high moisture uptake[27].

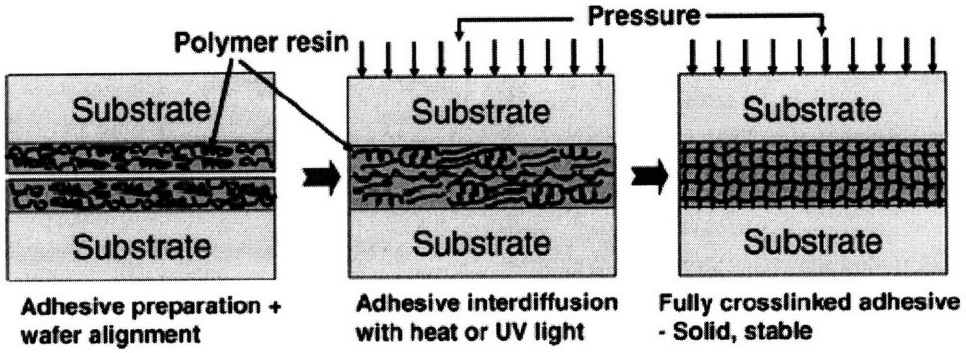


Fig 2.1: Adhesive bonding process using polymers such as BCB as intermediate glue layer[27].

2.2 BONDING ARCHITECTURE

Various architectural aspects may be explored in the process of wafer bonding and stacking. They differ in the sequence of processes used (via-first / via-last)[29] or the sequence of the interfaces being bonded (face-to-face [F2F] – back-to-back [B2B] / face-to-back [F2B])[30] or the elemental blocks involved in the bonding (chip-to-chip [C2C], chip-to-wafer [C2W] and wafer-to-wafer [W2W])[31]. Let us explore each of these in greater detail.

2.2.1 VIA-FIRST & VIA-LAST PROCESS

In the process of bonding 3D devices, the through-silicon via (TSV) via interconnecting the metallization layers of different wafers could be fabricated in two sequences. One sequence is where the via could be formed before bonding so that the TSV are bonded upon wafer contact. This is called the VIA-FIRST approach[29]. The other sequence is where the dielectric passivation layers of the wafers are bonded together and this is followed by etching high aspect ratio holes to form TSV and interconnect the device layers of the various wafers. This is called the VIA-LAST

approach[29]. Table 2.2 provides a brief comparison of these two approaches of TSV fabrication[29, 32]. Based on the various wafer bonding techniques described in Table 2.1, direct, anodic, eutectic and adhesive bonding are all compatible only with the via-last approach where the bonding is initiated between any two material interfaces and through-silicon via interconnections formed after the bonding process. Metal thermocompression bonding is however compatible for both via-first and via-last approaches.

Table 2.2: Comparison of the Via-First and Via-Last approaches to TCB bonding.

VIA-FIRST Approach	VIA-LAST Approach
• TSV formed on individual wafers prior to bonding. Here the material of contact during bonding is the Cu via.	• TSV fabricated after the individual wafers are bonded. Here the material of contact during bonding is the top-most dielectric passivation layer or other material layers (such as adhesives) coated on each wafer.
• Aspect ratio requirement for TSV is lower since TSV is formed on each individual wafer prior to bonding[32].	• Aspect ratio requirement for TSV is high since TSV is formed through the bonded thick stack of Si substrate[32].
• High signal bandwidth between device layers and higher interconnection density.	• Lower signal bandwidth and lower interconnection density since the aspect ratio of TSV achievable is limited by DRIE as well as the DRIE trench tapering angle.

2.2.2 F2F-B2B / F2B-F2B BONDING

The bonding interfaces for stacked wafers could be alternating face-to-face (F2F) and back-to-back (B2B) or consistently face-to-back (F2B) for every interface as illustrated by Fig 2.2 for the case of copper thermocompression bonding[30] where "face" refers to the back-end-of-line (BEOL) metallization layers of a processed wafer while "back" refers to the bulk Si substrate on which front-end device transistors are grown. It has been suggested that it is more favorable to bond wafers in an F2F-B2B configuration as compared to a F2B-F2B configuration since every alternating F2F interface enables a very high density of inter-wafer interconnections[30] and every alternating B2B segment may be used to fabricate integrated microchannels[33] in the Si substrate regions where through-silicon via (TSV) does not exist to enable efficient device cooling and effective 3D heat extraction through microfluidic flow. If an F2B-F2B configuration is used, then high density of interconnections cannot be achieved between any two bonding interfaces thus limiting the device functionality and performance. All the wafer bonding techniques in Table 2.1 are compatible for both F2F-B2B and F2B-F2B bonding interfaces.

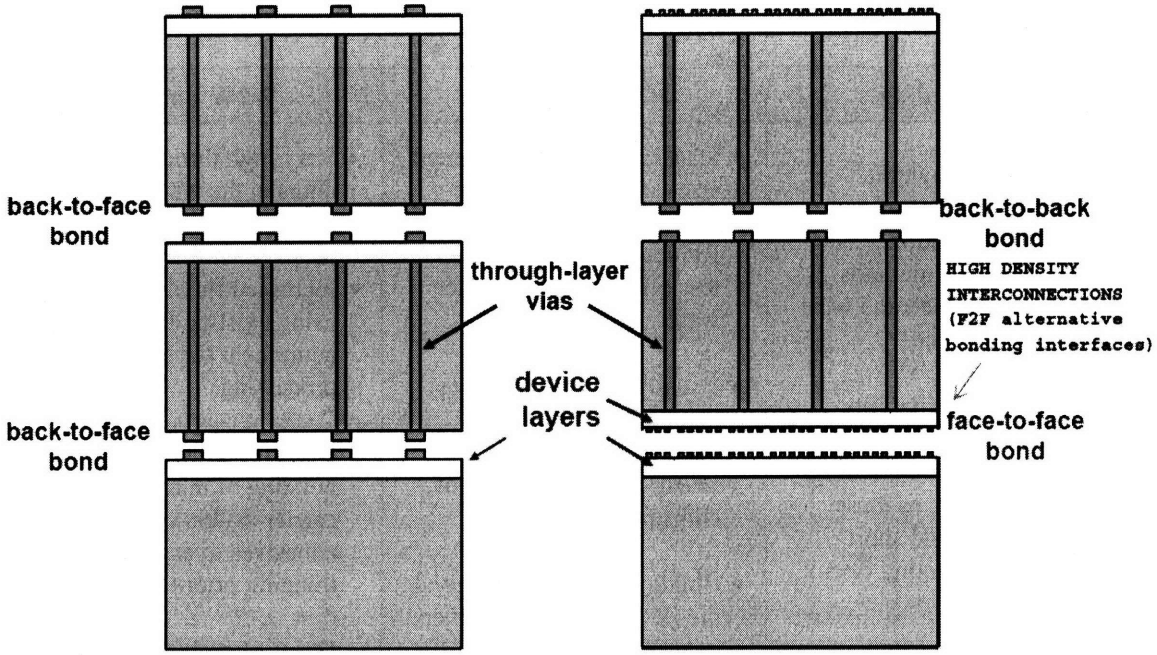


Fig 2.2: TCB achieved either by B2F bonding or alternative F2F-B2B bonding strategies[30].

2.2.3 C2C – C2W – W2W BONDING

The elemental blocks of a bond could be either a chip or the entire wafer. This brings about three possible combinations of structures - chip-to-chip (C2C), chip-to-wafer (C2W) and wafer-to-wafer (W2W) bonding[31]. The differences between these bonding schemes are highlighted in Table 2.3. Based on the comparison provided, from a mass scale production perspective, where high throughput and yield are both required, W2W bonding seems to be the best approach to bonding and this is indeed the technique adopted by most companies that have developed novel electronic devices using 3D integration since it requires minimal investment in acquirement or modification of existing processing equipments (most standard fabrication equipments in a fab are for wafer-scale processing) for the additional 3D processes. All the bonding techniques in Table 2.1 are compatible for C2C, C2W and W2W stacked structures.

Table 2.3: Comparing and contrasting the three different bonding approaches – C2C, C2W and W2W [31].

C2C Bonding	C2W Bonding	W2W Bonding
• Very low throughput. • Traditional manufacturing and packaging methods such as die attach and wire bonding required. • More serious reliability concerns in the case of high density wire bonding interconnection as these wire bonds could short each other affecting circuit functionality[32]. • Highest yield if "known good die (KGD)" are identified and bonded.	• Stacking of dies of different sizes such as a 12" logic device Si wafer with a 4" RF device GaAs wafer – less efficient use of larger wafer. • Usually lower throughput than W2W bonding. Throughput is very sensitive to the number of chips per wafer. • Bonding with "known good die (KGD)" ensures higher overall yield than W2W. • Bonding of multiple dies on a base wafer – formation of via after bonding is difficult – via-first bonding approach is preferred. • Need to adjust the center of force while permanently bonding all the chips to the wafer base when some die on the base wafer are not KGD and therefore not bonded to any chip on top. • Limited substrate back-thinning capability due to presence of non-uniform unbonded vacant sites on base wafer. • Flexible chip size, reduced design cost, shorter time to market. • Less stringent alignment requirements than W2W bonding.	• Very high throughput as all chips in the wafers are bonded at once. • Increased flexibility of using existing fab equipment for further processing. • Need for temporary bonding of thin wafers with carrier wafers using adhesives to enable wafer thinning prior to bonding. • Chips of each stacking level need to be of the same size. • Very stringent alignment requirements; yield is highly sensitive to alignment. Relatively lower yield process.

2.3 FUNDAMENTALS OF THERMOCOMPRESSION BONDING

Thermocompression bonding (**TCB**) typically involves bonding of the metal layers on the bonded wafers. There are various process parameters and physical factors that affect the metal-metal bond toughness. All these factors need to be controlled and optimized in order to achieve a good bond quality. The most prominently used material for TCB is copper (Cu) since it is also the material of choice for the current generation of nano-interconnects. Table 2.4 lists out the key factors that influence the bond quality[25, 33].

From Table 2.4, it is evident that good bonding can be achieved with a high applied load and CMP polished surface along with either a high temperature bonding or with high vacuum condition at low temperature. This argument brings us to two distinct modes of TCB namely high temperature thermocompression (**HTTC**) and low temperature thermocompression (**LTTC**). The distinct features of these two bonding approaches is presented next.

Table 2.4: Various process parameters and factors affecting quality of thermocompression bonding.

PARAMETERS	EFFECTS
BONDING TEMPERATURE	• High temperature bonding at around 400 – 500^{0}C is typically used for Cu bonding as these high temperatures cause decomposition of Cu_xO if any formed[25]. • Low temperature bonding (<100^{0}C) would be desirable so as to minimize the thermal mismatch induced residual stresses in the fabricated device and metallization layers[33].
ANNEALING TEMPERATURE	• Post-bond annealing at moderate temperatures helps in enhancing grain growth and inter-diffusion and forming a good bond interface[25].
VACUUM LEVEL	• To prevent surface re-oxidation of Cu and minimize presence of surface contaminants during the bonding process, an ultra-high vacuum (UHV) level of about 10^{-10} Torr is desirable. Current wafer bonders however are not equipped with this facility and vacuum levels around 10^{-5} Torr is the current standard[33].

MATERIAL	• Although Cu is the standard material of choice for TCB, Au may also be an attractive option. Bond quality depends on the yield stress and work hardening index. Since these two material properties are lower for Au as compared to Cu, the true contact area of bonding for Au could be higher than Cu, leading to a low resistance contact although resistivity of Au is higher than Cu[25]. • Oxidation of Au is kinetically not very feasible as compared to the spontaneous non self-passivating oxidation process in Cu. Oxide coated metal bonding leads to very low bond quality depending on the number of oxide monolayers formed[25]. • Processing issues associated with Au limit its applicability and it also introduces deep donor trap levels in the forbidden bandgap of Si affecting performance of minority carrier devices.
GEOMETRY	• Bond quality affected by thickness of bonding metal layers. Thicker layers undergo increased plastic deformation and enhance bond quality[34]. • Higher surface roughness of wafers is detrimental to a good bond quality. Reduction of surface roughness requires chemical mechanical polishing (CMP)[25]. • Smaller pattern feature sizes increase bond strength since load pressure is inversely proportional to the area of the feature. • Orientation of the features with respect to any crack initiation sites also affects the bond integrity. If crack is oriented perpendicular to the features, then fracture resistance is higher since multiple crack initiation and nucleation events would be necessary for complete bond fracture[35]. • Bonding surface pattern density and non-uniformity in pattern density across wafer have an effect on bond quality.
PROCESSING	• Surface pre-bond cleaning using acetic acid or HCl or RCA and reducing gas (N_2 / H_2) purge in the bonding chamber to remove any native oxide helps enhance bond toughness. Plasma activation of surface (SAB)[16] improves bond quality. • Post-bond annealing in order to facilitate grain growth, atomic self-diffusion and recrystallization at the metal bonding interface that helps increase bond toughness[25].
APPLIED PRESSURE	• Higher applied pressure enables elastic deformation of bowed wafers and enhances bond quality as a result[25].
BONDING DURATION	• Bond duration is an important criterion especially for low temperature bonding where sufficient time is required for grain growth and atomic interdiffusion when the kinetics is unfavorable.

2.3.1 HIGH TEMPERATURE THERMOCOMPRESSION (HTTC)

High temperature thermocompression (HTTC) bonding involves bonding of metal coated wafers at relatively high temperatures of around 400 – 500^{0}C at moderate vacuum levels of about 10^{-5} Torr[25]. The high temperature causes the metal layer to have a low yield stress and undergo substantial plastic deformation to form a good interface and strong metallic bond under a moderate to high applied load. A typical scheme for HTTC could be to have a pre-bond chamber for wafer cleaning and alignment at a very low vacuum of 10^{-3} Torr, followed by a high vacuum bonding chamber at 10^{-6} Torr and subsequently a post-bond annealing chamber also at a low vacuum of 10^{-3} Torr as illustrated in Fig 2.3. This kind of a scheme is currently being implemented by *Tezzaron*® and *EV Group*®[36].

There are various problems associated with the HTTC process. The large thermal expansion coefficient mismatch induces differential expansion of various material layers in the processed device wafers causing high residual stresses to be developed that could cause the wafers to bow or warp. This could degrade the performance characteristics of the fabricated devices. Therefore, use of high temperature is to be avoided.

2.3.2 LOW TEMPERATURE THERMOCOMPRESSION (LTTC)

The problems associated with the use of a high temperature may be resolved by using a low temperature (possibly room temperature) process. However, at low temperatures, since oxide decomposition is unfavorable, other suitable measures need to be taken that include use of UHV to avoid an oxidizing ambient as far as possible and in-situ pre-bond cleaning of the wafer surface using acetic acid and reducing gas purge (H_2 / N_2) as well as plasma activation for enhancement of bonding[33]. As indicated in Fig 2.3, the vacuum levels needed for LTTC could be as high as 10^{-10} Torr[33]. All the bonding processes including cleaning and alignment are performed at 10^{-10} Torr without any break in the vacuum. The use of LTTC has not been adopted in the industry yet and it is a topic of current research at various research institutions and universities, including *MIT, US* and *Institute of Microelectronics* (IME), *Singapore.*

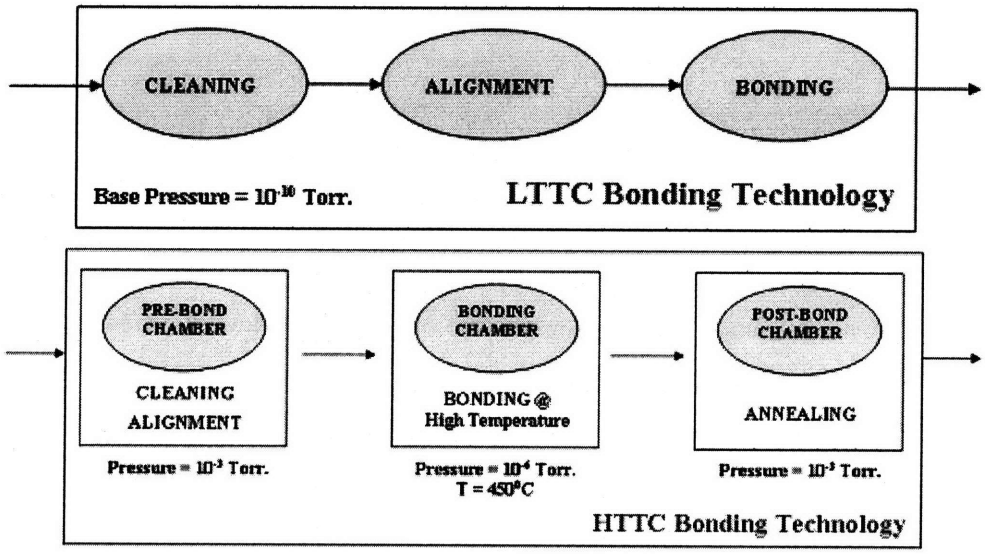


Fig 2.3: Typical bonding process sequence for HTTC and LTTC bonding technology.

2.3.3 ISSUES WITH LTTC TECHNOLOGY

The commercializing potential of the LTTC technology depends on the yield and throughput of this new process as well as the additional costs involved in using UHV vacuum pumps and chambers to maintain the bonding chambers at 10^{-10} Torr. Moreover, the yield and throughput of this new technology remains a major issue of concern. Unlike the HTTC process where the high temperature enables good and fast bonding due to favorable kinetics that facilitates grain growth and diffusion, the LTTC process is not thermally activated and therefore a longer bonding duration would be required for good adhesion to be achieved although recrystallization of copper can take place even at room temperature since Cu has an intrinsic high grain boundary mobility at room temperature[37]. This in turn translates to a lower throughput for LTTC thus requiring more LTTC bond chambers and vacuum pumps to cater to the production rate in the industry. All these concerns are addressed in a later chapter which presents a cost model comparing the LTTC and HTTC technologies from an economic perspective. Table 2.5 summarizes some of the key differences between the HTTC and LTTC technologies described above.

Table 2.5: Comparison of the HTTC and LTTC bonding technologies for TCB[25, 33].

HTTC Bonding	LTTC Bonding
• Bonding temperature ~ 400 – 500^{0}C → favorable kinetics for good bonding in a shorter duration as copper oxide decomposition is favored at these high temperatures. Higher throughput.	• Bonding temperature < 100^{0}C (or room temperature) → kinetics not very favorable for bonding. Longer duration needed to achieve good adhesion. Lower throughput.
• Higher thermal expansion coefficient mismatch induced residual stresses. Device performance affected[33].	• Minimal thermal induced stresses. Device performance unaffected[33].
• Lower vacuum levels needed. Surface activation or plasma treatment may not be required.	• UHV vacuum of 10^{-10} Torr required. Surface activation or plasma treatment may be helpful[33].
• Yield is affected by the high CTE mismatch induced residual stresses.	• Yield is highly sensitive to the vacuum level achieved and bond duration.
• Already commercialized[38].	• Need for UHV systems incurs extra expenditure. Still in research phase.

2.3.4 PROCESS SEQUENCE FOR TCB

There are various processing steps needed to realize Cu TCB. After the wafers have been fully processed including front-end-of-line (FEOL) as well as back-end-of-line (BEOL) (devices and interconnects fabricated) using their corresponding sequence of processes, Cu leads that protrude out of the wafer surface need to be fabricated. This involves a sequence of additional process steps as listed in Table 2.6[39]. This is just one of the possible process flows that could be considered. Other process sequences may also be acceptable. It is necessary to ensure during these process steps that the temperature is kept low to avoid affecting the device performance.

Fig 2.4 shows a schematic of the process sequence used for a two-wafer F2F bonding where the passivating oxide layer is recessed to expose the Cu patterns on the bonding surfaces[40].

Table 2.6: Typical process sequence for Cu TCB[39].

PROCESS SEQUENCE for TCB	
1.	**LITHOGRAPHY** – The regions on the processed passivated wafer surface where etching is to be carried out for deposition of through-silicon via (TSV) needs to be defined.

2.	**DRIE ETCHING** – The standard DRIE BOSCH® process (SF_6 / CF_4 chemistry) which is used in MEMS processing is to be used here for etching high aspect ratio (AR) holes or trenches for TSV via.
3.	**COPPER SEED LAYER DEPOSITION** – A seed layer of Cu is to be deposited at the high AR trench bottom to enable subsequent electroplating of Cu to fill the TSV trench.
4.	**COPPER ELECTRODEPOSITION** – Having etched the TSV holes, blanket electrodeposition of copper is performed to form Cu filled TSV and additional Cu blanket films on the surface of the wafer.
5.	**CHEMICAL MECHANICAL PLANARIZATION (CMP)** – A CMP process is used to flatten the wafer surface prior to bonding and polish away the extra Cu films on the wafer surface.
6.	**OXIDE ETCH** – Etch away a small layer of inter-metal dielectric (IMD) on the surface of the wafer to cause the TSV Cu leads to protrude.
7.	**WAFER CLEANING** – Use RCA or acetic acid solution to clean the wafer and strip out any intrinsic metal oxide layers formed.
8.	**SURFACE ACTIVATION** – Use O_2 or Ar plasma to activate the surface prior to bonding. This step is however optional.
9.	**ALIGNMENT** – Ensure precise alignment of the wafers with minimal alignment errors.
10.	**BONDING** – Bring the wafers into contact and apply sufficient load to so as to cause plastic deformation of the contacting metal surfaces and enable metallic bonding to take place.
11.	**ANNEALING** – After bonding, perform a moderate temperature anneal (500^0C) to allow for grain growth, Cu interdiffusion and creation of a good adhesion bond interface.

2.3.5 PROCESSING ISSUES IN TCB

There are various processing issues to be considered during the thermocompression bonding process. These issues need to be tackled effectively in order to achieve a high bonding yield and sufficient true contact area of the bond. Some of the key issues are discussed below:

DISHING – In patterned Cu lines to be bonded, the use of CMP for polishing these lines prior to actual bonding could result in "dishing" effects as shown in Fig 2.5[25]. As a result of dishing, the true contact area of patterned wafers that are bonded is very low thus resulting in poor bonding quality. Even large applied loads may not be helpful in minimizing dishing effects much since the depth of these dished pits can be as high as around 50 nm.

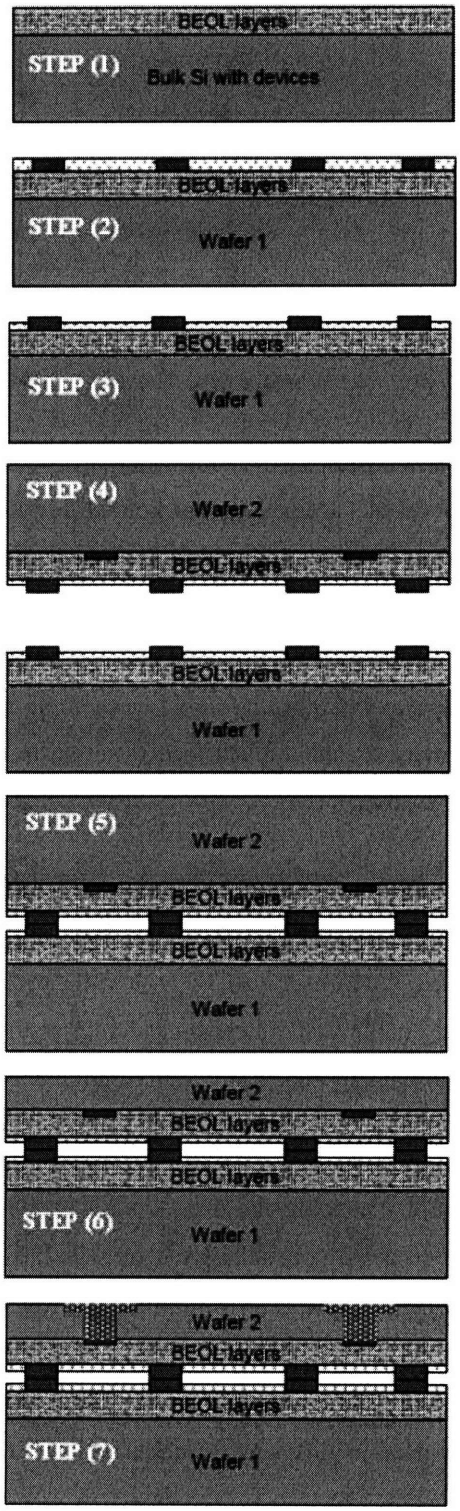


Fig 2.4: Typical process sequence for F2F TCB patterned Cu layer bonding – Steps - (1) FEOL + BEOL; (2) oxide layer deposition, patterning and Cu pad formation; (3) oxide layer recess to expose Cu pads; (4) F2F alignment; (5) Thermocompression bonding; (6) CMP to back grind top wafer and (7) lithography and patterning for TSV and probe-pads[40].

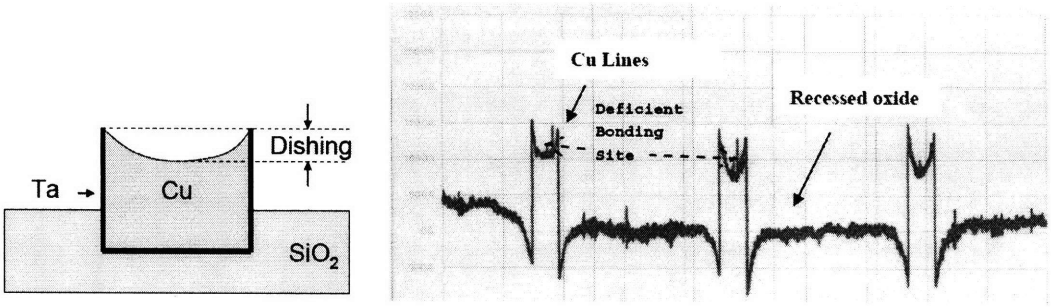


Fig 2.5: Illustrating the dishing effects observed in patterned Cu lines due to CMP[25].
The figure on the right is the actual profilometer image used to determine the depth of a Cu dish surface.

GLOBAL BONDING NON-UNIFORMITY – While dishing effects account only for local bonding non-uniformities for patterned Cu lines, global non-uniformities[30] in the bonding area could also exist due to wafer bow and warping induced by the FEOL and BEOL processing of the wafers and insufficient elastic deformation at the edges of the bowed wafers to achieve good contact. These bowing effects are detrimental to bond quality on a global wafer scale. An additional source of global bonding non-uniformity could be the non-uniform density of pattern features and wrong center of gravity for the applied load resulting in non-uniform pressures at different locations of the bonding wafers.

CARRIER WAFERS – The substrate bulk layer of the wafers that are bonded need to be thinned in order to stack more levels of wafers. Substrate thinning and TSV fabrication after bonding could be detrimental to the bond quality and therefore, it is usually carried out before the bonding process. It is difficult to handle thin wafers for bonding as they are brittle and tend to warp or bow easily. Temporary bonding of thin substrates to carrier wafers is a useful approach to enable good bonding.

The sequence followed for temporary bonding and debonding is shown in Fig 2.6[31]. The device wafer is first bonded to a carrier wafer using an adhesive layer with the device layer face down in contact with the adhesive layer. This is followed by wafer thinning and subsequent bonding of the carrier supported thinned wafer with another wafer. Finally, after bonding, when the carrier support is no longer required, appropriate temperature or UV light or chemical solutions are used to detach the carrier wafer finally resulting in a successful thinned wafer bonding.

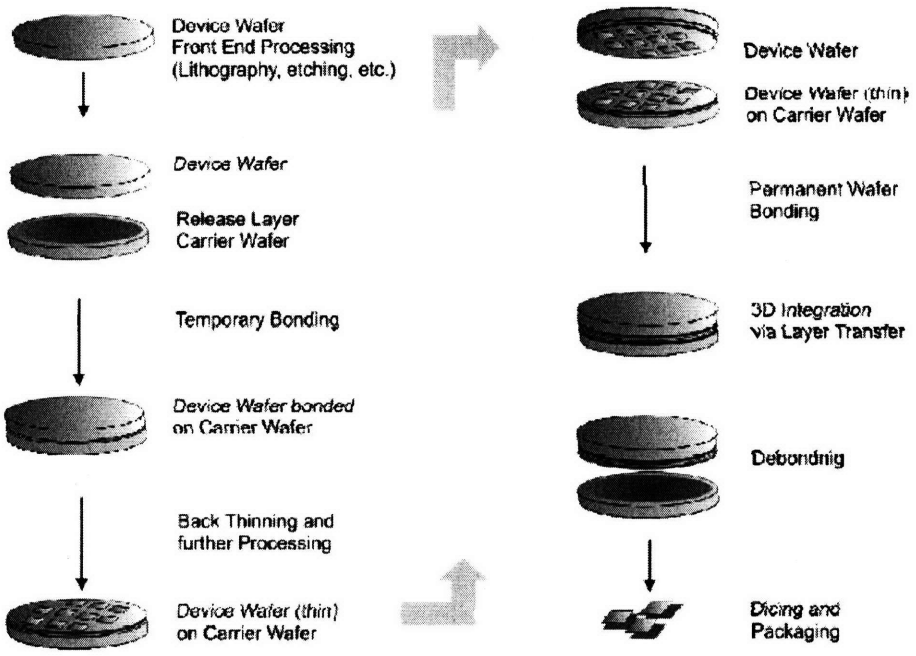


Fig 2.6: Process sequence for wafer bonding involving use of carrier wafer to handle thin substrates[31].

WAFER ALIGNMENT – For sub-micron high density pattern features to be bonded, the alignment of the wafers prior to and during the bonding period needs to be very precise. However, there are limits to the accuracy achievable in alignment. There are two methods of alignment – direct and indirect. Direct alignment involves direct live IR imaging of alignment keys on the wafer prior to bonding while indirect alignment involves the use of an external reference positioning system.

Devices with low interconnection density can tolerate alignment errors around 2 μm while in the case of high interconnect density, alignment accuracy in the sub-micron range would be required[31]. Alignment errors could arise either prior to bonding during the alignment phase due to the performance limitation of the aligning equipment or during bonding due to temperature and pressure non-uniformity that could cause bowing or warping and increase misalignment errors. Statistical process control (SPC)[31] is required in order to minimize alignment errors as far as possible.

2.3.6 ELECTRONIC IMPLICATIONS OF TCB

It is necessary to examine the effects of wafer bonding on the electrical device and circuit performance parameters. Some of the electronic implications of TCB based wafer bonding are

discussed in Table 2.7[13]. Although not specific to TCB, in general, all wafer bonding based 3D integration schemes have similar implications on the electrical device performance characteristics.

Table 2.7: Implications of TSV based Cu TCB on electrical device performance[13].

IMPLICATIONS OF TCB on ELECTRICAL DEVICE PERFORMANCE
1. **POWER** – 3D integration results in a smaller wire length distribution as compared to 2D with the largest reduction observed for the longest paths. Shorter wires imply lower average load resistance and capacitance and decrease the number of repeaters needed for long wires thereby causing less power loss. Compared to 2D, 3D ICs are expected to improve the wire efficiency by 15% and reduce total active power by more than 10%.
2. **NOISE** – Shorter wires in 3D have lower wire-to-wire capacitance resulting in less noise coupling between signal lines. Reduced number of repeaters also ensures lower noise and higher signal integrity. Moreover, electromagnetic interferences such as interconnect crosstalk, wire-substrate coupling and inductance effects are much lower in the case of 3D IC.
3. **FAN-OUT** – Since 3D ICs have a lower wiring load, a greater number of logic gates may be driven implying higher fan-out.
4. **INTERCONNECTS** – As interconnects (Cu) in the 2D circuits are further downscaled and the barrier layer thickness (Ta) unable to be proportionately downscaled, surface scattering effects of electrons become dominant in addition to the electron bulk scattering mechanisms such as phonon scattering. This increases the effective resistivity of Cu nano-interconnects significantly thereby motivating the need for 3D ICs so that further downscaling of interconnects can be avoided and yet performance improvement achieved due to lower total global interconnect length in a 3DIC. Increases in interconnect temperature due to joule heating effects also cause the resistivity of Cu to increase. Avoiding further downscaling in 2D by moving to a 3D layout prevents further aggravation of joule heating.
5. **INDUCTANCE** – Reduction of wire length helps reduce inductance and presence of second substrate close to the global wires might also help lower the inductance by providing shorter current return paths provided the substrate resistance is sufficiently low.

CHAPTER 3

3. PHYSICS & MECHANICS OF WAFER BONDING

3.1 PHYSICS & MECHANICS OF WAFER BONDING

Having looked at wafer bonding and its classifications, techniques, associated process sequence, process and material issues, failure mechanisms and its effects on the electrical device performance, it is necessary to take a physical perspective and analyze the bond strength of bonded wafers with respect to various factors that would impact it. This requires development of a mechanics-based model to quantify bond strength. This chapter presents the model developed to characterize the bond strength of bonded wafers.

Wafer bonding is accomplished by bringing the wafers into contact with each other so that chemical bonds could be formed at the interface. Since the forces of attraction are short range, sufficient load is to be applied to bring the rough (non-flat) surfaces into contact. Since the wafers are typically bowed as illustrated by Fig 3.1, we can model the bonding process such that the wafers come into contact at the centre and then the applied load causes elastic deformation of the wafers and the bond front propagates from the centre towards the edge[34]. As the bonds are formed, the surface energy is lost and interface energy is gained. In addition, elastic energy is also stored when bowed wafers are bent for bonding to be initiated.

Taking the surface energy for wafers 1 and 2 to be γ_1 and γ_2 and the interfacial energy to be γ_{12}, the net change of energy due to the formation of the bonded interface is known as *Dupre work of adhesion* (W) and is expressed as in (2). This work of adhesion refers to the energy available per unit area to bond two surfaces. The requirement for a successful bonding to take place is that the work of adhesion must be sufficient to cause the wafers to deform elastically to a common shape.

$$W = \gamma_1 + \gamma_2 - \gamma_{12} \tag{1}$$

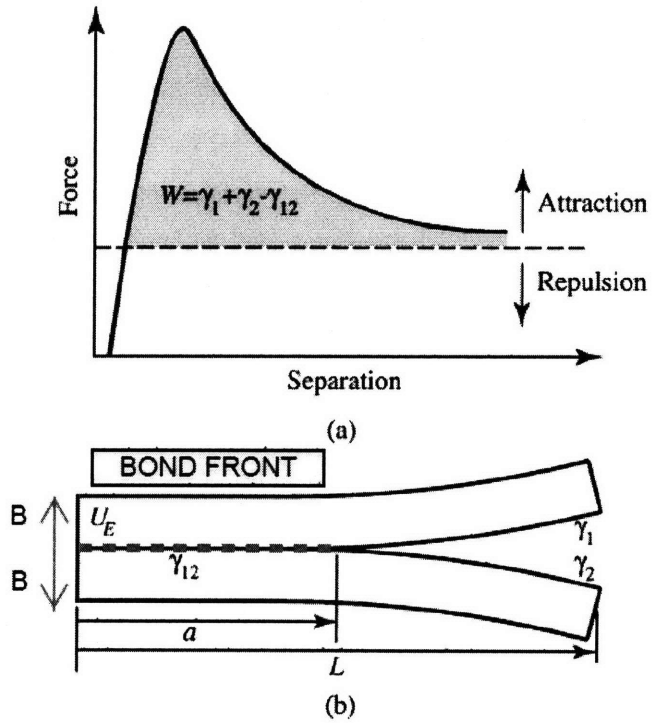
Given that the two wafers being bonded each have a width (B), the total energy in the system, U_T as a function of bond front position, a, is given by (2) where the first term, U_E is the elastic energy accumulated in the wafers as they conform to one another and is a function of the bond front position. The second and third terms refer to the total interface and surface energies of the bonded and unbonded regions of the bond face respectively[34].

$$U_T = U_E + \gamma_{12} \cdot [aB] + (\gamma_1 + \gamma_2) \cdot [(L-a) \cdot B] \tag{2}$$

The system attains equilibrium when the total system energy is minimized. Therefore, the bond front would propagate until the equilibrium condition in (3) is satisfied, where A is the area of the bonding interface when wafer bonding is considered in 3-D.

$$\frac{dU_T}{da} = 0 \xrightarrow{3-D} W \geq \frac{dU_E}{dA} \tag{3}$$

As long as the inequality condition in (3) is satisfied, the bond front of the bonding interface will continue to progress from the centre towards the edge of the wafer. The quantity dU_E/dA refers to the *strain energy accumulation rate* and it is a function of the wafer geometry and the material properties.



(a) A typical force separation curve for two surfaces. The area under the curve represents the work of adhesion. (b) The change in system energy as two surfaces are bonded. Surface energy (γ_1, γ_2) is lost, interface energy (γ_{12}) and strain energy (U_E) are gained as a increases.

Fig 3.1: Force-separation curve for two wafer surfaces and illustration of the bond front for bonding of bowed wafers[34].

Surface imperfections in the wafer will affect the quality of the bond adhesion and these imperfections may be categorized into three types – (a) wafer bow at the global wafer scale due to residual stresses that arise upon thin film deposition; (b) surface waviness (warping) at the

millimeter scale and (c) surface roughness at the nanometer scale. Let us first analyze the effect of wafer bow on the bonding success.

3.1.1 EFFECT OF WAFER BOW[34]

Fig 3.2 shows the case of two bowed wafers with initial curvatures, κ_A and κ_B, thicknesses h_A and h_B, elastic moduli E_A and E_B and a common Poisson ratio (υ) where the bond front has propagated up to $r = a$ and another length of $(b\text{-}a)$ remains to be bonded. Given this bonding situation, the strain energy, U_{Ei} for each wafer may be modeled in terms of the wafer curvature and the other parameters as given by (4) making use of the *linear plate theory*. In (4), κ_f refers to the final wafer curvature after bonding.

$$U_{Ei} \propto E_i h_i^3 \cdot (\kappa_f - \kappa_i)^2 \cdot \frac{a^2 b^2}{(1-\nu_i)\cdot\left[b^2(1+\nu_i)+a^2(1-\nu_i)\right]} \tag{4}$$

Using (5) where the total nominal bonding area $A = \pi a^2$ and summing up the strain energy accumulation rates for both the wafers being bonded, the overall strain energy accumulation rate may be given by (6) where $U_E = U_{E1} + U_{E2}$. This parameter dU_E/dA may now be compared with the work of adhesion (W) to determine the extent to which the bowed wafer surfaces would bond and how successful the bonding would be.

$$\frac{dU_{Ei}}{dA} = \frac{dU_{Ei}}{da}\cdot\frac{da}{dA} \tag{5}$$

$$\frac{dU_E}{dA} = \frac{1}{6}\frac{E_A E_B h_A^3 h_B^3}{E_A h_A^3 + E_B h_B^3}\cdot(\kappa_A - \kappa_B)^2 \cdot \frac{(1+\nu)}{(1-\nu)}\cdot\frac{1}{\left[(1+\nu)+R^2(1-\nu)\right]^2} \tag{6}$$

Note from Eq. (4) that the strain energy, U_E, scales as the bond front propagates. The effect of wafer bow (curvature) on the extent of bonding may be determined from (6) and by comparing it with (1).

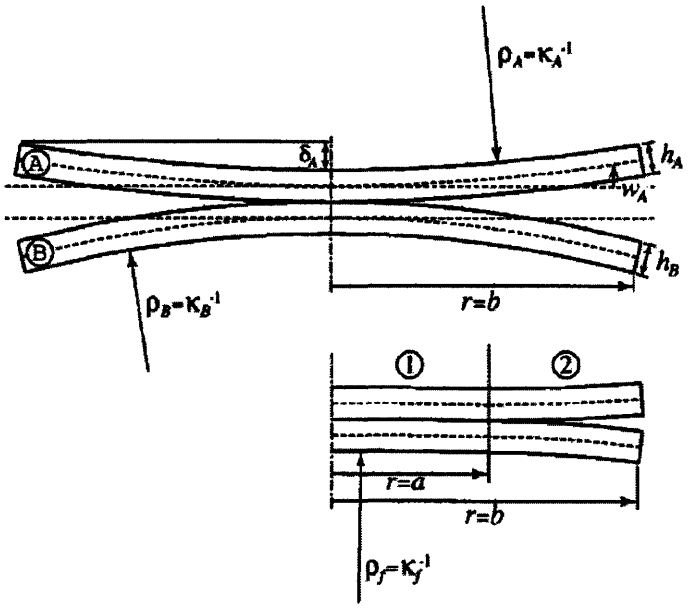
3.1.2 EFFECT OF PATTERNING[34]

In most cases, the Cu films on the wafers to be bonded by TCB are not blanket wafers. Instead, they consist of patterned Cu lines that protrude out from the processed wafers. When bonding patterned lines, since the nominal surface area of contact is now only a fraction of the overall wafer surface area, the energy available to deform the wafers elastically is reduced. As a result, successful bonding becomes more difficult to achieve. Given that the fraction of patterned wafer area in contact during bonding is p_a, then using (5), the modified expression for dU_E/dA is given

by (7), As seen, since the strain energy accumulation rate [dU_E/dA] for patterned features is larger, bonding is more difficult to achieve for a fixed W (determined based on the material of bonding of the two wafers).

$$A' = p_a \cdot (\pi a^2) = p_a \cdot A \Rightarrow \left(\frac{dU_E}{dA}\right)_{patterned} = \frac{1}{p_a} \cdot \left(\frac{dU_E}{dA}\right)_{blanket} \quad ; \; p_a \leq 1 \tag{7}$$

It should however be noted that when the patterned wafers have large areas of region etched out, the stiffness of the wafer to be bonded might be reduced thus making it slightly easier for bonding to be achieved. The reduced stiffness makes it easier for the wafers to deform elastically thereby resulting in better bond quality. Such reductions in stiffness are possible only when the etched pits are very deep which is only the case for MEMS fabrication.



Schematic of bonding two bowed wafers showing assumed geometry and notation used. As shown, κ_A is a positive curvature and κ_B is a negative curvature.

Fig 3.2: Illustration of the bonding of two bowed wafers with different curvatures and the bond front propagation[34].

3.1.3 EFFECT OF MATERIAL & DIMENSIONAL PARAMETERS[34]

From Eq. (6), it may be deduced that the strain energy accumulation rate (dU_E/dA) depends linearly on the elastic modulus, square of the curvature and the cube of the thickness. It is however, insensitive to the Poisson's ratio. The strong dependence of dU_E/dA on the thickness suggests that wafer thickness must be precisely controlled and variations in the thickness on rough wafers could be detrimental to a good bonding. Also, bonding of thicker materials will

require better flatness control. The thickness ratio of the two wafers to be bonded also determines the quality of the bond formed as illustrated by Fig 3.3. Based on Fig 3.3, in order to keep dU_E/dA low, it is always better to have one of the wafers being bonded very thin.

Fig 3.4 shows the change in dU_E/dA as bonding occurs for bowed wafers and the bond front propagates. As seen, for blanket bonding, bonding becomes easier as the bond front propagates while the opposite effect is observed for wafers with large area of non-contactable patterned area.

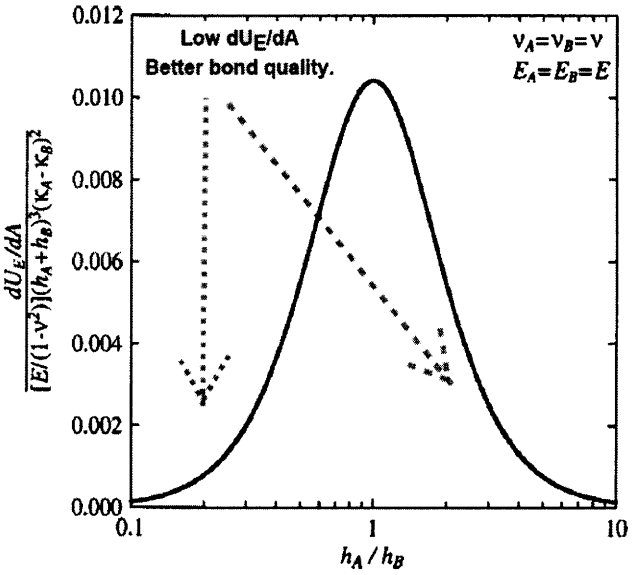


Fig 3.3: Reduction in strain energy accumulation rate for wafers A & B with very different thicknesses[34].

3.1.4 EFFECT OF SURFACE ROUGHNESS & APPLIED LOAD[41]

As mentioned earlier, there are three ranges of surface imperfections wherein the largest of them is the bowing of wafers while the smallest are the nanometer scale surface roughness effects. The surfaces of the wafers to be bonded are never perfectly flat and would always be subjected to surface roughness which can only be partially minimized by CMP. Given the surface roughness, the actual true area of contact between wafer surfaces would be different from the nominal circular area of the wafer. The quality of the bonded wafer is likely to be dependent on the "true" contact area (A_T) and not the nominal contact area (denoted here as A_N)[41].

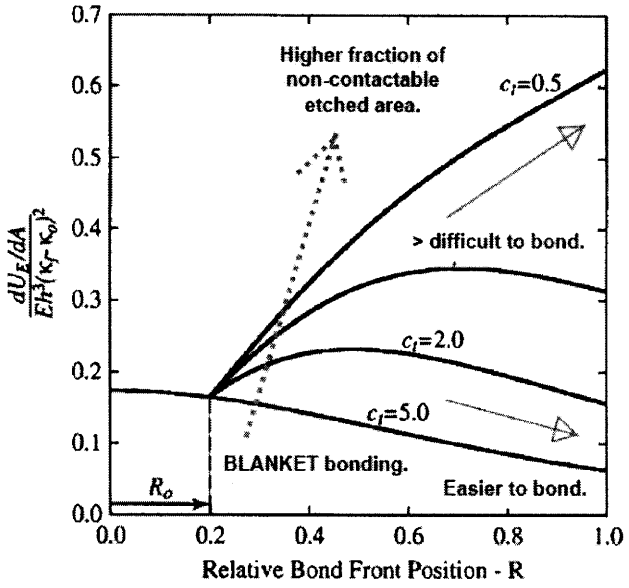


Fig 3.4: Variation of strain energy accumulation rate as the bond front propagates for blanket and patterned wafer bonding[34].

Leong *et al.*[41] have developed a *true contact area* model that helps analyze the effects of surface roughness as well as applied load (L) on the true contact area. The wafer surface is modeled to be consisting of asperities with a certain asperity density (η), mean asperity radius ($\overline{R}$) and standard deviation of the asperity summit heights (σ_s). The *asperity deformation model* has been used accounting for the effects of elastic and plastic deformation components and the work hardening (x) and yielding (Y) effects involved in metal-metal bonding. The analysis revealed that the predominant component of the deformation is plastic and elastic contributions to contact area formation are negligible assuming the wafers are not bowed. The applied load and true contact area are described by expressions (8) and (9) respectively. In these expressions, d refers to the mean interfacial separation of the two wafers to be bonded and φ(z) refers to the standardized normal distribution.

$$L = 3\cdot(2)^{1+x/2}\eta A_N \pi \cdot \overline{R}^{1-x/2}\cdot Y\cdot\left(\frac{0.2}{\varepsilon}\right)^{x}\cdot\sigma_s^{\,1+x/2}\cdot\int_{d/\sigma_s}^{\infty}\left(\frac{z-d}{\sigma_s}\right)^{1+x/2}\varphi(z)\,dz \tag{8}$$

$$A_T = 2\eta A_N \pi\cdot\overline{R}\cdot\sigma_s\cdot\int_{d/\sigma_s}^{\infty}\frac{z-d}{\sigma_s}\cdot\varphi(z)\,dz \tag{9}$$

The equations above apply for the case of blanket wafer bonding. However, in the case of patterned wafers, assuming the asperity density to be uniform across the whole wafer, the

nominal and true contact areas may both be assumed to be scaled down by the fraction of nominal wafer area being bonded (p) as shown in (10).

$$A_T^{'} = A_T \cdot p$$
$$A_N^{'} = A_N \cdot p \tag{10}$$

Fig 3.5 shows the materials used for Cu bonding. The purpose of using Ta is to act as an intermediate adhesion layer between Cu to SiO_2 and to prevent Cu diffusion into SiO_2 and Si. Fig 3.6 shows the wafer bonding map with the range of yield values for different combinations of the values for σ_s and applied load. It was found and verified that the true contact area of bonding is less than 1% of the nominal contact area and that for a given applied load, the impact of surface roughness (σ_s) on the true contact area decreases for increasing surface roughness. Fig 3.7 shows the monotonic relationship between dicing yield and the true contact area, where the dicing yield is taken to be indicative of the bond quality.

From the figures, it is evident that irrespective of the surface roughness, a high applied load would always be sufficient in achieving a large true contact area that could result in ~ 100% dicing yield. The dicing yield appears to suddenly saturate when a threshold true contact area is reached. In the case of patterned wafer bonding, the model presented above overestimates the dicing yield. It is to be noted that all the data in these graphs pertains to HTTC bonding at T = 300^0C. The temperature dependent parameters in the above model are the yield stress (Y) and work hardening index (x) both of which increase with decreasing temperature thereby suggesting that a much higher applied load and improved surface flatness would be very critical for a successful bond for LTTC.

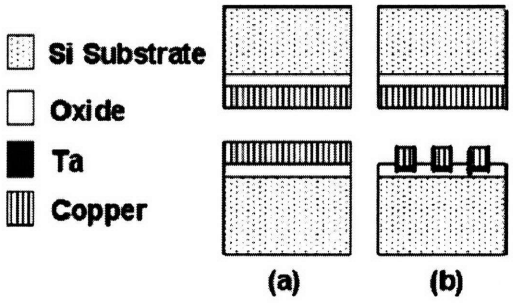


Fig 3.5: Various material interfaces present during Cu TCB bonding[41].

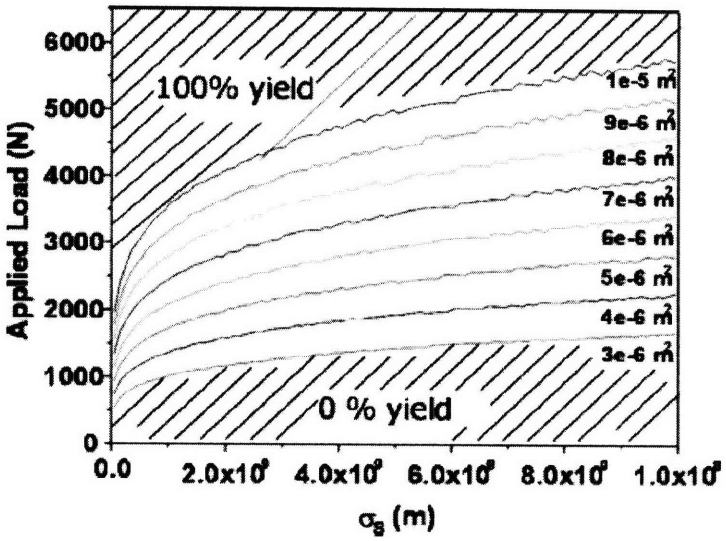


Fig 3.6: Yield map showing the possible yield for different combination of values of applied load & surface roughness[41].

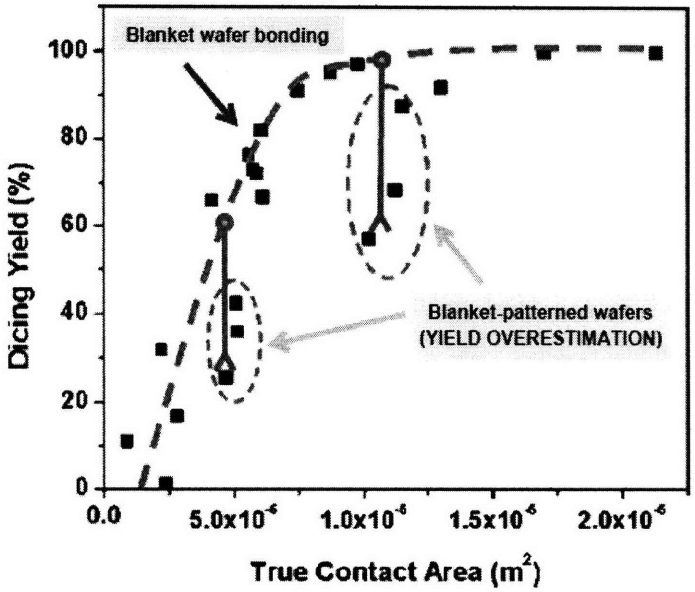


Fig 3.7: Relating the true contact area between bonded metal layers to the dicing yield[41].

The *true contact area* model presented has some limitations which need to be addressed in order to make it more robust. It does not account for the temperature dependent kinetics of grain growth and atomic diffusivity across the bonding interface which could help improve the bonding area of contact. The effect of bond duration is very important as it would need to be large enough for unfavorable kinetic conditions at low temperatures for LTTC in order to achieve a well bonded interface. However, this is not included in the model. The vacuum levels used in the bonding

chamber have a large effect on the number of oxide monolayers formed on the Cu surface. The number of monolayers of Cu_xO formed will determine the bond quality. The decomposition of Cu_xO also depends on the bonding temperature. These vacuum level effects need to be considered in future models. The true contact area model does not explicitly account for the wafer bow effects. Instead it assumes that the applied load is sufficient enough and the wafers are compliant enough to be flattened. Finally, the overestimation of yield is thought to be due to the effects of dishing, which was discussed earlier, which reduces the true contact area drastically. These dishing effects also require further analysis.

3.1.5 EFFECT OF SURFACE QUALITY & TEMPERATURE[33]

It is to be noted that the work of adhesion as given by (1) is not a constant material property. Instead, it is dependent on the temperature since surface energy of a material depends on the temperature. Moreover, the work of adhesion is also affected by the applied load which contributes to an extra energy component corresponding to plastic deformation[33]. Unlike previous approaches, the quality of bonding could also be assessed from a fracture mechanics perspective. The maximum thermodynamic work of adhesion between two identical Cu surfaces is given by (11) where γ_{Cu} and γ_{GB} refer to the surface energy and grain boundary energy of Cu. At room temperature, for bulk Cu, W ~ 3 J/m^2.

$$W = 2\gamma_{Cu} - \gamma_{GB} \tag{11}$$

Fracture tests have been performed to determine the work of adhesion (W) under different conditions. Fig 3.8(a) shows the variation of W with an atomic force microscopy (AFM) cantilever tip induced applied force for work of adhesion measurement at room temperature and UHV (LTTC conditions)[42]. It is seen that when the applied force is close to 0.7 μN, the measured W approaches that of bulk Cu implying that two ultra-clean Cu surfaces under controlled ambient can be as strong as bulk metal, even at room temperature. Fig 3.8(b) shows the variation of W with temperature under UHV (oxide-free clean Cu surface) and oxidized Cu surface conditions[42]. It may be deduced that for clean Cu surfaces, room temperature bonding is sufficient to obtain the desired W target of 3 J/m^2 while for oxidized Cu surfaces, the same W is achievable only at HTTC conditions of T = 300^{0}C. This illustrates the significance of having UHV conditions around 10^{-10} Torr in order to prevent oxidation and surface contamination (typically by hydrocarbons residing in the process chambers).

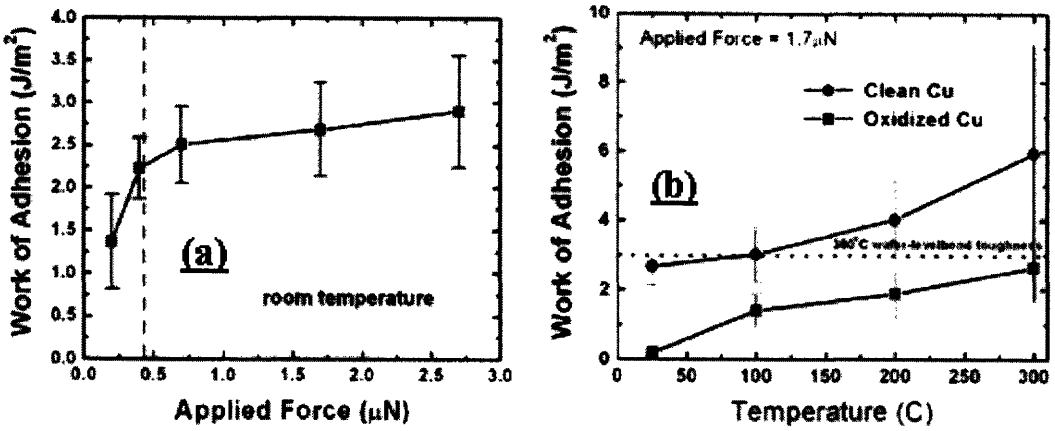


Fig 3.8 (a) – Work of adhesion variation with an AFM tip induced applied force. (b) - Work of adhesion variation with temperature and surface quality[42].

CHAPTER 4

4. RELIABILITY OUTLOOK & FAILURE MECHANISMS

4.1 FAILURE MECHANISMS IN TCB

Past research investigations have revealed that there are various failure mechanisms observed in the bonded wafers. Some of these are *yield-related* failure mechanisms implying that they usually occur prior to product shipment while others are *reliability-related* failure mechanisms. Table 4.1 lists out some of the common failure mechanisms that have been observed.

Table 4.1: Common failure mechanisms observed in TCB wafers.

FAILURE MECHANISMS for TCB WAFERS	SOLUTION
1. **VOID NUCLEATION & GROWTH**[43] – Voids exist at the bonded interface due to local surface / interface contamination and surface roughness. These voids are mobile and may diffuse along grain boundaries. Upon grain growth, since the grain boundary area decreases, the voids diffuse to triple points where their motion is impeded and void growth occurs (Fig 4.1). Another source of voids is the high vacancy concentration in Cu layers. Vacancies absorbed at grain boundaries also accumulated to form voids. These interfacial voids are typically formed to accommodate for the high tensile stresses induced when the bonded material is cooled down to room temperature (thermal stress relaxation) (Fig 4.2). This happens because the thermal stresses in Cu layer (800 – 1200 MPa) cooled to room temperature after bonding (from 300 – 400^{0}C) is more than the yield stress (262 MPa). Presence of tensile stress and annealing condition enhances dislocation climb resulting in emission of vacancies that migrate and coalesce to form voids. *Yield-related failure mechanism.*	• Bonding at low temperature to minimize thermal tensile stress induced in the Cu layer. • CMP process to lower surface roughness. • Anneal Cu layer in inert N_2 ambient before bonding so as to enable grain growth and drive vacancies to free surface for self-annihilation.
2. **CORROSION / OXIDATION**[44] – Exposure of bonding surfaces to oxygen causes a few monolayers of Cu_xO to grow thereby degrading the metallic bond quality. Air in the gap between patterned Cu lines leads to corrosion (depletion of metal and formation of voids). *Yield-related failure mechanism.*	• Use UHV vacuum to keep partial pressure of O_2 as low as possible. • Use RCA / acetic acid clean to etch out any initial native oxide on the Cu surface.

3. **ELECTROMIGRATION (EM)** – Although electromigration and associated joule heating effects could favor diffusion at the bond interface[25] and help improve true contact area and bond quality, considering the TSV as an interconnect line, the anode end of the TSV on one end of the wafer would be subjected to compressive stresses and extrusion failures while the cathode end could experience voiding to accommodate the tensile stresses. EM may not be an issue in TSV with thick dimensions as the current density could be quite low. However, for narrow TSV, EM could pose a problem. *Reliability-related failure mechanism.*	• Use a short TSV if feasible such that the critical length and ***jL*** Blech product is not exceeded. This would require substantial wafer thinning. • Alloying of Cu with Mn to improve EM resistance.
4. **STRESS MIGRATION (SM)** – Considering the TSV as any other via in an interconnect structure, high temperature processing and subsequent cooling could result in stress-induced voiding (SIV) failures due to CTE mismatch induced residual stresses[45]. *Yield-related failure mechanism.*	• Use low temperature processing and bonding.
5. **FRACTURE** – Presence of cracks in the metal feature lines or dielectric layers to be bonded could cause the cracks to propagate and eventually lead to fracture. The use of a large applied load during bonding could cause the low-K inter-metallic dielectrics (IMD) to crack and cause Cu-low-K TDDB failures. *Yield / Reliability related failure mechanism*	• Patterned lines improve fracture resistance as crack nucleation and growth at every new pattern is energetically unfavorable. • Reduce applied load during bonding to avoid low-K dielectric failures.
6. **THIN FILM DELAMINATION** – Presence of voids at the metal bonded interface could accumulate laterally and cause the thin film to delaminate[44]. *Reliability-related failure mechanism*	• Bonding at low temperature to minimize thermal tensile stress induced in the Cu layer so that driving force for void nucleation, growth and coalescence is minimized.

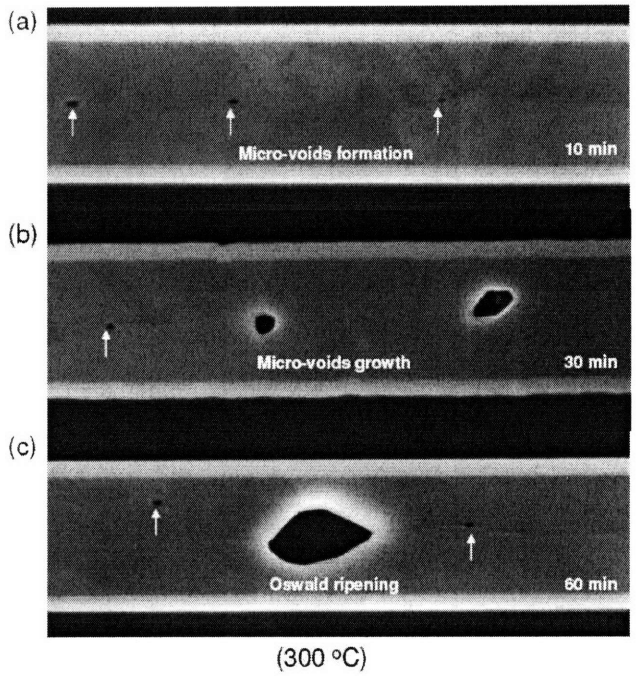


Fig 4.1: Void nucleation and growth in a Cu TCB at a bonding temperature of 300^{0}C. Void growth is caused by grain boundary diffusion, vacancy annihilation and stress gradient induced driving force[43].

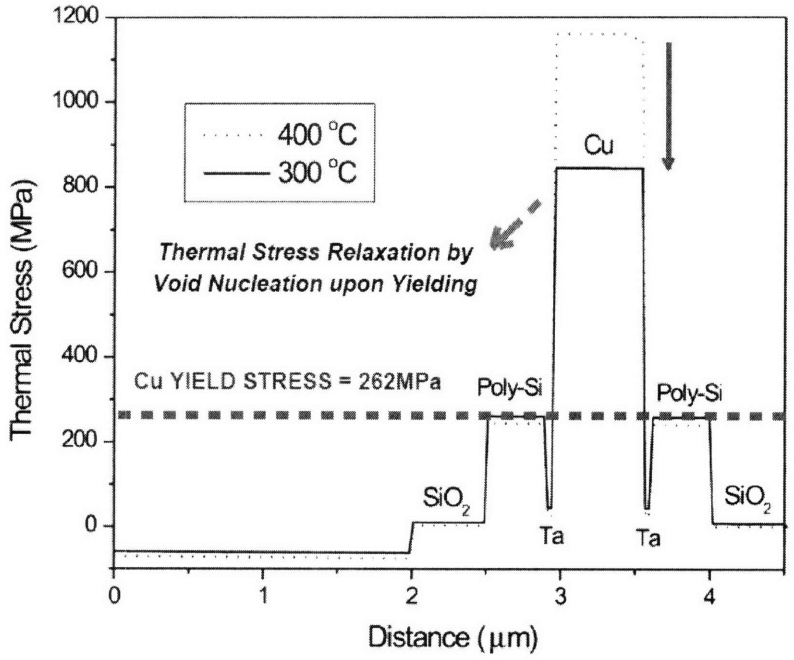


Fig 4.2: Thermal stresses in the thin film stack during Cu TCB for HTTC bonding temperatures of 300^{0}C & 400^{0}C [45].

4.2 PACKAGING & HEAT DISSIPATION FOR 3D IC TCB DEVICES

In the case of 3D integration, since packaging is done only after all the dies are vertically stacked on top of each other, the packaging cost could be lower as compared to conventional chip stacking techniques such as system-in-package (SiP) [chip stack multi-chip module (MCM)] or package-on-package (PoP) which involves stacking of SiP using flip-chip bonding techniques. In these packing technologies, the chips in the package communicate through off-chip signaling. In SiP and PoP each chip is packaged separately and then integrated from the outside (Fig 4.3)[46]. This incurs much more packaging cost as compared to having a single package for the overall 3D IC chip.

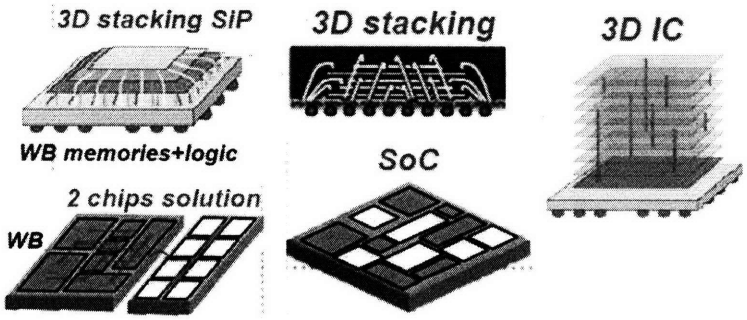


Fig 4.3: Various packaging technologies for a 3DIC[46].

For a 3D IC with multiple stacking levels, heat dissipation is a major concern since heat is released from each of the stacked dies. For the same chip area, a 3D device when compared to a 2D device has a larger interconnect cross-section enabling the interconnect resistance to be lowered thereby enhancing the frequency of operation. Since dynamic power dissipation is proportional to the frequency as indicated in (11), a large amount of heat is dissipated in 3D ICs.

$$P_{dynamic} = CV^2 f \propto \frac{1}{R} \tag{11}$$

The presence of interconnect joule heating can also increase the peak temperature in 3D ICs due to strong thermal coupling with the neighboring interconnects and the active layers giving rise to higher interconnect temperatures that result in lower electromigration resistance. Fig 4.4 illustrates the heat dissipation in 2D and 3D ICs assuming a single source of heat sink through the package at the bottom of the stack. An analytical model of the heat flow for the case of a 3DIC suggests that the temperature rise varies linearly with power density and varies as the square of the number of active layers, n[13].

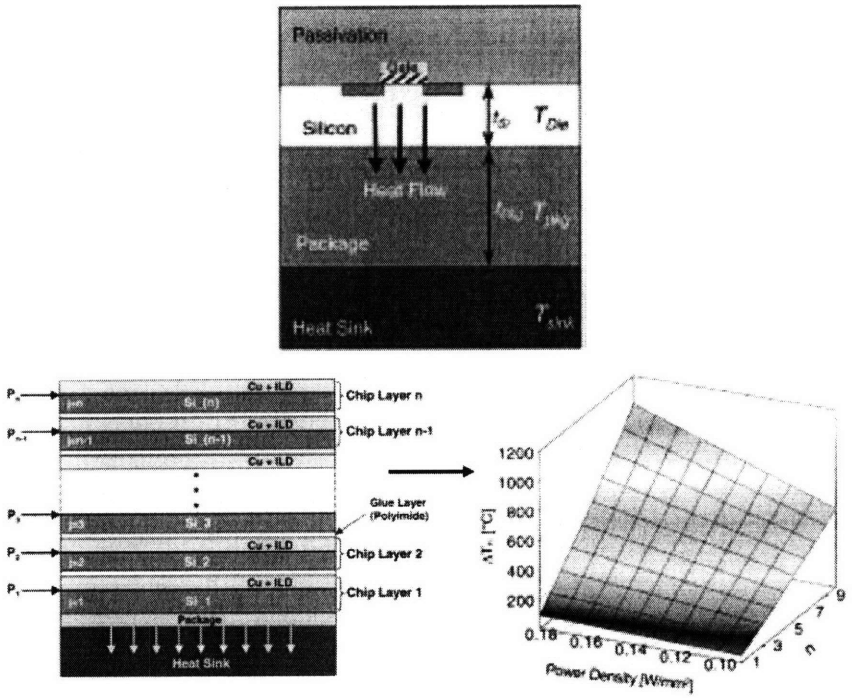


Fig 4.4: Modeling the increased heat dissipation in 3D ICs as compared to conventional 2D ICs[13].

Various strategies may be implemented to enable effective heat sinking from the 3D IC. One of the approaches is to make dummy vias which are insulated from the actual electrical circuitry wherein these thermal vias help in conducting heat away. The other approach is to create integrated microchannels in the B2B bonding layers in between the TSV so that coolants can be pumped through these microchannels to remove heat and reduce the overall thermal resistance of the 3D circuit as shown in Fig 4.5. These approaches however limit the density of TSV interconnection achievable.

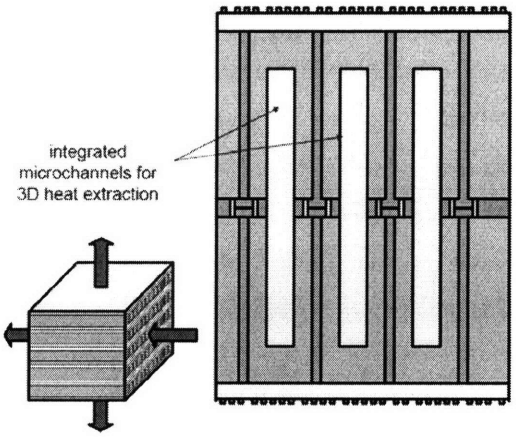


Fig 4.5: Use of integrated microchannels for effective 3D heat extraction[30].

CHAPTER 5

5. MICROSTRUCTURE ANALYSIS OF BONDED INTERFACE

To determine the quality of the bond, two techniques could be adopted. Either the bonded wafers could be subjected to fracture tests and the bond toughness quantitatively determined using fracture mechanics or the microstructure of the bonded interface could be observed using TEM to qualitatively assess the adhesion strength. Fig 5.1 shows the microstructure of two Cu bonded samples[47]. The sample on the right has more defects some of which include twinning defects, voids and dislocations. It is clear by observation that the bond adhesion for the sample on the left is better than the one on the right. The uniform distribution of the defects is indicative of a homogeneously bonded layer.

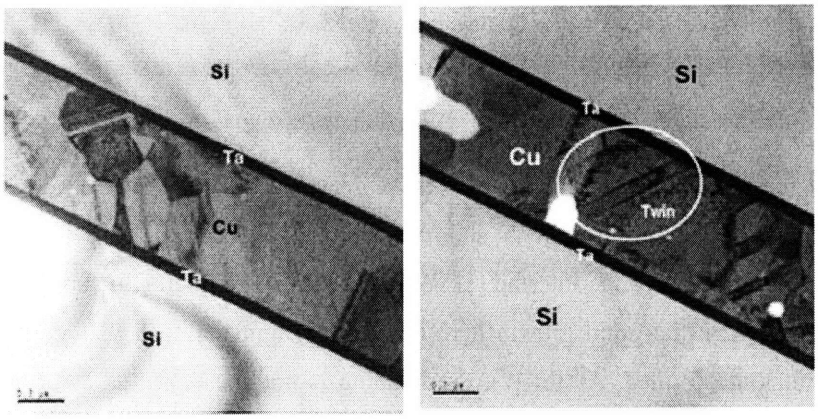


Fig 5.1: Microstructural defects observable at the Cu bonded interface[47].

Strong grain growth occurs during the bonding and annealing phases. Analysis of the microstructure reveals that the grain growth stops after sufficient post-bonding anneal and the copper grain structure evolves to the one shown in Fig 5.1. During the initial bonding process, a (220) *abnormal grain growth* (AGG)[48] is observed. Upon annealing, the preferred grain orientation of the entire film shifts from (111) to (220). The effects of yielding and biaxial strain / surface energy minimization have been cited as possible reasons for the evolution of this preferred grain orientation. The Cu grains are subjected to in-plane stresses due to the presence of biaxial strains when these Cu leads are attached to the thick non-compliant Si substrate. The yielding stress of (220) grains is much lower than (111) and hence yielding occurs in (220) grains first causing them to grow faster and making them the preferred orientation. This AGG phenomenon is undesirable since electromigration (EM) resistance is sensitive to the crystallographic texture and a (220) texture is known to be less resistive to EM than the original

(111) texture when the wafers were unbonded for Cu. Note that not all grains become (220) after annealing. However, the grain size as well as the fraction of grains with (220) texture saturate during the annealing phase only[48].

Fig 5.2(a) shows the microstructure desired for a successful bonding where the interface is no longer observable. The bond adhesion in Fig 5.2(b) is the case where the grain growth and atomic diffusion have been insufficient to get rid of the interface. Since the grain structures at the interface are distinctive and have not interacted, the bond toughness in this case is very low.

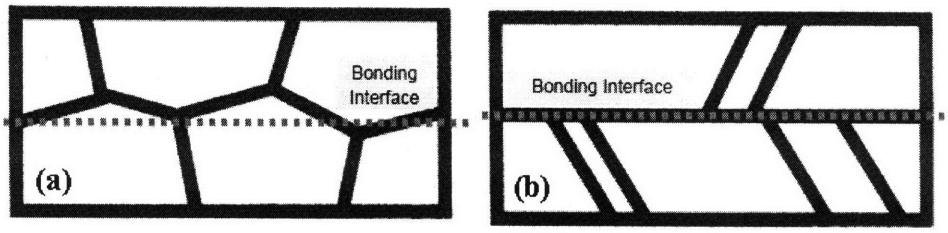


Fig 5.2: Microstructure of a (a) well-bonded interface and a (b) poorly bonded interface[47].

Fig 5.3 depicts the three kinds of microstructures observable after bonding a Cu-Cu bonded interface. In (a), sufficient grain growth and diffusion have occurred such that a uniform microstructure is formed where the interface is no longer seen. The microstructure in (b) is very similar to (a) except that the grain growth here is more phenomenal such that single through-thickness Cu grains are formed. As for (c), the bonding is not successful as evidenced by the observable interface and the larger number of void defects.

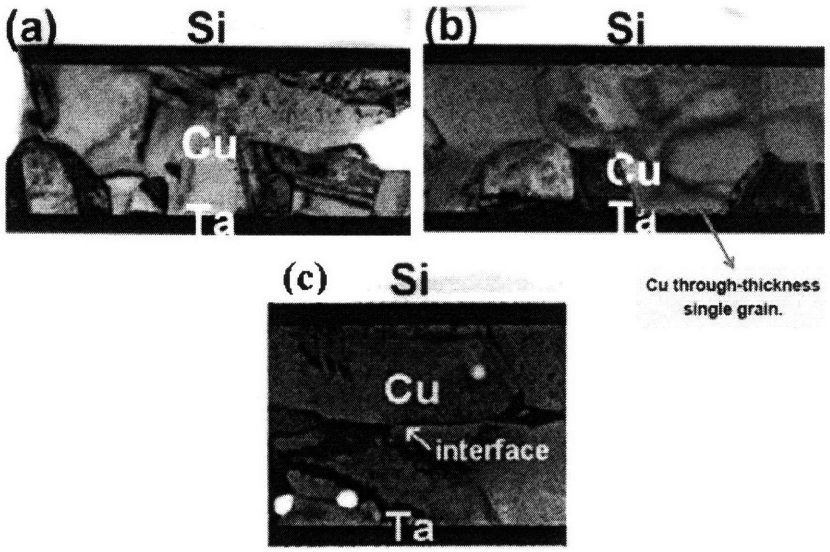


Fig 5.3: Various possible microstructures in a bonded Cu interface[49].

Fig 5.4 shows a morphology and strength map for Cu TCB at different bonding temperatures and annealing durations for a given vacuum level and applied load[49]. As mentioned earlier, annealing is required to ensure that the bonding interface is removed through grain growth and diffusion across it. Bonding at lower temperatures is therefore increasingly difficult although it is achievable under UHV conditions.

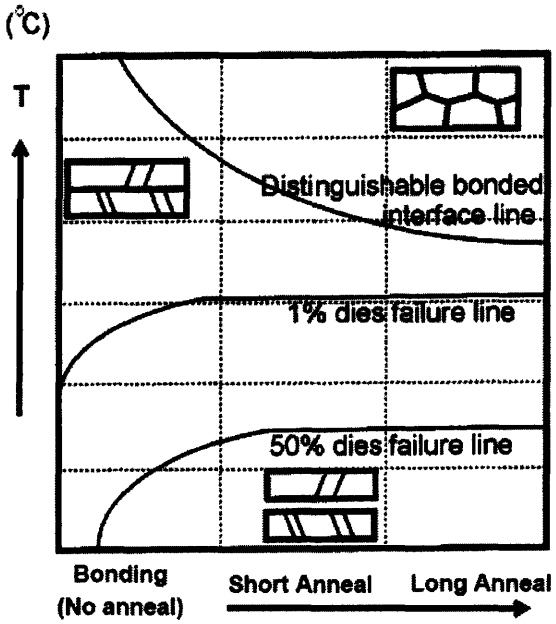


Fig 5.4: Morphology and strength map for copper wafer bonding under different bonding temperatures and conditions[49].

CHAPTER 6

6. YIELD & RELIABILITY MODELING APPROACH FOR 3DIC

6.1 IMPORTANCE OF YIELD & RELIABILITY MODELING

Any new technology being developed in its research phase may seem very attractive in a lab setup. However, when commercialization of the incumbent technology is considered, there are various factors to be looked into that may limit its feasibility. Some of these include reproducibility of the process, cost implications, throughput, manufacturing yield, process flow modifications and operational reliability. All these factors need to be favorable in order to successfully commercialize a technology. Yield, reliability, throughput and other factors all have an indirect implication on the cost. The semiconductor industry has always been pushing forward to improve yield as much as possible as it has a major cost implication and it is also used as a yardstick to gauge the manufacturing competency of a company. Yield is all the more an important consideration for 3D integration since this is one of the last stages in the process line and low yield at this stage would have heavy cost implications since the scrapped wafers have been through the complete process line. For a new technology, there is insufficient information on the possible yield and it is therefore very necessary to develop a yield modeling approach to characterize the expected yield of the process.

The aim of this chapter is to develop a yield model (included in the Appendix) from a statistical perspective and make use of the physical model of wafer bonding presented earlier so that the yield of the LTTC process could be predicted for different process parameter conditions. Recent studies in statistical literature suggest that the early life reliability of a device could also be predicted based on the yield information thereby nullifying the earlier requirement to perform accelerated life tests on a certain sample of data and subsequent extrapolation which could be time-consuming, expensive and inaccurate too. Predicting the early life reliability for a new technology is also important since it provides information on the expected field returns and the associated warranty cost implications. The warranty period to be set for a new technology based device is determined based on these early life reliability predictions.

6.2 FACTORS AFFECTING LTTC YIELD

Before looking into the statistical yield model to be developed for 3D ICs, it is worth analyzing the various factors that impact the yield of a wafer stacking process. Table 6.1 below lists out these factors[50].

Table 6.1: Factors affecting the yield of 3DIC[50].

FACTORS AFFECTING YIELD OF 3DIC
1. **DIE AREA** – Yield is a function the die area. The larger the die area, the higher the probability of finding a killer defect which could cause chip failure[51]. 3D IC technology helps reduce the die area on each wafer level stack and therefore improves yield of each individual stacked die. However, it is to be noted that on each die, extra space is to be reserved for fabricating TSV and this additional space accommodation is expected to cause yield to be affected.
2. **VIA SIZE & DENSITY** – Wafer 3D stacking requires TSV interconnects to bond B2B wafers. The circuit functionality determines the density of TSV and their size. The larger the density and smaller the dimensions of the TSV, the more difficult it is to achieve precise alignment. More stringent alignment requirements result in lower yield as temperature affects alignment accuracy owing to wafer bowing effects induced by the thermal residual stresses during alignment and bonding. The number of vias to be implemented is dependent on the circuit design although the stacking method defines an upper limit to their density.
3. **CIRCUIT DENSITY** – Use of 3D IC has helped reduce the circuit density and the need for aggressive scaling. The denser the circuitry, the smaller the feature size, the greater the chance for a defect to be a "killer" defect.
4. **NO. OF MASKING STEPS** – 3D technology helps reduced the number of mask levels needed for each die / wafer in the stack. Use of every additional mask increases the chances of error, contamination and breakage.
5. **PROCESS MATURITY** – The more mature a process is, the higher its yield is likely to be. Wafer level stacking is a well-researched and established process in the MEMS community which is now being adopted for 3D IC. Therefore, the yield of the stacking process is likely to be quite high.
6. **EXTRA PROCESSING STEPS** – There are additional lithography, etching, DRIE, Cu electrodeposition and other steps needed for realizing TSV as highlighted in Table 2.6. These additional steps could be detrimental to the yield.
7. **CONTAMINATION** – Foreign particles caught between the wafers during bonding cause voids, peeling and delamination thereby affecting bond integrity and resulting in a lower yield. As mentioned earlier, these contaminants could be avoided by using UHV in the bonding chamber and outgassing the chamber prior to any bonding so that any hydrocarbon residual particles in the chamber walls are removed. The source of these hydrocarbon particles is the oil vacuum pumps used for creating UHV.
8. **EDGE EFFECTS** – Wafers are typically bowed such that the inter-wafer gap is larger at the edges than at the center causing the bond strength around the edges of the wafer to be weaker, making them vulnerable to chipping, peeling and delamination. As a result, stacked dies cut out from wafer edges are likely to be of lower yield. Therefore, there is a certain spatial failure distribution for 3D bonded ICs on a wafer. However, take note that there are nanoscale spatial variations in surface roughness that also locally impact the yield in a region of the wafer.

9. **CHIP DESIGN** – Flexible and good circuit design maximizes process separation and optimization, adds robustness and employs redundancy / repair schemes for the circuit thus helping in yield enhancement.

10. **TRUE CONTACT AREA**[25] – The higher the true contact area, the higher the expected yield of the stacked wafers. True contact area depends on the surface roughness, applied load and many other factors discussed above. The lower the surface roughness and higher the applied load, the better the yield as revealed by Fig 3.6 and Fig 3.7.

6.3 STATISTICAL YIELD MODEL

The complete details of the yield model developed have been included in the Appendix. Please refer to Appendix for the procedure and details of the model developed. It is to be noted that this model has not been verified and is intended just to give the reader an overview of the approach to adopt while modeling yield for a new device technology.

CHAPTER 7

7. COMMERCIALIZATION POTENTIAL - LTTC TECHNOLOGY

The analysis in the previous chapters focused on the technical, physical and manufacturing aspects of Cu TCB bonding where the various bonding techniques, their process and material issues, physical mechanisms modeling the bond quality and a statistical outlook for bonding yield estimation were discussed. A technology can be considered successful if and only if it crosses the research phase and gets commercialized and implemented in the industrial process line. Many new technologies investigated tend to show positive results in a lab setup but fail to be repeatable or end up being too expensive or difficult to control and optimize. Such technologies do not have any impact on the industry or society and simply remain a research topic of interest without practical use. There are various factors to be considered when analyzing a new technology and substituting it for an earlier one. These factors shall be examined for our LTTC technology in this chapter. We shall compare the LTTC bonding approach with other conventional approaches currently adopted in the industry.

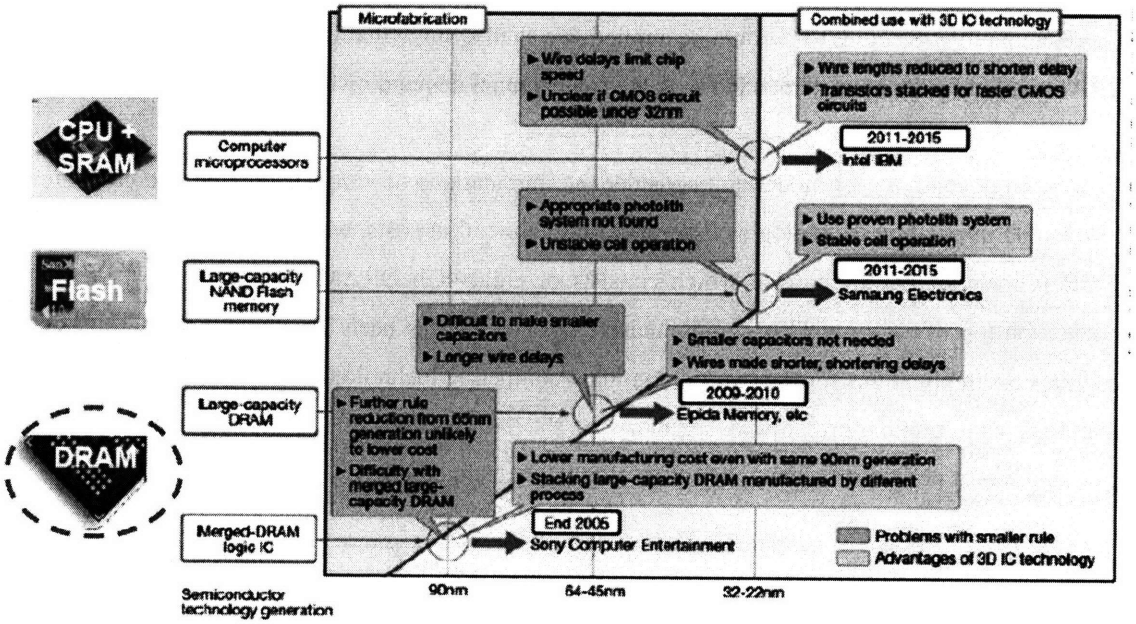


Fig 7.1: Popular applications for 3D ICs based on the technology generation[46].

7.1 DEVICE APPLICATIONS OF 3DIC

Various devices have been or will be fabricated and implemented using the 3DIC concept. Some of these include a variety of stand-alone memories (DRAM, cache memories), CMOS image sensors (for digital signal processing applications), FPGAs, mixed signal ASICs,

processor/memory stacks, NAND flash, RF and optical MEMS devices etc... Some of these applications are listed in the 3D technology timeline given in Fig 7.1[46].

7.2 APPLICATION OF FOCUS FOR LTTC TECHNOLOGY

Although various device applications exist for 3DIC, the most impactful one in terms of immediate need and economic potential needs to be chosen for implementing the LTTC approach in it. From Fig 7.1, a near-term focus indicates that a high capacity DRAM device is the current application that is hyped about and has a promising potential for 3D implementation. Fig 7.2 clearly indicates that Cu bonding and TSV based 3DIC will find large scale mass production for DRAM compared to all other applications for the next few years[46]. Given these market trends, 3D-DRAM has been chosen as the application of focus for the LTTC bonding approach that we are investigating.

As indicated by Fig 7.3, although DRAM devices are available in various storage capacities, the one Gigabit (1 Gb) DRAM is the current generation of DRAM devices with a worldwide market demand amounting to about 1.5 billion in 2008[52]. As our intention is to look into the near term future technology where LTTC could be applied, we shall assume that in a few years time, a 4 Gb DRAM would be the most demanded with the same annual demand of 1.5 billion.

In order to develop a cost model and consider the implications of vertical stacking and compare various 3D integration technologies in terms of the fabrication costs, we consider fabrication of a 4 GB (Gigabyte) DRAM device which consists of eight 4Gb DRAM chips [1 byte ≡ 8 bits] stacked on top of each other. A comprehensive cost model has been developed considering the various cost implications for the two predominant competing technologies viz. HTTC and LTTC. The following section provides a summary of the fabrication cost components and the net production cost per 4 GB device for the two alternative technologies.

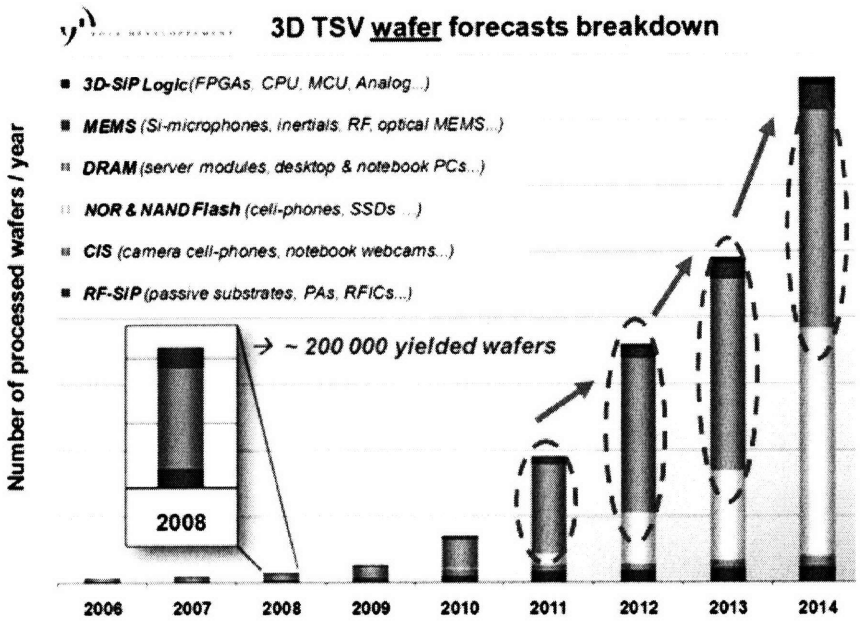


Fig 7.2: Exponential growth potential for3D DRAM technology in the near future provides attractive opportunities for commercializing the LTTC technology[46].

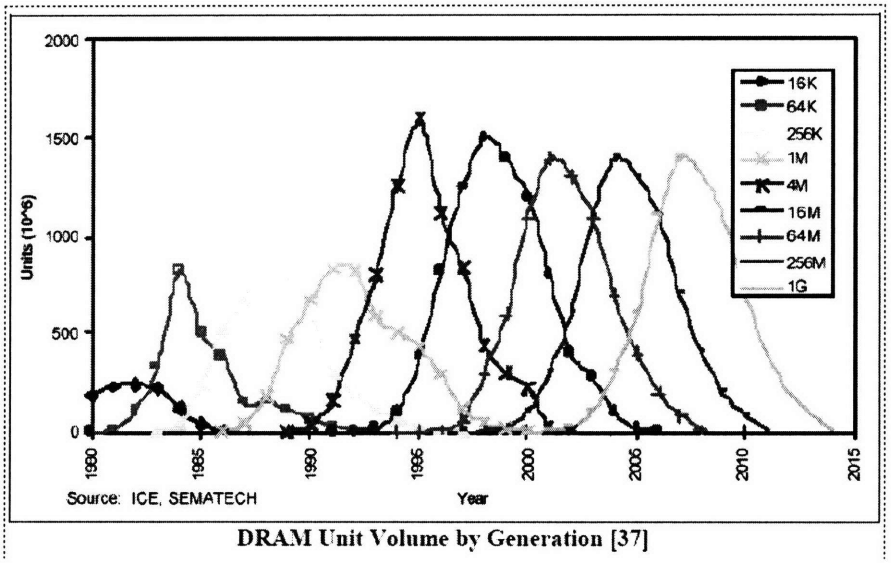


Fig 7.3: Trend of market for different DRAM with different storage capacities[52].

7.3 COST ANALYSIS

7.3.1 COMPONENTS OF COST MODEL

There are various costs involved in the fabrication of a device. Some of these are *fixed costs* such as real estate, clean room foundry establishment, equipments and technology design. Others such as power consumption, material cost, processing cost, packaging, testing (burn-in), labor etc…

are *variable costs*. All these cost components need to be considered in determining the effective cost incurred in fabricating the device.

Table 7.1 summarizes the costs involved in making a 4GB DRAM device for the three bonding technologies for the case of a well established company which is expected to have a high market share of around 20%. It also provides some other general information with their industry standard values.

Table 7.1: Various cost factors and process information considered in development of the cost model[*,+].

INFORMATION	VALUE
Estimated Market Share[*]	20%
Initial cost of unprocessed wafer[53]	$50/wafer
Processed cost of an 8" wafer (after standard CMOS process) [*]	$3000/wafer
Global market size for DRAM devices[52]	1.5 billion
Process defect density[*]	0.1/cm^2
Size of a 4 Gb DRAM chip (70 nm technology) [*]	0.80 cm^2
Wafer yield[53]	99.5%
Die yield on good wafer[53]	91.9%
Cost of fab setup (equipments + maintenance + real estate)[53]	$1 billion
Creation of mask set[53]	$1 million
Cost of chip design[53]	$0.4 billion
Standard CMOS process cost per 4 Gb chip[+]	$10 /chip
Testing cost per chip[*]	$0.0025/chip
# of chips stacked[*]	8
Expected market price of 4GB DRAM (in 2011) [*]	$125.00

Cost Component	Wire Bond	HTTC	LTTC
Packaging (3D technology) cost[+]	$0.44/chip	$0.25/module	$0.38/module
Assumed Bonding Yield [*]	*95%*	*95%*	*98%*
Threshold Yield Required for Breakeven[+]	*97.9%*	*94.6%*	*95.4%*
Overall Yield[+]	*86.9%*	*86.9%*	*89.6%*
Throughput (wafer/hr) (WPH)	*3.2*	*10*	*2*[*]
Total processing cost of 4GB DRAM[+]	$144.45	$120.77	$97.29
Expected market price for 4GB DRAM (2011) [*]	$125	$125	$125
Time to Breakeven (years) [+]	∞ (LOSS)	2.35	0.15

Note: [+] (Computed result); [*] (Estimation).

7.3.2 ANALYSIS & JUSTIFICATION OF COST MODEL

Based on the information provided above, it is apparent that for the future 4GB DRAM that is stacked using eight 4 Gb DRAM chips, the manufacturing cost is found to be the lowest for LTTC. This is predominantly because we have assumed the yield for the LTTC technology to be as high as 98% when compared to HTTC for which we consider the yield to be relatively lower at 95%.

The high yield for LTTC in comparison to HTTC and wire bonding may be justified as follows. Since LTTC is performed at close to room temperature, the residual stresses induced by this process is very minimal and hence global and local wafer bowing and warping effects on the bonding wafers is very limited. As a result, the alignment for LTTC is expected to be very good. The low residual stress also implies that thin film delamination and stress-induced voiding (SIV) failures are less likely to occur in LTTC. Moreover, since pure electrodeposited Cu can recrystallize at room temperature[37] and has a high intrinsic grain boundary mobility[54], good Cu bonded interfaces may be achieved at low temperatures itself and high temperature bonding to enhance kinetic feasibility at the expense of induced residual stresses may not really be necessary. As long as the applied load is sufficiently high, a good yield bond can be achieved[25]. Based on these arguments, we may conclude that LTTC process is expected to have a much higher yield as compared to HTTC.

As for wire bonding, although this established process has had a high yield of close to 99.2%[55], when the density of interconnection is high in the case of 3D DRAM devices, the wiring could get shorted and lead to degradation in the yield. Hence, we have assumed that wire bonding yield drops to 95% in the case of high interconnection density. Cost of wire-bonded packaging is found to be much higher than LTTC and HTTC based packaging.

As for throughput considerations, although LTTC has a much lower throughput than HTTC, since the cost of wafer bonders and UHV equipments that are additionally required for LTTC process are insignificant as compared to other standard equipments such as DRIE, CMP, lithography etc..., LTTC still ends up to be much cheaper than HTTC owing to its higher expected yield which offsets the additional equipment acquirement expenditures. Since wire bonding involves chip stacking instead of wafer stacking and also since every wire bond needs to be serially processed, the wire bond process has a very low throughput as indicated by Table 7.1. Therefore, wire bonding is not cost-effective and may not be a viable option for future 3D DRAM devices.

The cost analysis and its justification presented above reveals that an established company such as Samsung® with more than 20% market share[56] for DRAM memory devices would be able to breakeven earliest if the LTTC technology were to be adopted as opposed to either the wire bonding or HTTC technologies. Therefore, there is a clear motivation from an economic perspective for a large scale manufacturing plant to adopt the LTTC approach to TCB bonding and Cu 3D integration so that the production cost per chip is low.

7.3.3 SENSITIVITY ANALYSIS, THRESHOLD YIELD & THROUGHPUT

Fig 7.4 shows the sensitivity of the fabrication cost of a 4GB DRAM device for different throughput and bonding yield values for the LTTC technology. As revealed by this figure, the fabrication cost is largely insensitive to the throughput until a threshold throughput of 1 wafer/hour below which the number of UHV bonders required is large enough to affect the overall effective fabrication cost of the DRAM device significantly. Also, it may be seen that the fabrication cost is highly sensitive to the bonding yield. This high sensitivity is justified by Eq. (12) below where the overall yield (Y_{3DIC}) of a 3D stacked device is proportional to the bonding yield ($Y_{Cu\ BOND}$) raised to the power of (N-1) where N is the number of die stacking levels (N = 8 in our case). This large power of N causes the bond yield to affect the overall 3D device yield significantly which in turn reflects in the high fabrication cost sensitivity for small variations in yield.

For an assumed market price of close to $120, in order to achieve breakeven, we require a threshold yield for LTTC of 95.4%. In the case of HTTC, the threshold yield is found to be much lower at 94.6%. Therefore, in the event that the LTTC threshold of 95.4% is not met, then the current HTTC technology would continue to have its commercial viability. However, based on our analysis of the various failure mechanisms that may be avoided by the use of low temperature bonding, we may confidently presume that the LTTC threshold yield would be easily achievable.

$$Y_{3DIC} = \left(Y_{wafer} \cdot Y_{die}\right)^{N} \cdot \left(Y_{Cu\,bond}\right)^{N-1} \tag{12}$$

Although the threshold yield values for LTTC and HTTC look close, it should be noted that based on Eq. (12) where the bond yield is raised to the power exponent of (N-1), a difference of 1% in threshold yield could have a very large impact on the overall yield due to this exponent. Hence, the difference in threshold yield of 94.6% (HTTC) and 95.4% (LTTC) is to be considered significantly different.

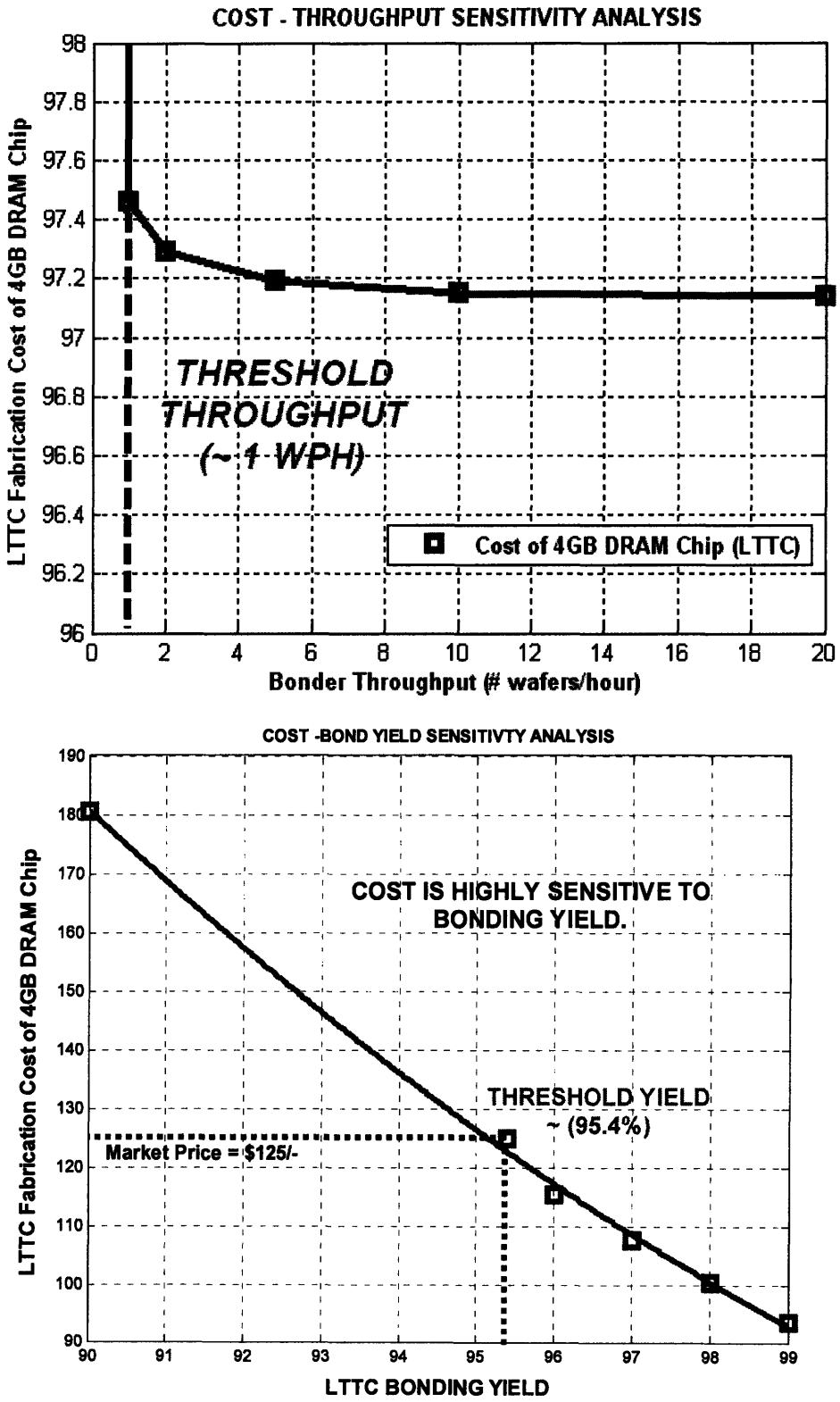


Fig 7.4: Sensitivity of fabrication cost for different throughput and bonding yield values.

7.3.4 MANUFACTURING COST ANALYSIS FOR A START-UP

Table 7.2: Cost implications of setting up a new foundry for LTTC TCB for a new start-up with low market share.

Cost Components for a Start-Up	Value
Market price for 4GB DRAM	$125/module
Estimated market share	0.1%
Estimated start-up yield	96%
Initial cost of unbonded processed DRAM chips	$90/module
Cost of bonding per 4GB DRAM stack	$32.19/module
Total processing cost of 4 GB DRAM	$122.19/module
Annual Profits	$6.33 million
Time to Breakeven (years)	3.25

If a new start-up company were to implement the LTTC technology, then the cost considerations and the decisions to be taken could differ. As a new start-up company which is assumed to buy planar processed DRAM wafers from large scale manufacturers and perform only bonding and 3D integration, an optimistic market share could only be around 0.1%. As shown in Table 7.2, the time to breakeven for a new start-up company specializing in LTTC bonding alone could be around 3 - 4 years for an estimated market price of $125/module with an annual profit of $6.33 million for a starting yield of 96%. Although this looks attractive, it is to be noted that in a start-up company, it is hard to achieve yields above 90% for the initial few periods of operation as compared to established firms which can ramp up the yield to high levels within a short span of time. Therefore, the estimate of profit made here could be quite optimistic. Given the uncertainty in achieving the desired yield, investment in a manufacturing start-up would be a high risk – high return idea.

An alternative avenue to explore would be to file a patent for the LTTC technology and license it out to the established DRAM manufacturers for a royalty or licensing fee. Filing a patent is a critical process that requires careful analysis and examination of the intellectual property (IP) landscape to ensure that there are no previous patents filed by others on a technology that is very similar to ours so that risks of patent infringement are avoided (in order to avoid legal litigation issues which are expensive and time-consuming). Let us now explore the IP landscape in brief.

7.4 IP LANDSCAPE

Table 7.3 presents the details of some of the closest patents to LTTC that have been filed and approved in the past[57-62]. A detailed insight into the claims in these patents reveals that none of them talk about Cu bonding at room temperature specifically. The patents on Cu bonding involve high temperatures of 200 – 400^{0}C (HTTC) while the patents on low temperature bonding are for Si and SiO_2 based direct bonding. Also, these patents have not specifically looked at application of Cu 3D technology for DRAM stacking.

Since the principles of the LTTC technology proposed is very much different from those that have been patented so far, there is minimal risk of any patent infringement and therefore, a patent may be filed for the LTTC enabled Cu 3D device integration. This enables acquirement of some portion of the IP landscape in this field that could be utilized for economic gains by licensing and royalties as mentioned earlier.

We may suggest that MIT can file a patent on this LTTC technology in the United States as well as in other countries such as Korea and Germany where the major DRAM manufacturers (Samsung®, Hynix®, Qimonda® etc...) have setup their fabrication plants. The patent, once applied, goes through a comprehensive review and typically takes about 3 years to get approved.

Given the extremely low risk of any patent infringement, a good opportunity would be to license out the patent to the semiconductor giants all around the world and make money through licensing fees and royalties. This would be an interesting strategy to pursue provided the companies can be convinced about the novelty, attractiveness and benefits of adopting and shifting over to our new LTTC 3D bonding technology. This should be possible as our analysis shows that the LTTC technology is a boon from both the technological as well as the economic perspective.

Table 7.3: List of the patents that are similar to LTTC technology and yet quite distinct and different in their scope. The scope of these patents is highlighted in the last column.

PATENT No.	PATENT TITLE	PATENT ISSUE DATE	SCOPE OF CLAIMS
0099796 A1[57]	Method of forming a multi-layer semiconductor structure having a seam-less bonding interface. (R.Reif *et al.*, MIT)	May 11, 2006	• Temperature ~ (250 – 400^{0}C). • Bonding material = Cu.
6, 853, 067 B1[58]	Microelectromechanical System using Thermocompression Bonding. (M.B.Cohn & J.T.Kung) (Microassembly Tech. Inc., CA)	Feb 8, 2005	• Temperature = 400^{0}C. • Hermetic sealed cavity by ring-shaped bonding interface at the border. • Bonding material = Cu, Pt, Pd, Ir.
4, 444, 352[59]	Method of Thermocompression Diffusion Bonding Together Metal Surfaces (H.H.Glascock *et al.*, GE, NY)	Apr 24, 1984	• Temperature = (280 – 320)^{0}C. • Load = 1500 – 5000 psi. • Bonding material = Cu, Au, Ag. • Patterned Cu line bonding.
7, 335, 572 B2[60]	Method for low temperature bonding and bonded structure. (Tong, Q.Y. et al.) (Ziptronix Inc., NC, US)	Feb 26, 2008	• Room temperature to 100^{0}C. • Chemical bonding of materials such as Si, SiO_2, Si_3N_4. • Ammonia based cleaning. • Bond strength – (500 – 2000) mJ/m^2. • Grinding and polishing prior to bonding.
5, 503, 704[61]	Nitrogen based low temperature direct bonding. (Bower R.W. et al.) (University of California)	Apr 2, 1996	• Low bonding temperature, annealing at 500^{0}C. • Make wafer bonding surface hydrophilic and reactive by use of NH_3 plasma and / or HF. • Material – Nitride deposited Si, Ti, SiO_2, GaAs, InP. • Application – III-V on Si optoelectronic integrated circuits (OEIC).
0287264 A1[62]	Method and Equipment for Wafer Bonding (Rogers, T.)	Dec 13, 2007	• Single chamber for cleaning, in-situ surface activation, alignment and bonding.

Based on the analysis of the key global industry players in 3DIC, the following licensing plan (*patent portfolio*) may be adopted as shown in Table 7.4. Based on the collective market share of the above listed companies in the 3D DRAM market, royalties can be obtained from up to 50% of the global sales in 3D DRAM. The overall 3D DRAM market sales amounts to an average of $10 billion and a 0.1% royalty fee on annual sales would easily generate an income from licensing of about $5 million / year which is a significant income given the low initial investment of about $20,000 for filing and getting each patent approved. This is a low risk-good return strategy as high risk initial investments such as foundry setup etc... are avoided and breakeven time is very short.

Table 7.4: Patent portfolio showing the filing and subsequent licensing (royalty) plans in different countries.

COUNTRY of PATENT FILING	COMPANY TO LICENSE TO	LICENSING FEE / ROYALITIES
United States	Micron®	0.1% of 3D-DRAM sales
Germany	Qimonda®	0.1% of 3D-DRAM sales
Korea	Samsung®, Hynix®	0.1% of 3D-DRAM sales

7.5 SUPPLY CHAIN PERSPECTIVE

As discussed earlier, the LTTC bonding process does not disturb the existing process lines of any technology. It comes into the process line and supply chain only after each technology's processing is completely done (FEOL processes + BEOL processes) as illustrated in Fig 7.5. As an example, the processed wafers from *LOGIC*, *MEMORY*, *PHOTONICS* and *MEMS* technologies are each taken and stacked up vertically in the 3D integration stage of the supply chain. This vertical integration is then followed by dice sawing using a diamond cutter in order to break the stacked wafer down into its stacked blocks of chips followed by packaging, shipping and final distribution to customers. We place ourselves in this supply chain at the 3D integration stage where the license for our LTTC patent will be sold for royalty fees.

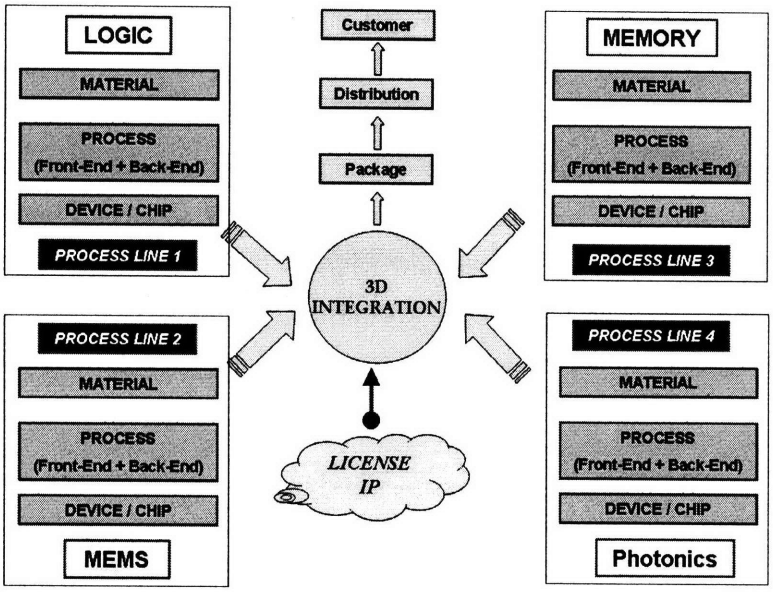


Fig 7.5: Supply chain model for 3D IC integration. Licensing of IP is performed at the 3D integration stage.

7.6 HYPE FACTOR

As far as 3D IC is concerned, there is a lot of hype about it in the recent past given the significant advantages that it offers in terms of better device performance, speed, lower packaging cost etc... Fig 7.5[63] shows a Gantt chart which illustrates the stages of the 3D technology in various companies. Companies such as Tezzaron® and IBM® were the first to venture into 3DIC commercial production in 2006 – 2007. This was followed by popular DRAM makers, Samsung® and Hynix® which have entered 3D technology while other giants such as Intel, Micron and Toshiba are still currently in the research phase.

The real scenario in the industry today for 3DIC is even more positive and encouraging than what is reflected in Fig 7.6 as some of the companies which are shown to be in the research phase are in actual fact already producing commercial products using 3D technology[64]. This includes Ziptronix Inc. which has filed many patents in 3DIC and is making chip-to-wafer (C2W) based system-on-chip (SoC) devices. Amkor has already begun commercial production of 3D chip packaged devices[64] and Zycube is using wafer-to-wafer stacking approach to make 3D devices with injection glue bonding, buried W or polysilicon vias and "micro-bump" connectors[64].

The increasing interest in 3D-IC amongst most players in the semiconductor industry is clearly evident. This is indicative of the hike in hype that currently exists for this technology and its

possible implications on the attractive licensing fees and royalties that could be expected as a result.

7.7 FUNDING PERSPECTIVE

Our initial fundamental research activities were funded by the Singapore-MIT Alliance (SMA) since the year 2003. Having come to a phase close to commercialization, it is necessary to look out for other funding agencies which include venture capitalist funding, MIT Technology Licensing Office (LTO), SEMATECH (United States) and the MOE (Ministry of Education), A*STAR (Singapore).

With continued funding, we hope to be able to work further towards improving the throughput of the LTTC process by suitably tuning the process parameters or redesigning the bonding system accordingly. Throughput is one of the major and only stumbling blocks that we need to overcome for a more successful and expedited commercialization of the LTTC technology. Further efforts need to be channeled towards improving throughput for the LTTC technology.

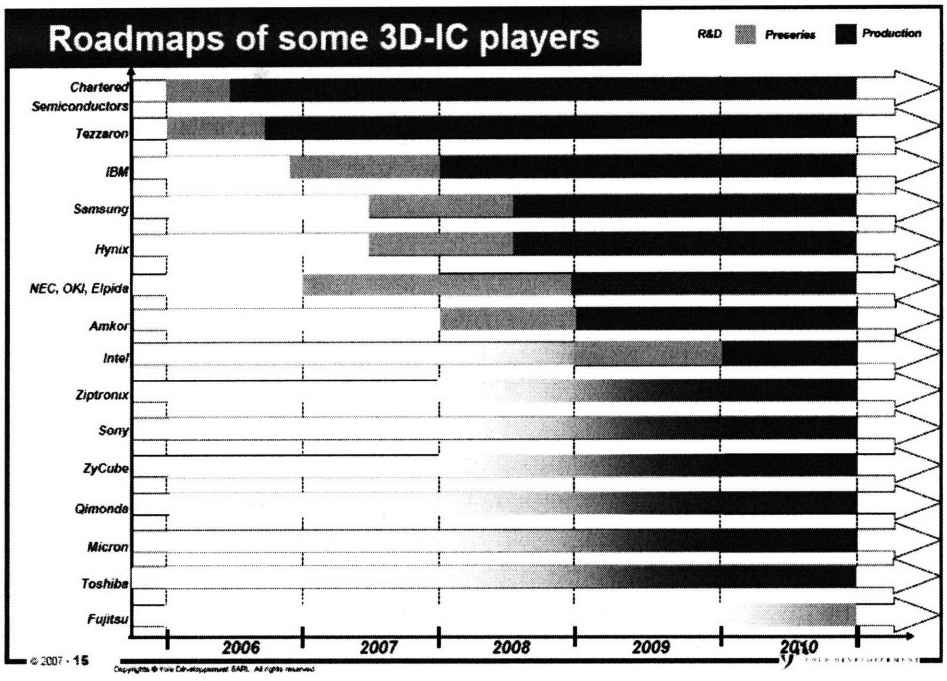


Fig 7.6: Technology timeline for the 3DIC technology in some of the major semiconductor companies around the world[63].

7.8 WOOING LICENSEES (CUSTOMERS)

To be able to achieve significant financial gain, it becomes necessary to attract semiconductor companies towards the LTTC technology and get them to be our licensees so as to benefit from the royalty fee. It is necessary to go through suitable avenues in order to communicate to the industry, the need for adopting the LTTC bonding process as a replacement of the existing integration processes. The possible avenues include journal papers, industry conferences, affiliations with industrial consortiums such as EMC^{3D} (Semiconductor 3D Equipments and Materials Consortium) as well as filing of more patents pertaining to the LTTC technology.

There are some *unique selling points* required to get the industry to embrace this new technology. Some of them could include the relatively high yield of this process, use of room temperature for bonding, potential to stack even more wafers vertically (due to minimal wafer bow effects), high profit margins when high market share can be achieved, fast time to breakeven etc... As a licensing start-up company, it would be necessary to get listed in the press often so as to make others in the industry feel our presence and necessity.

7.9 STRATEGY TO ADOPT

Based on the analysis presented, it is found that setting up a non-manufacturing start-up with licensing LTTC technology as the main strategy is a low risk – high return solution. Therefore, we recommend this approach to be the most suitable if MIT decides to commercialize the LTTC technology.

CHAPTER 8

8. COMPARISON WITH COMPETING TECHNOLOGIES

Having analyzed the LTTC technology from various perspectives, it is necessary to summarize the findings of the work presented so far, to look at the advantages and disadvantages of LTTC in comparison to other competing technologies and to provide certain yardsticks that would indicate what conditions need to be achieved in order to commercialize LTTC with sustainable profit margins.

Table 8.1: Comparison of various features of the different wafer bonding technologies.

BONDING TECHNIQUE	Alignment	Expected Yield	Throughput	Process & Equipment Cost	Sensitivity to Bonding Surface[25]	Applied Load[28]
LTTC	Good	Good	Low	High	High	Large
HTTC	Poor[18]	Poor	High	Moderate	High	Large
Direct	Good[18]	Good	High	Low	High	Low
Anodic	Moderate	Moderate	High	Low	Moderate	Low
Eutectic	Good	Good	High	Moderate	Low	Low
Adhesive	Good	Good	High	Moderate	Low	Low

Table 8.1 presents a general comparison of the various bonding technologies in terms of features such as alignment, expected yield, throughput, processing cost, sensitivity to surface features and applied force required. It may be seen that LTTC is a favorable technique when considering the alignment and yield. As discussed earlier, alignment is good because of the low temperature process that minimizes residual stresses and yield is enhanced as a consequence. However, its throughput is quite low since pumping of UHV systems takes long and bonding duration also needs to be kept high to facilitate substantial interface diffusion of Cu atoms at these kinetically unfavorable low temperatures. LTTC has higher equipment costs due to a low throughput and also the additional requirement for UHV pumps and chambers. Since the bonding interface in LTTC is a hard metal surface with no viscosity, surface roughness plays a significant role in determining the quality of the bond formed. To cause considerable elastic and plastic deformation of the hard metal bonding interface and facilitate good adhesion, high applied loads are also necessary. Although application of a large applied force is possible, there could be limitations to it since low-K dielectric materials in the BEOL layers which have weak mechanical integrity could easily crack upon high loading stress.

Based on the cost model presented in the previous chapter, we may present some useful yardsticks required for various factors in order for LTTC to be successfully commercializable and replace the current HTTC technology. It is found that a minimum yield of 95.4% would be required if LTTC is to replace HTTC. This yield has been observed in a laboratory setup and our arguments in the previous chapter also strongly indicate that achieving this yield would not be an issue. As for alignment accuracy, a value of 0.25 μm would be required. This should hopefully be achievable for LTTC in the near future since there is minimal thermal expansion induced mismatch affecting any alignment and there are more advanced instrumentation tools available for accurate alignment[31]. As far as the throughput is concerned, since the cost of UHV systems and wafer bonders is relatively small compared to the cost of other standard fab equipments, the overall cost is found to be not very sensitive to the bonding throughput.

CHAPTER 9

9. CONCLUSION

This work looked at the low temperature thermocompression (LTTC) bonding technology for wafers using Cu as the bonding interface material in order to realize high performance heterogeneous system-on-chip (SoC) and DRAM devices that enable better developments in the near future for the microelectronics industry. The ability to commercialize the LTTC technology has been investigated from various perspectives including technology, science, manufacturing, cost, supply chain, intellectual property (IP), etc... Based on the comprehensive and in-depth analysis, the LTTC technology is found to be favorable from most dimensions. Our investigations reveal that manufacturing as a new start-up for this technology could be favorable but is a high risk strategy. Rather, an alternative approach to setup a new licensing company with zero manufacturing initiative is found to be low risk – high return favorable strategy.

Some risk factors do exist that could hinder our efforts to woo companies to adopt the LTTC technology for DRAM. One of them is the recent downfall in DRAM prices as a result of excess supply and high inventory stocking. Also, the low throughput of LTTC could be a major hindrance in convincing companies to consider adopting this technology although our cost model reveals that the overall processing cost is not very sensitive to the bonding throughput.

Our continued focus will be on 3D technology research for the near-term and future, focusing specifically on LTTC. There are still various avenues to be further studied and explored in LTTC that will help enhance our understanding of this technology. Some of these are listed in Table 9.1.

A summary of our strategy is provided in the form of a flowchart in Fig 9.1. Given the benefits of adopting LTTC, we shall be licensing out our patents to the semiconductor 3D giants across the world and achieving economic success through licensing fees and royalties.

Table 9.1: Further research to be carried out to comprehensively understand the LTTC technology.

FURTHER RESEARCH AVENUES TO EXPLORE
• **YIELD** – Based on the yield model presented in the Appendix, yield optimization needs to be performed in order to determine the best set of process parameters that would optimize the bonding yield. Consistency in yield requires the use of statistical process control (SPC) with a drive towards the 6σ process.

- **RELIABILITY** – Thermomechanical reliability of LTTC bonded stacks must be analyzed both by testing as well as by finite element simulations. Electromigration (EM) and stress migration (SM) issues in TSV and Cu bonded interfaces deserve in-depth analysis. This requires us to fabricate suitable EM test structures with TSV and Cu-bonded elements and subsequently subject them to accelerated testing and perform failure analysis.

- **STATISTICAL MODELING** – Reliability of TSV and Cu bonding is to be quantified by developing reliability block diagrams to model 3DICs and using accelerated life testing (ALT) to find out the stress lifetime of 3D devices and extrapolating these to normal field use conditions to determine the median time to failure of 3D structures. The presence of multiple reliability-related failure mechanisms in LTTC based structures requires the use of multi-modal statistics for accurate reliability analysis.

- **PROCESS OPTIMIZATION** – The various processes such as DRIE[65], CMP, UHV bonding etc... and thin film deposition techniques (Cu electrodeposition) need to be optimized in order to avoid process-induced defects and fabricate more reliable TSV – Cu bonded device structures.

- **DEVICE PERFORMANCE** – Influence of bonded Cu wafers and TSV on the transistor device characteristics needs further investigation. Device performance could be affected by TSV as revealed by some recent finite element simulations[66].

- **MECHANICAL MODELING** – The true contact area model presented in Chapter 3 needs to be extended to include the effects of bonding temperature and bonding duration time and also account for the UHV low background pressure that suppresses the formation of oxide layers on the Cu bonding surface.

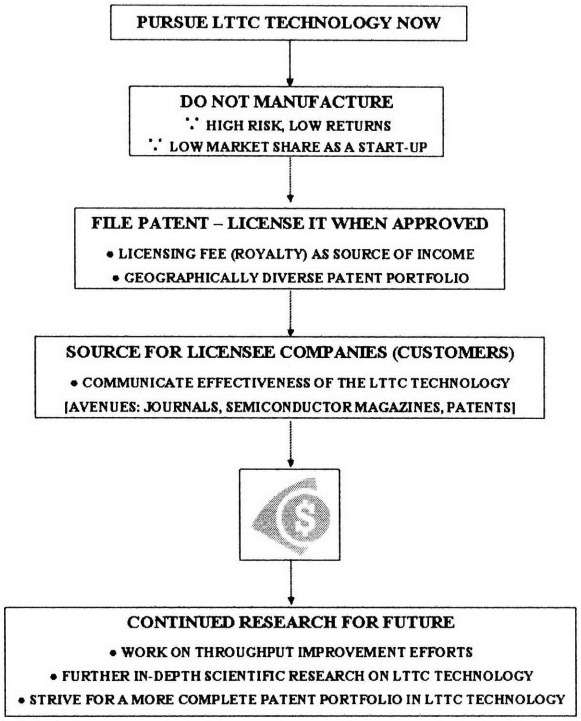


Fig 9.1: Summary of the strategy to be adopted in commercializing the LTTC technology.

APPENDIX

I have attempted to develop a quantitative model to evaluate the yield of Cu bonded die / wafers. The details of the model are presented in this Appendix.

A. STATISTICAL YIELD MODEL

Yield is technically defined to be the fraction of devices operating before the product is shipped. In other words, it may be regarded as the quality or reliability at time t = 0. *Yield loss* is the complement of yield referring to the percentage of manufactured devices that failed during test.

A.1 DEFECTS

Yield loss is typically caused by defects which can be classified as "*yield defects*" or "*reliability defects*"[51]. Yield defects refer to those defects that have a defect size more than the threshold defect size for failure at time t = 0. On the contrary, reliability defects refer to those defects where the initial defect size is low but as the device operates some failure mechanisms cause the defect size to increase and approach the threshold defect size after some time, *t*. Defects are characterized to have a certain defect density and defect size distribution. In the case of wafer bonding, as may be seen in Fig A.1, the defects or voids or unbonded areas are not distinct and discrete. Rather, they are continuous throughout the wafer. Therefore, defects cannot be used as a criterion to quantify yield since the defect density cannot be determined when they are not distinct and discrete. To tackle this issue, we use the contacted area spots on the wafers to quantify yield. As evidenced by Fig A.1, the contact area spots are distinct when bonding occurs and we could associate them with a spot density and spot size distribution.

A.2 CONTACT AREA SPOTS

Fig A.1 shows a typical bonded wafer with the areas of contact indicated as spots with the applied load being successively increased. These localized areas of contact can be thought to have a *contact area spot* (CAS) density and size distribution denoted by f(D) and s(a) respectively.

Although we typically look at the total true contact area as a criterion to determine the bond quality, we could alternately look at bonding from a nanoscale perspective by analyzing the individual contact areas of each of the contacting asperities at the bonded interface of the wafers as illustrated by Fig A.2. If the contact area of two asperities is very small, it would be easy to "debond" that contact since the debonding force / area during crack propagation is quite large. However, if the asperity contact area is large, then resistance to debonding would be higher and

the contact more intact. This allows us to choose a "*critical threshold contact area*" below which bonding is weak and debonding occurs easily. Based on this logic, let us now develop the statistical yield model for 3DIC.

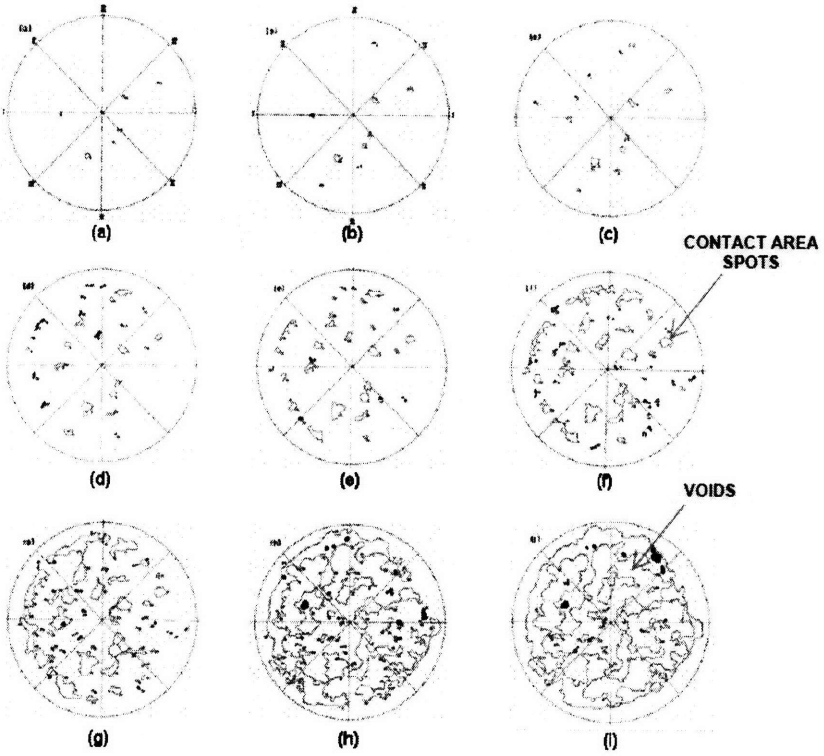


Fig A.1: Contact areas for bonded wafer at different applied load conditions[25].

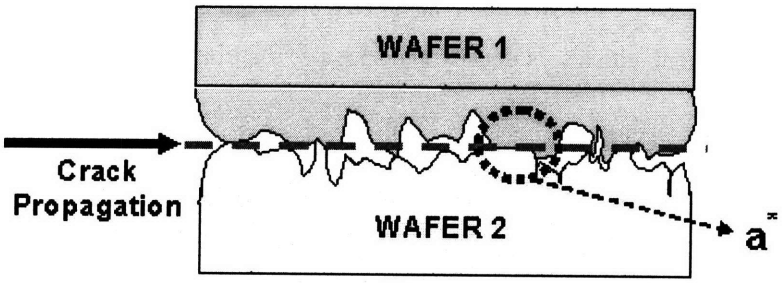


Fig A.2: Analysis of bonded interface by looking at individual asperity contact areas during crack propagation.

A.3 STOCHASTIC YIELD MODEL

A.3.1 NOMENCLATURE

Given below are the symbols used in developing the yield model. There are some terminologies used here. "*Good yield spot*" refers to the asperity contact points which have a contact area larger than the critical contact area (a^*) and hence do not fail upon burn-in test or during wafer dicing.

"*Good reliability spot*" refers to the asperity contact points which have an initial contact area so large that although, as time evolves, failure mechanisms such as stress migration cause voids to form, the contact area at time t , $a(t) > a^*$ thereby causing no reliability issues.

N – Random variable representing number of contact area spots (CAS) in the bond interface.

$\mathbf{N_Y}$ – Random variable representing number of spots that are "*good yield spots*".

$\mathbf{N_R}$ – Random variable representing number of spots that are "*good reliability spots*".

$\mathbf{A_0}$ – Random variable representing contact spot area at initial time (t = 0).

$\mathbf{A_t}$ – Random variable representing contact spot area at any time t.

n – Total number of asperity contacts.

$\mathbf{n_Y}$ – Arbitrary number of good yield spots in the bond interface.

$\mathbf{n_R}$ – Arbitrary number of good reliability spots in the bond interface.

$\mathbf{p_Y}$ – Probability that an asperity contact is a "good yield spot".

$\mathbf{p_R}$ – Probability that an asperity contact is a "good reliability spot".

a – Contact area of an arbitrary spot.

$\mathbf{a^*}$ - Critical threshold contact area below which bond could fail.

s(a) – CAS size distribution.

f(D) – CAS density distribution.

A.3.2 PROBABILITY THEORY FOR THE MODEL

An asperity contact could be a yield loss spot (n_Y), reliability loss spot at time 't' (n_R) or an area of contact so large that it may not undergo bond failure up to the given time 't' ($n - n_Y - n_R$).

The probability mass function (p.m.f) representing the number of contact area spots (n_Y, n_R, $n - n_Y - n_R$) may be expressed using the *multinomial distribution* which is similar in nature to the binomial distribution as follows[51]:

$$pmf(n_Y, n_R, n - n_Y - n_R) = \frac{n!}{n_Y! n_R! (n - n_Y - n_R)!} \cdot {p_Y}^{n_Y} \cdot {p_R}^{n_R} \cdot (1 - p_Y - p_R)^{n - n_Y - n_R} \quad \text{(A-1)}$$

Where n_Y and n_R are integers since they represent the number of contact area spots.

The probability p_Y that a contact spot is a "good yield spot" can be expressed as in (A-2) where $\mathbf{a^*}$ refers to the *critical (threshold) contact area* causing device failure.

$$p_Y = \Pr(A_0 \geq a^*) = \int_{a^*}^{\infty} s(a)da \quad \text{(A-2)}$$

From (A-1), the distribution for number of good yield spots (N_Y) may be expressed as in (A-3).

$$pmf(n_Y) = \sum_{n=0}^{\infty} \Pr(N_Y = n_Y | N = n) \cdot \Pr(N = n) = \sum_{n=0}^{\infty} \binom{n}{n_Y} \cdot (p_Y)^{n_Y} \cdot (1 - p_Y)^{n_Y} \cdot pmf(n) \quad \text{(A-3)}$$

The bonding yield (Y_B) may now be defined as the probability that there exists at least one good yield spot in the bonding interface. This may be expressed by (A-4).

$$Y = pmf(n_Y \geq 1) = 1 - pmf(n_Y = 0) \quad \text{(A-4)}$$

The probability p_R that a contact spot is a "good reliability spot" can be expressed as in (A-5) and the reliability function is defined similar to the yield function above in (A-6). The time-dependent decrease in contact area (A_t) due to failure mechanisms such as stress migration, electromigration etc... needs to be determined from a physical perspective based on observations of void nucleation and growth kinetics.

$$p_R = \Pr(A_t \geq a^*; A_0 \geq a^*) \quad \text{(A-5)}$$

$$R_B(t) = pmf(n_R \geq 1) = 1 - pmf(n_R = 0) \quad \text{(A-6)}$$

The expression for p.m.f (n) depends on the contact area density distribution, f(D), as follows where A is the area of the die or wafer considered and D is the asperity density[51].

$$pmf(n) = \int_0^{\infty} \frac{(AD)^n \cdot e^{-AD}}{n!} \cdot f(D) dD \quad \text{(A-7)}$$

There are various density distributions [f(D)] available such as constant density, uniform density, Erlang density and Gamma density. The most commonly used density distribution is the *Gamma density* model which is widely applicable. It is expressed in (A-8) with parameters α and β. In most cases, the contact area density is expected to be higher at the centre than at the edges for bowed wafers unless sufficient load is applied such that the contact area is uniformly distributed.

$$f(D) = \frac{1}{\Gamma(\alpha) \cdot \beta^{\alpha}} \cdot D^{\alpha - 1} e^{-D/\beta} \quad \text{(A-8)}$$

A.3.3 USE OF THE TRUE CONTACT AREA MODEL

Having developed the yield model from a stochastic perspective, it is necessary to relate it to the process parameters of the thermocompression bonding process so that the expected yield for various combinations of process parameters could be estimated. This is made possible by using the true contact area model[25, 41] developed in Chapter 3.

The asperity density (D) in Eq.(A-8) is the same asperity density, denoted by η in the *true contact area* model. The CAS size distribution is expressed by (A-9) and illustrated by Fig A.3 in which the parameter a_c could be approximated as the mean contact area spot size which could be determined from the overall true contact area (A_T) and asperity density (η) by (A-10). In order to maintain the condition for yield neutrality, the parameters *b*, *c* and *d* are set to *b=1*, *c =1* and *d=3* always.

$$s(a) = \begin{cases} c \cdot a_c^{-b-1} \cdot a^b \; ; 0 \le a \le a_c \\ c \cdot a_c^{d-1} \cdot a^{-d} \; ; a_c \le a < \infty \end{cases} \tag{A-9}$$

$$a_c = \frac{A_T}{(\eta \cdot A_N)} \tag{A-10}$$

Note that A_T in Eq.(A-10) is calculated from the *true contact area* model and it depends on the applied load (L), asperity density (η), surface roughness (σ_s) and asperity radius (R). Some of these parameters are determined by AFM scan of the unbonded Cu film on the wafer surface.

The fitting parameters of the yield and reliability model developed are **α**, **β**, and **a***. While the parameters α and β could be determined or precisely assumed from the contact area spatial distribution observed during actual bonding, the only fitting parameter that needs to be found is the critical threshold contact area (**a***).

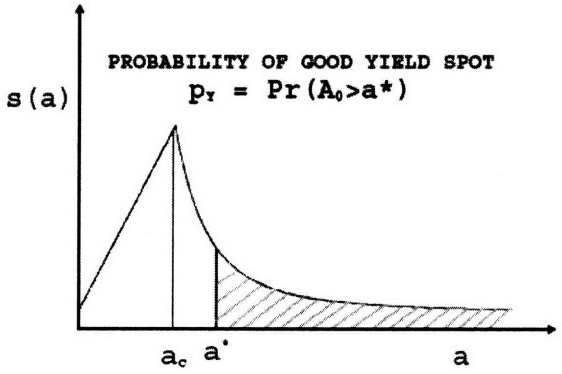


Fig A.3: Typical contact area spot size distribution with mean contact area of a_c[51].

Experimental yield data such as that shown in Table A.1 may be used to estimate the value of **a***. Once this is done, all the parameters of the yield model are determined and it can then be used to predict the yield for any combination of bonding process parameters {L, η, σ_s}.

Table A.1: Experimental data on dicing yield that can be used to calibrate the yield model developed[41].

Table 12 Details of the different bonding experiments. Results of surface roughness characterizations, calculated true contact areas, and the dicing yield for each of the experiments. All wafers were bonded at 300 °C. (rms roughness is the root-mean-square roughness of the wafer surface measured with AFM. The scan area was $1 \times 1\ \mu m^2$. A minimum of six scans were taken for each wafer surface and the average value was taken).

	Load (lI)	Nominal contact Area (m^2)	RMS roughness (m^2)	d (nm)	True contact area (m^2)	Dicing yield (%)
Blanket (CMP)-blanket (CMP)	400	0.03142	1.05, 1.05	3.03	$8.98E^{-07}$	11.1
	1000	0.03142	1.05, 1.05	2.76	$2.21E^{-06}$	31.9
	2000	0.03142	1.05, 1.05	2.55	$4.16E^{-06}$	66.0
	2550	0.03142	1.05, 1.05	2.48	$5.58E^{-06}$	76.4
	4550	0.03142	1.05, 1.05	2.29	$9.77E^{-06}$	97.2
	8000	0.03142	1.05, 1.05	2.10	$1.70E^{-05}$	100.0
	10000	0.03142	1.05, 1.05	2.01	$2.13E^{-05}$	100.0
Blanket (CMP) blanket (CMP and etched)	4550	0.03142	1.05, 5.83	2.66	$6.05E^{-06}$	81.9
	4550	0.03142	1.05, 2.34	2.66	$7.44E^{-06}$	91.0
	10000	0.03142	1.05, 5.83	2.43	$1.30E^{-05}$	91.7
Blanket (CMP and etched)-blanket (CMP and etched)	2000	0.03142	4.38, 4.90	2.94	$2.39E^{-06}$	1.4
	2000	0.03142	2.50, 1.50	2.86	$2.82E^{-06}$	16.7
	4550	0.03142	4.14, 5.53	2.86	$5.75E^{-06}$	72.9
Blanket (as deposited)-blanket (CMP and etched)	4550	0.03142	5.92, 8.42	2.80	$6.12E^{-06}$	66.7
	4550	0.03142	5.92, 2.93	2.63	$5.89E^{-06}$	72.2
Blanket (as deposited)-blanket (as deposited)	6000	0.03142	5.92, 5.92	2.76	$8.72E^{-06}$	95.1
Blanket (CMP)-patterned (50 μm)	4550	0.01271	1.05, 8.63	2.50	$5.08E^{-06}$	42.4
	10000	0.01271	1.05, 8.63	2.23	$1.15E^{-05}$	87.5
Blanket (CMP)-patterned (175 μm)	4550	0.00578	1.05, 10.00	2.23	$5.11E^{-06}$	36.0
	10000	0.00578	1.05, 10.00	1.95	$1.12E^{-05}$	68.4
Blanket (CMP)-patterned (310 μm)	4550	0.00400	1.05, 11.95	2.15	$4.69E^{-06}$	25.6
	10000	0.00400	1.05, 11.95	1.90	$1.02E^{-05}$	57.0

Experimental Results

Compare with the theoretical **YIELD MODEL** developed & calibrate the yield model parameters...

A.4 YIELD FOR MULTIPLE DIE STACKING

Our analysis so far has focused on the bonding yield when two wafers (blanket or patterned) are bonded together. Typically, the number of wafers that could be bonded is around 4-5. Therefore, the overall bond yield (Y_B) of a stacked die or wafer must account for these multiple bonding steps. Every additional layer of stacking causes a cumulative reduction in the overall yield of the 3D structure. The bond yield, Y_B, for an N-level stacking may be expressed by (A-11) where $Y_{K/K+1}$ refers to the bond yield when wafers / dies K and K+1 are bonded. The bonding yield for every successive stacking is increasingly lower because as additional wafers are added to a stack, it becomes less compliant and more difficult to overcome the bowing effects even if sufficient load is applied. Therefore, this reduction in compliance results in a lower quality of bonding with additional wafers.

$$Y_B = \prod_{K=1}^{N-1} Y_{K/K+1} \quad ; \quad Y_{N-1/N} < Y_{N-2/N-1} < \ldots < Y_{1/2} \tag{A-11}$$

A.5 CUMULATIVE YIELD OF 3DIC

Apart from the defective bond interfaces between wafers, other sources also result in yield loss of a 3DIC. These include process contaminants and extrinsic defects that affect the yield of each die fabricated by planar processing. Moreover, the initial wafer used for fabrication could also be defective. Considering all these possibilities, the cumulative yield of a 3DIC may be expressed as in (A-12) where the standard expression for die yield, Y_{die}, is given by (A-13)[67] which resembles the *negative binomial yield model* with D_{unit} representing the defect density (defects/area), A_{die} referring to the defect-sensitive area of the die and P is a constant which is found to have a value of 7 for the current generation of CMOS technology.

$$Y_{overall} = \left(Y_{wafer} \cdot Y_{die}\right)^{N} \cdot Y_{B} \tag{A-12}$$

$$Y_{die} = \left[1 + \frac{D_{units} \cdot A_{die}}{P}\right]^{-P} \tag{A-13}$$

REFERENCES

[1] International Technology Roadmap for Semiconductors – ITRS (2007).

[2] Stathis, J.H., "Reliability limits for the gate insulator in CMOS technology", *IBM Journal of Research and Development*, Vol. 46, No. 2/3, pp.265-286, (2002).

[3] Topol, A.W. *et al.*, "Three-dimensional integrated circuits", *IBM Journal of Research and Development*, Vol. 50, No. 4/5, pp.491-506, (2006).

[4] Lu, J.Q., Cale, T.S. and Gutmann, R.J., "Wafer-level three-dimensional hyper-integration technology using dielectric adhesive wafer bonding", *Materials for Information Technology: Devices, Instruments and Packaging*, Springer-Verlag, London, pp.386-397, (2005).

[5] Patrick, L., *Conference on Frontiers of Characterization & Metrology for Nanoelectronics*, (2007).

[6] Thompson, C.V., "Carbon Nanotubes as interconnects: Emerging technology & potential reliability issues", *IEEE International Reliability Physics Symposium*, (2008).

[7] Wang, A.W. and Saraswat, S.C., "A strategy for modeling of variations due to grain size in polycrystalline thin film transistors", *IEEE Transactions on Electron Devices*, Vol. 47, No. 1035, (2000).

[8] Subramanian, V., Toita, M., Ibrahim, N.R., Souri, S.J. and Saraswat, K.C., "Low leakage Germanium-seeded laterally crystallized single-grained 100nm TFTs for vertical integration applications", *IEEE Electron Device Letters*, Vol. 20, No. 341, (1999).

[9] Neudeck, G.W., Pae, S., Denton, J.P. and Su, T., "Multiple layers of Silicon-on-Insulator for nanostructure devices", *Journal of Vacuum Science & Technology B*, Vol. 17, No. 3, 994, (1999).

[10] Yamauchi, N., "Polycrystalline silicon thin films processed with silicon ion implantation and subsequent solid-phase crystallization: Theory, experiments and thin-film transistor applications", *Journal of Applied Physics*, Vol. 75, No. 7, 3235, (1994).

[11] Yoon, S.Y., Kim, S.K., Oh, J.Y., Choi, Y.J., Shon, W.S., Kim, C.O. and Jang, J., "A high performance polycrystalline silicon thin-film transistor using metal-induced crystallization with Ni solution", *Japanese Journal of Applied Physics*, Part 1, 7193, (1998).

[12] Low, Y.L. and O'Connor, K.J., "Electrical performance of chip-on-chip modules", *IEEE Transactions on Advanced Packaging*, Vol. 22, 321, (1999).

[13] Banerjee, K., Souri, S.J., Kapur, P. and Saraswat, K.C., "3-D ICs : A novel chip design for improving deep-submicrometer interconnect performance and Systems-on-Chip Integration", *Proceedings of the IEEE*, Vol. 89, No. 5, (2001).

[14] Shimbo, M., Furukawa, K., Fukuda, K. and Tanzawa, K., "Silicon-to-silicon direct bonding method", *Journal of Applied Physics*, Vol. 60, No. 8, 2987, (1986).

[15] Lasky, J., "Wafer bonding for silicon-on-insulator technologies", *Applied Physics Letters*, Vol. 48(1), 78, (1986).

[16] Belford, R.E. and Sood, S., "Surface activation using remote plasma using hydrophilic bonding at elevated temperature", *Electrochemical Solid State Letters*, Vol. 10(5), H145, (2007).

[17] Gui, C., Elwenspoek, M., Tas, N. and Gardeniers, J., "The effect of surface roughness on direct wafer bonding", *Journal of Applied Physics*, Vol. 85(10), 7448, (1999).

[18] Farrens, S. and Sood, S., "Bonding Solutions for 3D Integration", *Advanced Packaging*, pp.29-31, April, (2008).

[19] Wang, C. and Lee, C., "An eutectic bonding technology at a temperature below the eutectic point", *42nd Electronics Components & Technology Conference*, 502, (1992).

[20] Tilmans, H., Van de Peer, D. and Beyne, E., "The indent reflow sealing (IRS) technique – A method for the fabrication of sealed cavities for MEMS devices", *Journal of Microelectromechanical Systems*, Vol. 9(2), 206, (2000).

[21] Wallis, G. and Pomerantz, D., "Field assisted glass-metal sealing", *Journal of Applied Physics*, Vol. 40(10), 3946, (1969).

[22] Schmidt, M., "Wafer-to-wafer bonding for microstructure formation", *Proceedings of the IEEE*, Vol. 86(8), 1575, (1998).

[23] Cho, S. and Erdmann, F., "An on-chip hermetic packaging technology for micromechanical devices", *Solid-State Sensor and Actuator Workshop*, 229, (1998).

[24] Li, Y. and Bower, R., "Systematic low temperature silicon bonding using pressure and temperature", *Japanese Journal of Applied Physics*, Vol.37(3A), 737, (1998).

[25] Leong, H.L., "Quantitative analysis of the mechanical and electrical properties of Cu-Cu bonds for three-dimensional integrated circuits", *SMA PhD Thesis*, (2007).

[26] Tsau, C.H., "Fabrication and characterization of wafer-level gold thermocompression bonding", *MIT PhD Thesis*, (2003).

[27] Cale, T.S., Lu, J.Q. and Gutmann, R.J., "Three-dimensional integration in microelectronics: Motivation, processing and thermomechanical modeling", *Chemical Engineering Communications*, Vol.195, pp.847-888, (2008).

[28] Niklaus, F., Stemme, G., Lu, J.Q. and Gutmann, R.J., "Adhesive wafer bonding", *Applied Physics Reviews – Focused Review*, Vol. 99, 031101, (2008).

[29] Lu, J.Q., Cale, T.S. and Gutmann, R.J., "Wafer-level three-dimensional hyper-integration technology using dielectric adhesive wafer bonding", *Engineering Materials & Processes Book Series – Materials for Information Technology*, Springer London Publishers, pp.405-417, (2005).

[30] Thompson, C.V. and Tadepalli, R., "Bonded Cu Interconnects for Three-Dimensional Integrated Circuits", Vol. 970, (2007).

[31] Matthias, T., Wimplinger, M., Pargfrieder, S. and Lindner, P., "3D Process Integration – Wafer-to-Wafer and Chip-to-Wafer Bonding", *Materials Research Society Symposium*, Vol. 970, (2007).

[32] Chylak,B. and Qin, I.W., "Packaging for multi-stack die applications", *Semiconductor International*, (2004).

[33] Tadepalli, R., "Characterization and requirements for Cu-Cu bonds for three-dimensional integrated circuits", *MIT PhD Thesis*, (2007).

[34] Turner, K.T. and Spearing, S.M., "Modeling of direct wafer bonding: Effect of wafer bow and etch patterns", *Journal of Applied Physics*, Vol. 92, No. 12, (2002).

[35] Tadepalli, R., Turner, K.T. and Thompson, C.V., "Effects of patterning on the interface toughness of wafer-level Cu-Cu bonds", *Acta Materialia*, Vol. 56, pp.438-447, (2008).

[36] Discussions with EV Group® at NTU (March, 2007).

[37] Hau-Riege, S.P. and Thompson, C.V., "In-situ transmission electron microscope studies of the kinetics of abnormal grain growth in electroplated copper films", *Applied Physics Letters*, Vol. 76, No. 3, pp.309-311, (2000).

[38] Doe, P., "Real demand drivers appear for 3D ICs if makers can produce them in volume", *Solid State Technology*, October, (2005).

[39] Burkett, S. *et al.*, "Materials aspects to consider in the fabrication of through-silicon vias", *Materials Research Society Symposium*, Vol. 970, (2007).

[40] Gan, C.L., *SMA PhD Project Proposal*, (2007).

[41] Leong, H.L., Gan, C.L., Thompson, C.V., Pey, K.L. and Li, H.Y., "Application of contact theory to metal-metal bonding of silicon wafers", *Journal of Applied Physics*, Vol.102, 103510, (2007).

[42] Tadepalli, R. and Thompson, C.V., "Formation of Cu-Cu interfaces with ideal adhesive strengths via room temperature pressure bonding in ultra-high vacuum", *Applied Physics Letters*, Vol. 90, 151919, (2007).

[43] Tan, C.S., Chandrakasan, A. and Reif, R., "Progress in copper-based wafer bonding", *Materials Research Society Symposium*, Vol. 970, (2007).

[44] Tan, C.S., "Progress in copper-based wafer bonding", *VLSI Multi-level Interconnection Conference (VMIC)*, (2007).

[45] Tan, C.S., Reif, R., Theodore, N.D. and Pozder, S., "Observation of interfacial void formation in bonded copper layers", *Applied Physics Letters*, Vol. 87, 201909, (2005).

[46] "3DIC & TSV Report", *Yole Developpement*, November, (2007).

[47] Chen, K.N., Fan, A., Tan, C.S. and Reif, R., "Bonding parameters for Blanket Copper Wafer Bonding", *Journal of Electronic Materials*, Vol. 35, No. 2, pp.230-234, (2006).

[48] Chen, K.N., Fan, A., Tan, C.S., Reif, R. and Wen, C.Y., "Microstructure evolution and abnormal grain growth during copper wafer bonding", *Applied Physics Letters*, Vol. 81, No. 20, pp.3774-3776, (2002).

[49] Chen, K.N., Tan, C.S., Fan, A. and Reif, R., "Morphology and Bond Strength of Copper Wafer Bonding", *Electrochemical and Solid-State Letters*, Vol. 7(1), G14-G16, (2004).

[50] Patti, R., "Impact of Wafer-level 3D Stacking on the Yield of ICs", *Future Fab International*, Section 7, Metrology / Failure Analysis, Issue 23, pp.103-105, (2007).

[51] Kim, K.O., "Relating integrated circuit yield and time-dependent reliability for various defect density distributions", *IEEE Transactions on Reliability*, Vol. 55, No. 2, pp.307-313, (2006).

[52] "DRAM Pricing – A White Paper", *Tachyon Semiconductor*, (2007).

[53] "Economic Model of Chip Manufacturing", *University of Massachusetts*, Computer Science Department, Course 635A, Lecture 2.

[54] Vandermeer, R.A., Jensen, D.J. and Woldt, E., "Grain boundary mobility during recrystallization of copper", *Metallurgical and Materials Transactions A*, Vol. 28A, pp.749-754, (1997).

[55] Lau, J.H. and Lee, S.W.R., "Chip Scale Package: Design, Materials, Process, Reliability & Applications", *Mc Graw Hill Professional Publishers*, (1999).

[56] Shilov, A., "Samsung's Memory Market Share Skyrockets – DRAM eXchange", Xbit Laboratories, http://www.xbitlabs.com/news/memory/display/20070727053634.html, (2007).

[57] Reif, R. *et al.*, "Method of forming a multi-layer semiconductor structure having a seam-less bonding interface", US Patent "0099796 A1", (2006).

[58] Cohn, M.B. and Kung, J.T., "Microelectromechanical System using Thermocompression Bonding", US Patent "6,853,067 B1", (2005).

[59] Glascock, H.H. *et al.*, "Method of Thermocompression Diffusion Bonding together Metal Surfaces", US Patent "4, 444, 352", (1984).

[60] Tong, Q.Y. *et al.*, "Method for low temperature bonding and bonded structure", US Patent "7, 335, 572 B2", (2008).

[61] Bower, R.W. *et. al.*, "Nitrogen based low temperature direct bonding", US Patent "5, 503, 704", (1996).

[62] Rogers, T., "Method and Equipment for Wafer Bonding", US Patent "0287264 A1", (2007).

[63] "Market Trends for 3D Stacking", *Yole Developpement*, November, (2007).

[64] http://www.tezzaron.com/technology/3D%20IC%20Summary.htm:"3D IC Industry Summary", *Tezzaron Semiconductors*, (2008).

[65] Ranganathan, N., Prasad, K., Balasubramanian, N. and Pey, K.L., "A study of thermo-mechanical stress and its impact on through-silicon vias", *Journal of Micromechanics & Microengineering*, Vol. 18, 075018, (2008).

[66] Okoro, C. *et. al.*, "Analysis of the induced stresses in silicon during thermocompression Cu-Cu bonding of Cu-through-vias in 3D-SIC architecture", *Electronic Components & Technology Conference (ECTC)*, pp.249-255, (2007).

[67] "Technology and Economics of High Performance Systems", *University of Massachusetts*, Computer Science Department, Course 635A, Lecture 2.