Characterization of Process Variability and Robust Optimization of Analog Circuits

by

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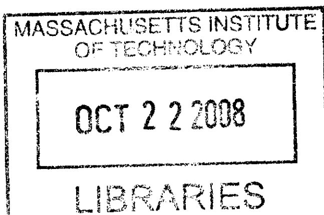

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Abstract

Continuous scaling of CMOS technology has enabled dramatic performance enhancement of CMOS devices and has provided speed, power, and density improvement in both digital and analog circuits. CMOS millimeter-wave applications operating at more than 50GHz frequencies has become viable in sub-100nm CMOS technologies, providing advantages in cost and high density integration compared to other heterogeneous technologies such as SiGe and III-V compound semiconductors.

However, as the operating frequency of CMOS circuits increases, it becomes more difficult to obtain sufficiently wide operating ranges for robust operation in essential analog building blocks such as voltage-controlled oscillators (VCOs) and frequency dividers. The fluctuations of circuit parameters caused by the random and systematic variations in key manufacturing steps become more significant in nano-scale technologies. The process variation of circuit performance is quickly becoming one of the main concerns in high performance analog design.

In this thesis, we show design and analysis of a VCO and frequency divider operating beyond 70GHz in a 65nm SOI CMOS technology. The VCO and frequency divider employ design techniques enlarging frequency operating ranges to improve the robustness of circuit operation. Circuit performance is measured from a number of die samples to identify the statistical properties of performance variation. A back-propagation of variation (BPV) scheme based on sensitivity analysis of circuit performance is proposed to extract critical circuit parameter variation using statistical measurement results of the frequency divider.

We analyze functional failure caused by performance variability, and propose dynamic and static optimization methods to improve parametric yield. An external bias control is utilized to dynamically tune the divider operating range and to compensate for performance variation. A novel time delay model of a differential CML buffer is proposed to functionally approximate the maximum operating frequency of the frequency divider, which dramatically reduces computational cost of parametric yield estimation. The functional approximation enables the optimization of the VCO and frequency divider parametric yield with a reasonable amount of simulation time.

Thesis Supervisor: Duane Boning
Title: Professor of Electrical Engineering and Computer Science

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Remembering my first day at MIT, I was so nervous since I was totally misled by the sign "Welcome to Hell" at the Harvard Bridge. Of course, you can feel like being in the middle of Hell when there is 30 inches of snow all around you in January. However, certainly it cannot be Hell when you have so many talented people around you, and they are willing to help you do what you really want to do. I feel very fortunate and privileged to spend my past six years at MIT, and this conclusion would have never been possible without the help and support of great people who I have met during my PhD.

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Chapter 1

Introduction

Over the past few decades, CMOS technology has been the mainstream in digital integrated circuit (IC) design, and in recent years CMOS technology has become the dominant path for analog IC design as well. Delay and active power consumption in digital CMOS circuits have been continuously improved by scaling of MOS transistor feature size and mobility enhancement techniques. Technology scaling has also had significant impact on analog circuit design, greatly improving the operating frequency of the active and passive components in analog building blocks in particular [9].

Figure 1-1 shows the trend of the unity current gain frequency (cutoff frequency) f_T, maximum oscillation frequency (unity power gain frequency) f_{MAX}, and effective gate length L of the CMOS devices in current and near future technologies in the ITRS road [8]. Since f_T is inversely proportional to L, as shown in Equation (1.1) below [70], the high frequency performance of the CMOS device has improved with feature size scaling.

$$f_T \approx \frac{g_m}{C_{gs}} \approx \frac{v_{sat}}{2\pi L}. \tag{1.1}$$

In Equation (1.1), v_{sat} is saturation carrier velocity, g_m is the maximum transconductance, and C_{gs} is gain-to-source capacitance of a CMOS device. In modern sub-100nm technology nodes, the cutoff frequency of CMOS devices is beyond several hundred giga-hertz. For example, NMOS f_T greater than 330GHz was reported recently in a 65nm technology node [61]. As a result, CMOS technology is quickly replacing SiGe

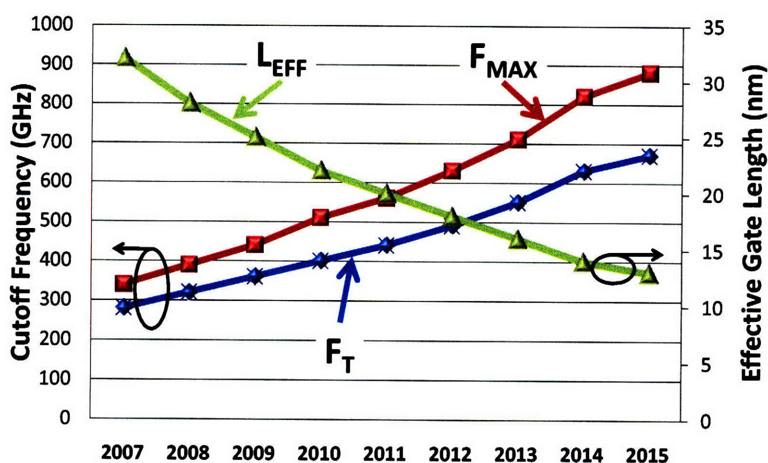


Figure 1-1: Trend of mm-wave CMOS performance in near future [8]

bipolar and III-V technologies for the implementation of analog building blocks for millimeter-wave (mm-wave) applications operating over 50GHz, because of intrinsic advantages in CMOS manufacturing cost and high density integration.

However, not every scaling impact is positive in analog circuit design. Though the cutoff frequency has increased dramatically, it has become more difficult to achieve high signal-to-noise ratio (SNR), intrinsic gain, and linearity because of reduced allowable voltage swing caused by V_{DD} scaling, degraded intrinsic gain g_m/g_{ds} and noise characteristics in sub-100nm CMOS technologies [41]. In particular, the process variability in the device and interconnect parameters has become one of the main concerns in analog circuit design in nano-scale technologies. Dynamic operating ranges of analog building blocks become smaller as nominal operating frequency increases, and therefore, parametric yield loss caused by process variation in high frequency analog building blocks has become a critical limiting factor for the yield of mixed-signal System-on-Chip (SoC) applications.

For the improvement of manufacturing yield in high performance analog circuits, new approaches for the characterization of variability in circuit parameters, the assessment of circuit performance variation, and design methodologies to maximize the parametric yield are required, as summarized in Figure 1-2. Efficient test structures are needed to capture the variability of important circuit parameters in analog circuit

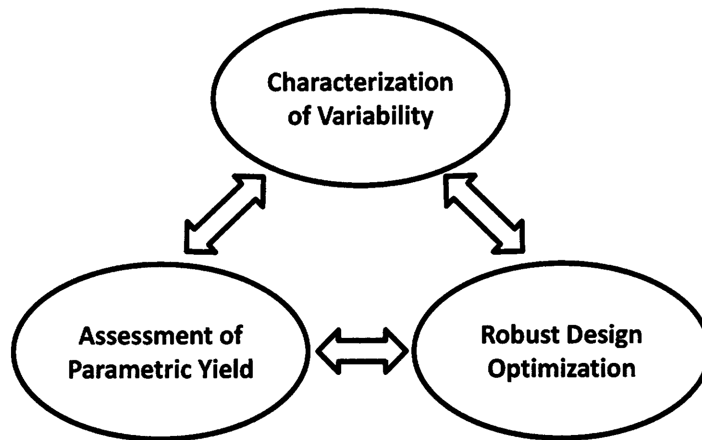


Figure 1-2: Design for manufacturability of analog circuits by the interaction between variation characterization, yield assessment, and robust optimization.

design. A good test structure provides a solid information link between design and technology by supplying feedback to manufacturing to investigate control problems in manufacturing steps such as oxidation, ion implantation, and lithography, or by providing parameter statistics to designers for the estimation of parametric yield.

An accurate and computationally efficient yield assessment method for complex analog circuits is one of the important requirements for yield improvement. Estimating the performance variation caused by inter-die and within-die variation of circuit parameters is a time-consuming task, as it typically requires a large number of simulation runs to obtain a sufficient set of statistics. Computationally efficient evaluation of performance variables to accelerate simulation speed and preserve estimation accuracy is strongly needed for yield assessment.

Last, robust optimization methodologies to directly or indirectly improve the parametric yield of analog circuits by finding optimal design points and circuit condition are required. Conventionally, analog circuit design has depended intensively on a designer's circuit intuition. However, to consider complex variation impacts in design optimization, computer-aided design optimization methodologies must support design procedures to correct the causes of parametric yield loss and to reduce the risk of costly re-spins in advanced technologies.

This thesis contributes new approaches for the characterization of process vari-

ability and methodologies for the robust optimization of high-speed analog circuit design. To develop and demonstrate these approaches, the design and implementation of a manufacturable mm-wave voltage-controlled oscillator (VCO) and frequency divider as high-speed building blocks of a phase-locked loop (PLL) are presented. The design optimization of the VCO and frequency divider is focused on achieving wide frequency operating ranges to improve manufacturability against process variation.

We show that the VCO and frequency divider circuits can be used as high-speed analog benchmarking circuits to characterize the statistical properties of analog circuit performance and critical circuit parameters in a manufacturing process. This is demonstrated through the statistical measurement of the VCO and frequency divider performance over multiple wafers. We present statistical analysis of the VCO and frequency divider performance variation to characterize important systematic and random variation patterns and the primary reasons of parametric yield loss. A sensitivity-based parameter extraction scheme is suggested and tested using the performance measurement data to estimate the statistical variation in critical circuit parameters.

Finally, a key ingredient of our methodology is robust optimization and compensation for improved yield. Dynamic compensation of performance fluctuation by active circuit tuning is a general trend in the robust optimization of digital and analog circuit performance. This thesis proves that the parametric yield of the VCO and frequency divider circuits can be improved by tuning the bias condition of the frequency divider to compensate for the divider performance variation. In addition, we suggest a computationally efficient yield estimation method for the frequency divider circuit, which allows a designer to explore the entire design space and to find the maximum yielding design point within a reasonable amount of design time and computational resource. Statistical simulation results show that the parametric yield can be maximized for given statistical distributions of important circuit parameters by the yield estimation.

In this chapter, we introduce the motivation for addressing process variability in high performance IC design in Section 1.1. In Section 1.2, we review the important sources of variation in semiconductor manufacturing processes. Statistical method-

ologies for the analysis of variation impact on circuit performance and variation-aware design methodologies are discussed and reviewed in Section 1.3. The organization of this thesis is shown and the contributions are summarized in Section 1.4.

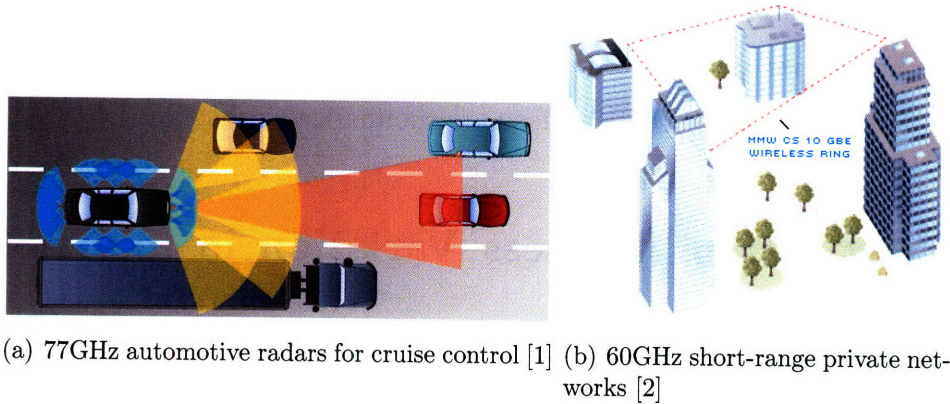
1.1 Motivation: Process Variation in millimeter-Wave CMOS Design

In recent years, mm-wave applications for high data-rate communication and passive imaging using the unlicensed 7GHz bandwidth around 60GHz and the 77GHz automotive radar band, respectively, have drawn significant attention; examples are pictured in Figure 1-3. Traditionally, mm-wave monolithic microwave integrated circuits (MMICs) have been implemented in heterogeneous III-IV technologies such as GaAs and InP because of their excellent high frequency performance due to higher electron mobility and higher breakdown voltages. Though CMOS devices provided superior cost effectiveness and higher levels of integration, the device performance could not provide sufficient speed to enable mm-wave operations in silicon. However, the continuous scaling of the silicon device feature size below 100nm, stress-induced mobility enhancement, and the improvement in circuit design techniques have enabled the implementation of mm-wave applications in CMOS technologies [33].

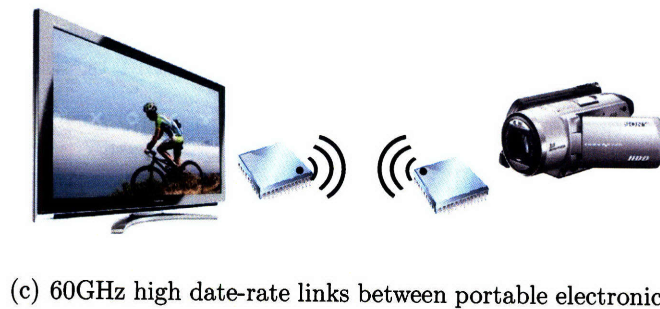
A PLL is an essential building block for high frequency clock generation in RF/mm-wave and digital applications. A typical second-order PLL circuit consists of a phase and frequency detector, a charge pump, a low pass filter (LPF), a VCO, and a frequency divider. We define a *PLL front-end* as containing a VCO and a 2:1 frequency divider [1] as depicted in Figure 1-4. Since the PLL front-end circuit operates at the highest frequency in the entire system, speed, power consumption, and noise characteristics of the PLL front-end must be considered carefully in the early stages of design.

In particular, in the mm-wave frequency regime over 50GHz, an LC-tank based VCO is a better choice compared to a ring-oscillator based VCO, due to its high

[1] called as *pre-scaler* in some references



(a) 77GHz automotive radars for cruise control [1] (b) 60GHz short-range private networks [2]



(c) 60GHz high date-rate links between portable electronics

Figure 1-3: Millimeter-wave applications

frequency operation and lower phase noise characteristics. However, the frequency tuning range of an LC-VCO is significantly narrowed by the reduced capacitance ratio between a varactor and parasitics present in deeply scaled CMOS devices. Moreover, the operating range of the frequency divider becomes limited for a reduced input power due to the power loss in the interconnect between the VCO and frequency divider. Without sufficient performance margin in VCO and frequency divider designs, process variation can cause a mismatch between the frequency tuning range of the VCO and the operating range of the frequency divider, which can result in a serious functional yield problem during the total mm-wave PLL integration.

A typical high-speed frequency divider generates a self-oscillation frequency when the input of the divider is biased to DC (discussed in detail in Section 2.3.2). The self-oscillation frequency is sensitive to circuit parameters such as the threshold voltage, channel length, parasitic capacitance, and load resistance. For example, 23.9% of $3\sigma/\mu$ variation in the self-oscillation frequency of CML static frequency dividers has been reported in a 65nm SOI CMOS technology [67]. Previously, 21.5% of $3\sigma/\mu$

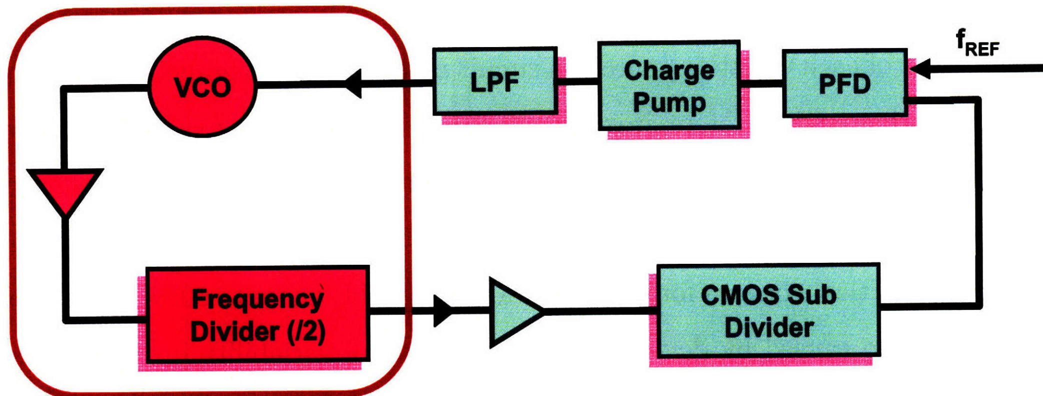


Figure 1-4: High-speed building blocks in a phase-locked loop (PLL). The PLL front-end consists of the VCO and frequency divider, circled at left.

in the self-oscillation frequency was reported in a 90nm SOI CMOS for a similar circuit implementation [87]. Even though systematic components of the performance variation can be reduced by circuit techniques and process control improvement, the impact of unavoidable random fluctuation in circuit parameters becomes more significant as circuit performance improvement is more dependent on the feature size scaling of the device and interconnects.

1.2 Sources of Variation

One of the key drawbacks of nanometer scale CMOS technology is the increasing degree of variability in device and interconnect parameters, which affects the performance and power consumption of digital and analog circuits. The process variability issues in high-performance CMOS in the sub-100nm regime have been studied intensively in recent publications (e.g., [10], [16], and [15]). A modern semiconductor manufacturing process can be classified into front-end of line (FEOL) and back-end of line (BEOL) clusters. The FEOL consists of manufacturing steps for active devices: lithography, implantation, oxidation, shallow-trench-isolation, etching, etc. On the other hand, the BEOL comprises the steps for creating interconnects: deposition, etching, chemical-mechanical polishing, etc. Variability can be involved in every man-

ufacturing step in front- and back-end processing.

The impact of each variation source on circuit performance is highly dependent on circuit application, and therefore, it is difficult to say which group of variation sources is providing a dominant impact. For example, when a circuit is sensitive to mismatch between device characteristics (e.g., SRAM cell static noise margin), the front-end variability is a critical concern for overall parametric yield. Close to 90% of canonical path delay is also caused by device variability instead of variability in interconnect parameters [82]. On the other hand, in global signal paths such as clock distribution nets, the variability in interconnect wires contributes to overall clock skew. In high frequency VCO design, the variability in metal inductors is a critical contributor to the variation in resonant frequency.

The classification of process variation based on a spatial range is also important. The total variation of a parameter P can be divided into lot-to-lot, wafer-to-wafer, across-wafer (die-to-die), within-die, and random components as shown in Equation (1.2).

$$\Delta P = \Delta P_{L2L} + \Delta P_{W2W} + \Delta P_{D2D} + \Delta P_{WD} + \Delta P_{R} \tag{1.2}$$

Each circuit parameter has a different portion of variance from each range of variation depending on the physical characteristics of major variability contributors. For example, a significant portion of the variation in the threshold voltage is random since the threshold voltage variation is contributed by the intrinsic randomness of dopant fluctuation in the channel. On the other hand, the variation in interconnect parameters is highly systematic since the variation in BEOL is highly dependent on layout pattern-density and wafer-level non-uniformity of manufacturing conditions.

In this section, we classify the sources of variation in IC performance by the variation in FEOL, BEOL, and environmental changes. Physical characteristics of each variation source are reviewed individually. The variation sources in FEOL include threshold voltage, channel length, and miscellaneous sources such as channel stress, oxide thickness, and aging. In BEOL, chemical-mechanical polishing (CMP) is the

main source of variation in the physical dimension of metal wires. Lithography-induced variation and the fluctuation of contact resistance are also contributors to performance variation in the BEOL. The IC performance is also sensitive to the variation of operating environment such as power supply voltage and surrounding temperature. The impact of the environmental variability on circuit performance must be characterized precisely to devise an adaptive compensation scheme for supply- or temperature-induced performance variation.

1.2.1 Front End Variation

Figure 1-5 shows the physical manifestations of the front-end variability in device characteristics. The primary causes of device variability are: random dopant fluctuation, oxide thickness variation, and line-edge roughness of gate polysilicon. For designers, the physical sources of variation from various manufacturing steps in FEOL such as photo-lithography, etching, and ion-implantation can be aggregated and expressed by the variation in two critical device parameters used in analog and digital circuit simulation: threshold voltage and channel length. We discuss physical causes and suggested models of variation in the threshold voltage and channel length.

Threshold Voltage Variation

The major process parameters affecting the threshold voltage of a MOS device are the doping concentration in the channel of the device and of the gate material, the channel length, and the thickness of the silicon-dioxide insulating film. As a result of the continuous scaling of MOSFET feature size, the threshold voltage variation due to random dopant fluctuation has become more significant. Manufacturing steps, such as ion implantation and annealing, have intrinsic random characteristics since the dopant atoms penetrate and diffuse through the crystal lattice in a random fashion. As a result, the final number and location of the dopant atoms are random variables. Variation due to the limited number of dopant atoms becomes a significant cause of the threshold voltage fluctuation.

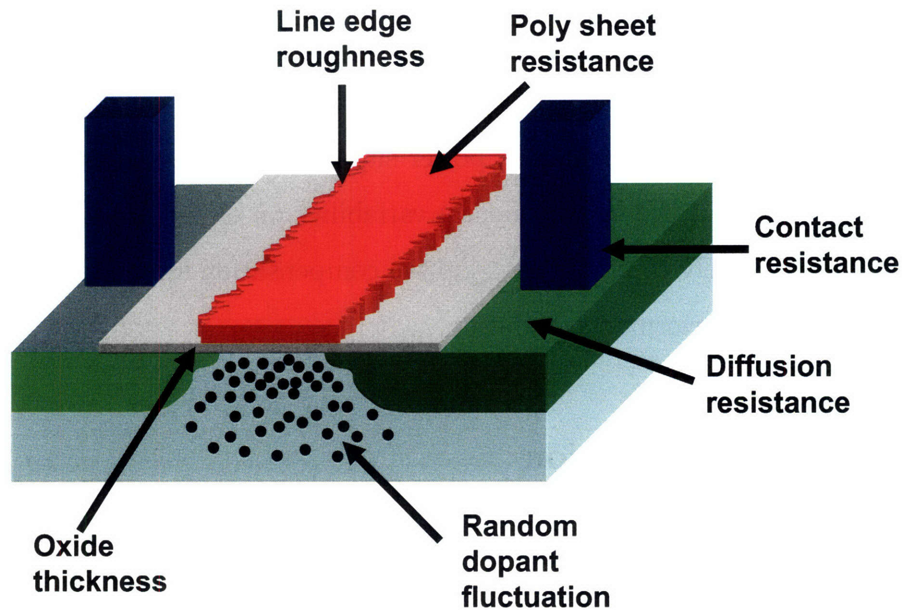


Figure 1-5: Sources of process variation in front-end of line

The variability of threshold voltage becomes a serious issue in digital circuit design since power consumption due to leakage current has increased significantly in high performance CMOS devices. Since the leakage current is exponentially dependent on the threshold voltage of CMOS devices, total power becomes more sensitive to the increased variability of the threshold voltage [31]. In analog design, the within-die variation of the threshold voltage causes mismatch in device pairs, which degrades the circuit performance of SRAM cells, differential amplifiers, comparators, and other sensitive circuits. Mean-value shift of the threshold voltage between dies, or inter-die variation, can also affect operation of circuits that depend on parameter values rather than matching in circuit performance.

The intrinsic variation of the threshold voltage associated with depletion charge, implantation, fixed oxide charge, and oxide granularity was predicted and treated analytically in the classical Pelgrom's model [85]. The feature size dependency of the standard deviation of the threshold voltage mismatch was experimentally confirmed and widely used in the prediction of variability in circuit performance. Based on the theoretically predicted $(L_{eff}W_{eff})^{-0.5}$ dependency, a useful empirical expression

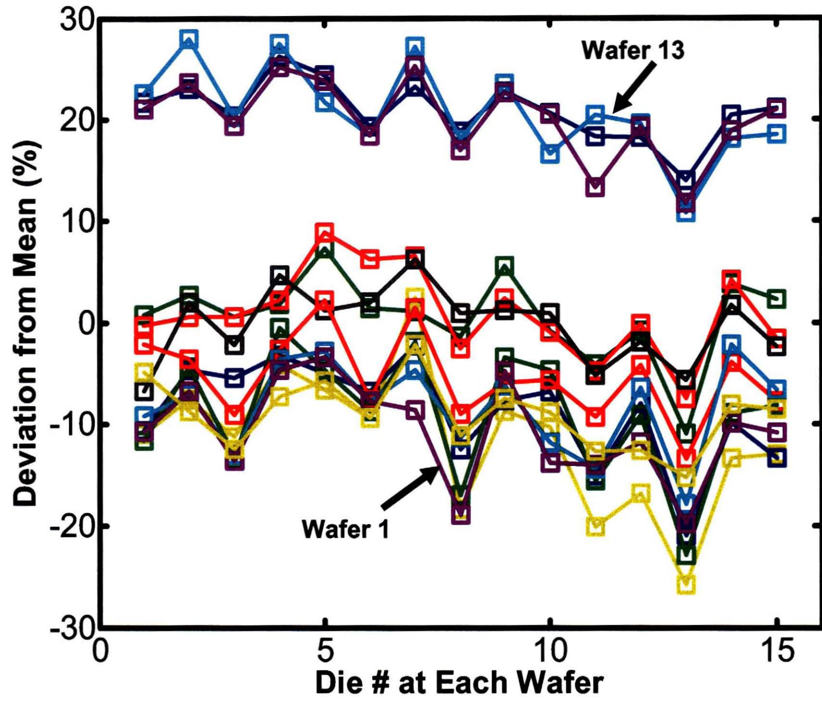
of $\sigma(V_{TH})$ in sub-100nm gate length devices was developed in [7] as Equation (1.3). Model coefficients were fitted to the results from atomistic simulation considering the discrete random number of dopant atoms and their random positioning over a three-dimensional channel space.

$$\sigma(V_{TH}) = 3.19 \times 10^{-8} \frac{t_{OX} N^{0.4}}{\sqrt{L_{eff} W_{eff}}} [V], \tag{1.3}$$

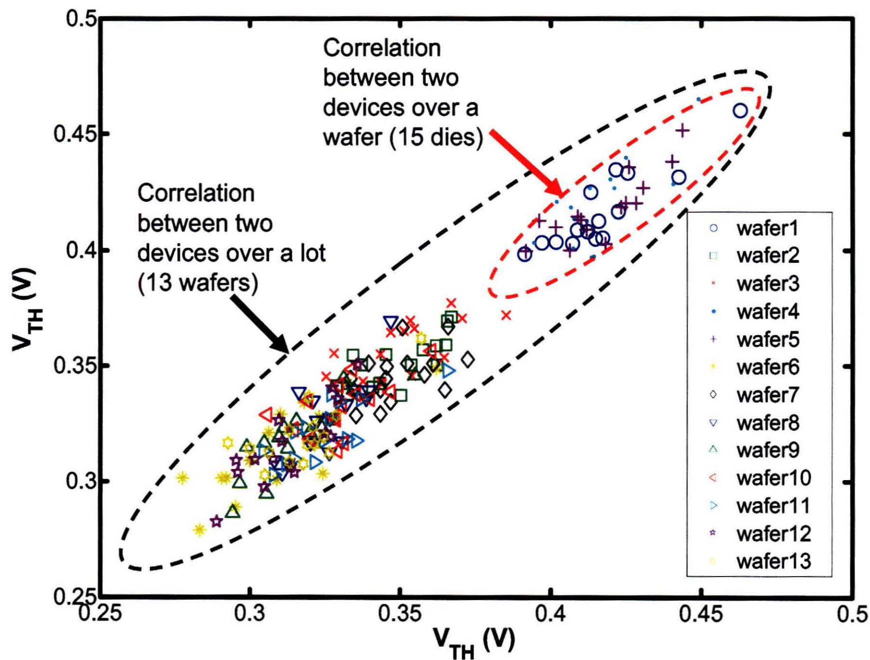
where t_{OX} is the thickness of the silicon dioxide film, and N is the number of dopant atoms in the channel.

While the within-die variation becomes more significant in scaled processes, die-to-die and wafer-to-wafer variation components are still the main contributors in overall threshold voltage variability. Figure 1-6 shows the threshold voltage variation of minimum channel length devices in a 65nm CMOS technology over 13 wafers. From each wafer, 15 dies are sampled for threshold voltage measurement. The threshold voltage is measured based on a threshold current method, giving the gate-to-source voltage (V_{GS}) when the drain current crosses a reference current level while the drain-to-source voltage (V_{DS}) is close to zero (e.g., at 0.1V). In Figure 1-6(a), each curve shows the die-to-die variation in each wafer. The similarity of each curve shows strong wafer-to-wafer spatial correlation of the threshold voltage variation. The highly systematic wafer-level die-to-die variation results in the strong correlation between two devices within the same die, as shown in Figure 1-6(b).

While the threshold current method for the measurement of the threshold voltage is convenient, it is difficult to avoid including also some impact of from channel length variation to achieve the measurement of pure threshold voltage variation. A V_{TH} measurement scheme indifferent to ΔL to capture the stochastic behavior of the within-die threshold voltage variation has been presented in [34]. The method in [34] measures a sub-threshold leakage current ratio between CMOS devices at a bias condition where the ratio is highly sensitive to the threshold voltage difference while the channel length variation impact is negligible. Figure 1-7(a) shows the ratio between the sensitivities of sub-threshold current to threshold voltage change and



(a) Wafer-to-wafer variation



(b) Correlation between two devices

Figure 1-6: Normalized threshold voltage variation of NMOS device in 65nm CMOS technology over 13 wafer (15 dies per wafer).

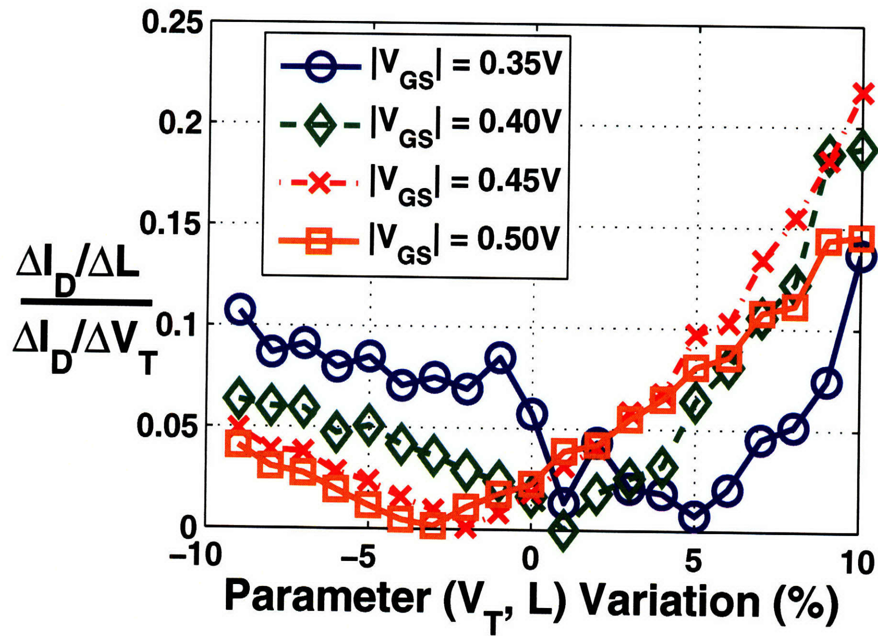
channel length change at different V_{GS} voltages. The results in Figure 1-7(b) show a highly stochastic trend of the within-die variation of the threshold voltage, with no notable spatial correlation between the devices. The correlation coefficient between two devices is close to zero and indifferent to separation distance between the devices.

Channel Length Variation

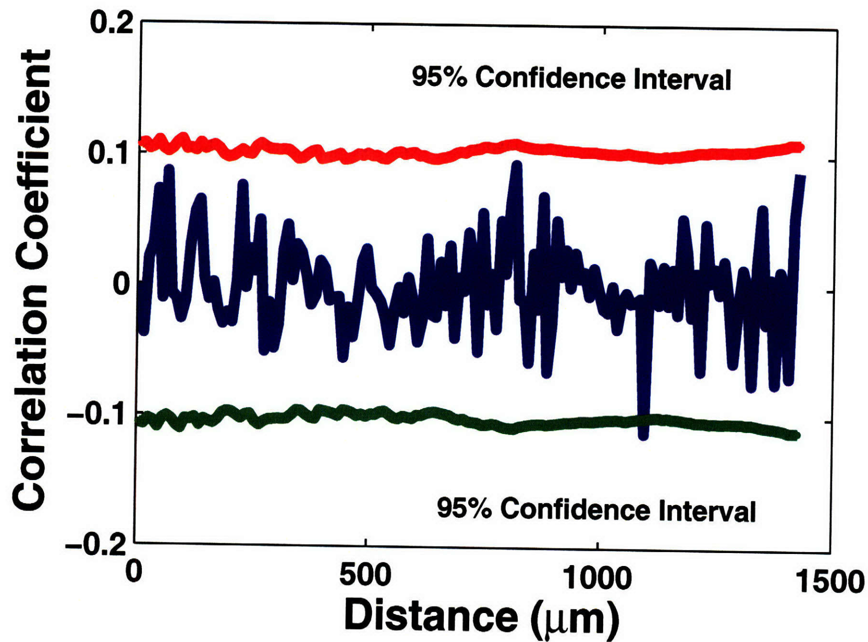
The variation in the effective channel length of the devices directly affects the saturation current in strong inversion. Channel length variation is induced by various manufacturing steps, including mask printing, exposure in photo-lithography, etching, spacer definition, and source and drain implantation.

The channel length variation can be divided into systematic and random portions. As a dominant factor of the channel length variation, the variability in photolithography is known to be highly systematic. As a result, wafer-level channel length variation patterns induced by temperature and material thickness non-uniformity in photo-lithography are likely to be systematic [81]. The systematic variation components can be decomposed using sophisticated statistical methods introduced in [97]. The randomness of the channel length variation is highly affected by line-edge roughness (LER) in gate printing. The reasons for the increased LER in the deeply scaled processes include the random variation in the number of incoming photons during exposure and the contrast of aerial images, as well as variation in the absorption rate, chemical reactivity, and molecular composition of the photo-resist. The impact of LER is certainly growing as the minimum channel length of the devices shrinks down below 100nm where sub-wavelength resolution assistant features (SRAFs) are in use to overcome the systematic variations due to limitations of the patterning processes [80] [30].

The within-die variation component of the channel length variation is quickly becoming a significant factor in performance variation, in particular, for mismatch-sensitive circuit examples such as SRAM cells and differential amplifiers. Intuitively, the transistors laid out close to each other are likely to have similar characteristics



(a) Sensitivity ratio between threshold voltage and channel length variation



(b) Spatial correlation as a function of separation distance

Figure 1-7: Sub-threshold current-based within-die threshold voltage variation measurement [34].

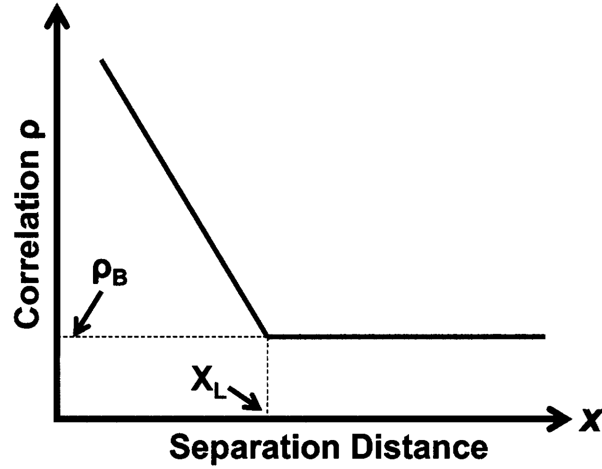


Figure 1-8: Spatial correlation model of channel length variation [40].

compared to the transistors far apart. Various formula have been introduced to model the spatial correlation of the channel length variation in terms of the distance between the transistors. An early empirical form of the spatial correlation in channel length variation was suggested in Pelgrom's model [85]. An empirical piece-wise linear form of spatial correlation with a few parameters was introduced, as shown in Figure 1-8 [40]. In this model, the correlation coefficient as a function of separation distance x is defined as in Equation (1.4):

$$\rho(x) = \begin{cases} 1 - \frac{x}{X_L}(1-\rho_B), & x \leq X_L \\ \rho_B & x \geq X_L \end{cases} \tag{1.4}$$

where X_L and ρ_B are model parameters.

Theoretically, the piece-wise linear form as a spatial correlation function cannot result in the valid generation of random numbers satisfying any distance-based correlation matrix from layout. Theoretically valid forms of the spatial correlation function and a robust extraction method of the model parameters for the spatial correlation function were studied in [107]. A general family of spatial correlation functions is as follows,

$$\rho(v) = 2\left(\frac{bv}{2}\right)^{s-1} K_{s-1}(bv)\Gamma(s-1)^{-1}, \tag{1.5}$$

where K is the modified Bessel function of the second kind, Γ is the gamma function, b and s are fitting parameters that decide the shape of the correlation function, and v is the separation distance between the devices.

Miscellaneous Front-End Variation Sources

Historically, silicon dioxide film thickness is extremely tightly controlled in a thermal oxidation process. However, as the feature size and oxide thickness scaling has continued, the oxide thickness has reached an atomic-level scale, near 10Å, which corresponds to approximately five atomic layers of silicon dioxide. Physical limitations such as interface roughness and oxide layer non-uniformity lead to increased variability of the effective oxide thickness.

Variation in the oxide thickness can affect the electrical properties of the device such as the threshold voltage and carrier mobility. In particular, the gate leakage current of a thin film CMOS device by quantum-mechanical carrier tunneling through the gate oxide is exponentially sensitive to the dielectric thickness. Beyond the 65nm technology node, the gate leakage current is comparable to the sub-threshold leakage through the channel, and the variability in the gate leakage current is quickly becoming a growing source of circuit performance variation [24]. The impact of the oxide thickness variation on device electrical properties can be characterized by atomic-level 3D device simulation [7].

Electron mobility improvement by mechanical stress has been another driving force for device performance enhancement, in addition to feature size scaling. Shallow trench isolation (STI) is one dominant source of mechanical stress in a MOSFET channel. The mismatch in thermal expansion coefficients of different materials and the volume expansion of silicon dioxide cause the channel stress in the oxidation step that follows the formation of STI. The STI-induced stress and its impact on electron and hole mobility is highly dependent on the layout, in particular, on the size of the active area and the distance to the STI edge [81]. Therefore, the variability of the electrical characteristics of the devices by mechanical stress is highly systematic and layout-dependent.

1.2.2 Back End Variation

As CMOS technology scales, the contribution of interconnect parameters to the overall circuit performance becomes more important. Accurate modeling of parasitic capacitance and resistance of interconnect wires becomes essential to achieve accurate estimation of system performance. In particular, modeling the variation of the interconnect performance is critical to estimate the manufacturing yield of high performance digital and analog circuits. The recent survey in [79] shows that the overall time delay variation increases, and in particular, the portion of the within-die variation in the interconnect parameters becomes more significant.

Variation in the BEOL cluster of manufacturing causes the variability of the interconnect parameters. Modern sub-100nm process nodes provide more than 10 metal layers in their BEOL stacks. The BEOL flow consists of a repeated sequence of metal and dielectric layer deposition steps. After the deposition of a dielectric layer, photolithography and etching steps follow to build holes and trenches for vias and metal lines. After a thin barrier is deposited, electroplating fills the spaces for the vias and wires with copper. The electroplating leaves unwanted over-filled copper, and a chemical-mechanical polishing (CMP) step follows to remove the over-filled metal and planarize the surface for the following metallization.

In previous studies, CMP is found to be a critical source of systematic within-die variation in thickness of metal wires [71]. Figure 1-9 portrays the variation in thickness of metal wires by dishing and erosion after CMP, which is highly dependent on the feature size and pattern density of the layout. Pattern-dependency can also be observed in the CMP of dielectric materials for the planarization of shallow-trench isolation (STI) and inter-dielectric layers (ILDs). Physical understanding and a pattern-dependent fitting model of the dielectric CMP variation is provided in [106].

Furthermore, the topography of over-filled metal after electroplating is highly correlated to after-CMP topography, since the amount of excess metal impacts clearing time and degree of over-polish. The pattern-dependent variation of electroplating

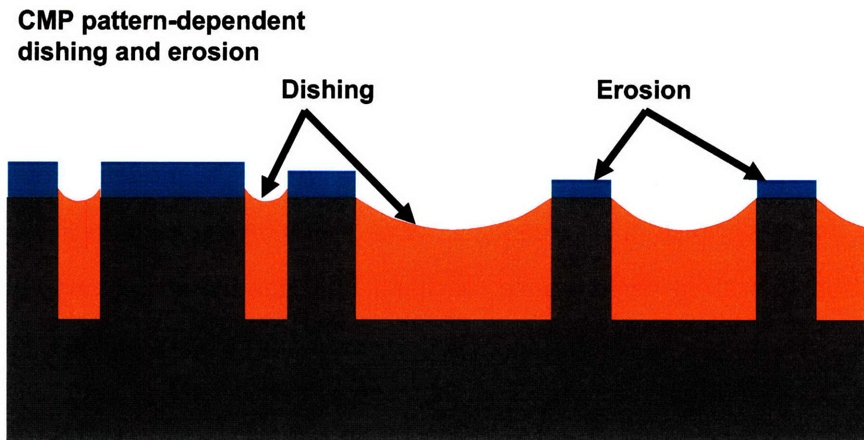


Figure 1-9: Pattern-dependent CMP variation of metal and oxide thickness in planarization steps.

topography and its impact on CMP was studied in [20]. To improve the planarity of the post-CMP surface, the pattern density of every metal layer in the layout must be regulated by strict design rule checks (DRCs) at the design stage. Insertion of CMP dummies improves the planarity significantly, but the parasitic capacitance added by the metal dummies must be considered in post-layout simulation for accurate performance estimation.

Since CMP variation is highly layout pattern-dependent, a significant portion of interconnect variation is systematic. Therefore, interconnect performance variation can be predicted using the pre-processing of interconnect parameters, such as parasitic resistance and capacitance, based on the CMP variation models. The impact of metal wire and ILD thickness variation on time delay was investigated in [72], where simulations with the CMP pre-processor showed 30% increase in the delay of $5mm$ bus lines due to copper CMP variation.

Corresponding with the scaling of device feature size, the physical dimensions of interconnect have been shrunk down as well, to fully exploit the increased density of active devices. The resistivity of contacts and vias becomes one of the critical factors in circuit performance, since the number of metal layers, contacts, and vias increases as the circuit complexity increases in the advanced process nodes. Open-failure in the contact and via is a common problem caused by defects. In recent

technologies, the parametric variation of the contact resistivity has become one of the important variation factors in circuit performance estimation, as shown in Figure 1-10. Efficient test structures must be introduced to characterize the statistical properties of the contact resistance variation and its layout-dependency in deeply scaled CMOS processes and the measured characteristics must be included in circuit simulation for better accuracy in interconnect modeling [19].

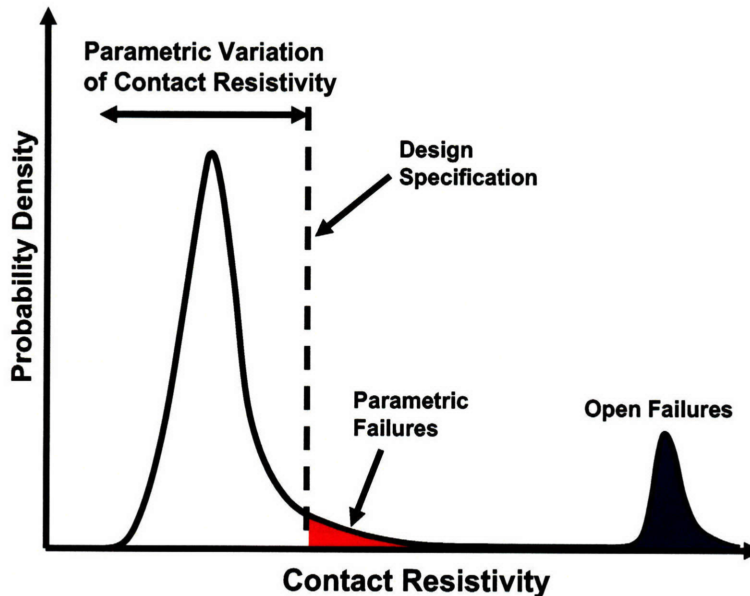


Figure 1-10: Variation of contact resistivity identifying parametric- and open- failure of contacts and vias.

1.2.3 Environmental Variation

Another aspect of IC statistical modeling is to include the effect of environmental parameters such as temperature and power supply voltages, which contribute significantly to circuit performance variability. The effect of supply voltage fluctuations can easily be modeled in circuit simulators (e.g., SPICE) since power sources are always explicitly defined in the circuit models. The modeling of temperature impact depends on the circuit simulator and device model used in the simulation. If a circuit simulator has a built-in temperature model, then temperature can be treated as one of the circuit parameters. Otherwise, an external temperature model has to be de-

fined in addition to the circuit simulator, to pre-calculate the simulation parameters influenced by temperature.

An empirical variation model of the delay, active power consumption, and stand-by leakage of a ring oscillator to power supply and temperature fluctuation is suggested and evaluated in [98]. While the delay and active power consumption are fairly linear to the power supply and temperature variation, the leakage power shows an exponential dependency on the environmental variations. Linear fitting of the frequency, active power variation, and log(leakage) of a seven-stage ring oscillator example and excellent fitting accuracy are shown in [81].

Typically, both supply voltage and temperature can be defined as independent random variables, which influence all components in a circuit. Thus temperature and supply voltages can be directly added to the group of variability factors in statistical circuit models [109]. However, while physical variability has random and systematic components, environmental variability is largely deterministic since it depends on the dynamic operation of circuit building blocks. Therefore, the study of environmental variation naturally focuses on the efficient prediction and bounding of the variation in work load, power consumption, and operating frequency of circuit building blocks.

As a dynamic compensation scheme for environmental variations, techniques such as frequency and power supply scaling, localized toggling, and migrating computation to different hardware units can be utilized for dynamic thermal management in multi-core microprocessor application [96].

1.3 Statistical Design of Analog Circuits

Process variation is certainly not a newfound issue in semiconductor manufacturing; it was a primary concern in the early days (1970's) of IC manufacturing [36] [84]. The relationship between the control of manufacturing steps and the variability of relevant transistor parameters was investigated, particularly to help guide the improvement in the control of the manufacturing conditions in order to reduce the fluctuation of critical circuit parameters.

Recently, process variation has drawn significant attention, resulting in a sharp increase in the number of publications in various circuit and computer-aided-design (CAD) conferences and journals. Process variation impact on the performance of circuits and micro-architectures, and mitigation methodologies for the variation impact, have been heavily discussed in many references (e.g., [16] and [15]). Compared to the process variation studies in the 1970's, today's variation research is typically focused on design-related issues: efficient characterization of variation parameters, development of variation models in critical circuit parameters, assessment of parametric yield at design time, and the statistical optimization of circuit performance.

In this section, we review parametric yield assessment techniques and variation-aware design methodologies to mitigate the variation impact and to improve the manufacturing yield.

1.3.1 Statistical Analysis of Performance Variation

Statistical circuit analysis requires both the characterization of the variability in device and interconnect behaviors, and the ability to translate the device and interconnect variability to circuit performance variability, i.e., statistical circuit simulation. Worst-case corner based circuit simulation and performance optimization have been the most commonly used method to achieve the robustness of analog circuit design [32]. The purpose of the corner-based analysis is to identify the corners in parameter space which corresponds to the worst circuit performance. The tolerance of circuit parameters are finite and bounded, and the simulations at each corner of the parameter space can estimate the boundary of the circuit performance space as shown in Figure 1-11.

The corner-based analysis leads circuit designers to a well-posed problem: meeting the performance specifications at every possible corner of active and passive component models. However, there are several practical issues that limit the usage of worst-case based design optimization.

- The worst-case design optimization often results in a pessimistic over-design.

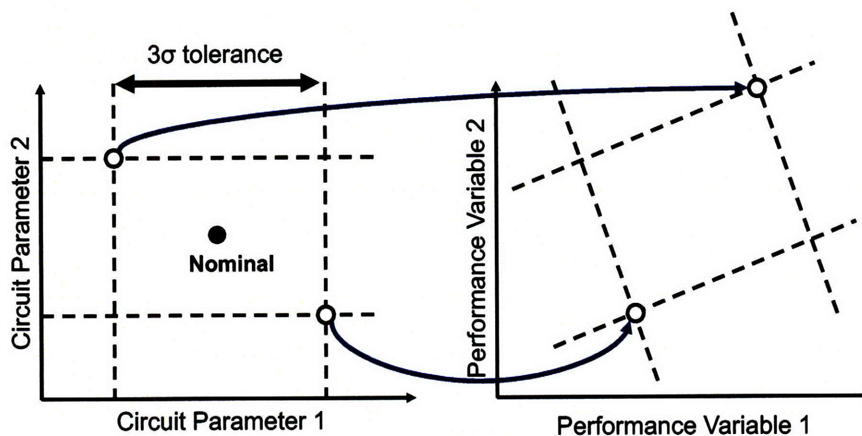


Figure 1-11: Worst case analysis of circuit performance based on the corners of circuit parameters. Corners may be based on statistical models, e.g. $\pm 3\sigma$ bound, or $\pm 1.5\sigma$ bounds as pictured here.

A subset of circuit parameters may be tightly correlated with each other since they are affected by the same manufacturing steps, and therefore, a subset of the variation corner have a negligible likelihood of occurrence in reality. The design optimization over all possible parameter corners can lead to the degradation of nominal circuit performance at more realistic corners, and the reduction of overall parametric yield.

- Computational cost of considering all possible parameter corners is too expensive. In particular, if the within-die variation of circuit components becomes a primary concern, the combinational increase in the number of parameter corners is exponential and it becomes impractical to consider all parameter corners for each circuit component.

- Non-linearity of circuit behavior cannot guarantee the one-to-one matching of circuit parameter space corners and performance space corners.

Alternatively, Monte Carlo analysis is commonly used for the characterization of the performance distribution, based on the given statistics of circuit parameters. In addition to a nominal parameter set of device and interconnect models (e.g., BSIM4), the additional variables for critical variation parameters are sampled from given statistics for each iteration of circuit simulation. The accuracy of the estimates from Monte

Carlo analysis depends on the number of iterations, since the confidence intervals of the estimates are a function of the number of Monte Carlo runs. Monte Carlo analysis captures the non-linearity of complex circuit behaviors and provides a realistic distribution of performance variables to determine the parametric yield in design stages.

Modern device and interconnect models include numerous parameters for fine-tuning of the models to match the measured hardware characteristics. As the number of model parameters increases, it becomes more difficult to consider the joint probability density function of the overall parameter set in Monte Carlo analysis. Principal component analysis is a commonly used technique to preserve the correlation between device and interconnect parameters while reducing the number of independent parameters by representing all the parameters as a linear combination of orthonormal principal components. For example, in [73], from the characterization data of 192 parameters of an individual test device, six principal components can be extracted to reduce the number of sampling variables significantly while explaining 96% of the variance and preserving the correlation in the entire parameter set.

Even though Monte Carlo analysis results in accurate estimates of performance variation, it is computationally expensive to repeat the circuit simulation a sufficient number of times to achieve accuracy in the statistical estimates. Recently, a number of alternative simulation methods have been proposed to achieve the accuracy of full Monte Carlo simulation while reducing the computational cost dramatically [64] [105]. Even though the methods show good error performance in digital logic simulation, it is difficult to explain the variation in complex analog circuits which have a number of non-linear performance variables.

A *response surface model* (RSM) is a commonly used functional approximation for the estimation of circuit performance to bypass the full circuit simulation in Monte Carlo analysis [17]. RSMs are constructed by computing the coefficients of linear or quadratic polynomials which represent the performance variables so as to minimize the mean-square errors at sampled simulation points. The number of the sampled evaluation points must be equal to or larger than the number of coefficients to obtain

a unique or approximated solution. Various methods to generate response surface models and the evaluation of model accuracy are described in [17].

The accuracy of the RSM-based yield estimation can be improved simply by using a higher order fitting model. In particular, when the variation ranges of the circuit parameters become large, the linear assumption of output variables over the circuit parameter range is no longer valid. By increasing the order of the RSM, the non-linearity of circuit behaviors can be captured to improve the fitting accuracy. A risk of over-fitting is an issue, potentially affecting the stability of model coefficient calculation in higher order model fitting.

Alternatively, the estimation accuracy of the RSM can be improved by understanding the underlying physical meaning of circuit parameters, and introducing translation variables between the circuit parameters and output variables. For example, as shown in Figure 1-12, when the underlying non-linear or discontinuous circuit behavior is known, conducting lower order RSM fitting to intermediate parameters and evaluating the output variables based on the translated intermediate parameters can improve both accuracy and stability of the model fitting. In Chapter 4, we show the accuracy enhancement for the RSM of current-mode logic (CML) buffer time delay and frequency divider performance by introducing intermediate variables which translate fundamental circuit parameters such as sheet resistance, threshold voltage, and channel length to physical time delay components.

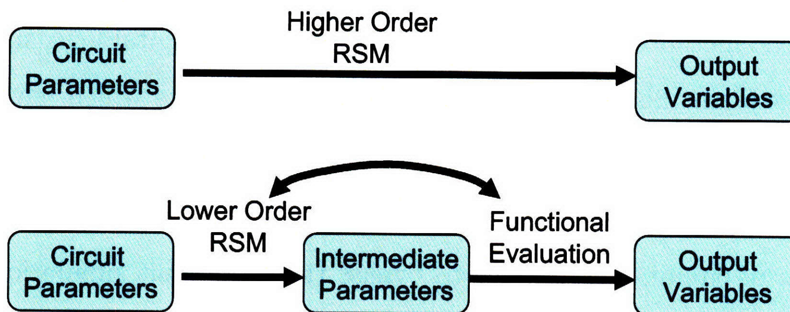


Figure 1-12: Improvement in a higher order RSM, through the translation of circuit parameters into intermediate parameters by understanding underlying physical circuit behaviors.

1.3.2 Variation-Aware Circuit Design

The goal of the analysis of variation impacts and yield estimation techniques is to maximize the parametric yield of digital and analog circuits by tuning design parameters appropriately. From the analysis of performance variation, circuit designers must have optimization strategies for minimizing the impact of parameter variation on the circuit performance and maximizing the yield. In this section, we summarize several trends in variation-aware design methodologies in analog circuits and large-scale micro-architectures: equation-based robust optimization, post-silicon tuning, and regular fabric design style.

The equation-based robust optimization proceeds by converting the yield optimization problem to a classical non-linear programming problem based on appropriate approximation of circuit behaviors to special functions [108]. A standard formulation of robust optimization problems can be as follows.

$$\begin{aligned} &\textbf{minimize } \sup_{u \in U} f_0(y,u) \\ &\textbf{subject to } \sup_{u \in U} f_i(y,u) \leq 0, \; i = 1, \ldots, m, \end{aligned} \tag{1.6}$$

where y is the design variable, u represents the variation variables, and the set U is a space describing the uncertainty of u. An optimization technique called *geometric programming* (GP) formulates the circuit behavior by *posynomial* functions whose general form is as follows [18]:

$$f(x) = \sum_{k=1}^{K} c_k x_1^{a_{1k}} x_2^{a_{2k}} \ldots x_n^{a_{nk}}, \tag{1.7}$$

where $c_k > 0$, $a_{ik} \in \mathbf{R}$, and $x_1, \ldots, x_n$ are real positive variables. It is known that GP-based problems can be solved efficiently and accurately due to recent optimization theory progress [46], and the robust optimization problem size based on GP grows linearly with the number of uncertainty parameters [108]. The equation-based robust optimization can find an optimal design point without scanning through the entire design space. However, the posynomial fitting error of non-linear performance vari-

ables for various analog circuits cab pose significant limitations on the optimization accuracy.

Post-silicon tuning techniques can be used to compensate for circuit performance variation after fabrication. Compensation of the variation in time delay and leakage power consumption of digital logic using adaptive body bias (ABB) voltage control was studied in [103]. Bidirectional ABB is used for both NMOS and PMOS devices to increase the percentage of dies that meet both frequency requirements and leakage constraints. The control of NMOS and PMOS body bias values individually for each die can reduce die-to-die frequency variations (σ/μ) by an order of magnitude, and 100% of the sampled dies are shown to become acceptable in meeting the clock frequency and leakage power specifications. Furthermore, a theoretical foundation for joint design-time and post-silicon optimization using adaptive body-bias control considering the variation of delay and leakage power in digital circuits was studied in [69]. The problem is cast as an adjustable robust linear program and solved in a computationally efficient way. Experimental results indicate that a designer can greatly benefit from the synergy of combining the design-time and post-silicon optimization techniques, due to the ability of post silicon optimization solutions to tune the circuit parameters to the realization of uncertain data which is not possible to know at design time.

Alternatively, it is widely recognized that physical regularity in layout improves the control of variability, and regularity in IC design has received extensive attention in recent years. In sub-100nm CMOS technologies, the design rule check (DRC) enforces regularity in layout by restricting the pattern density and routing direction of polysilicon gates and interconnect wires. Various forms of regular design styles have been proposed, including restrictive design rules, PLA-based fabrics, homogeneous gate-array-like fabrics, and heterogeneous regular fabrics [100]. One way to systematically enhance the design regularity is to implement ICs using a library of regular logic bricks. The advantage of the design style based on the regular logic bricks for the manufacturability of digital circuits has been studied in [86]. Micro-architecture design based on a pre-characterized brick library can provide not only the reduction

of the variability in speed and power consumption, but also more predictable performance distribution at the design stage by using the pre-characterized data. The trade-off between the improvement of parametric yield and design costs such as area, power, and complexity introduced by regularity must be investigated.

In this thesis, we specifically focus on variation characterization coupled with robust optimization methods for high performance analog circuits. We classify the robust optimization of analog circuits into two categories in Chapter 4: static and dynamic optimization. In the static optimization, design-time optimization in other words, designers optimize the design variables, such as device sizes and resistance and capacitance values, at the design stage to achieve a maximized estimated parametric yield. The static optimization assumes that the statistical properties of variation parameters (e.g., V_{TH}, ΔL, and R_{SH}) are given from the pre-characterization. Computational cost of statistical simulation (e.g., Monte Carlo) is the most serious issue in the static optimization strategy. To consider the complex behavior of process variation such as within-die variation and its spatial correlation in the yield estimation, there must be a sufficient number of iterations in Monte Carlo simulation. In particular, the number of performance variables in analog circuits is typically much larger than that of digital circuits, and thus yield estimation demands more Monte Carlo runs. Furthermore, since the variability of circuit-level parameters is dependent on the design variables, the distribution of the performance variation and parametric yield must be evaluated at each design point.

The dynamic or post-silicon optimization, on the other hand, finds tunable knobs in a creatively designed circuit to compensate for the performance variability after fabrication. Increasing the degree of freedom in output characteristic tuning involves additional circuit-level design techniques and feedback control issues. The dynamic optimization technique is highly dependent on circuit specifics, and each circuit needs a different strategy to tune output characteristics. For example, to improve the matching properties in differential pairs of circuit components, redundant design and proper selection mechanism that finds closely matched pairs can be introduced [65]. A power supply voltage, a reference current, and a bias voltage can be used as a

tunable knob for many analog circuits such as oscillators and amplifiers. However, since the performance variables of an analog circuit are tightly correlated with each other, the trade-off between the performance variables must be carefully considered in the dynamic optimization schemes.

1.4 Contributions and Organization of This Thesis

This thesis is organized as follows. Chapter 1 enumerates the sources of variation in VLSI manufacturing process, their impact on high-speed analog circuit performance. Statistical approaches for robust IC design including the statistical analysis of circuit performance variation and variation-aware design methodologies are shown in this chapter.

Chapter 2 describes the design issues in key mm-wave building blocks, the VCO and frequency divider, considering variability of circuit parameters to improve the manufacturability of PLL design. A 70GHz PLL front-end circuit consisting of the VCO and frequency divider has been implemented in a 65nm SOI CMOS technology. The device and circuit are optimized to provide sufficiently wide operating ranges of the PLL building blocks in a mm-wave frequency regime to improve manufacturability in the deeply scaled CMOS process.

Chapter 3 shows statistical measurement results of the mm-wave building blocks. The operating frequency and power consumption of PLL front-end circuits have been measured in an automated mm-wave measurement setup over 300mm wafers. We report individual performance variation characteristics of the VCO and frequency divider. Furthermore, a back propagation of variation (BPV) method to characterize the variation in important circuit parameters is presented based on the measurement data, and the statistical properties of the performance variation over multiple wafers are analyzed using a constrained principal component analysis (CPCA) to identify a dominant factor of the performance variation.

Chapter 4 analyzes the statistical properties of the VCO and frequency divider circuits and shows dynamic and static robust optimization approaches to achieve a

maximum parametric yield of the PLL front-end circuit. Statistical measurement results show that the frequency divider variation is the major concern for overall yield of the PLL front-end, and we provide analysis of the failure mechanism caused by process variation. The bias condition of the frequency divider can be dynamically tuned to change the operating range of the divider and maximize the yield of the PLL front-end, while satisfying output phase noise and power specifications.

Furthermore, we provide an empirical quadratic time-delay model based on physical time delay and frequency locking range components using DC circuit parameters, which shows excellent fitting accuracy to the maximum operating frequency variation over design migration and local parameter variation. Experimental results show that the parametric yield of the PLL front-end can be estimated over the entire design space in a reasonable amount of simulation time to achieve the optimum design point for the maximum yield.

Chapter 5 concludes this thesis and provides suggests for process variation research in mm-wave circuit design. In Appendix A, process variability of a high-speed ring-oscillator based VCO and statistical analysis of experimental results are discussed.

The primary contributions of this thesis can be summarized as follows.

- Design and implementation of a manufacturable VCO and a frequency divider operating up to 90GHz in CMOS technology.

- Measurement and analysis of manufacturing variation in VCO and frequency divider performance and power.

- Extraction of critical circuit parameters based on the statistical measurement results of the frequency divider at multiple bias conditions.

- Dynamic optimization of the VCO and frequency divider parametric yield by bias tuning of the frequency divider.

- Suggestion of a computationally efficient time delay model for the fast yield estimation of the PLL front-end and statistical optimization.

1.5 Summary

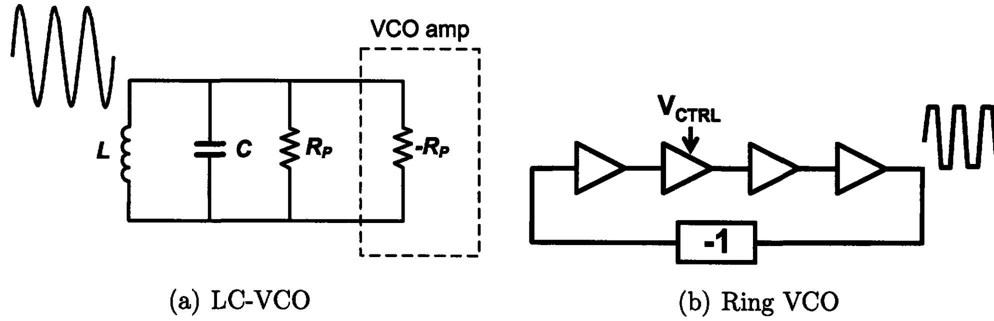
In this chapter, we introduced the process variability issues in high-speed analog circuit design. The operating frequency of CMOS applications has reached the mm-wave regime over 50GHz mainly by continuous scaling of the MOS transistor feature size. The aggressive scaling has introduced a parameter variability issue in digital and analog circuit design. Various manufacturing steps contribute to the variation of CMOS device and interconnect parameters and overall circuit performance. Therefore, a benchmarking task to characterize the performance level variation properties is strongly needed to provide useful guidelines for circuit designer to optimize the parametric yield of designs. To optimize the parametric performance yield, statistical design methodologies are used, whose goal is not only to meet the design specifications for nominal circuit performance, but also to achieve desired parametric yield despite the existence of parameter variation.

Chapter 2

Design of Manufacturable mm-Wave PLL Building Blocks

A PLL is an essential building block to generate a reference clock signal for most RF/mm-wave applications and micro-architectures [11]. The PLL needs a VCO and a frequency divider for local clock generation and output frequency leverage from an input reference frequency, respectively. Typically, in an integer-N PLL with a deep frequency division ratio greater than 1000, the frequency divider consists of a *pre-scaler* providing an initial divide-by-two function followed by a sub-divider for deep sub-division. Since the VCO and pre-scaler are operating at the highest frequency in the system, they draw significant design attention in order to meet the specifications of frequency operating range, phase noise, power consumption, and other requirements.

The operating frequency of a VCO achievable in CMOS has been continuously improved by the scaling of the device feature size. Generally, a designer has two choices for the implementation of the VCO, depending on required performance specifications: an LC-tank based VCO (LC-VCO) and a ring-oscillator based VCO (ring-VCO) as shown in Figure 2-1. The LC-VCO utilizes the resonance of an LC-tank with the cancellation of parasitic resistance by active devices for the oscillation frequency generation (Figure 2-1(a)). Since the LC-tank consists of passive components, the LC-VCO provides high operating frequency and low phase noise, which make the LC-VCO suitable for RF/mm-wave applications. However, the LC-VCO has a nar-



(a) LC-VCO

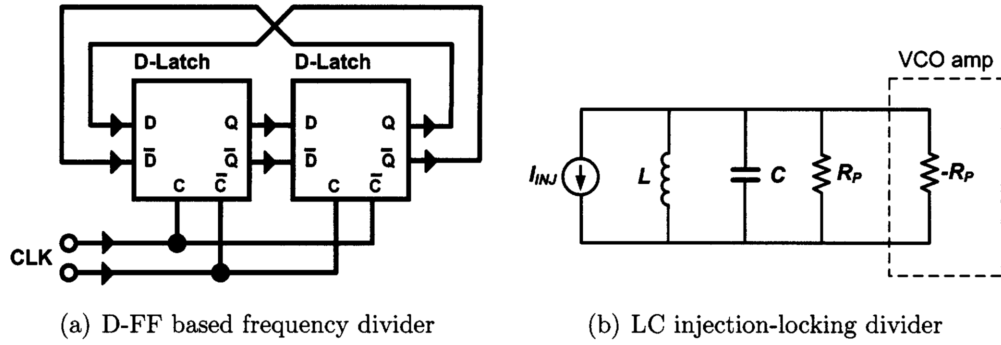
(b) Ring VCO

Figure 2-1: VCO structures

row frequency tuning range, large area for passives, and static power consumption as disadvantages.

The ring-VCO consists of a ring of variable delay stages with proper inversion as shown in Figure 2-1(b). Each delay stage can be implemented by a single-ended or differential inverter with load resistance or bias current control to change the time delay. Typically, the ring-VCO provides a wide frequency tuning range, a multi-phase output, small power and area consumption, and easy implementation. However, the main disadvantage of the ring-VCO is larger phase noise compared to the LC-VCO with the same power budget. Furthermore, the osciilation frequency and power consumption of the ring-VCO is highly sensitive to process variability of the devices, which is relatively much larger than that of the passive components in the LC-VCO. Appendix A shows the experimental results of a ring-VCO performance variation, including oscillation frequency, power consumption, and output phase noise, in a 90nm SOI CMOS technology. As a result, the ring-VCO is suitable for clock generation for digital logic and micro-processors, which have tight area and power budgets and loose phase noise specifications.

There are various design methodologies for the divide-by-two frequency divider implementation. The most commonly used topology is a master and slave latch based architecture as shown in Figure 2-2(a). From a digital circuit point of view, this structure operates as a flip-flop to change its state at a rising or falling edge of an input clock, to output half of the input clock frequency. For mm-wave frequency division, this structure can be used as a frequency divider based on an injection-locking ring



(a) D-FF based frequency divider (b) LC injection-locking divider

Figure 2-2: Frequency divider structures

oscillator to provide a wide frequency operating range and easy implementation. The detailed operation of this structure as an injection-locking ring oscillator is described in Section 2.3. Similarly, an LC-tank based injection locking oscillator can be used as a mm-wave frequency divider (Figure 2-2(b)). The output frequency of the LC-tank is locked to half of the frequency of an injected current source through the mixing behavior of active devices [59]. The pros and cons of the LC injection-locking frequency divider are similar to those of the LC-VCO: high and accurate frequency operating range with excellent phase noise performance but a narrow operating range with large area and power consumption.

In this chapter, we describe the design and analysis of a manufacturable mm-wave PLL front-end circuit implemented in 65nm SOI CMOS technology. The mm-wave PLL front-end consists of an LC-VCO, a 2:1 current-mode-logic (CML) frequency divider in a master and slave latch based architecture, and a cascoded buffer amplifier between the VCO and frequency divider as shown in Figure 2-3. One of the challenging issues in mm-wave CMOS VCO and frequency divider design is manufacturability; a wide VCO frequency tuning range (FTR) is required in order to cover the desired frequency range in the presence of process variation. In addition, the frequency operating range of the divider must be sufficiently wide for proper frequency division over the entire VCO tuning range. Conventionally, the frequency divider has a significant amount of performance variation since the circuit performance is based on the electrical properties of the CMOS devices with minimum feature size. Therefore, the frequency operating range variation of the divider circuit must be precisely

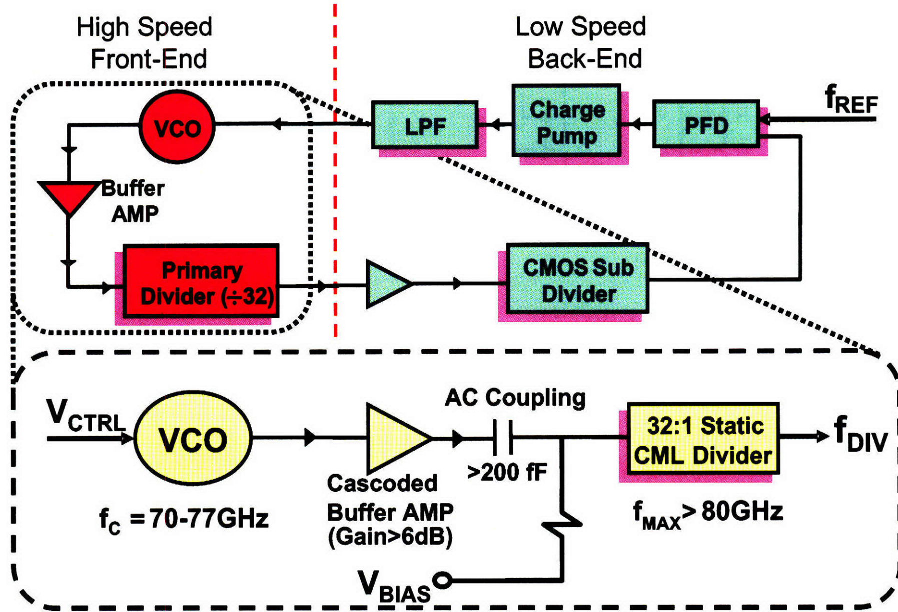


Figure 2-3: PLL high-speed front-end circuit consisting of a VCO, a frequency divider, and a buffer amplifier.

characterized and optimized during design.

Section 2.1 shows previous design examples of a mm-wave VCO and frequency divider and their output characteristics. Section 2.2 and 2.3 describe design details of the mm-wave VCO and frequency divider examined in this work. Section 2.4 depicts the actual implementation of the VCO and frequency divider test vehicles in a 65nm CMOS technology.

2.1 Previous Work on mm-Wave VCO and Frequency Divider

High frequency VCOs and frequency dividers are essential building blocks for most mm-wave applications. Typically, SiGe and III-V technologies have been appropriate selections for the implementation of VCOs and frequency dividers operating above 50GHz frequency [62] [104]. However, as the minimum feature size of CMOS devices has shrunk down below 100nm, VCOs and frequency dividers operating at over

50GHz have been reported in CMOS technologies. Here, we review several design examples of mm-wave CMOS LC-VCOs and frequency dividers and discuss their output characteristics in terms of frequency operating ranges, which are important from a process variability perspective.

The output frequency of an LC-VCO is mainly determined by the resonance frequency of the LC-tank, and therefore, a mm-wave output frequency is still achievable by precise design of passive components without using sub-100nm technologies. However, to obtain a reasonable frequency tuning range, the parasitic capacitance in active devices must be minimized since the frequency tuning range is determined by the ratio between the varactor capacitance tuning range and the lumped capacitance at the VCO output nodes. In [99], Tiebout et al. reported a 1V 51GHz VCO in a 0.12μm bulk CMOS technology with low-k dielectric. The area of the VCO circuit was minimized to reduce the parasitic capacitance and to constrain the component dimensions well below the wavelength of a 50GHz signal (6mm) so that the lumped model assumptions are valid. An excellent power consumption of 1mW was achieved, while the frequency tuning range is from 50.89 to 51.64GHz at $I_{TAIL} = 1mA$, resulting in an FTR of only 1.46%.

A 63GHz VCO was implemented in a 0.25μm CMOS technology in [68] by Liu et al. A push-push cross-coupled topology was employed to achieve high frequency operation, high output power, and good phase noise. Coplanar waveguides and asymmetrical coplanar strips were used to reduce substrate loss, which results in the degradation of the inductor Q. A MOS varactor is used for frequency tuning. Due to the limitation by the parasitic capacitance at output nodes, the achieved FTR of 2.5GHz (3.97%) is still very small.

A 40GHz CMOS VCO in a 90nm SOI CMOS technology was reported in [37] by Fong et al. This LC-VCO employed a complementary topology for phase noise improvement and power consumption reduction. The VCO used an accumulation-mode MOS varactor for a wide capacitance tuning ratio, and a single-loop copper inductor with high-Q to achieve good phase noise. The measured FTR of this VCO is 15.8% (from 34.9 to 40.9GHz), which provided excellent manufacturability for commercial

production. The VCO in this thesis inherited key design features of this VCO to achieve 77GHz center frequency with a wide FTR and reasonably good phase noise in a 65nm SOI CMOS technology.

For the sound joint operation of the VCO and frequency divider, the frequency operating range of the frequency divider must fully cover the frequency tuning range of the VCO with sufficient margin. To accommodate the increase of the system operating frequency, the requirement of the maximum operating frequency for the frequency divider becomes extremely high in mm-wave applications. Furthermore, as the operating frequency increases, the attenuation of the input signal from the VCO to the frequency divider becomes worse, and the operating range of the divider become narrower due to the reduced input signal power. The reduced operating range of the frequency divider quickly becomes a serious issue for manufacturability in commercial production.

Typically, an LC-resonator based injection-locking frequency divider (LC-ILFD) is used to achieve a high operating frequency [89]. However, the locking range of the LC-ILFD is generally narrow, and the limited operating range causes a parametric yield loss by process and environmental variations. On the other hand, a tail-injection ring oscillator-based ILFD (ring-ILFD) has a wider locking range, occupies smaller chip area, and has lower power consumption [74]. Here, we introduce several design examples of both LC-ILFDs and ring-ILFDs operating at multi-gigahertz range in CMOS technologies.

A 40GHz regenerative divider with an operating range of 2.3GHz (5.75%) was implemented in 0.18μm CMOS by Lee et al. in [59]. The frequency divider uses a Miller divider scheme with inductive peaking, which provided both high frequency operation and wider locking range compared to a conventional injection-locking frequency divider.

A CML frequency divider with static architecture was implemented in 0.12μm and 90nm SOI CMOS technologies in [88] and [87], respectively. Even though the divider employed a static divider architecture, the bias condition and load resistance values were configured to generate a self-oscillation frequency without an input signal.

At around twice the frequency of the self-oscillation signal, the divider operates as a ring-oscillation based ILFD. Because of the multiple injection sources of an input signal, the ring-oscillation based ILFD provides a wide frequency locking range compared to the LC-resonator based ILFD. The detailed analysis of the locking range characteristics of the ring-oscillator based ILFD is presented in [75].

2.2 Design of mm-Wave Voltage Controlled Oscillator

Achieving both high frequency operation and a wide frequency tuning range are difficult challenges in mm-wave VCO design. In general, it is desirable for the resonator to include a large multi-turn inductor for better Q to achieve better phase noise performance, and a large varactor with high C_{max}/C_{min} ratio for a wider frequency tuning range. The frequency tuning range (FTR) of an LC-VCO is proportional to a capacitance tuning range of the LC-tank. The capacitance tuning range (CTR) can be defined using the varactor capacitance and fixed parasitic capacitance at output nodes as follows [38]:

$$\mathrm{FTR} \propto \mathrm{CTR} = \frac{C_{v,max} + C_{fix}}{C_{v,min} + C_{fix}}, \tag{2.1}$$

where C_v is the varactor capacitance and C_{fix} is the fixed parasitic capacitance.

However, at high frequency as in the mm-wave regime, both inductance L and varactor capacitance C_v in the resonator are limited to small values, because the oscillation frequency f_O is determined by

$$f_O = \frac{1}{2\pi\sqrt{L(C_v + \Delta C)}} \tag{2.2}$$

where ΔC is the change in capacitance achievable by varactor tuning. When the center frequency $f_{O,\mathrm{C}}$ (ΔC=0) is fixed, L must be minimized to achieve a large frequency tuning range since the capacitance tuning range increases monotonically as C_v increases. However, to reduce output phase noise, L must be maximized to

achieve a high Q of the inductor, since the quality factor of the inductor dominates the overall quality factor of the LC tank. This imposes a design trade-off between frequency tuning range and phase noise.

The VCO design in this work focuses on achieving a wide frequency tuning range for improved manufacturability against process variation. Several circuit components are employed to improve the frequency tuning range.

- A large accumulation-mode MOS (AMOS) varactor with a good C_{max}/C_{min} ratio and Q.
- Relaxed pitch SOI transistors to reduce parasitic capacitance (C_{fix}) by 30% compared with normal pitch bulk CMOS devices.
- A single-turn top-level-only inductor achieving small inductance with high Q.

Figure 2-4 shows the schematic diagram of the LC-tank based VCO used in this work. The VCO circuit employs a complementary design to achieve the wide FTR and power reduction. It has a symmetric complementary negative g_m (NFET for M_1 and M_2, and PFET for M_3 and M_4), and an LC tank with a C-shape inductor L and AMOS varactors M_7 and M_8. The VCO outputs V_{OUT+} and V_{OUT-} are buffered by source followers M_5 and M_6. The oscillating output node of the LC-VCO is DC-biased at around half of V_{DD} by proper sizing of the PFET and NFET. This biasing provides maximum capacitance tuning range to the AMOS whose capacitance is controlled by the voltage between V_{CTRL} and the biased output nodes. V_{CTRL} can be changed from zero to V_{DD} to fully tune the AMOS capacitance.

In this VCO, we use SOI CMOS devices which have lower parasitic diffusion-to-substrate capacitance due to buried oxide layer isolation. The transistors are multi-fingered, and the gate pitch of the fingers are stretched to enhance carrier mobility and to reduce parasitic capacitance between gate and source (drain) terminals. The reduced parasitic capacitance at output nodes obtained by using the relaxed pitch SOI CMOS devices provides a large capacitance tuning range for the LC-tank, and as a result, a wide frequency tuning range of the VCO is achievable.

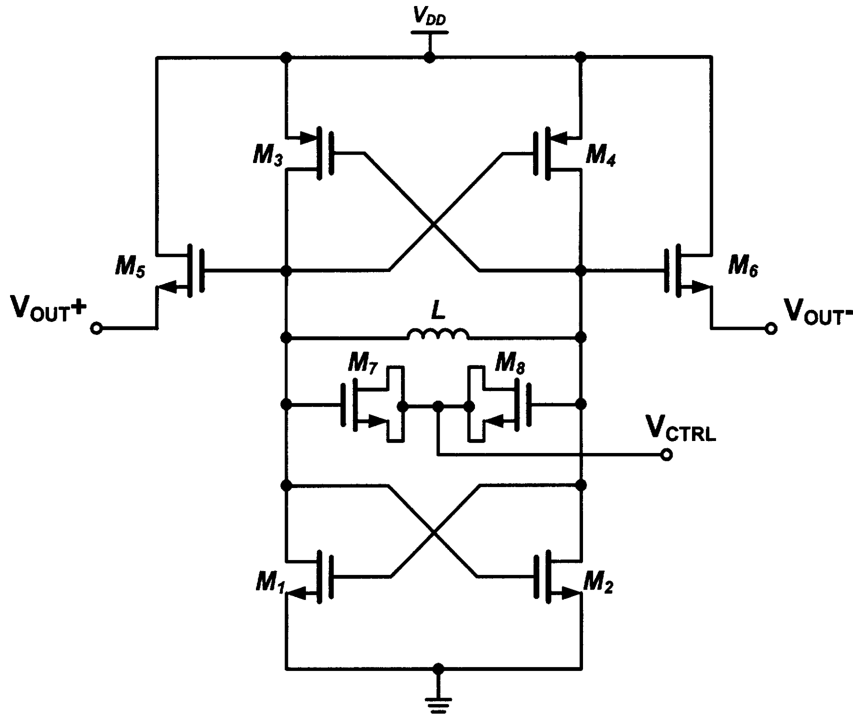


Figure 2-4: Schematic of complementary LC-VCO design using an AMOS varactor (M_7 and M_8) and a C-shape inductor (L).

The use of a small inductor allows larger varactors for wider capacitance tuning. The smaller size inductor also results in lower substrate capacitance due to smaller physical area. A single-turn structure in this VCO eliminates inter-winding capacitance. The inductor has been implemented in a 1.2μm thick copper top-level metal layer to reduce parasitic capacitance to substrate, and to achieve highest possible Q in this CMOS technology.

However, since the skin depth of copper at 80GHz is 0.16μm which is more than six times thinner than the top metal layer, the resistance of the inductor is likely to be decided by the skin depth. Stacking lower level metals reduces substrate isolation without improving series resistance due to the skin effect, and hence would also degrade the Q of the inductor. The degraded Q by the skin effect limits the phase noise performance of the VCO in mm-wave operation.

While the wide capacitance tuning range of the AMOS is achievable by using PFETs for proper biasing, the PFETs contribute additional parasitic capacitance to

output nodes, lowering the maximum attainable oscillation frequency. However, the complementary design using PFETs consumes less power and provides better phase noise compared to a design using cross-coupled NFETs with inductive loads [44].

2.3 Design of mm-Wave Frequency Divider

Achieving both high frequency division and a wide frequency operating range of the frequency divider requires proper selection of divider architecture, device-level optimization, and circuit parameter tuning. An injection-locking frequency divider (ILFD) is the most commonly used architecture for mm-wave frequency division. Conventionally, the injection-locking mechanism is based on either an LC oscillator or ring oscillator depending on system requirements. The LC-ILFD provides higher frequency operation compared to the ring-ILFD by using the resonant frequency of an LC-tank. The ring-ILFD has an advantage in frequency operating range since the locking range of the ring-ILFD is much wider than that of the LC-ILFD within the same power budget.

By using a 65nm SOI CMOS technology whose NFET cut-off frequency is more than 300GHz, mm-wave frequency division over 50GHz is achievable in a ring-ILFD architecture. A wide operating range of the ring-ILFD is beneficial for improving the manufacturability of the divider against process variation. In this work, we employ a ring-ILFD as the 90GHz frequency divider. The ring-ILFD can be implemented using a conventional D-FF architecture with variety of features for speed enhancement. The detailed description of the divider architecture and analysis of divider behavior are in following sections.

2.3.1 CML Based D-FF Architecture

The 2:1 frequency divider in this work uses a master and slave latch architecture to construct the D-FF, as shown in Figure 2-5. From a digital circuit point of view, the D-FF is toggled at a rising or falling edge of an input clock to output half of the input clock frequency. The maximum operating frequency is determined mainly by the load

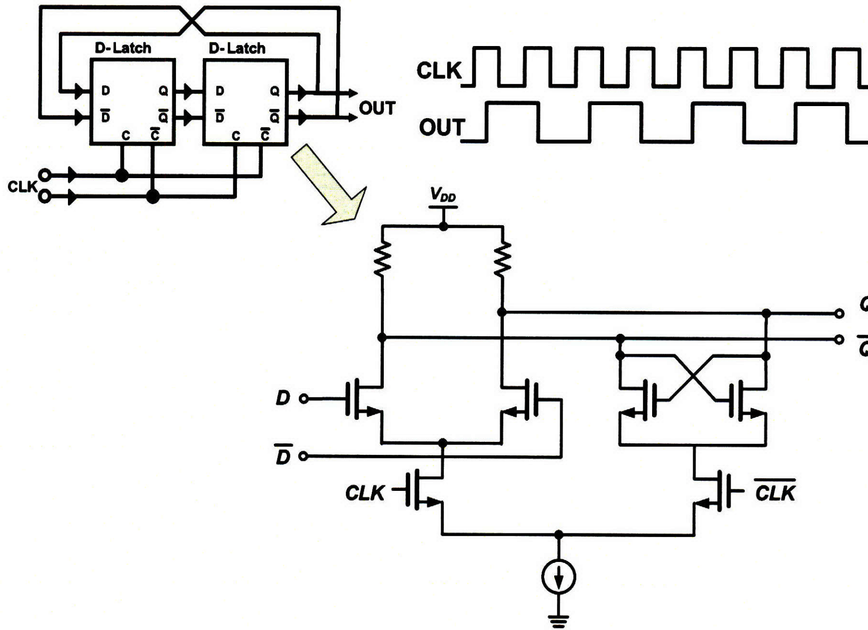


Figure 2-5: Divide-by-two using a D-FF based on CML latches

capacitance at output nodes and their driving currents. To achieve faster operation, a current-mode-logic (CML) latch is employed. A CML circuit uses resistor loads instead of conventional PMOS loads, or the polysilicon resistor loads provide smaller parasitic capacitance for high-speed operation compared to PMOS loads. Additional speed benefits can be obtained by using shunt inductive peaking at output nodes of CML circuits.

Figure 2-6 shows a schematic diagram of the mm-wave CMOS frequency divider used in this work. The bottom transistors (M_9 to M_{12}) are sized to 20μm to drive up to 20mA bias and dynamic currents, and to satisfy reliability requirements. The transistors for differential pairs (M_1, M_2, M_5, and M_6) are sized to 10μm to obtain an appropriate g_m for the desired frequency range. The size of the latch transistors (M_3, M_4, M_7, and M_8) is reduced to 8μm to decrease capacitive loading at output nodes while satisfying the self-oscillation condition given by Equation (2.3) with 230 Ω unsilicided polysilicon resistors [95]:

$$g_{m,L} \cdot R_L > 1, \tag{2.3}$$

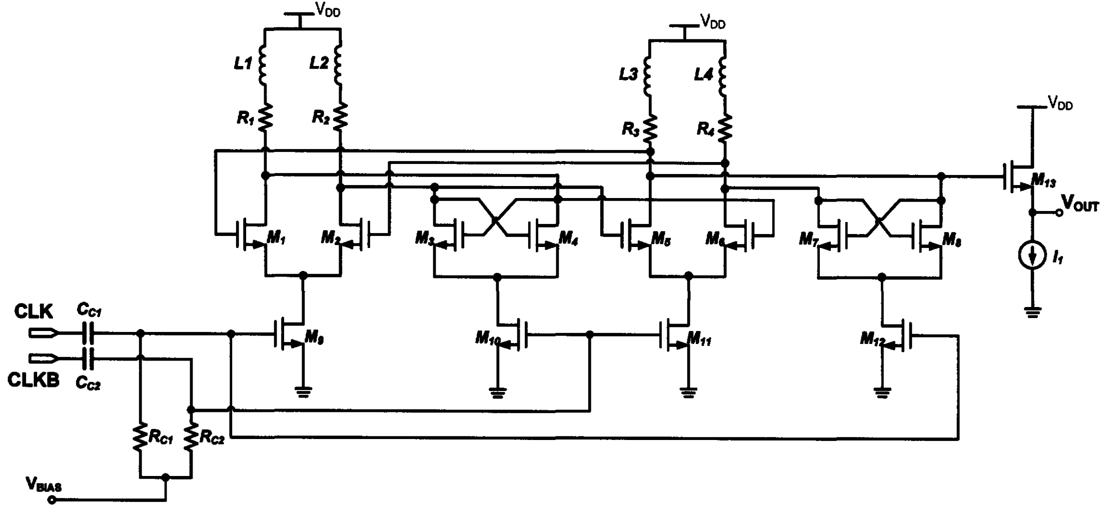


Figure 2-6: Schematic of the 90GHz frequency divider based on a static CML architecture.

where $g_{m,L}$ is the transconductance of the latch devices, and R_L is the resistance of the output loads. Together, these circuit and technology enhancements enable exceptionally high speed operation of the frequency divider up to 90GHz.

A cascoded amplifier with 100 Ω poly resistor loads is inserted as a buffer between the VCO and the frequency divider. A 200fF state-of-the-art vertical-natural-capacitor (VNCAP) is used for AC coupling of the VCO output signals to divider inputs. The VNCAP provides large capacitance density and highly symmetric configuration suitable for RF applications [25]. The buffer amplifier isolates the VCO output from large capacitive output loading including VNCAP parasitic capacitance to substrate (~20fF) and divider input capacitance (~10fF), and provides a gain of four at the VCO center frequency for power loss compensation.

The on-chip AC coupling by the VNCAP enables V_{BIAS} to be controlled externally to change the bias currents in the CML latches and tune the operating range and output signal swing of the frequency divider. We show the advantage of tuning the operating range by the V_{BIAS} control in Chapter 4.

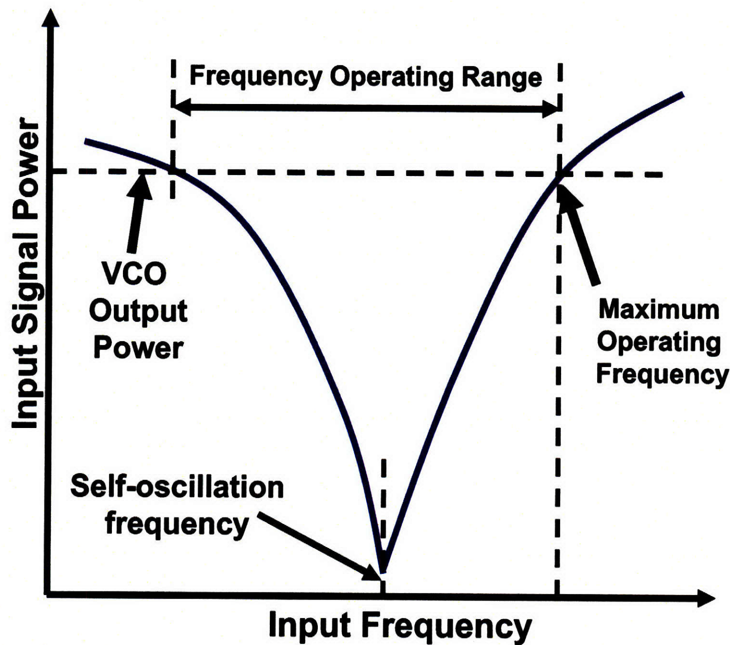


Figure 2-7: Input sensitivity curve of a frequency divider indicating self-oscillation frequency and maximum operating frequency for a given input signal power requirement as set by the available VCO output power.

2.3.2 Analysis of Self-Oscillation Frequency and Locking Range

The performance of a frequency divider can be fully characterized by measuring an input sensitivity curve as shown in Figure 2-7. At a certain input frequency of the divider, the corresponding point of the sensitivity curve indicates the minimum required power of an input signal to lock the divider output to the desired frequency (half of the input frequency). An injection-locking frequency divider generates a natural frequency, or self-oscillation frequency (f_{SO}), when there is no injected input signal. When the offset between the input frequency and $2 \cdot f_{SO}$ increases, the minimum required input signal to overcome the natural frequency of the circuit and drive to the desired output frequency also increases. As a result, the input sensitivity curve becomes V-shaped, and the bottom of the V-shape curve indicates $2 \cdot f_{SO}$. When the input signal power is fixed or specified, the minimum and maximum operating frequencies of the divider can be characterized by the input sensitivity curve as in Figure 2-7.

To set the frequency operating range of the frequency divider to a desired region, an analytic form of the self-oscillation frequency is strongly needed. When the input of the divider is tied to DC, a properly biased CML divider generates the self-oscillation frequency by constructing a four stage oscillation loop. In Figure 2-8, clock inputs are tied to ground and each device is approximated as a linear element based on a small signal assumption. Each stage consists of a transconductance component (g_{mD}), load resistance (R_L), output capacitance (C_P), and negative resistance ($-1/g_{mL}$) by the latch device. To satisfy Barkhausen's criterion for oscillation, the loop gain must be unity with 360 degree phase shift, and therefore, each delay stage must provide a 90 degree phase shift, assuming that all stages are identical. To result in 90 degree phase shift at each stage, the negative resistance must effectively cancel out the load resistance, and the output load impedance must become purely capacitive. Utilizing the oscillation condition, a first-order estimate of the self-oscillation frequency ω_{SO} is as follows.

$$\omega_{SO} = \sqrt[4]{\frac{g_{m1}g_{m2}g_{m3}g_{m4}}{C_{p1}C_{p2}C_{p3}C_{p4}}} \approx \frac{1}{R_L C_P} \cdot \frac{g_{mD}}{g_{mL}} \tag{2.4}$$

In Equation (2.4), g_{mi} is a transconductance of each differential pair, and C_{pi} is the lumped capacitance at each output node. The impact of mismatch in differential pairs on the self-oscillation frequency is reduced by averaging. By assuming that mismatch between stages is negligible, the self-oscillation frequency can be approximated as a function of effective load resistance R_L, lumped output capacitance C_P, and the ratio between transconductance of differential pair and latch devices g_{mD}/g_{mL} as in Equation (2.4).

The calculation of the self-oscillation frequency above is based on a small-signal and linear assumption. However, when the output signal swing becomes large as I_{TAIL} increases, the output signal starts to be rectified at V_{DD} and $V_{DD} - I_{TAIL} \cdot R_L$, and the linear assumption does not hold anymore. In transitions, the output capacitor is charged up through the load resistor R_L and the transition time is is largely governed by $R_L \cdot C_P$ delay. Therefore, the self-oscillation frequency is highly dependent on the circuit parameters I_{TAIL}, g_m/C_p, and $R_L \cdot C_P$, and their relationship is non-linear and

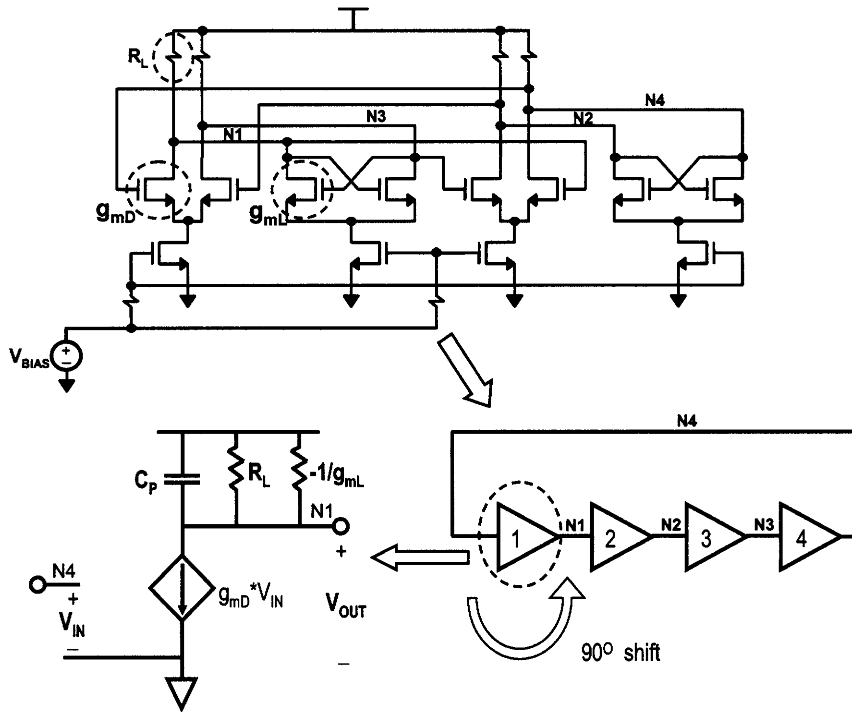


Figure 2-8: Small signal analysis of the static frequency divider in the self-oscillation mode

complex. In Section 4.3.1, we suggest a quadratic response surface model based on the parameters above to predict the self-oscillation frequency of the divider at each design point and bias condition.

The CML frequency divider operates as a free-running ring oscillator in the self-oscillation mode. When an external oscillating signal is injected into the self-oscillating loop, injection pulling and locking phenomena occur to change the oscillation frequency of the loop, which has become strongly correlated with the injected frequency depending on the signal power of the injection signal [4]. The injection locking scheme becomes the most commonly used frequency division technique in mm-wave frequency generation, due to its high frequency capability.

Figure 2-9 explains how an injection-locking oscillator works as a frequency divider. When there is no injection signal, the loop is in a steady-state satisfying Barkhausen's oscillation condition at ω_O. When an external signal is injected through the mixer, the loop oscillation frequency changes depending on the power of the in-

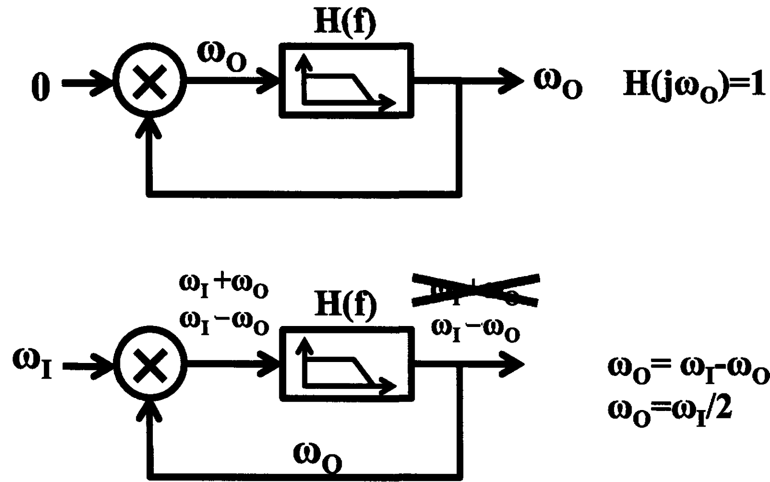


Figure 2-9: Behavioral model of the injection locking oscillator with frequency injection through a mixer.

jected signal. A weak injection signal pulls the loop oscillation without locking it. A pulled but unlocked oscillator traces a rich set of dynamics, which are of theoretical interest but of little practical consequence [75]. The oscillation loop settles at a different steady-state when the injection signal is sufficiently large to lock the loop. The output frequency of the mixer is both the sum and difference of the injected and locked output frequencies. Through a low-pass filter $H(jf)$, the higher frequency term $(\omega_O + \omega_I)$ is eliminated, and the locked output frequency is equal to the difference $\omega_O - \omega_I$, and as a result, the locked output frequency becomes half of the injected signal frequency.

The frequency locking range (FLR) ω_L of the injection locking divider is the maximum frequency offset of the injected input frequency ω_I from $2 \cdot \omega_{SO}$, that continues to lock the divider output at half of the injected frequency for a given injected input power. The FLR is an important characteristic since it determines the maximum and minimum operating frequencies of the divider. Typically, ω_L must be greater than three or four times of the frequency tuning range of the VCO to guarantee the robustness of the VCO-divider operation considering process and environmental variations.

The FLR of both LC-ILFD and ring-ILFD architecture has been intensively stud-

ied in many references (e.g., [75], [90], [92], and [13]), as the injection locking divider has become more important as a feasible solution of mm-wave frequency division in CMOS technologies. A general analytic form of ω_L was suggested in [92] and [13] as follows:

$$\omega_L \approx k \cdot \frac{\omega_{SO}}{2Q} \cdot \frac{I_{INJ}}{I_{OSC}}. \tag{2.5}$$

In Equation (2.5), Q is the quality factor of the oscillation loop, I_{INJ} is the peak value of the injection current, I_{OSC} is the peak value of the self-oscillation current (equal to the bias current I_{TAIL}), and k is a constant depending on circuit configuration. For an LC-tank based injection-locking divider, Q is the quality factor of the LC-resonant tank. In an injection-locking ring oscillator, Q is the slope of the phase versus frequency characteristic of the loop transfer function $H(f)$ in Figure 2-9, as follows:

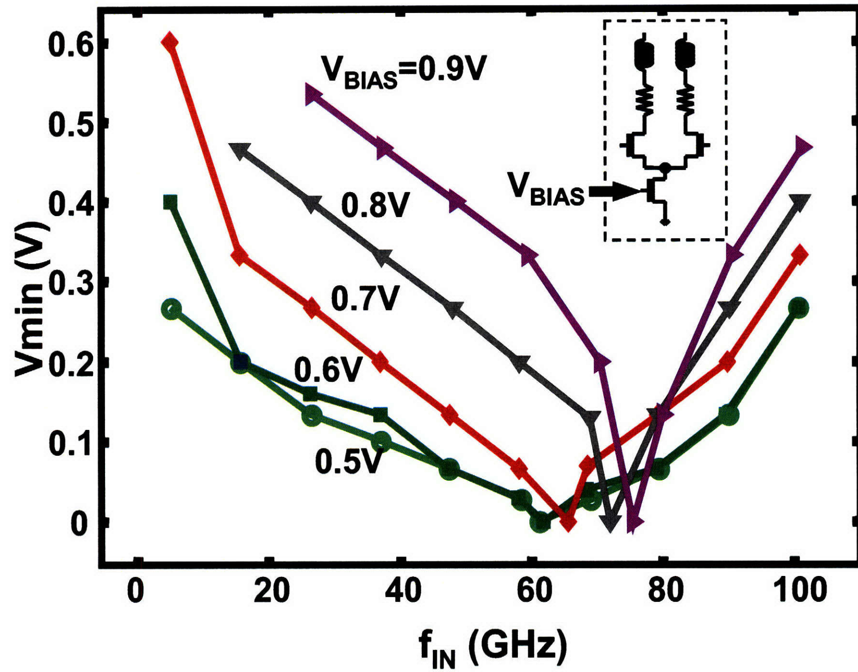
$$Q = \frac{d\measuredangle H(j\omega)}{d\omega}\Big|_{\omega=\omega_{SO}} \tag{2.6}$$

Since ω_L is inversely proportional to the quality factor Q, the LC-tank based injection-locking divider has much narrower FLR compared to the injection-locking ring oscillator that has a lower Q.

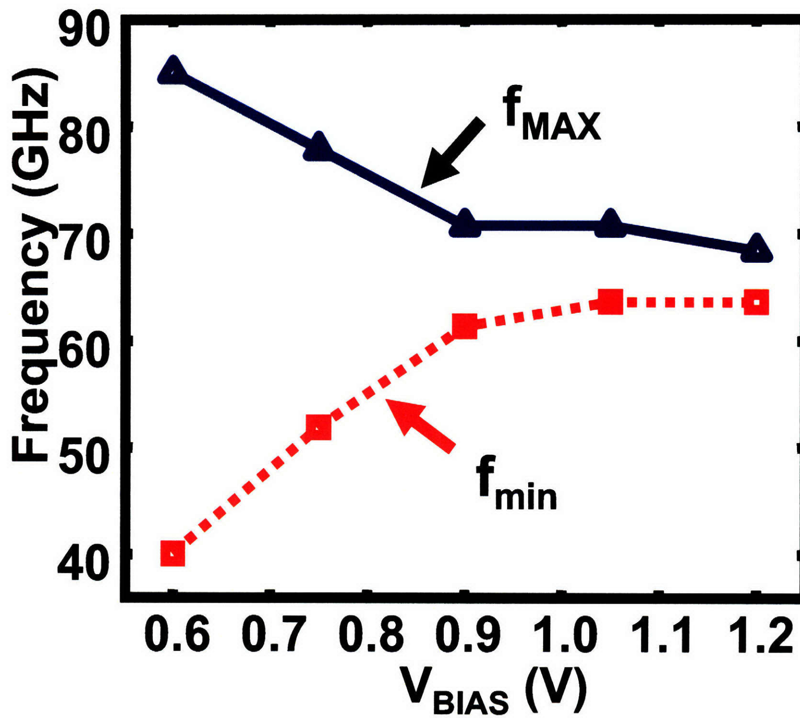
From Equation (2.4), the self-oscillation frequency is proportional to the transconductance of differential pair devices, which is proportional to $\sqrt{I_{TAIL}}$. From Equation (2.5), ω_L is roughly proportional to $1/\sqrt{I_{TAIL}}$, and therefore, a larger bias current results in the reduction of the locking range of the divider while increasing the self-oscillation frequency.

In Figure 2-10, the simulated operating ranges of the frequency divider at varying V_{BIAS} voltage from 0.5 to 0.9V shows that the divider operating range is highly sensitive to V_{BIAS}. Figure 2-10(a) shows the change in sensitivity curves as V_{BIAS} changes. Figure 2-10(b) highlights that increasing V_{BIAS} reduces the maximum operating frequency of the divider for a given input signal power. As a result, the frequency operating range of the divider can be externally tuned dynamically by V_{BIAS}. This tunability is used to compensate for the performance variation of the divider.

On the other hand, the output voltage swing V_{SW} of the divider is proportional



(a) Sensitivity curves



(b) Frequency operating range

Figure 2-10: Simulation results of the divider frequency operating ranges at different V_{BIAS} conditions.

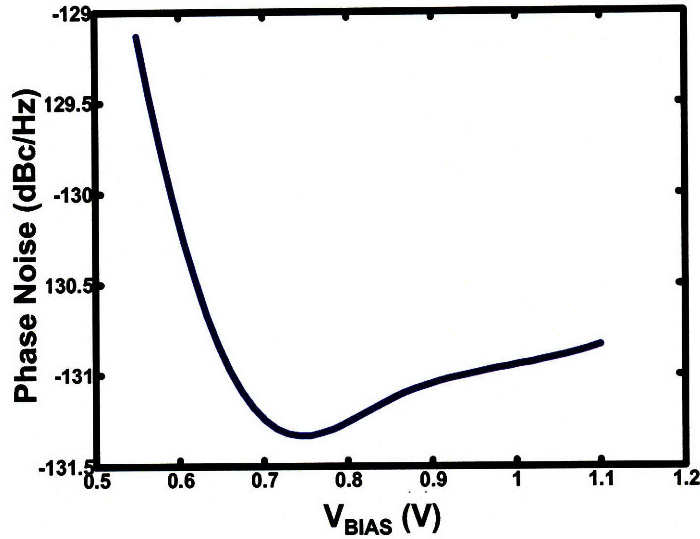


Figure 2-11: Simulated phase noise of the divided output signal at different bias conditions.

to I_{TAIL}, and for better signal-to-noise ratio (SNR) of the frequency divider output, a larger V_{SW} is preferred. Therefore, there is a trade-off between the operating range and the noise characteristic of the CML frequency divider. The bias condition (V_{BIAS}) can be optimized based on the specific requirements of phase noise. Figure 2-11 shows the change of the simulated output phase noise of the frequency divider over a sweep of V_{BIAS}. The output phase noise decreases as V_{BIAS} increases when the devices whose gates are connected to the clock input are in saturation. Beyond the boundary of saturation and triode regions of the clock devices, the phase noise starts to degrade, since the drain to source resistance of the clock devices becomes finite and the drain current noise of the differential pair and latch devices starts to appear in output signals. This characteristic provides a clear boundary of the phase noise enhancement achievable by V_{BIAS} increase, and is to be used as an optimization constraint in dynamic and static optimization of the circuit yield in Chapter 4.

2.4 Implementation of PLL Front-End Circuit

Test vehicles of the mm-wave PLL front-end circuit are implemented in 65nm SOI CMOS technology. Figure 2-12 shows the cross-sectional diagram of the SOI CMOS

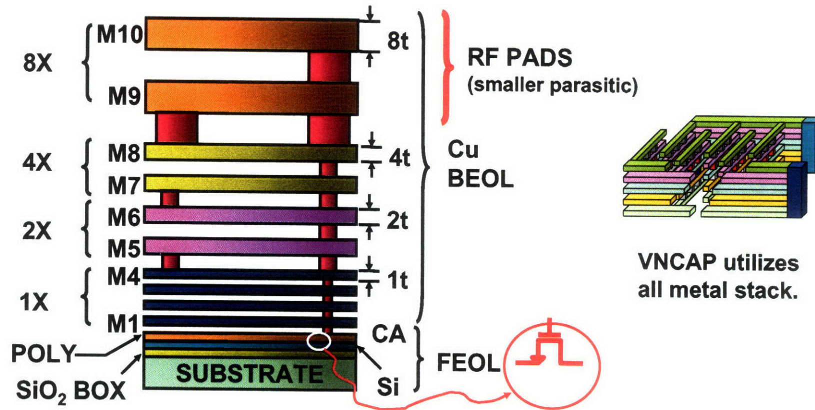


Figure 2-12: Cross sectional diagram of 65nm SOI CMOS technology with 10 metal layers. The technology provides a Vertical Natural Capacitor (VNCAP) for high-capacitance density and symmetric characteristic.

technology used in this work. Compared to bulk CMOS, FETs in SOI CMOS technology have lower parasitic diffusion-to-substrate capacitance due to buried oxide layer isolation. The reduced parasitic capacitance is advantageous for both VCO and frequency divider design to achieve high operating frequencies [54]. The technology has 10 metal layers, and the top metal layer is eight times thicker than M1 and M2 metal layers, which is suitable for the implementation of high-Q inductors and high frequency pads.

Figure 2-13 shows the layout and die photo of the frequency divider circuit. The placement of the ten transistors is optimized to minimize the area of metal wires to reduce the parasitic capacitance to substrate. Calculation from technology information shows that the interconnection through the top metal layer provides the optimum RC delay even though it adds parasitic resistance and capacitance from the vias though the metal stack. The shunt-peaking inductors are implemented using 300μm interconnect wires working as slab inductors by way of eddy current, to provide 330pH inductance for bandwidth enhancement.

We have three different vehicles for testing the frequency divider as listed in Table 2.1. DIV_1 has an initial layout with optimized devices sizes and relaxed placement and routing. DIV_2 has the same device sizing, and the area of interconnect wires is minimized to reduce wiring capacitance. On top of the DIV_2 layout, DIV_3 has 300

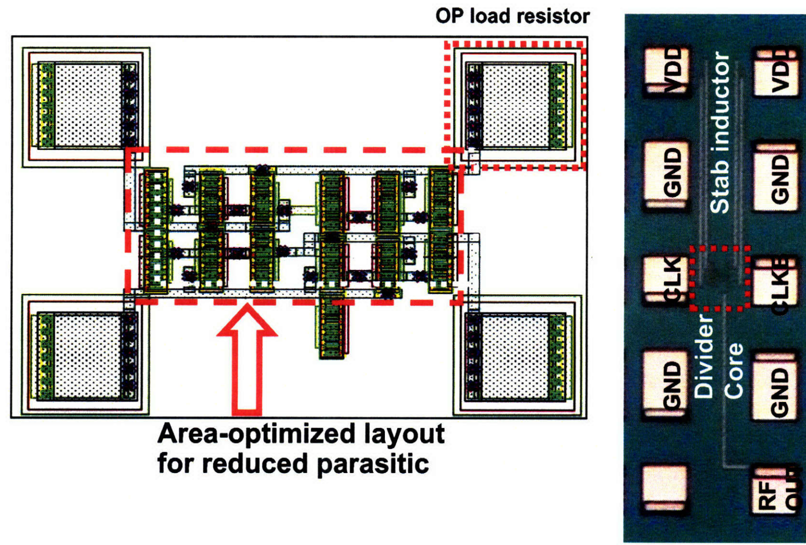


Figure 2-13: Layout and die photo of the frequency divider circuit in 65nm SOI CMOS technology.

Type	Description
DIV_1	Parasitic-aware initial design
DIV_2	Compact placement and routing for reduced wiring area
DIV_3	With inductive shunt peaking

Table 2.1: Test vehicles for frequency dividers.

μm slab inductors at each of the four output nodes to enhance the output bandwidth. Each vehicle has a pair of GSGSGSGSG pad sets for high frequency measurement.

We implement four different types of test vehicles for the PLL front-end containing both the VCO and frequency divider, as summarized in Table 2.2. The test vehicles have two different types of VCOs: VCO_1 and VCO_2. Both VCOs have the same LC-tank, but different sizing of NFETs and PFETs such that NFET/PFET sizes of VCO_1 and VCO_2 are 14μm/28μm and 17μm/34μm, respectively. Because of the difference in the parasitic capacitance of the devices, the center frequencies of VCO_1 and VCO_2 are 65 and 71GHz, respectively.

Figure 2-14 shows the layout and die photo of the combination of the VCO and frequency divider with a buffer amplifier in between. The physical dimension of the circuit is $65\mu m \times 85\mu m$. A number of VNCAPs are inserted between DC signals and

Type	Description
$VCODIV_1$	$VCO_1 + DIV_2$
$VCODIV_2$	$VCO_1 + DIV_2$
$VCODIV_3$	$VCO_2 + DIV_2$
$VCODIV_4$	$VCO_2 + DIV_3$

Table 2.2: Test vehicles for the PLL front-end.

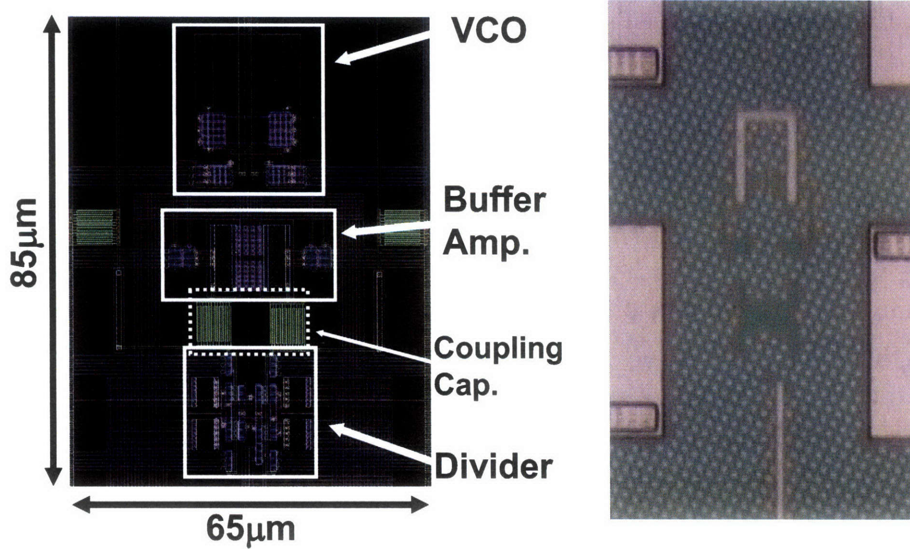


Figure 2-14: Layout and die photo of the VCO and frequency divider circuit in 65nm SOI CMOS technology.

ground to reduce noise at reference voltages and power supply.

2.5 Summary

In this chapter, we describe the design and analysis of a mm-wave PLL front-end circuit, which contains a VCO and frequency divider as high-speed building blocks of a PLL. A 77GHz LC-VCO is designed to achieve a wide frequency tuning range for improved manufacturability against process variation. The VCO employs complementary topology for phase noise improvement and power reduction, an accumulation-mode varactor for a wide capacitance tuning ratio, relaxed pitch devices for reduced parasitic capacitance, and a thick metal one-turn high Q inductor for improved phase noise performance. A 2:1 frequency divider is designed to operate up to 90GHz input

frequency. The divider employs a ring-oscillator based injection-locking frequency divider scheme for a wide frequency locking range. The divider is implemented using a D-FF architecture with CML latches and inductive shunt peaking for bandwidth enhancement. The self-oscillation frequency and frequency locking range of the divider are analyzed to obtain analytic forms of the divider performance. The bias condition of the CML divider can be tuned externally to change the frequency operating range. The PLL front-end circuit is implemented in a 65nm SOI CMOS technology that provides various features for high-speed analog circuit design including a vertical-natural capacitor, a 10-layer metal stack with an extra-thick top metal layer, and relaxed pitch devices for reduced parasitic capacitance.

Chapter 3

Statistical Measurement and Analysis

In this chapter, we show the measurement results of the VCO and frequency divider designed and presented in Chapter 2. We characterize nominal performance of the VCO including frequency tuning range, power consumption, and output phase noise. The variability of the minimum and maximum frequencies of the VCO over a 300mm wafer is also measured to estimate parametric yield of the VCO. For the frequency divider, we focus on the statistical characterization of the self-oscillation frequency at different bias conditions of V_{DD} and V_{BIAS}. Though the input sensitivity curve of a frequency divider provides detailed characteristics of the divider, the measurement of the input sensitivity curve is an extremely time-consuming task, requiring sweeping of both input power and frequency. The self-oscillation frequency of the divider, on the other hand, is an easy-to-measure performance variable and provides an excellent characterization of process variation in the frequency divider.

To obtain more information about parameter variability from statistical performance measurement data, we develop an extraction scheme in which circuit parameter variation is extracted from the self-oscillation frequency measurement of the divider at multiple bias conditions. The method is based on the sensitivity analysis of performance variables to the deviation of fundamental circuit parameters, using a back-propagation of variation (BPV) approach, which is a modified form of the method

shown in [35]. Experimental results presented here show the statistics of each circuit parameter and important correlation between the parameters. In addition, we present a simple yet effective method to analyze process variations using the statistics from manufacturing in-line data drawn from an extensive set of primitive test structures of devices and ring oscillators, without assuming any explicit underlying model for process variation. Based on a variant of principal component analysis (PCA), we are able to reveal systematic variation patterns existing on die-to-die and wafer-to-wafer levels individually.

Section 3.1 depicts the measurement setup and design-for-test features for automated performance measurement of mm-wave analog circuits. Section 3.2 shows the nominal performance of the VCO and frequency divider, verifying their functionalities. Section 3.3 provides the statistical measurement results of the VCO and frequency divider over 300mm wafers. Section 3.4 presents statistical analysis of the measured data of the VCO and frequency divider to identify variation in these key PLL front-end components.

3.1 Statistical Measurement for High-Speed CMOS Characterization

As operating frequencies of CMOS applications have reached the mm-wave regime, it has become more and more difficult for process engineers and circuit designers to characterize the device and circuit performance at such high frequencies. In particular, since process variability of circuit performance becomes a critical issue for parametric yield loss, statistical characterization of device and circuit performance by measuring a large set of circuit samples becomes essential to capture the variation properties of CMOS circuits in advanced technologies.

An on-wafer measurement scheme is necessary to enable measurement of a large number of die samples in the high frequency regime. On-board testing of a large number of circuit samples after packaging is extremely time-consuming, and demands

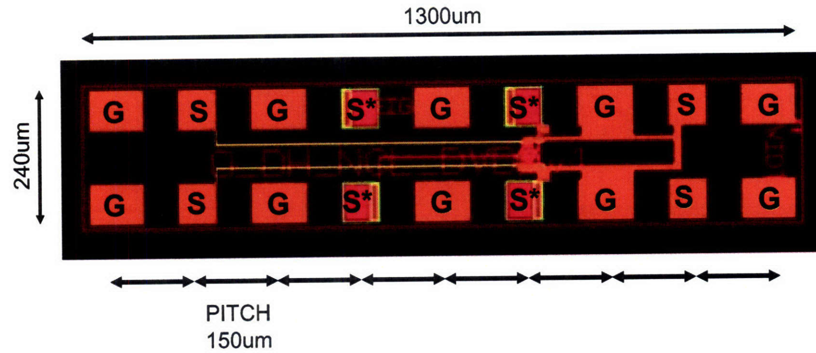


Figure 3-1: Ground and signal pad assignment of test circuits with physical dimension.

proper de-embedding techniques to exclude the effect of bonding wires and board traces on the circuit performance. For on-wafer measurement of mm-wave circuit test vehicles, pad assignment and interconnect length must be carefully considered during design to reduce overall area, IR drop in power supply wires, transmission-line effect for high frequency signals, and parasitic capacitance to substrate. The test structures in [29] and [27], for example, show highly optimized pad assignment and compact signal routing approaches to improve the measurement accuracy.

Figure 3-1 shows the pad assignment and physical dimensions of the test vehicles of the VCO and frequency divider in this work.[1] In the GSGSGSGSG[2] pad set, high frequency pads are centered and the test circuit is placed close to the high frequency pads to reduce the length of high frequency interconnects. The high frequency pads utilize only the two top metal layers to reduce parasitic capacitance to substrate, and to provide mechanical strength for repeated contacts by signal probes.

3.1.1 Measurement Setup for the mm-Wave PLL Front-End

Figure 3-2 shows the test setup for the on-wafer measurement of die samples on a 300mm wafer. A W-band measurement system is used to measure performance characteristics up to 110GHz frequency. The position of the probe set is automatically controlled to scan all die samples on each wafer. Circuit conditions for the test vehicles are programmed into a database, and measurement data of performance variables

[1] The pad marked by 'S*' indicates a high frequency signal pad.
[2] G and S indicate ground and signal pads, respectively.

Figure 3-2: Automated high-frequency measurement setup for VCO and frequency divider samples.

(e.g., oscillation frequency, phase noise, average current, etc.) is collected through the general-purpose-interface-bus (GPIB) of a spectrum analyzer and a current meter. We measure 12 sample wafers processed from the same lot, and each wafer contains 76 die samples. Statistical properties of the performance variation in the VCO and frequency divider are characterized over the wafer set.

3.2 Nominal Performance Measurement of PLL Front-End

Nominal performance of the VCO and frequency divider is measured to verify the proper operation of the circuits in desired frequency ranges. For the VCO, center frequency, frequency tuning range, phase noise, and power dissipation are important performance characteristics to be measured. In addition, we define a new figure-of-merit (FOM_T) that includes the frequency tuning range, to enable comparison of the measured performance of this VCO to other state-of-the-art CMOS VCOs operating in similar frequency ranges.

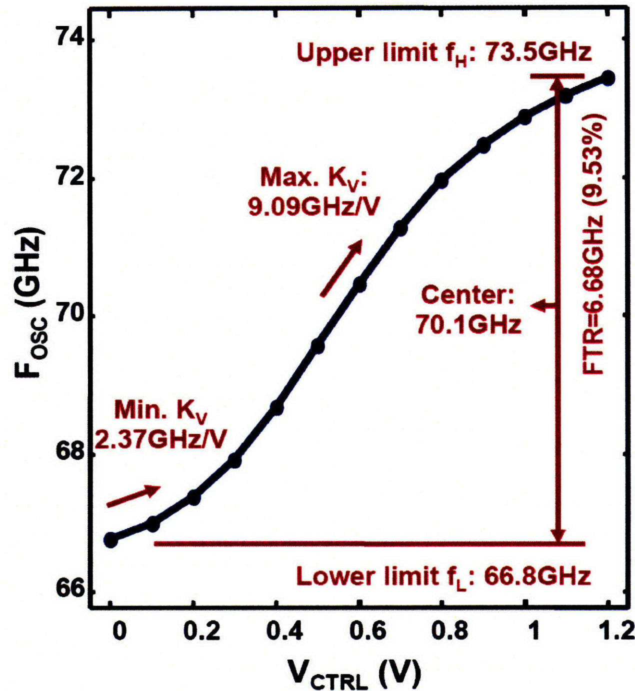


Figure 3-3: Frequency tuning range of the mm-wave VCO over a full range of V_{CTRL}.

For the frequency divider, we measure the full input sensitivity curve to characterize the divider performance. We also measure the self-oscillation frequency of the divider at different bias conditions to check hardware-to-model correlation. Power dissipation is measured to compare the performance of the divider with other state-of-the-art frequency dividers operating in the mm-wave frequency regime.

3.2.1 Measurement of VCO Performance

Figure 3-3 shows the output frequency change over the full tuning range of V_{CTRL} from zero to V_{DD}, for a representative VCO. The VCO is tunable from 66.8GHz to 73.5GHz, and the center frequency is 70.1GHz. As a result, the FTR is 6.68GHz, or 9.55% of the center frequency, which is relatively large compared to the design examples available in the literature for mm-wave CMOS VCOs shown in Table 3.1. The maximum VCO gain (Kv) is 9.09GHz/V at the center frequency, and the minimum Kv is 2.37GHz/V at the minimum frequency.

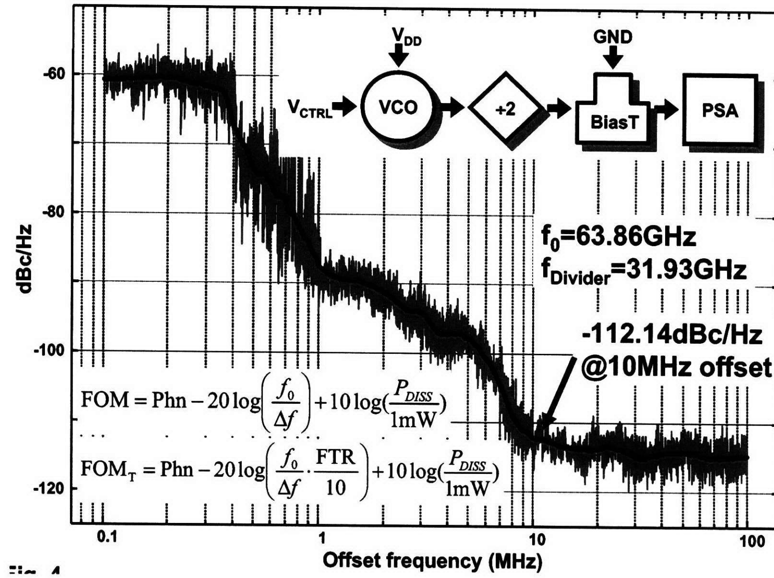


Figure 3-4: Phase noise characteristic of the VCO and the phase noise measurement set up.

Figure 3-4 shows the output phase noise characteristic of the VCO, and the test setup used for phase noise measurement. Since the VCO phase noise is not directly measurable due to limited output signal power and loss over 50GHz in the measurement equipment, the VCO output is divided by two using a frequency divider, and the divided output phase noise is measured by a spectrum analyzer assuming that the divider adds only a small constant amount of phase noise. The output phase noise was measured when the VCO output frequency is at 63.86GHz and the divided output frequency is 31.93GHz. Measured phase noise of the divided output is -112.14dBc/Hz at 10MHz offset. After 6dB compensation of the phase noise improvement by frequency division, the estimated VCO phase noise is -106.14dBc/Hz at 10MHz offset.

Table 3.1 shows the comparison of the performance of this VCO with other state-of-the-art CMOS VCOs operating at similar frequency ranges. We define $\mathrm{FOM_T}$ to compare the VCO performance including the impact of FTR as:

$$FOM_T = PN - 20\ log(\frac{f_O}{\Delta f} \cdot \frac{\mathrm{FTR}}{10}) + 10\ log(\frac{P_{DISS}}{1\mathrm{mW}}). \tag{3.1}$$

where PN is a measured phase noise, f_O is a center frequency of the VCO, FTR is

F_O (GHz)	FTR (%)	Phase Noise (dBc/Hz)	P_{diss} (mW)	FOM (dBc/Hz)	FOM_T (dBc/Hz)	Technology
51.2	1.39	-85	1.0	-179.19	-162.03	120nm CMOS [99]
56.5	10.27	-108	9.8	-173.13	-173.36	130nm CMOS [22]
64.3	7.00	-85	118.8	-160.41	-157.32	250nm CMOS [68]
89.7	2.68	-106	15.8	-173.08	-161.63	130nm CMOS [21]
98.5	2.54	-102.7	7.0	-174.12	-162.21	130nm CMOS [22]
103.9	1.92	-94	180	-151.78	-137.47	90nm CMOS [39]
105.2	0.19	-97.5	7.2	-169.37	-134.95	130nm CMOS [22]
114.0	2.11	-107.6	8.4	-179.50	-165.96	130nm CMOS [49]
130.9	1.68	-108.4	20	-177.73	-162.24	90nm CMOS [48]
192.1	0.68	-100	16.5	-173.49	-150.10	130nm CMOS [23]
70.2	**9.55**	**-106.14**	**5.4**	**-175.76**	**-175.36**	**This Work**

Table 3.1: Comparison with state-of-the-art CMOS VCOs.

a frequency tuning range in percentage, Δf is the frequency offset for the measured phase noise, and P_{DISS} is total power dissipation. The VCO in this work outperforms other CMOS mm-wave VCOs in FOM_T because of the wide frequency tuning range while achieving reasonably good phase noise and power consumption through use of a complementary topology.

3.2.2 Measurement of Frequency Divider Performance

Figure 3-5(a) shows the sensitivity curves of the frequency divider (with inductive peaking) in the fastest die sample at four different bias conditions of V_{DD} and V_{BIAS}. Because of the bandwidth limitation of the equipment used in this measurement, the divider has been biased to work over the input frequency range from 75GHz to 110GHz. The divider biased at V_{DD}=2.2V and V_{BIAS}=1.5V operates up to 100.2GHz for a 4.87 dBm differential input.[3]

The sensitivity curves at different bias conditions show that the operating range of this divider can be dynamically adjusted to the tuning range of the VCO by changing V_{DD} and V_{BIAS}. The lowest points of the sensitivity curves indicate the self-oscillation frequency of the divider. The measured power consumption is 52.4

[3]This is a 1.52X improvement in frequency performance over the fastest reported frequency divider in 90 nm CMOS [87].

mW and the switching energy at the self-oscillation frequency of 46GHz is 0.57 pJ.

Figure 3-5(b) shows the comparison of the simulation and measurement results for the self-oscillation frequency at various V_{DD} and V_{BIAS} conditions. The strong correlation between the simulated and measured self-oscillation frequency data verifies the integrity of the simulation model.

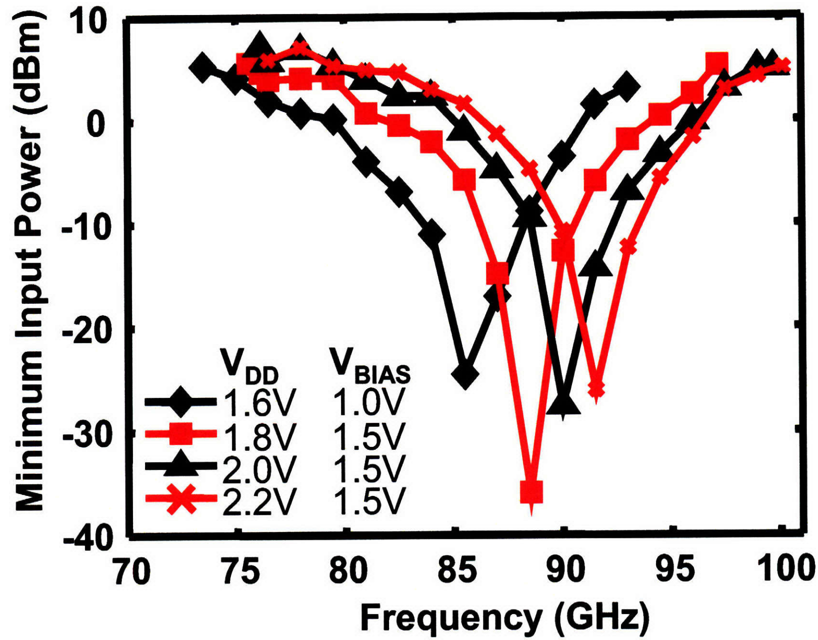
Table 3.2 shows the comparison of the measured performance with other state-of-the-art frequency dividers operating above 50GHz in various technologies. The maximum operating frequency of the CML frequency divider in this work is comparable with the dividers in compound semiconductor technologies such as SiGe and InP HBTs, while the power consumption is much smaller. Table 3.2 shows that the reduction in the switching energy at the self-oscillation frequency is at least 42% compared to other state-of-the-art dividers.

F_{SO} (GHz)	F_{MAX} (GHz)	Power (mW)	V_{DD} (V)	Switching Energy at F_{SO} (pJ)	Switching Energy at F_{MAX} (pJ)	Technology
48	66	80	1.8	1.667	1.212	90nm CMOS [87]
95	143.6	90	N/A	0.947	0.627	400GHz f_T InP [45]
77	100	122	3.3V	1.584	1.22	230GHz f_T SiGe HBT [57]
33	100	750	N/A	22.727	7.5	135GHz f_T InP [76]
65	110	1350	-5.2	20.769	12.273	225GHz f_T SiGe:C HBT [101]
71	96	770	-5	10.845	8.021	210GHz f_T SiGe HBT [93]
92.4	**100**	**52.38**	**2.2**	**0.567**	**0.524**	**This Work**
85.97	**91**	**25.13**	**1.6**	**0.292**	**0.273**	**This Work**

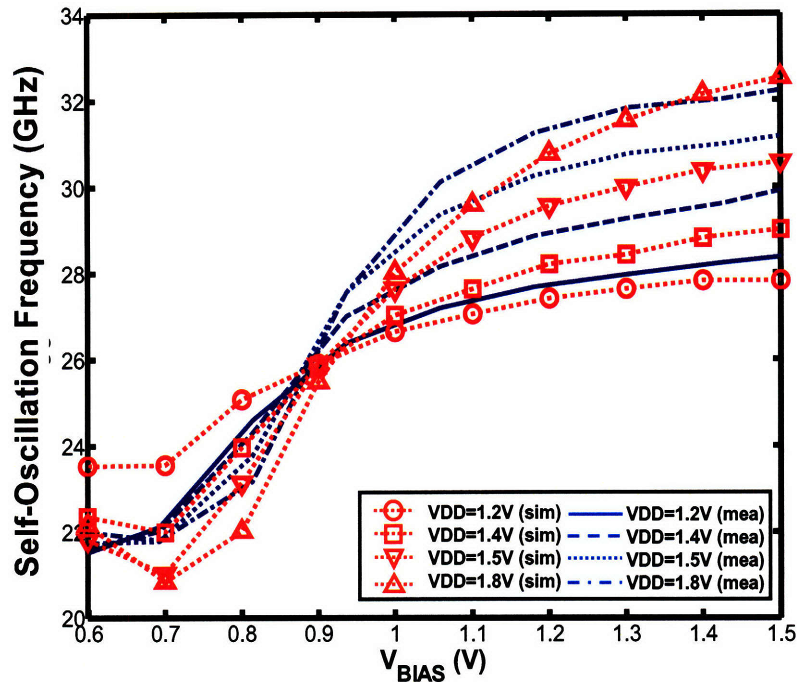
Table 3.2: Comparison with state-of-the-art frequency dividers operating over 50GHz.

3.3 Variation of VCO and Frequency Divider Performance

Statistical properties of the performance variation in the VCO and frequency divider must be characterized to build a realistic variation model and to calculate the para-



(a) Sensitivity curves at different V_{BIAS} and V_{DD} conditions



(b) Hardware-to-model correlation

Figure 3-5: Measured performance characteristics of the frequency divider.

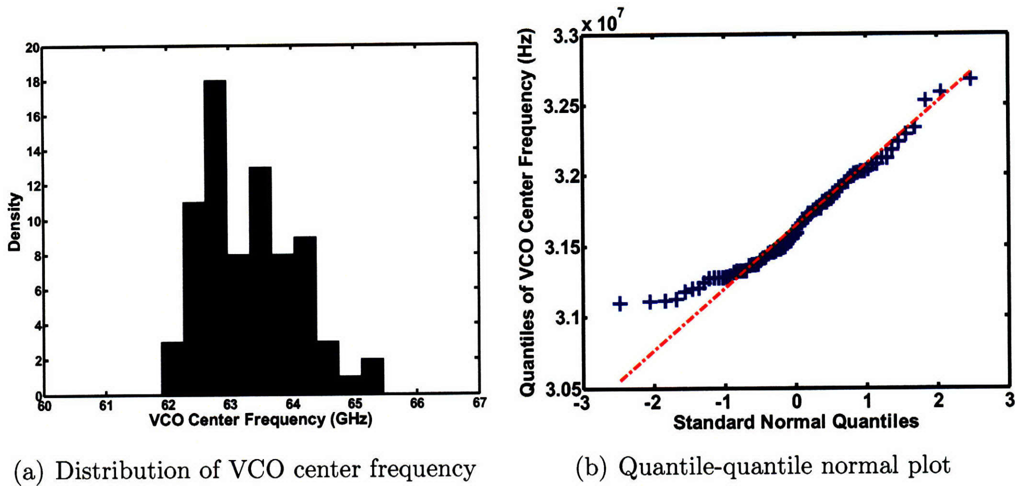
	Average	Std. Dev.	Normalized Deviation (%)	Max.	Min.
Maximum frequency (GHz)	71.0	0.82	1.15	73.5	69.9
Minimum frequency (GHz)	64.8	0.76	1.18	66.9	63.8
Center frequency (GHz)	67.9	0.79	1.16	70.1	66.9
FTR (GHz)	6.14	0.13	2.11	6.68	5.91
FTR (%)	9.05	0.17	1.90	9.53	8.72
Full range VCO gain (GHz/V)	5.11	0.11	2.11	5.57	4.93
Maximum VCO gain (GHz/V)	7.96	0.43	5.36	9.38	7.25
Minimum VCO gain (GHz/V)	1.72	0.43	25.0	2.37	0.11
I_{DD}(mW)@ V_{CTRL}=0V	4.48	0.51	11.4	5.15	3.59

Table 3.3: Statistics of VCO performance variation.

metric yield. In this section, we show the statistical measurement data of the VCO and frequency divider performance and their statistics over 300mm wafers. Systematic and random patterns of the performance variation are identified and the causes of the variation patterns are analyzed.

3.3.1 Variation of VCO Performance

The VCO output characteristics are measured at 57 dies in a 300mm wafer, and the statistics of performance variables are summarized in Table 3.3. Figure 3-6(a) shows the histogram of the VCO output frequency. The quantile-quantile normal plot in Figure 3-6(b) shows that the distribution of the VCO output frequency cannot be accurately modeled as Gaussian since it deviates from a normal distribution significantly in the lower tail. Since the output frequency of an LC-VCO is determined by the electrical parameters of an inductor and varactor whose physical dimension is large, the variation of the output frequency is relatively small compared to other performance variables affected by device characteristics. As a result, $3\sigma/\mu$ of the VCO output frequency is only 3.45% while the $3\sigma/\mu$ variation of I_{DD} is 34.2%. An average supply current I_{DD} is 4.48 mA when V_{DD}=1.2V, which results in 5.37 mW of power dissipation in the VCO core. Output buffers attached to the VCO core consume 3.96 mA of supply current at V_{DD}=1.2V.



(a) Distribution of VCO center frequency (b) Quantile-quantile normal plot

Figure 3-6: Statistical distribution of the VCO output frequency over a 300mm wafer (57 die samples).

Figure 3-7 shows the minimum and maximum output frequency of the VCO in one 300mm wafer. A common FTR shared by all VCO samples exists from 66.9 to 69.9GHz, which means that when a FTR requirement is within the common FTR, all the designed VCOs can satisfy the FTR specification. When we set the maximum frequency requirement to 70GHz, only three VCO samples fail to meet the maximum frequency requirement to result in 94.7% parametric yield in this wafer.

3.3.2 Variation of Frequency Divider Performance

To estimate the parametric yield of the frequency divider, measuring the maximum operating frequency (F_{MAX}) at a given input power is important. However, the F_{MAX} measurement is costly since it requires input frequency sweep and the detection of proper division. On the other hand, the self-oscillation frequency of the divider is more efficient to measure, and a large portion of the F_{MAX} variation can be explained from analysis of the self-oscillation frequency. For example, when the divider variation is sensitive to the variation in load resistance and capacitance of the divider output nodes, the self-oscillation frequency and F_{MAX} track each other with strong correlation. When the divider is sensitive to the variation in the bias current, the self-oscillation frequency and F_{MAX} vary to opposite directions with each other. The

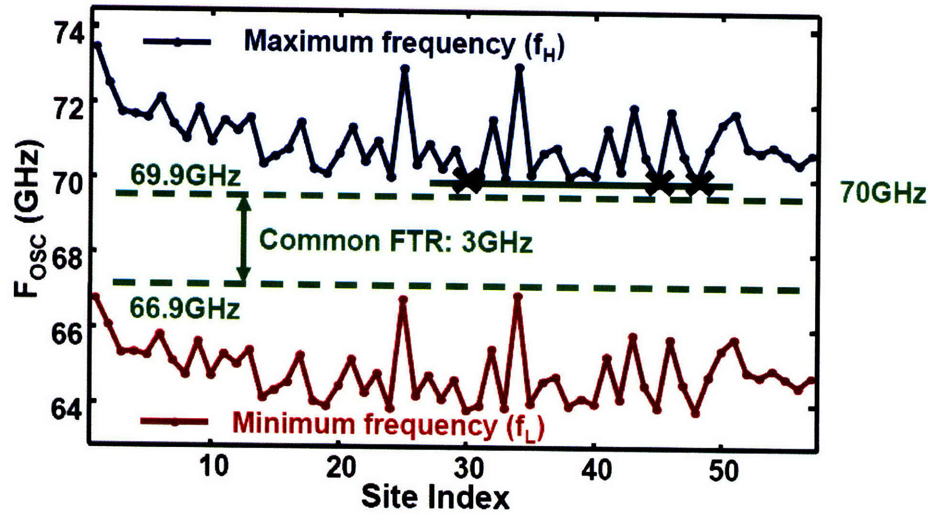


Figure 3-7: Minimum and maximum frequency of the VCO over a 300mm wafer.

correlation between the self-oscillation frequency and F_{MAX} at different bias conditions of the divider is shown in [55]. Therefore, we conduct statistical measurement of the self-oscillation frequency over multiple wafers, and investigate the systematic and random variation patterns of the self-oscillation frequency.

Figure 3-8 shows the variation of the self-oscillation frequency when V_{DD}=1.8V and V_{BIAS}=1.5V across a 300mm wafer. DIV_1 and DIV_2 are identically sized but DIV_2 has more compact placement and routing for decreased wire capacitance as explained in Section 2.4. DIV_3 has inductive peaking in addition to the layout of DIV_2. For the three different types of dividers, the self-oscillation frequency measurements show $3\sigma/\mu$ of 16.7% and a 22% range between the fastest and slowest dies. The difference between the performance of DIV_1 and DIV_2 is negligible; the self-oscillation frequency of DIV_2 is only 0.39GHz (1.3%) higher than that of DIV_1 on average. Therefore, the reduction of wire capacitance by compact placement and routing is not a major means for overall output capacitance reduction. The self-oscillation frequency of DIV_3 is consistently higher than DIV_2 by 2.57GHz due to the inductive shunt peaking.

In Figure 3-9(a), we show the wafer-level pattern of the self-oscillation frequency in a 300mm wafer. The fastest corner exists on the left-hand side of the wafer when the notch is aligned to the right. The wafer-level pattern shows a mixture of a circular

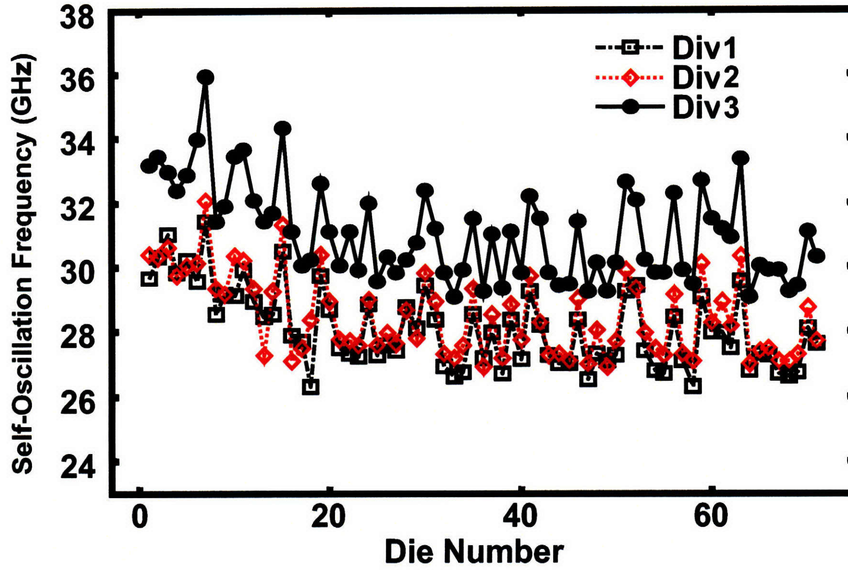
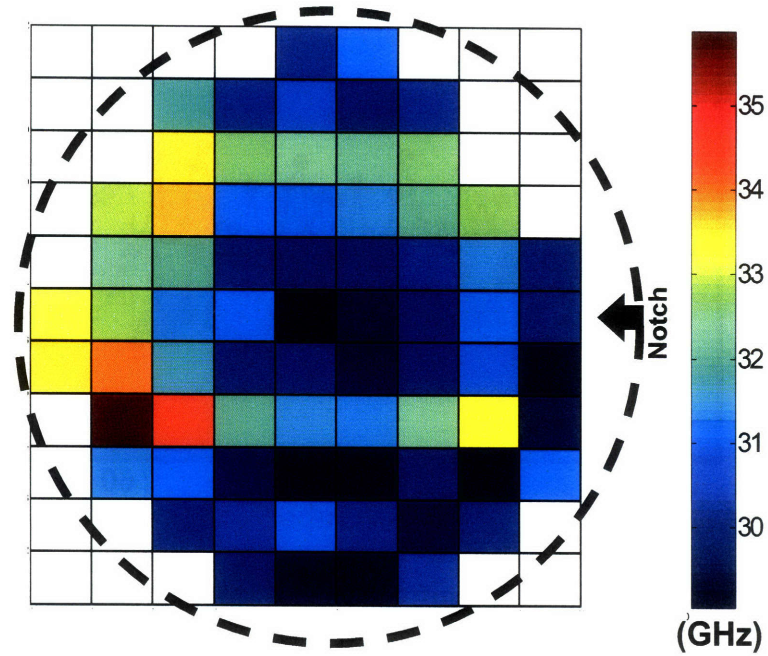


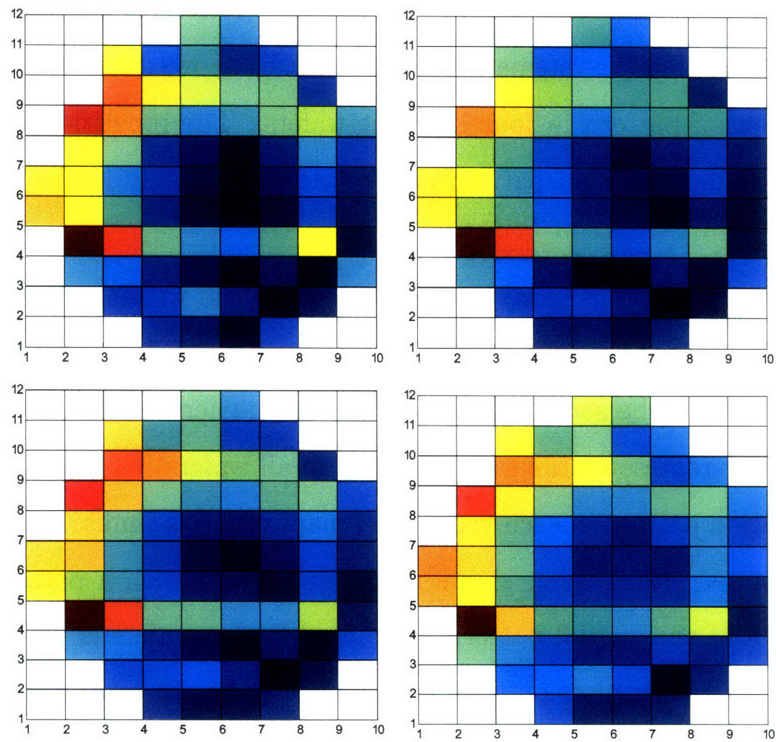
Figure 3-8: Variation of self-oscillation frequency of three frequency divider alternatives at a bias condition V_{DD}=1.6V and V_{BIAS}=0.75V.

shape trend and horizontal direction dependency. We note that the variation pattern across all wafers is highly systematic. Figure 3-9(b) shows the comparison of the wafer-level variation pattern in four different wafers. The repetition of the similar wafer-level die-to-die variation pattern can be verified visually in the four sampled wafers.

For more accurate comparison, Figure 3-10 shows the within-wafer variation for 11 different wafers at a fixed bias condition (V_{DD}=1.8V and V_{BIAS} =1.5V). The site index is sorted (where the sort is based on f_{SO} average across all 11 wafers, and the sorted die number represents the same location in all wafers) to visualize a common ascending variation pattern in each wafer-level map, which is similarly repeating over the entire wafer set. Each wafer shows a similar pattern with a parallel shift: the cross correlation of the spatial pattern between different wafers is 92% on average. Figure 3-11 shows scatter plots between each pair of wafers to verify the strong cross-correlation in spatial variation patterns across all wafer. Based on this result, with a pre-characterized profile of a reference wafer, we can estimate the divider performance of all dies in a random wafer with 1.5% average error by measuring a single die and checking the difference with the reference wafer profile.



(a) Wafer map of the self-oscillation frequency



(b) Comparison of multiple wafers

Figure 3-9: Wafer-level die-to-die variation pattern of the self-oscillation frequency of the divider over one 300mm wafer.

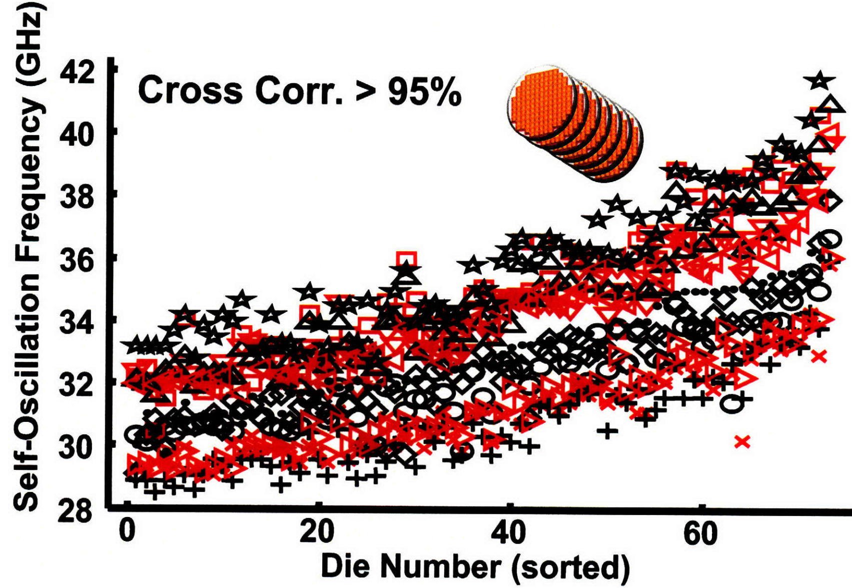


Figure 3-10: Variation of self-oscillation frequency of the frequency divider over 11 wafers. Symbol represents the wafer number.

Figure 3-12 depicts the distributions of the measured self-oscillation frequency over each of our 11 wafers. In Figure 3-12(a), the distribution of each wafer is fitted to a Gaussian distribution to visualize the trend of mean and standard deviation values. To check the Gaussian assumption of the wafer-level variation, Figure 3-12(b) shows a quantile-quantile normal plot of the distribution for each wafer and for the entire wafer set. As with the VCO center frequency previously shown in Figure 3-6, we see that the lower tail for divider self-oscillation frequency is non-Gaussian, with somewhat truncated f_{SO} at lower values. The mean value of each wafer spreads from 29.9GHz to 35.8GHz, and $3\sigma/\mu$ of each wafer ranges from 15% to 18%. Considering all 803 dies, $3\sigma/\mu$ total variation (within-wafer and wafer-to-wafer combined) is 23.8%.

3.4 Statistical Analysis of Measurement Data

While it is convenient to measure the self-oscillation frequency of the divider at various bias conditions of V_{DD} and V_{BIAS}, it is difficult to extrapolate the measured statistics of the self-oscillation frequency to similar circuit examples with different sizing and

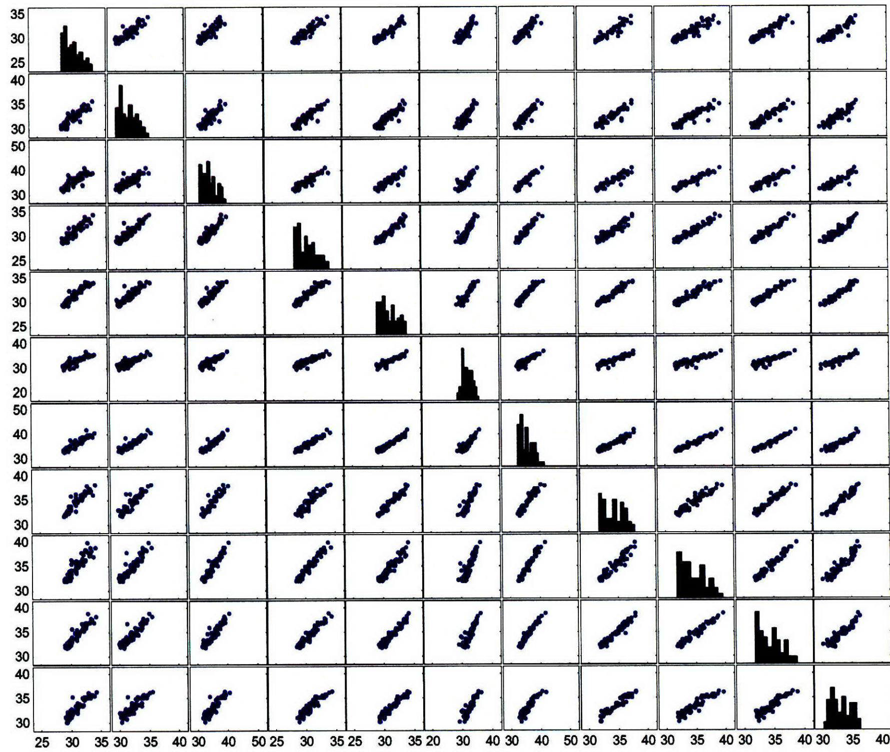
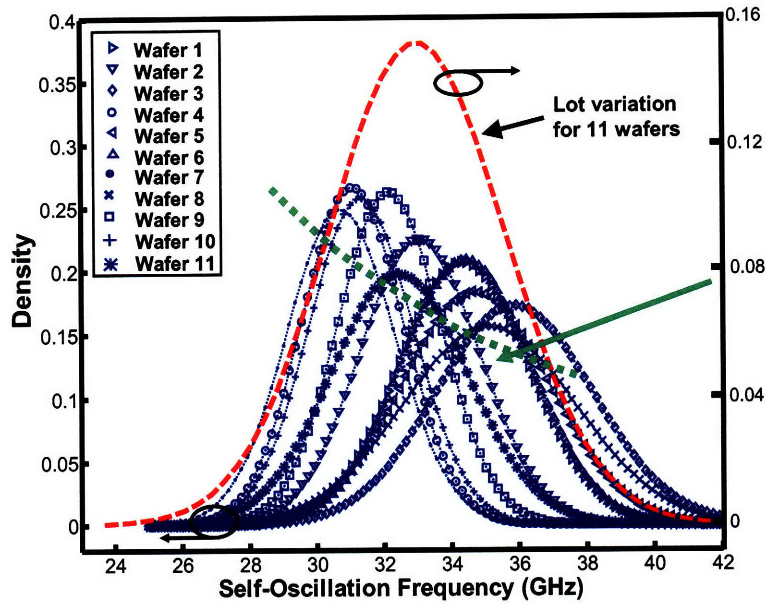


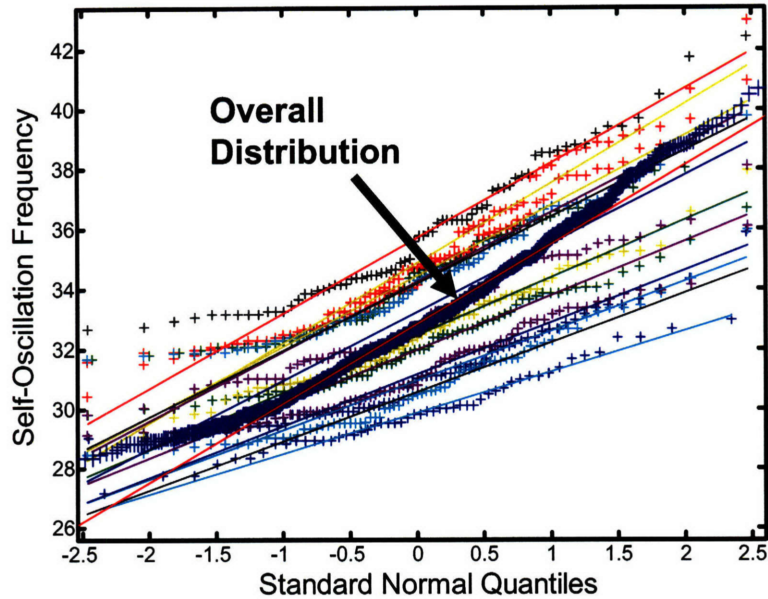
Figure 3-11: Scatter plots of f_{SO}, for corresponding dividers, between each pair of wafers.

topologies. The statistics of more fundamental circuit parameters (e.g., threshold voltage, channel length, parasitic capacitance, etc.) must be estimated from the measured performance statistics to assess the performance variation of general circuit examples. In this section, we present a back-propagation of variation method which extracts the deviation of fundamental circuit parameters, based on the measured self-oscillation frequencies at multiple bias conditions and on sensitivity analysis from model or simulation.

Alternatively, we also present a simple and practical method to decompose the process variability of complex analog circuits using the statistics of manufacturing inline measurement data, without assuming any underlying model for process variation. The experimental results show that a significant portion of the performance variation in complex RF/mm-wave analog circuits can be explained using the measurement data of primitive inline test structures (e.g., FETs, resistors, capacitors, ring oscillators, etc.).



(a) Gaussian fits



(b) Quantile-quantile normal plots

Figure 3-12: Statistical distribution of the self-oscillation frequency variation over each wafer and the entire wafer set.

3.4.1 Back-Propagation of Variation

For accurate estimation of circuit performance variation and robust optimization, the variability of critical circuit and process parameters must be precisely characterized and synchronized with simulation tools. Output frequency of a ring oscillator (RO) is a common performance metric to assess the inter-die and long range intra-die variation of delay and power consumption in digital circuits, motivated in part by the convenience of RO measurement [42]. However, since each ring oscillator generates one output frequency whose variation is a composition of various parameter fluctuations, it is difficult to extract the variation of individual circuit parameters for the measured oscillation frequencies.

Sensitivity-based parameter de-embedding is a useful technique to extract the fluctuation of individual parameters from measured output variables. Using parameter sensitivity calculated from device and interconnect models, the deviation of critical circuit parameters from their nominal values can be extracted. To determine the deviation of multiple circuit parameters, the same or larger number of output variables is needed. As an example, the measurement data for ring oscillator frequency f_O and leakage current I_{LEAK} are used to extract the variation of channel length ΔL and oxide thickness T_{ox} in [83].

For the CML frequency divider in this work, the main circuit parameters affecting the self-oscillation frequency are bias current, parasitic capacitance and load resistance. The bias current is a function of the threshold voltage of input transistors. Through simulation, the sensitivity of the self-oscillation frequency with respect to the change of the threshold voltage, parasitic capacitance and load resistance can be calculated at different bias conditions. In combination with these sensitivities, the measurement statistics of the self-oscillation frequency at multiple bias conditions can then be used to extract circuit parameter variations. This method is based on a first-order response surface model of the self-oscillation frequency as follows:

$$\Delta f_{SO} = \alpha \cdot \Delta V_{TH} + \beta \cdot \Delta R_L + \gamma \cdot \Delta C_L \tag{3.2}$$

where α, β, and γ are the sensitivity values of the self-oscillation frequency to each circuit parameter. The deviation of the circuit parameters from their nominal values can be calculated using the parameter sensitivity values (α, β, and γ) extracted from a circuit simulation model and the measurement data of self-oscillation frequency at multiple bias conditions.[4]

We denote α_i, β_i, and γ_i as the sensitivity values at the ith bias condition. $\Delta f_{SO,i}$ is the deviation of the measured self-oscillation frequency from its nominal (average) value at the ith bias condition. We can build a system of linear equations such that

$$\begin{bmatrix} \Delta f_{SO,1} \\ \Delta f_{SO,2} \\ \vdots \\ \Delta f_{SO,n} \end{bmatrix} = \begin{bmatrix} \alpha_1 & \beta_1 & \gamma_1 \\ \alpha_2 & \beta_2 & \gamma_2 \\ \vdots & \vdots & \vdots \\ \alpha_n & \beta_n & \gamma_n \end{bmatrix} \cdot \begin{bmatrix} \Delta V_{TH} \\ \Delta R_L \\ \Delta C_L \end{bmatrix} = \mathbf{S} \cdot \begin{bmatrix} \Delta V_{TH} \\ \Delta R_L \\ \Delta C_L \end{bmatrix}. \tag{3.3}$$

The least mean-square error solution of Equation (3.3) can be found by pseudo-inversion of the non-square matrix $\mathbf{S}$ as follows.

$$\begin{bmatrix} \Delta V_{TH} \\ \Delta R_L \\ \Delta C_L \end{bmatrix} = \mathbf{S}^T \cdot (\mathbf{S} \cdot \mathbf{S}^T)^{-1} \cdot \begin{bmatrix} \Delta f_{SO,1} \\ \Delta f_{SO,2} \\ \vdots \\ \Delta f_{SO,n} \end{bmatrix} \tag{3.4}$$

For the stable inversion of the sensitivity matrix $\mathbf{S}$, we re-condition $\mathbf{S}$ by multiplying different factors to each column to regularize the mean of each column. The final values of V_{TH}, R_L and C_L are re-scaled by the multiplication factors. Furthermore, the condition number of $\mathbf{S}$ become dramatically improved by increasing the number of bias conditions (the number of rows in $\mathbf{S}$). In the experiment, we use 12 bias conditions to reduce the singularity of $\mathbf{S}$ to achieve a robust sensitivity matrix inversion.

Additionally, when the amount of parameter variation increases, the first-order model cannot explain the performance deviation accurately in the presence of non-

[4]A similar technique directly calculating the standard deviation of the parameters was shown in [35].

Bias Condition (BC)	ΔV_{TH} (GHz/mV)	ΔR_L (GHz/Ω)	ΔC_P (GHz/fF)
BC1	-0.0312	-0.1145	-0.8565
BC2	-0.0401	-0.1159	-0.8648
BC3	-0.0458	-0.1165	-0.8918
BC4	-0.0291	-0.1252	-0.8872
BC5	-0.0445	-0.1151	-1.0340
BC6	-0.0544	-0.1162	-1.0902
BC7	-0.0272	-0.1369	-0.9047
BC8	-0.0440	-0.1292	-1.0348
BC9	-0.0322	-0.1345	-1.0764

Table 3.4: Sensitivity of the self-oscillation frequency to circuit parameters at different bias conditions.

linear circuit performance. A quadratic expansion of the response surface model can provide higher accuracy over local performance space as shown in [66]. Equation (3.3) can be expanded to a quadratic form:

$$\Delta f_{SO,i} = \mathbf{x}^T \cdot \mathbf{A}_i \cdot \mathbf{x} + \mathbf{b}_i \cdot \mathbf{x} + c_i \tag{3.5}$$

where $\mathbf{A}_i$, $\mathbf{b}_i$, and c_i are from quadratic response model fitting at each bias condition, and $\mathbf{x} = [V_{TH}\ R_L\ C_L]$. A non-linear equation solver such as `fmincon` in MATLAB can find the least mean-square solution of $\mathbf{x}$ for a set of Equation (3.5) for $i = 1, \ldots, n$.

Experimental Results of Parameter Extraction

The parameter extraction scheme for threshold voltage, load resistance, and lumped parasitic capacitance are tested using the divider self-oscillation frequency measurement results. The sensitivity matrix is calculated from SPICE simulations with device, passive, and interconnect models. The model-to-hardware correlation is verified Section 3.2.2, as shown in Figure 3-5(b), to demonstrate reasonable accuracy of the SPICE simulation results. The self-oscillation frequency is measured at all combinations of 21 V_{BIAS} steps and four V_{DD} steps. We select nine bias conditions that provide the most non-singular matrix $\mathbf{S}$ for the calculation in Equation (3.4). The sensitivity matrix of the nine bias condition is shown in Table 3.4.

Figure 3-13 summarizes the statistics of extracted parameter fluctuations. The

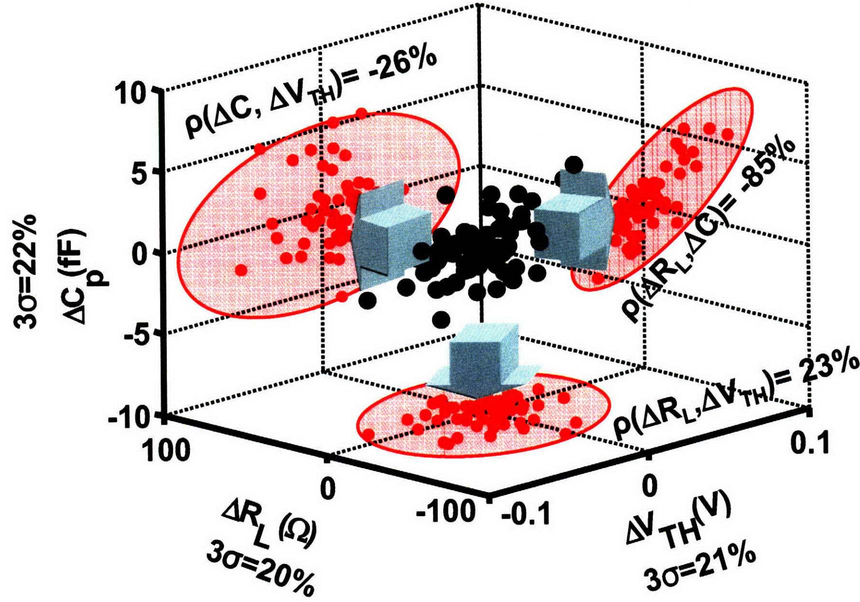


Figure 3-13: Extracted variation of V_{TH}, load resistance, and capacitance and their correlations

extracted $3\sigma/\mu$ of the threshold voltage, parasitic capacitance and resistance variation is 21%, 22% and 20%, respectively. For accurate Monte Carlo analysis of circuits, knowing the correlation between circuit parameters is essential. The scatter plot in Figure 3-13 shows a significant negative correlation ($\rho = -0.85$) between parasitic capacitance and resistance. The threshold voltage does not show notable correlation with other parameters. This correlation structure implies that the variation in physical dimension of poly-silicon load resistors is the major portion of the variation in total load resistance and output capacitance since the variation in the width of the poly-resistors causes the variation of resistance and parasitic capacitance to opposite directions.

Table 3.4 shows the sensitivity of each circuit parameter to the self-oscillation frequency at tested bias conditions. From the sensitivity analysis and the results from BPV anslysis, 3σ deviation of V_{TH}, R_L and C_P from their nominal values causes the change of the self-oscillation frequency by 2.23, 5.30, and 4.55 GHz, respectively, at a normal bias condition (BC5). As V_{BIAS} increases, the self-oscillation frequency becomes less sensitive to V_{TH}, but the sensitivity to R_L, and C_P increases.

3.4.2 Decomposition of Frequency Divider Variation

For the characterization of active and passive devices in a manufacturing process, in-line electrical measurement of primitive test structures is typically performed using parametric testers. To keep track of the performance and DC characteristics of devices or other circuit elements, assorted test structures and conditions have been employed [53]. For example, FET devices of different sizes and layouts are designed and fabricated to monitor critical electrical parameters such as threshold voltage, drive current, and leakage current. Useful implications from the large collection of this heterogeneous in-line measurement data can be extracted using various statistical methods [28].

We propose a statistical method to analyze manufacturing in-line data to separate die-to-die variation and wafer-to-wafer variation from overall circuit performance variation. Using the proposed method and a set of pre-production manufacturing in-line data collected from test structures built with a 65nm SOI CMOS technology, we evaluate the relative amount of systematic die-to-die and wafer-to-wafer variations in total in-line measurement data. Along with sensitivity analysis of circuit performance to the variation parameters, the contributions of systematic die-to-die and wafer-to-wafer variation can be evaluated separately. This method enables us to assess the effect of random variation, which cannot be explained by systematic variation components.

Constrained Principal Component Analysis

Principal Component Analysis (PCA) is a linear transformation of a set of random vectors to a new set of vectors, principal components (PCs) [50]. PCs are orthonormal and are ordered so that the first few PCs retain a large portion of the total variance in the set of original variables. The first PC can be visualized as the direction on which the variance of the projection of the original vector is maximized as expressed in Equation (3.6). Here, x is the original data vector, and w_i is the ith PC. Subsequent PCs are defined in the same way except they need to be orthogonal to the previous

PCs.

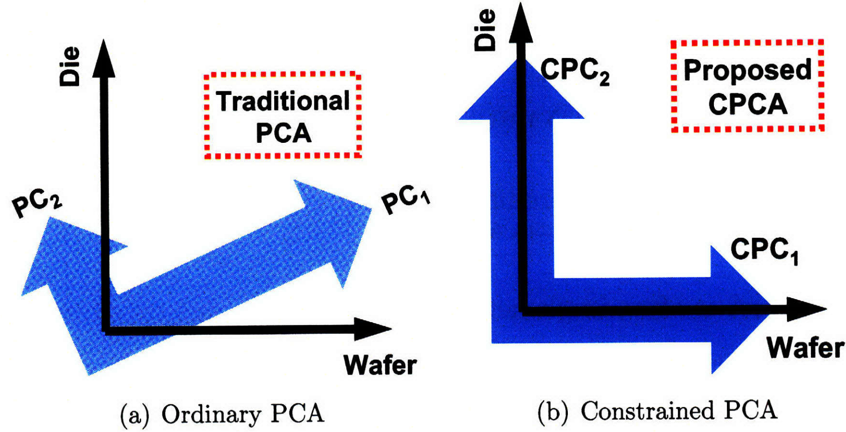
$$w_1 = \underset{||w||=1}{\operatorname{argmax}} \operatorname{var}(w^T x)$$
$$w_k = \underset{||w||=1, w \perp w_k \forall i=1,\ldots,k-1}{\operatorname{argmax}} \operatorname{var}(w^T x), \; k \geq 2 \tag{3.6}$$

In practice, PCA is often implemented with singular value decomposition of the covariance matrix of a given data set. PCA is a useful multivariate tool to reduce the dimension of the data set, to reduce noise, or to visualize the representative features of the given multidimensional data.

Here we discuss an enhanced approach appropriate to our need for understanding die-to-die and wafer-to-wafer variation. A constrained principal component analysis (CPCA) extracts constrained principal components (CPCs) which have the same properties as original PCs, but are constrained to a predefined subspace. Our goal is to extract the PCs of die-to-die or wafer-to-wafer variations separately for better understanding of the variation. In CPCA, CPCs can vary only in a guided set of dimensions which are consistent with die-to-die or wafer-to-wafer variation. Figure 3-14 exhibits the difference between CPCA and traditional PCA. Conceptually, PCA finds orthogonal coordinates which do not generally coincide with die and wafer variations. Therefore, the understanding of process variation using ordinary PCs would be perceptually difficult. On the other hand, CPCA guides the PCs to the die and wafer directions, leading to direct visualization of the variation dependencies in die-to-die and wafer-to-wafer. Only a few CPCs are examined for this purpose, because only a fraction of CPCs are sufficient to capture most of the information, as is also the case with PCs.

For our experiments using CPCA, 1109 in-line parameters from pre-production 65nm SOI CMOS technology wafers are used. A data set for each in-line parameter contains 520 samples (40 dies per wafer for 13 300mm wafers from the same lot). Various measurements from FET test structures (e.g. V_{TH}, I_{ON}, I_{OFF}), ring oscillators (ROs), SRAMs and capacitors are also obtained, as listed in Table 3.5.

Both ordinary PCA and CPCA were performed on an example data set for com-



(a) Ordinary PCA (b) Constrained PCA

Figure 3-14: Comparison of traditional PCA (a) vs CPCA (b).

Type	FET	RO	SRAM	Cap	**Total**
# of parameters	759	83	159	108	**1109**

Table 3.5: Categories of in-line parameters used in the CPCA analysis

parison. Figure 3-15 shows the cumulative variance which can be explained by the first 20 PCs and CPCs for PCA and CPCA, respectively. The first PC and CPC account for 31-34% of the total variance of the original data set. Using the first two CPCs, 57% can be explained, slightly less than the 61% for the ordinary PCs.

Experimental Results of CPCA on Frequency Divider Data

The CPC decomposition obtained from in-line data can be applied to the measured self-oscillation frequency (F_{SO}) of the CML frequency divider, to help understand spatial dependencies of F_{SO}. F_{SO} was measured from the same dies and wafers on which the in-line parameters used for the CPCA experiment were obtained. Figure 3-16 illustrates a sequence of projections of F_{SO} data onto successive CPCs in three dimensions, to visualize how F_{SO} can be reconstructed by adding one component at a time using an offset and the first four CPCs.

The bottom surface (z-axis) shows the measured F_{SO} from measured dies and wafers. The global offset shown at the top is an average of F_{SO} over all dies and wafers, thus a constant. The second surface from the top is the first CPC plus the offset, having only die-to-die (site dependent) variation. The next surface displays

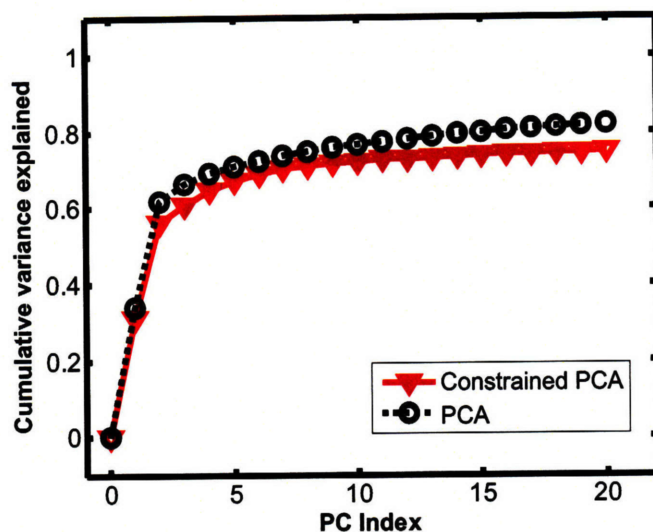


Figure 3-15: Comparison of cumulative variance explained by PCA and CPCA, for in-line DC test data.

the added contribution of the second CPC (wafer-to-wafer variation) on top of the previous surface. The sequence of the surfaces demonstrates how the original data can be successively reconstructed from or, equivalently, decomposed into a few CPCs. Note that these CPCs are calculated from the in-line DC test data and not from the F_{SO} data which is being analyzed. A weight for each CPC is obtained by projecting F_{SO} data onto each CPC space. The first four CPCs retain 66% of all the information of F_{SO} variation, which is significant because the test data (frequency of an RF circuit) and the training data for CPC calculation (in-line DC measurement data) are quite different in nature. The physical mechanism of how each in-line device-level parameter affects complex RF circuitry such as the frequency divider is elusive and challenging to analyze. However, the proposed algorithm and experimental data show that significant portion of the performance variation is systematic, and therefore, the CPCs obtained from in-line measurement can explain a substantial portion of the process variation in complex RF circuits.

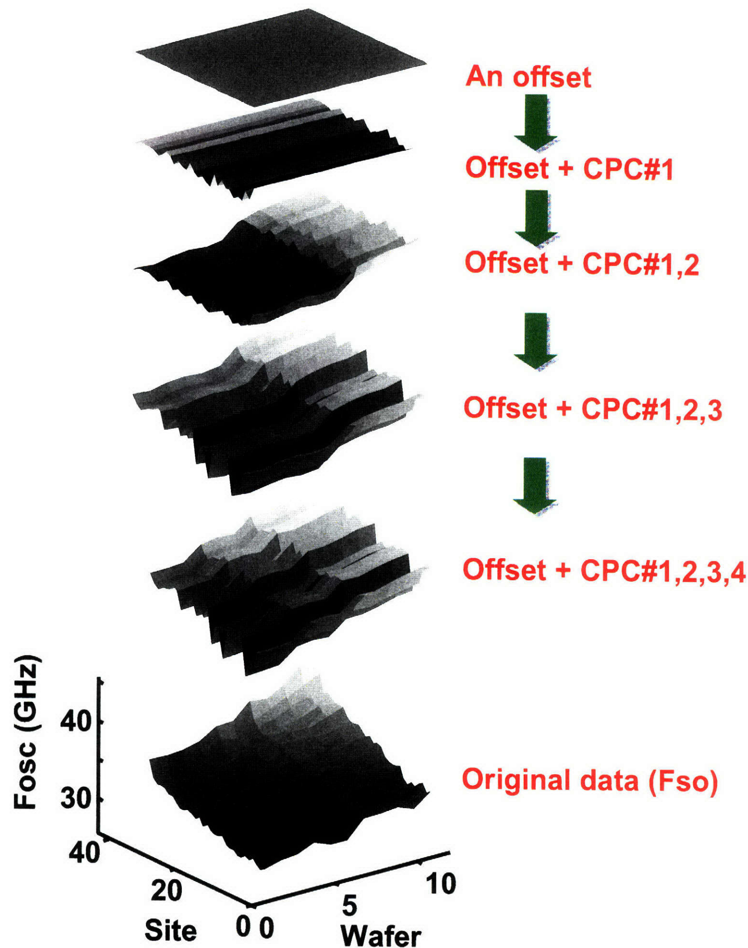


Figure 3-16: Decomposition of frequency divider self-oscillation frequency variation based on constrained principal component analysis.

3.5 Summary

In this chapter, we showed the statistical measurement results of the mm-wave VCO and frequency divider in a 65nm SOI CMOS technology. The implemented test vehicles have additional features for automated mm-wave performance measurement. The measurement data from 12 wafers and 76 dies from each wafer reveals trends in the variation of the VCO and frequency divider. The statistics of VCO measurement data show an improved frequency tuning range and parametric yield through careful device and circuit design. The variability of the divider performance is larger than that of the VCO, since the divider performance is determined by minimum sized

devices which have more relative variation. A strong systematic wafer-level pattern of the variability in the self-oscillation frequency of the divider is observed.

We provide an extraction scheme for circuit parameter variation estimation from the measurement data of the self-oscillation frequency of the divider at multiple bias conditions. The extraction method is based on the sensitivity analysis of circuit performance to the deviation of circuit parameters with a back-propagation of variation approach. Experimental results demonstrate that the statistics of each circuit parameter and the important correlation between the parameters can be successfully extracted. Additionally, process variation in electrical parameters of circuit components can be decomposed into die-to-die and wafer-to-wafer variation using a constrained principal component analysis. Constrained principal components calculated from primitive test structures can explain a significant amount of variance in the self-oscillation frequency variation of the divider, suggesting that the variation of complex circuit performance in a new technology can be predicted by the measurement data of a primitive test structure set.

Chapter 4

Robust Optimization of Analog Circuits

While analog circuits account for only a small fraction of the total transistor count in mixed signal ICs, they consume a considerable amount of the area and power of the entire system. Furthermore, analog design demands intense design effort, since analog design procedures are still strongly dependent on manual parameter tuning. In many cases, analog building blocks are responsible for costly manufacturing re-spins in advanced technologies due to faults and parametric yield loss. As a result, analog circuit design becomes a bottleneck for the design, verification, and migration of mixed signal ICs.

In contrast to digital design, analog circuit designers must consider a complex multi-dimensional performance space to optimize circuit performance [91]. In digital design, functionality, timing, and power consumption of logic gates are the primary concerns, and in many cases, the problem reduces to a transistor size optimization problem to meet given constraints of required operating frequency and power consumption. However, in analog design, there are often a large number of performance variables to be considered, and the definition of the performance space is highly dependent on the type of the analog building block. Typical output performance variables include gain, delay, noise, voltage swing, impedance, and power, as noted in Figure 4-1. Conceptually, the robust optimization of analog circuits consists of adding

a parametric yield consideration on top of the typical performance constraints.

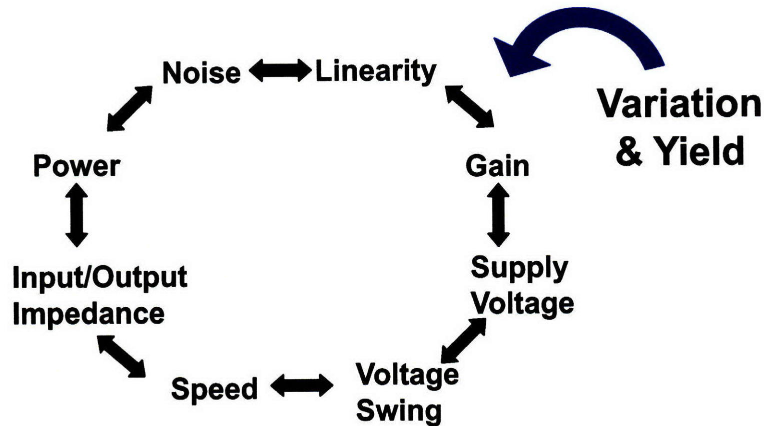


Figure 4-1: Robust optimization of analog circuits considering process variability and parametric yield constraints.

Traditionally, analog circuit design has been intensively dependent on the experience of circuit designers. However, as the operating frequency and design complexity of analog blocks, increases due to the scaling impact, computer-aided analog design and optimization tools are desperately needed to automatically size the devices and to bias circuits for optimal performance and maximum yield. In particular, as the cost of re-spins in advanced technologies is extremely high, accurate estimation of parametric yield becomes essential in the development of analog design tools.

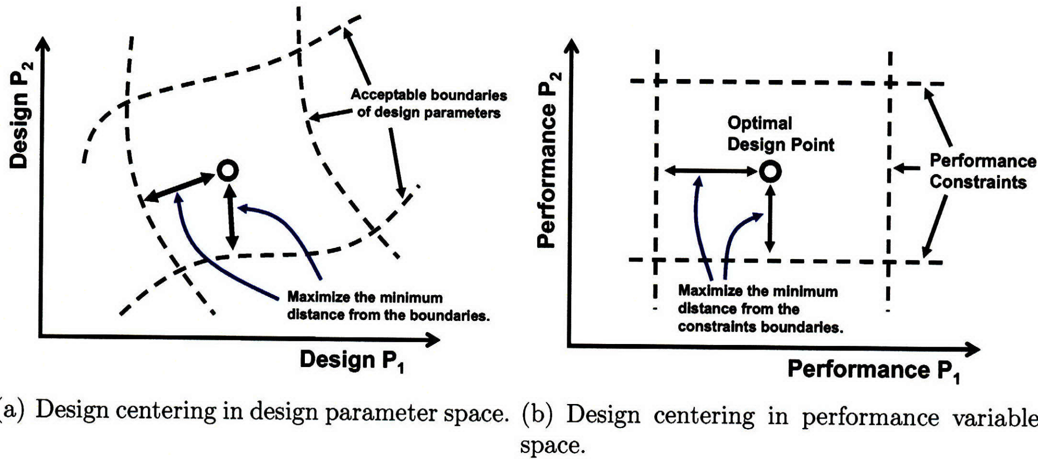
Unlike digital design, it is difficult to build a generic optimizer that can be used across the wide variety of analog building blocks since the behavioral characteristics of each analog circuit are extremely different from each other. Thus, instead of replacing analog designers, the optimization tool must help the designers by providing fast and accurate evaluation of circuit performance, and facilitating computationally efficient exploration over the multi-dimensional performance space. Furthermore, for the sake of high yield, there must be an efficient method to estimate parametric yield of analog circuits within a reasonable amount of time and computational resource.

In this chapter, we present a robust optimization methodology for analog circuit design, applied to our case study of VCO and frequency divider design. Section 4.1 introduces the background about static and dynamic optimization of parametric yield

in analog circuit design. Section 4.2 analyzes the performance variability of the VCO and frequency divider, and identifies the primary causes of functional failure in the PLL front-end circuit due to variability. The feasibility of dynamic performance optimization in the PLL front-end is verified by showing how the parametric yield changes through tuning of the bias condition of the frequency divider. The underlying trade-off in the dynamic tuning approach is also investigated. In Section 4.3, we describe a static yield optimization scheme of the PLL front-end, enabled by a numerically efficient performance evaluation model of the frequency divider. The parametric yield of the PLL front-end circuit can be optimized at the design stage by exploring over the entire design space within a reasonable amount of simulation time using the functional approximation.

4.1 Background: Yield Optimization of Analog Integrated Circuits

Various computer-aided design yield optimization methodologies for analog circuits have been suggested over the past several years [43] [63] [94]. Traditional yield improvement methodologies for analog circuits are based on *design centering*, which maximizes the margin of circuit parameters from acceptable boundaries to accommodate large-scale parameter variability. The design centering methodologies can be categorized based on the migrating parameter space: design parameter space centering and performance space oriented centering, as shown in Figure 4-2 [109]. Figure 4-2(a) shows the design parameter space centering method, which maximizes the minimum distance between a design point and the boundaries of an acceptable design space set by given performance constraints. A gradient-based deterministic optimization algorithm can be used to find the design point with maximum distance from the boundary. The computational cost of the search algorithm increases linearly with the number of design variables [5]. On the other hand, in the performance space oriented centering (Figure 4-2(b)), generalized distances between the lower and



(a) Design centering in design parameter space. (b) Design centering in performance variable space.

Figure 4-2: Design centering methodologies for indirect yield improvement.

upper specifications of output performance variables and simulation results are used to construct a suitable objective function to be optimized [66]. The performance centering methodology eliminates the costly search or generation of the acceptable boundary of the design parameter space, and provides computationally efficient operations. However, the relationship between design parameters and output performance variables are likely to be non-linear and discontinuous in analog circuits. Thus, without knowing the actual statistical distribution of the output performance variables, the centering in the performance space cannot achieve true yield maximization [109].

As the CMOS feature size scaling goes below 100nm, target performance of analog circuits becomes extremely high, and allowable performance margin of the high performance analog design has been reduced significantly. Thereby, the traditional statistical design methodologies based on design centering cannot provide properly optimized designs in advanced technologies. Instead, the effort of robust optimization in nano-scale technologies must better focus on circuit-level techniques to achieve large performance margin by using dynamic tunability and computationally efficient techniques for estimating parametric yield of complex analog circuits. We classify the robust optimization approaches of analog design as dynamic and static optimization methodologies. The following sections introduce the previous work related to the dynamic and static optimization of analog circuit yield.

4.1.1 Dynamic Optimization of Analog Circuit Yield

As industry standards for system performance become higher, analog blocks must meet more stringent performance metrics for bandwidth, gain, linearity, jitter, power, and chip area. To achieve the performance targets despite increasing variability, the degradation of performance in each building block or the operating range mismatch between these building blocks must be compensated with correction circuits that provide in-situ measurement and dynamic calibration of the circuit performance [10]. Finding an appropriate performance knob to provide a sufficient amount of tunability with allowable impact on other performance variables is a prerequisite for a dynamic compensation methodology. Design cost of adding the in-situ measurement and feedback circuitry to control the performance knob is also a critical concern.

In digital circuit design, adaptive control of power supply and body bias voltages (V_{SB}) can reduce the variation in delay and leakage power consumption of general logic gates significantly, as shown by Tschanz et al. in [103] and by Chen et al. in [26]. A similar technique can be adapted to analog circuits; for example, in differential CML comparators and summers, a DC offset arising from within-die variation can be corrected by measuring a tail current from each leg of the outputs and applying an offset current from a current digital-to-analog converter (IDAC) block to achieve constant and calibrated output values. A range of DC offset in voltage comparators can be reduced by a factor of a dozen using a low-resolution IDAC [52]. The area overhead of the IDAC circuitry is roughly proportional to the maximum range of the offset cancellation, assuming a fixed resolution. The additional chip area for the DC offset cancellation will be directly proportional to the variability, assuming that the IDAC is not affected by variability.

An adaptive post silicon tuning methodology to effectively reduce random device mismatches for analog circuits was proposed by Li et al. in [65]. A traditional approach to reduce random mismatch between supposedly identical components is simply increasing the physical size of the components. Following Pelgrom's model [85], the standard deviation of the mismatch is inversely proportional to the square

root of the component area. However, increasing the size of the devices is counter to the scaling trend, and other performance variables such as speed and noise can be degraded. Instead, a pair of components can be decomposed into N sub-components and a sub-set of the sub-components that results in the best matching characteristic can be adaptively selected by a dynamic programming algorithm. The experimental results in [65] demonstrate that the standard deviation of device mismatch exponentially decreases as area increases using such a post-silicon tuning methodology.

4.1.2 Static Optimization of Analog Circuit Yield

As the variability of critical circuit parameters and design complexity of analog circuit increase, indirect yield optimization techniques such as design centering in the performance space can no longer provide true optimization of the parametric yield of analog circuits. For accurate estimation of parametric yield, statistical distributions of performance variables must be estimated at each design point, and the parametric yield must be calculated based on the estimated performance statistics. By employing the estimated yield as an objection function, direct yield optimization techniques, such as a gradient based search algorithm, can find the optimal design point achieving the highest yield. We refer to this procedure as a static or design-time optimization of analog circuits, as opposed to a dynamic or post-silicon optimization in the previous section.

For static optimization, the trade-off between the accuracy and computational cost of yield estimation is a critical concern. The accuracy of the yield estimation can be obtained simply by a large number of Monte Carlo iterations with full SPICE simulation, consuming a large amount of time and computational resources. To reduce the computational cost in performance evaluation, a response surface model (RSM) is a commonly used technique, as shown in Section 1.3.1. When the variation of circuit parameters is sufficiently small, a linear RSM can capture a significant portion of the performance variation. The statistics of output variables modeled by the linear RSM can then easily be calculated when the parameter variation is assumed to be Gaussian.

However, as the circuit parameter variability increases, the linear RSM can no longer explain the performance variability accurately. As an improvement, non-linear RSMs (e.g., quadratic polynomials) can be utilized to capture large-scale process variability. However, such models result in non-normal distributions for circuit performance, which are difficult to capture efficiently since the distribution model is unknown. Li et al. presented a computationally efficient estimation method to characterize the distribution of output variables modeled by non-linear RSMs in [64].

Estimating parametric yield at a large number of design points to find the maximum yielding point is a simple and practical approach for robust design. The calculation of the parametric yield can be accelerated by the RSM-based yield estimation shown above. Since the computational cost to estimate the yield over the entire design space is still expensive, a gradient-based search algorithm can be employed to avoid full exploration of the design space [109]. Alternatively, equation-based yield optimization described in Section 1.3.2 can be used for computational efficiency, based on the assumption that performance variables can be well-approximated by special functions (e.g., posynomial functions) [63] [108].

The static and dynamic optimization methodologies can be combined to maximize the overall yield improvement. For digital circuit design, a unified optimization methodology involving design-time gate-level sizing and post-silicon die-level body bias tuning and their impact of parametric yield were presented by Mani et al. in [69]. In the following sections, the yield benefit in the VCO and frequency divider circuits achievable through dynamic bias voltage tuning and static design parameter optimization is estimated, and an experimental result is shown in Section 4.3.3.

4.2 Dynamic Yield Optimization of PLL Front-End

To compensate for the variation of the PLL front-end circuit dynamically, the primary cause of parametric yield loss must be identified first. Figure 4.2 shows the compar-

ison between the variation of the VCO tuning range and the divider self-oscillation frequency over a 300mm wafer. The wafer-level die-to-die variation pattern is highly systematic for both the VCO and frequency divider; the cross correlation between different wafers is more than 90% on average, as discussed in Chapter 3. From the measurement of 65 dies (sites), $3\sigma/\mu$ of the VCO center frequency variation is 3.52%, and the variation of the self-oscillation frequency is 17%. The divider variation is around five times larger than the VCO variation, since the divider performance is primarily determined by the electrical parameters of the transistors, while the performance of the LC-VCO is mainly determined by passive components such as an inductor. The physical size of the inductor is much larger than that of the minimum channel length devices; the parameter variability of the passive components is much larger than that of the active devices.

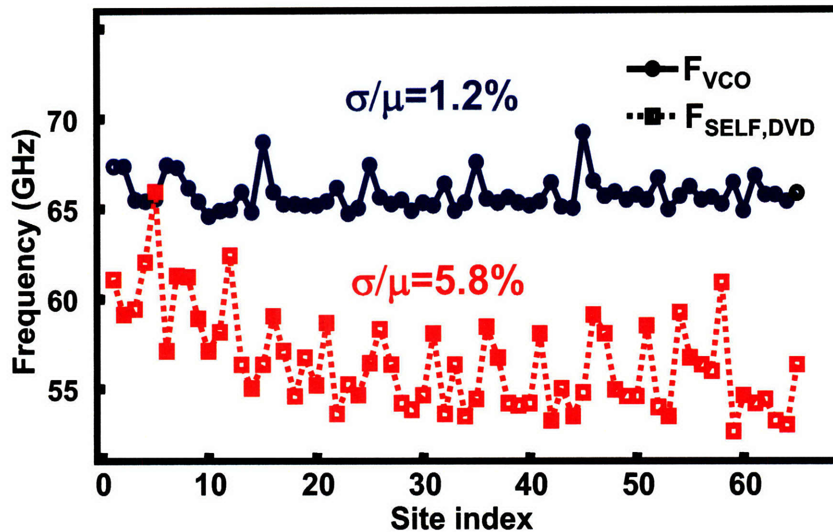


Figure 4-3: Comparison of the variation of VCO minimum frequencies and frequency divider self-oscillation frequencies over 65 dies on one 300mm wafer.

Despite the high wafer-to-wafer correlations of the individual circuits is high, the spatial correlation between the two variations, as seen from the scattering diagram in Figure 4.2, is not significant (ρ=0.17). Thus the VCO and frequency divider operating ranges do not track each other in the presence of significant inter-die variation.

This result suggests an important concern in the PLL front-end design: the divider operating range must cover the VCO tuning ranges in both of the worst case combinations (e.g., fast VCO-slow divider and slow VCO-fast divider) to guarantee high manufacturing yield.

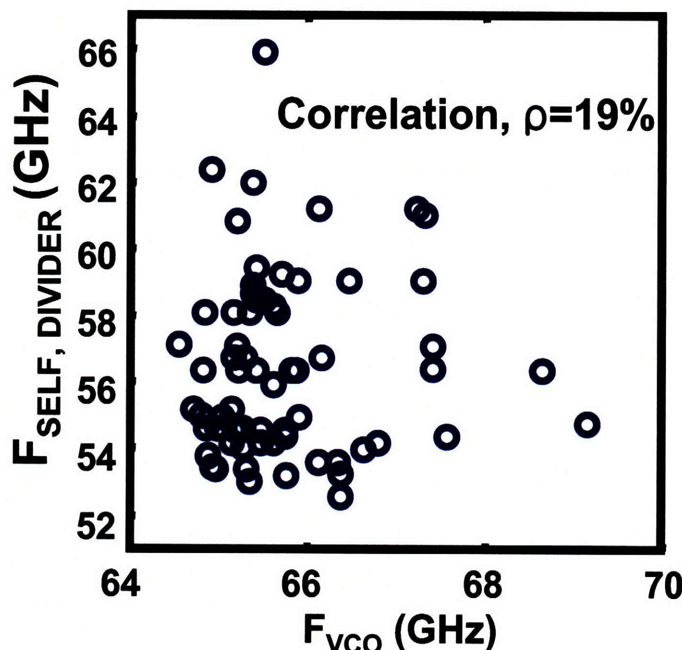


Figure 4-4: Correlation between the variation of the VCO and frequency divider over 65 dies on one 300mm wafer.

From the comparison of the variation in the VCO and frequency divider, it becomes clear that variation in the divider is the dominant cause of functional failure in the operation of the VCO-divider combination. The frequency operating range of the divider must fully cover the tuning range of the VCO in order to divide the VCO output frequency properly. However, in the mm-wave band, it is difficult to achieve more than 15% for the frequency operating range of the frequency divider, for a 0 dBm reference input signal. From the measurement data, 17% $3\sigma/\mu$ variation in the self-oscillation frequency of the divider was observed, and this can cause a serious yield loss in the PLL front-end circuit.

In this section, we analyze the failure mechanism of the PLL front-end circuit caused by the process variation in the divider.

In Section 2.3.2, simulation results showed that the frequency operating range of the CML frequency divider can be tuned by the control of a bias current. We verify that this tunability can be utilized to compensate for the variation of the divider and improve the parametric yield of the PLL front-end circuit by measurement results. We discuss a performance trade-off between the parametric yield and phase noise performance of the divider output.

4.2.1 Failure Mechanism of PLL Front-End Circuit

The change of threshold voltage in the tail transistors ($M_9, \ldots, M_{11}$ in Figure 2-6) is nearly equivalent to the V_{BIAS} changes of those transistors. For a fixed V_{BIAS}, a lower threshold voltage gives higher gate overdriving voltage and results in a larger bias current in the CML buffers. The larger bias current increases the self-oscillation frequency and reduces the frequency operating range in the frequency divider. To analyze the process variation impact on the performance of the VCO and frequency divider, Figure 4-5 illustrates how the change of V_{BIAS} affects the operation of the VCO-divider combination.

In Figure 4-5, at $V_{BIAS,1}$, the input sensitivity curve of the frequency divider is well below the VCO output power level over the VCO tuning range; the frequency divider operates in the full VCO tuning range properly. As V_{BIAS} increases to $V_{BIAS,2}$, the self-oscillation frequency increases to shift the sensitivity curve toward the VCO tuning range, but the VCO output power becomes partly below the input sensitivity curve in the VCO tuning range since the sensitivity curves becomes steeper. That is to say, the VCO no longer provides enough output power in part of the tuning range to drive the divider at the desired output frequency, and the divided frequency falls between the self-oscillation and desired divided frequencies in the failure region. V_{BIAS} can be increased even more to set the self-oscillation frequency at the center of the VCO tuning range ($V_{BIAS,3}$), but it does not guarantee stable operation over the full VCO tuning range since the input sensitivity curve becomes extremely steepened. A small amount of variation in this condition can shift the sensitivity curve out of the VCO tuning range and cause a serious mismatch problem between the operating

ranges of the VCO and frequency divider.

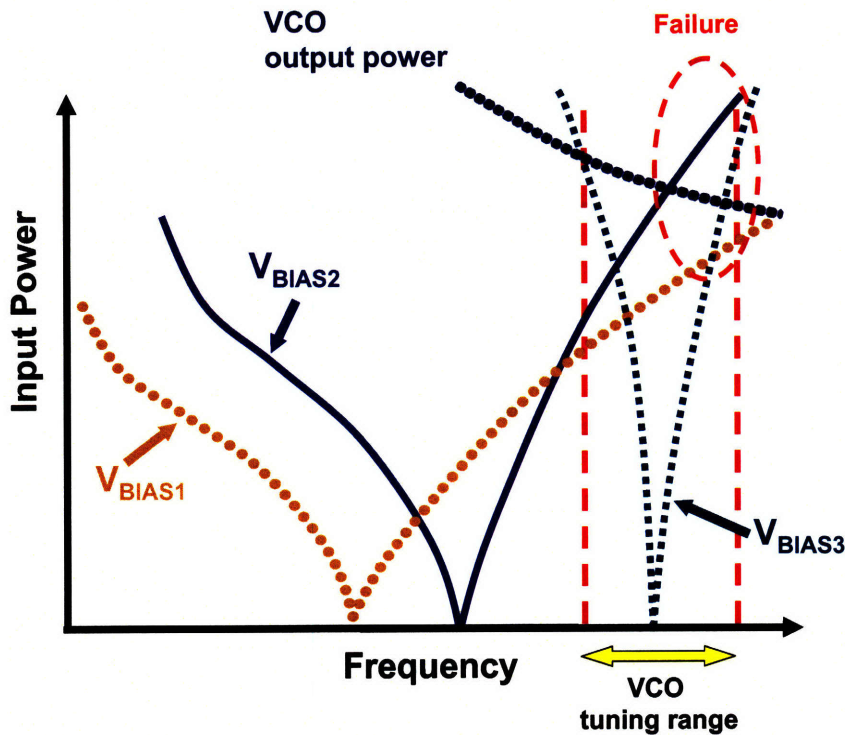


Figure 4-5: Failure analysis of the PLL front-end circuit in the presence of significant divider variation.

On the other hand, higher V_{BIAS} results in larger output swing and provides larger gate over-drive of input devices to stabilize the divider performance against threshold voltage variation. Therefore, to minimize the power consumption and functional failures in a fixed tuning range while obtaining reasonably large output swing for better phase noise characteristics, the optimal V_{BIAS} condition should be determined in the PLL front-end integration. Figure 4-6 shows the divider output frequency as V_{CTRL} changes from 0 to 1.2V for one of our 65 tested dies. When V_{BIAS} moves from 0.5 to 0.7V, the divider correctly generates the divided frequency. At V_{BIAS}=0.8V, the divided frequency is down-shifted slightly since the sensitivity curve becomes close the VCO output power and the self-oscillation frequency starts to be mixed into the divider output (injection-pulling). At V_{BIAS}=0.9V, the divider output departs from the desired output in the middle V_{CTRL} range and instead converges to the divider self-oscillation frequency, since the VCO output power is smaller than the

minimum required input power of the divider to be locked at the desired frequency. When V_{BIAS}=1.0 or 1.1V, the input power is well below the sensitivity curves, and the divider generates constant self-oscillation frequencies rather than divided VCO output frequencies.

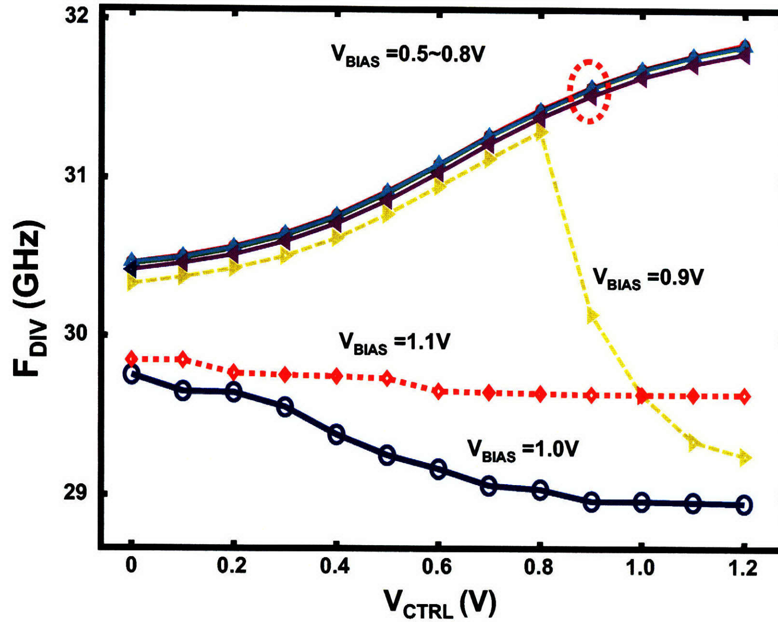
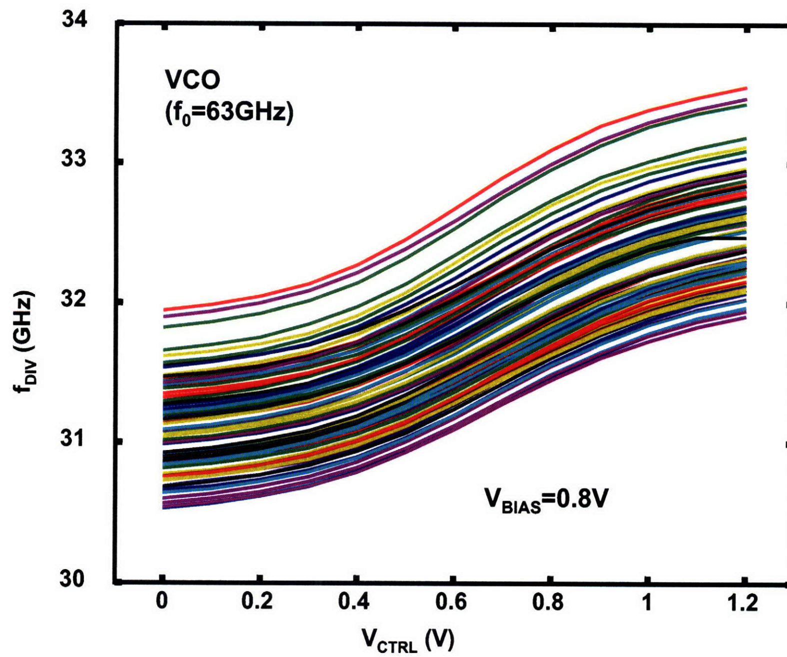


Figure 4-6: Divided output frequency of the PLL front-end circuit at different bias conditions of the frequency divider.

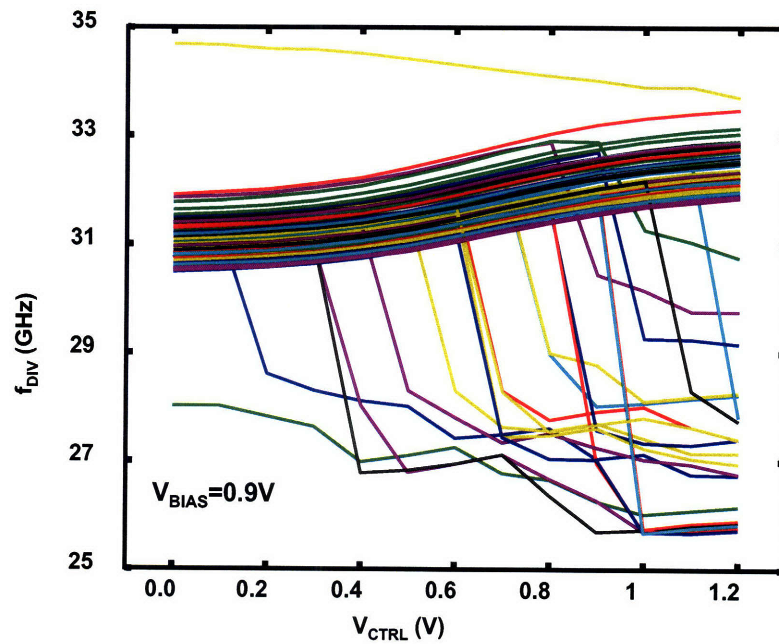
Figure 4-7 shows the output frequency of the PLL front-end circuit over the tuning range of the VCO at critical V_{BIAS} conditions. At V_{BIAS}=0.8V, all 65 dies from a 300mm wafer functions properly in dividing the VCO output over the full tuning range. However, at V_{BIAS}=0.9V, more than 50% of the dies fail to divide the VCO output over the full tuning range. Therefore, the optimal V_{BIAS} condition to achieve both maximum functional yield and the lowest phase noise characteristic must be between 0.8 and 0.9V.

4.2.2 Optimal Bias Condition for Maximum Yield

We define a sound PLL front-end die sample as one in which the divider operating range completely covers the tuning range of the VCO. Figure 4-8 shows the yield



(a) V_{BIAS}=0.8V



(b) V_{BIAS}=0.9V

Figure 4-7: VCO-divider outputs from 76 die samples over a wafer.

Type	Description
$VCODIV_1$	$VCO_1 + DIV_2$
$VCODIV_2$	$VCO_1 + DIV_2$
$VCODIV_3$	$VCO_2 + DIV_2$
$VCODIV_4$	$VCO_2 + DIV_3$

Table 4.1: Test vehicles for the PLL front-end.

of the four different test vehicles of the PLL front-end when V_{BIAS} changes from 0.4 to 1.1V. The configurations of the four PLL front-end test vehicles are described in Table 4.1. The yield of $VCODIV_1$ and $VCODIV_2$ is less than $VCODIV_3$ and $VCODIV_4$ since the center frequency of VCO_1 is higher than that of VCO_2. Comparing $VCODIV_3$ and $VCODIV_4$, the addition of inductive peaking has some benefit when V_{BIAS} is at its highest. The layout optimization does not show notable benefit between $VCODIV_1$ and $VCODIV_2$. When V_{BIAS} is from 0.5 to 0.8V, the yield of $VCODIV_3$ and $VCODIV_4$ is 100%. Considering output phase noise, V_{BIAS} of 0.8V is the optimal yielding point for $VCODIV_3$ and $VCODIV_4$. For $VCODIV_1$ and $VCODIV_2$, V_{BIAS} of 0.7V gives the maximum yield.

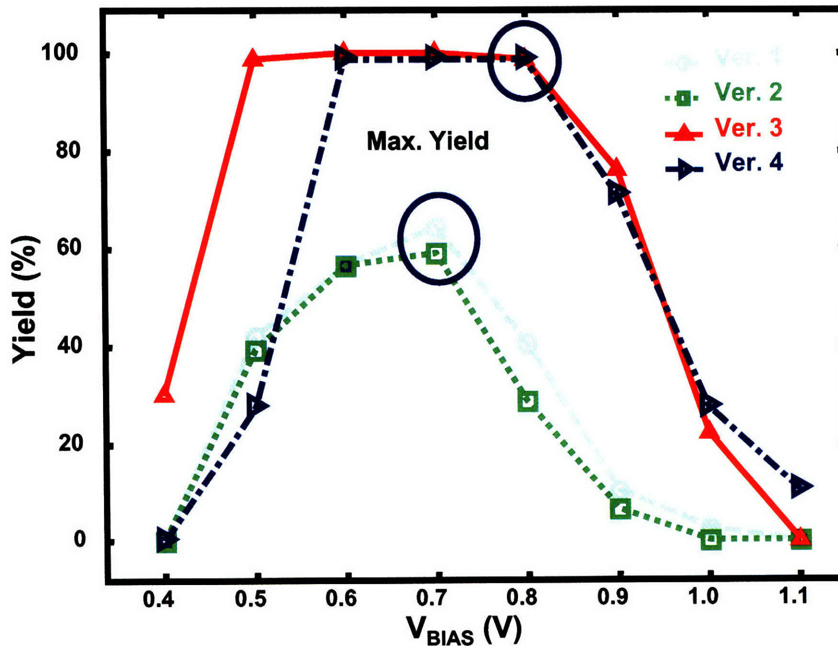


Figure 4-8: Functional yield of the PLL front-end circuit at different bias conditions of the frequency divider over four VCO and divider design alternatives.

4.3 Static Yield Optimization of PLL Front-End

While the dynamic bias tuning of the frequency divider helps to improve the parametric yield of the PLL front-end circuit, the circuit parameters must initially be optimized at design time to maximize the manufacturing yield for given specifications. Several indirect and direct static yield optimization methodologies were introduced in Section 4.1.2. The static optimization methods are based on the estimation of the circuit parametric yield using the statistics of circuit parameters. Monte Carlo is a most commonly used technique to assess the parametric yield of a given circuit. Exploration of the design space to find the maximum yielding point using the Monte Carlo yield estimation is a simple and well-defined task. However, Monte Carlo includes a large number of iterations and becomes extremely time-consuming when the circuit is large and high accuracy is needed. Avoiding the simulation cost of Monte Carlo simulations while preserving the estimation accuracy has been a critical issue in CAD research.

In the PLL front-end, the frequency divider is the main concern in variability-induced functional failure, based on the variation statistics in Section 4.2.1. The distribution of the divider maximum operating frequency must be estimated accurately to calculate the parametric yield of the PLL front-end. However, the maximum operating frequency cannot be evaluated by a single transient simulation. Instead, it requires a sequence of transient analyses to sweep the input frequency of the divider with a small incremental step, in order to find the boundary of the divider operating range accurately.

Figure 4-9 shows the input sensitivity curve and the evaluation to find the maximum operating frequency at a given reference input power. To achieve high accuracy evaluation of the maximum operating frequency, a sequence of transient simulations is needed with a fine input frequency step to find the frequency at which the divider starts to fail the proper frequency division.

A common binary search can be helpful to reduce the number of transient simulations required for the maximum operating frequency evaluation. Figure 4-10 explains

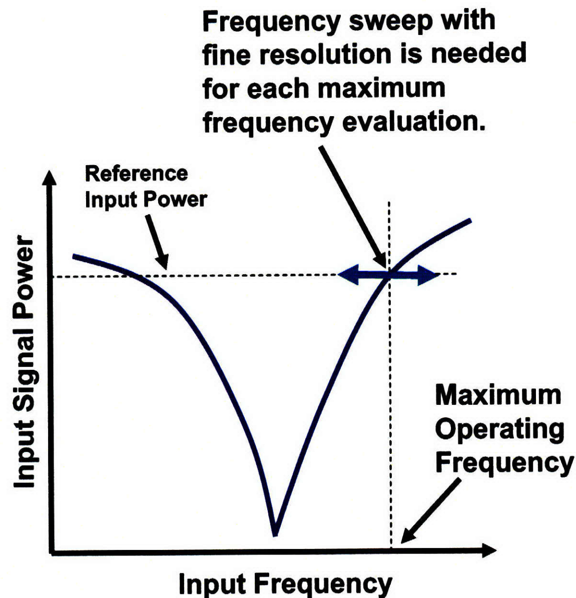


Figure 4-9: Evaluation of maximum operating frequency of the frequency divider. Sequence of transient simulation with a fine frequency step is needed to evaluate the maximum operating frequency with high accuracy.

the binary search scheme. The frequency divider is simulated with a coarse input frequency step to set an initial frequency interval which includes the maximum operating frequency. The size of the frequency interval is reduced by half at each transient simulation to check the proper frequency division at the mid-point of the interval. The accuracy of the maximum operating frequency evaluation increases in logarithmically as the number of transient analyses increases.

Even though the circuit size of the frequency divider is small, each evaluation of the maximum operating frequency demands multiple transient simulations, and the total computational cost for estimating the parametric yield over the entire design space using Monte Carlo analysis will be extremely large. To bypass the full transient circuit simulation, we need a numerically efficient functional approximation of the maximum operating frequency. In the following, we suggest a new frequency model for a CML buffer-based ring oscillator, which is fitted by only DC circuit parameters. We extend the frequency model to explain the maximum operating frequency of the divider by adding a term based on an understanding of the locking range of the

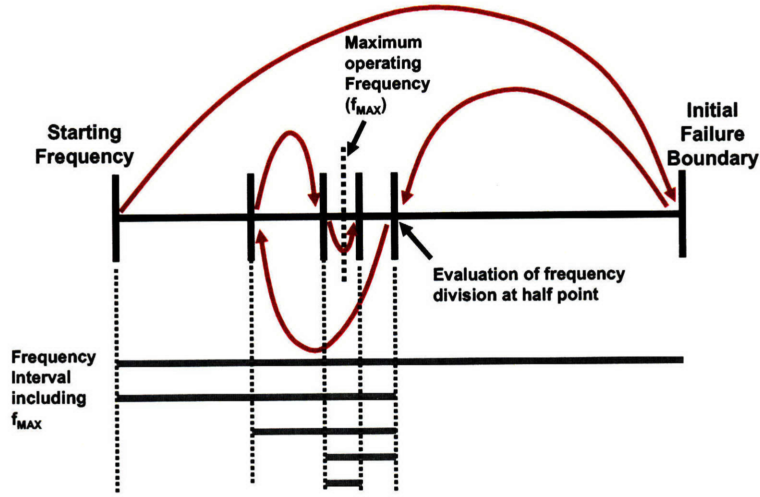


Figure 4-10: Binary search scheme of the maximum operating frequency of the divider.

ring-ILFD discussed in Section 2.3.2.

4.3.1 Estimation of Frequency Divider Performance

The maximum operating frequency of the frequency divider, f_{MAX}, can be represented as follows.

$$f_{MAX} = f_{SO} + \Delta f, \tag{4.1}$$

where f_{SO} is the self-oscillation frequency and Δf is the frequency locking range of the divider.

In the self-oscillation mode, the divider is operating as a four-stage CML buffer-based ring oscillator (Section 2.3.2). Therefore, we first build a model for the oscillation frequency of a CML buffer-based ring oscillator.

Figure 4-11 shows a simple CML delay buffer. The delay buffer consists of a differential pair of CMOS devices (M_1 and M_2), resistor loads (R_1 and R_2), a tail current source (I_{TAIL}), and lumped output capacitance (C_1 and C_2). In a CML buffer, a full voltage swing at the output node is simply

$$V_{SW} = I_{TAIL} \cdot R_L. \tag{4.2}$$

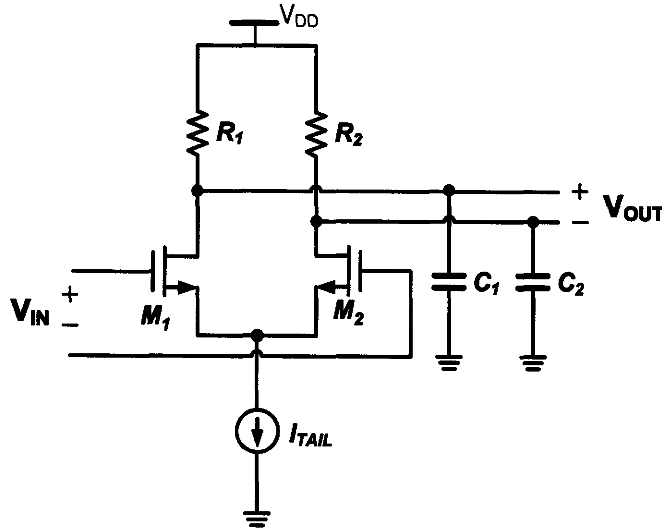


Figure 4-11: A CML differential delay buffer.

Historically, a complete analytic model of the propagation delay even in a simple CMOS inverter has been extremely hard to obtain. The model in [12] provided a surprisingly complex analytic propagation delay model in a CMOS inverter, assuming a piecewise linear input signal. However, the complexity of the model prevented the practical use of the propagation delay model in conventional circuit design. It becomes even more complicated if the buffer is used as a stage of a ring oscillator, since the assumption that the shapes of input and output signals are identical except for inversion and time delay must be added in the calculation.

Typically, the propagation delay of a CML buffer is modeled by assuming the exponential decay of the output signal as follows [3].

$$t_d = \frac{C_L \cdot V_{SW} \cdot ln2}{I_{TAIL}} = \frac{I_{TAIL} R_L \cdot C_L \cdot ln2}{I_{TAIL}} = R_L C_L \cdot ln2 \quad (4.3)$$

However, the major drawback of the model in Equation (4.3) is that it cannot explain the dependency of time delay on the tail current I_{TAIL}. The propagation delay of a CML buffer must be a function of I_{TAIL} since this current changes the transconductance of differential pair devices to give different strength of output load capacitor discharging. Appendix A shows the change of the output frequency of a ring-based

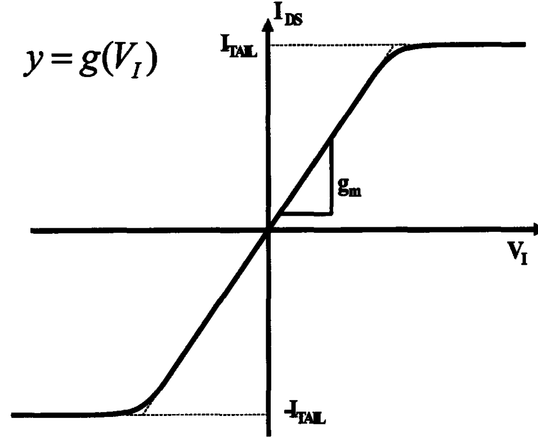


Figure 4-12: Transconductance function $g(V)$ of the differential pair in Equation (4.4).

VCO to verify the change of the propagation delay through I_{TAIL} control.

To represent the propagation delay of the CML buffer as a stage of a ring oscillator, we first start from the node equations of the CML buffer. A key assumption in the equation building is that the input signal $V_I(t)$ and the output signal $V_O(t)$ are identical except for inversion and propagation delay t_d as follows:

$$V_O(t) = -V_I(t + t_d).$$

Using the assumption above, a final differential equation as a function of $V_O(t)$ can be developed as follows.

$$\frac{dV_O(t)}{dt} = -\frac{1}{R_L C_L} V_O(t) + \frac{g(V_O(t + t_d))}{C_L}, \tag{4.4}$$

where $g(V)$ is the transconductance of the differential pair as described in Figure 4-12. From observation, Equation (4.4) is non-causal and non-linear, and therefore, it is extremely hard or impossible to obtain an a closed-form solution of Equation (4.4).

Instead, we can build an RSM of the propagation delay t_d based on the circuit parameters of the CML buffer. We reviewed in Section 1.3.1 that the accuracy of an RSM can be improved by either increasing the complexity of the fitting model or

introducing physical understanding of non-linear or discontinuous circuit behaviors. In this work, we do both to improve the modeling accuracy. Figure 4-13 shows the transient simulation result of the input and output signals in the CML buffer, assuming that the number of stages is sufficiently large for the signals to saturated to their minimum and maximum values. Since this is a differential operation, charging and discharging of output capacitance happen simultaneously. In an early part of the transition, discharging operation of a load capacitor dominates the transition, so that the signal slope can be approximated by g_m/C_L. In a later part of the transition, charging up operation from V_{DD} through the output resistor R_L becomes stronger, and the transition time is mainly determined by an $R_L C_L$ time constant. Following this analysis, we define two time delay components as below.

$$
\begin{aligned}
t_1 &= C_L/g_m \\
t_2 &= R_L \cdot C_L
\end{aligned}
\tag{4.5}
$$

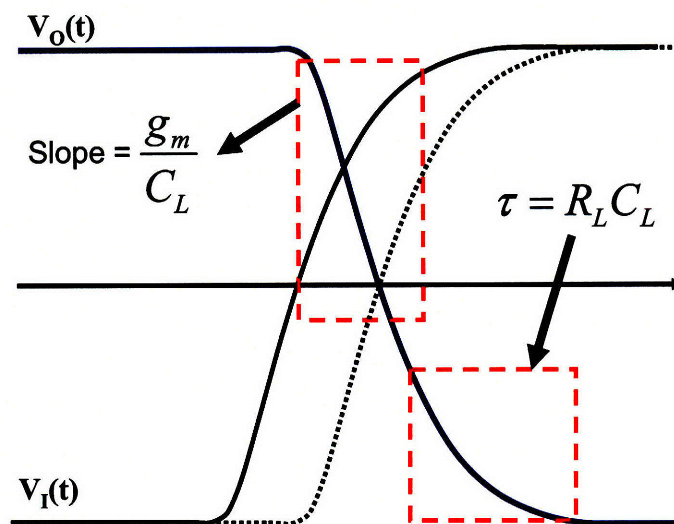


Figure 4-13: Timed input and output signals of the CML buffer, and physical time delay components.

The RSM of t_d can be developed based on the two time delay components t_1 and t_2 in Equation (4.5). We use a quadratic RSM since it provides stable model coefficient calculation and captures second-order non-linearity of output variables [110]. The

quadratic RSM can be formulated as follows.

$$\begin{aligned} \mathbf{x} &= (t_1, t_2, \ldots, t_k)^T, \\ t_d(\mathbf{x}) &= \mathbf{x}^T \cdot \mathbf{A} \cdot \mathbf{x} + \mathbf{B} \cdot \mathbf{x} + c, \\ f_{SO} &= \frac{1}{N \cdot t_d(\mathbf{x})}, \end{aligned} \tag{4.6}$$

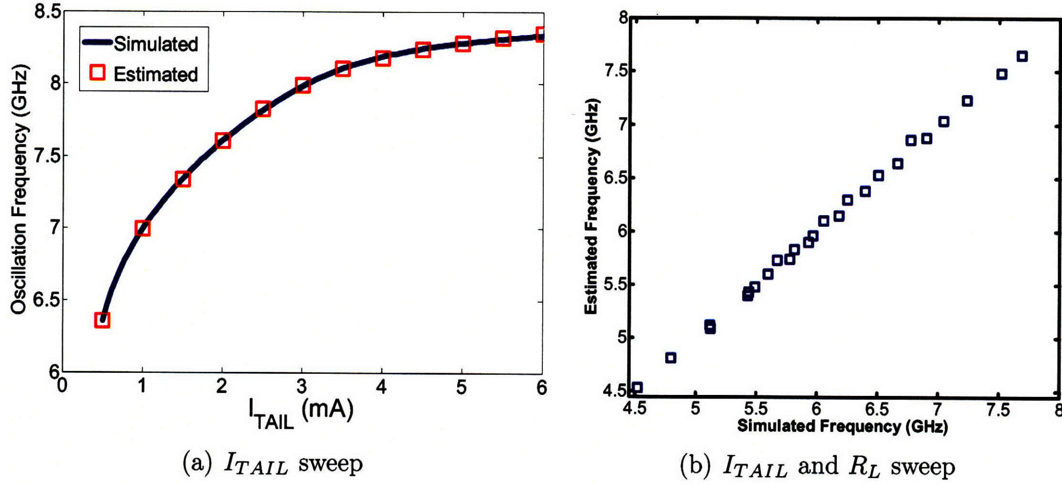
where $\mathbf{A}$ and $\mathbf{B}$ are quadratic and linear terms of the RSM, respectively, and c is a constant term. $t_d(\mathbf{x})$ is the propagation delay of each CML buffer stage, and f_{SO} is the oscillation frequency of a CML ring oscillator with N stages. The coefficients of $\mathbf{A}$, $\mathbf{B}$,and c can be calculated from the evaluated f_{SO} at multiple design points. The sample design points must cover a sufficiently large portion of design space with reasonable density to achieve an accurate RSM over the design space. Each sample point provides a linear equation defining the quadratic RSM coefficients. Therefore, the calculation of the quadratic model coefficients is a simple matrix inversion problem as follows.

$$\begin{aligned} \mathbf{f} &= \mathbf{S} \cdot \mathbf{p} \\ \mathbf{p} &= \mathtt{pinv}(\mathbf{S}) \cdot \mathbf{f} \end{aligned} \tag{4.7}$$

where $\mathbf{p} = (a_{11}, \ldots, a_{kk}, b_1, \ldots, b_k, c)$ is the model coefficients, $\mathbf{f} = (f_1, \ldots, f_n)$ is a vector of the simulated frequency at n sampled design points, $\mathbf{S}$ is a matrix of quadratic terms of $\mathbf{t}$ at the sampled design points, and $\mathtt{pinv}(\mathbf{S})$ is a pseudo-inversion of the matrix $\mathbf{S}$ which gives the least mean-square error solution of the linear equations. Since the matrix $\mathbf{S}$ is likely to be singular, singular-value decomposition (SVD) and minimum tolerance setting for the eigenvalues of $\mathbf{S}$ must be conducted for the robust pseudo-inversion of $\mathbf{S}$.

In practice, we test the quadratic RSM using a 11-stage CML ring oscillator. The design space of the ring oscillator has four dimensions: the lumped capacitance at output node, bias current of the CML buffer, size of transistors, and load resistance. The model coefficients are calculated by the simulation results using more than 10 sample design points. Figure 4-14 shows the quadratic RSM fitting result. Figure 4-

14(a) shows the comparison between the simulated oscillation frequency over a full range of I_{TAIL} and the estimated frequency from the quadratic RSM. Figure 4-14(b) shows the scattering plot between the simulated and estimated frequencies at different R_L's and device sizes. The estimation error in Figure 4-14(b) is 0.54%, which is much smaller than the 13.59% standard deviation of the simulated frequency.



(a) I_{TAIL} sweep

(b) I_{TAIL} and R_L sweep

Figure 4-14: Quadratic modeling fitting of the oscillation frequency of a CML buffer-based ring oscillator.

We next use the suggested quadratic RSM for the estimation of the self-oscillation frequency of a CML frequency divider. The time delay components of the RSM are as follows.

$$\begin{aligned} t_1 &= C_L/g_{m,\text{DIFF}}, \\ t_2 &= C_L/g_{m,\text{LATCH}}, \\ t_3 &= R_L \cdot C_L, \end{aligned} \tag{4.8}$$

where $g_{m,\text{DIFF}}$ and $g_{m,\text{LATCH}}$ are the transconductance values of the differential pair and latch devices, respectively. R_L and C_L are load resistance and lumped output capacitance, respectively. The quadratic RSM of the self-oscillation frequency is developed as a function of $\mathbf{x} = (t_1, t_2, t_3)$ and its fitting accuracy is shown in Figure 4-15(a).

In addition to the self-oscillation frequency, the frequency locking range of the

divider must be determined in order to calculate the maximum and minimum operating as in Equation (4.1). We review the analytic form of the divider locking range as follows (Equation (2.5) in Section 2.3.2).

$$\omega_L \approx k \cdot \frac{\omega_{SO}}{2Q} \cdot \frac{I_{INJ}}{I_{OSC}}$$

The divider locking range is a strong function of the self-oscillation frequency ω_{SO}, injected signal current swing I_{INJ}, quality factor of the oscillation loop Q, and current swing of the self-oscillation signal (bias current) I_{OSC}. Assuming that input signal swing is constant, I_{INJ} is proportional to the transconductance of the tail devices in Figure 2-6. ω_{SO} is already fitted to using t_1, t_2, and t_3 in Equation (4.8), and we add a new term as shown in Equation (4.9) to model the locking range ω_L.

$$t_4 = g_{m,TAIL}/I_{OSC}. \tag{4.9}$$

The loop quality factor Q is a complex function of $g_{m,DIFF}$, $g_{m,LATCH}$, R_L, and C_L [13]. We do not build a separate model for Q but still achieve a sufficient amount of fitting accuracy.

In our example, the coefficients of the RSMs for the self-oscillation frequency and locking range are calculated based on the simulation results over 125 sample design points. Similar to the CML ring oscillator, the design space covers the changes in the capacitance at output nodes, bias voltage, size of transistors, and load resistance. Figure 4-15 shows the fitting result of the self-oscillation and maximum operating frequency of the frequency divider for 0 dBm reference input signal. A 0.18μm bulk CMOS model was used for the simulation. The fitting error for the divider performance is 0.90% and 1.47% for the self-oscillation and maximum operating frequencies, respectively. In the next section, we present experimental results based on using the quadratic RSM for the estimation of the parametric yield of the frequency divider in the presence of parameter variation in threshold voltage, channel length, parasitic capacitance, and sheet resistance.

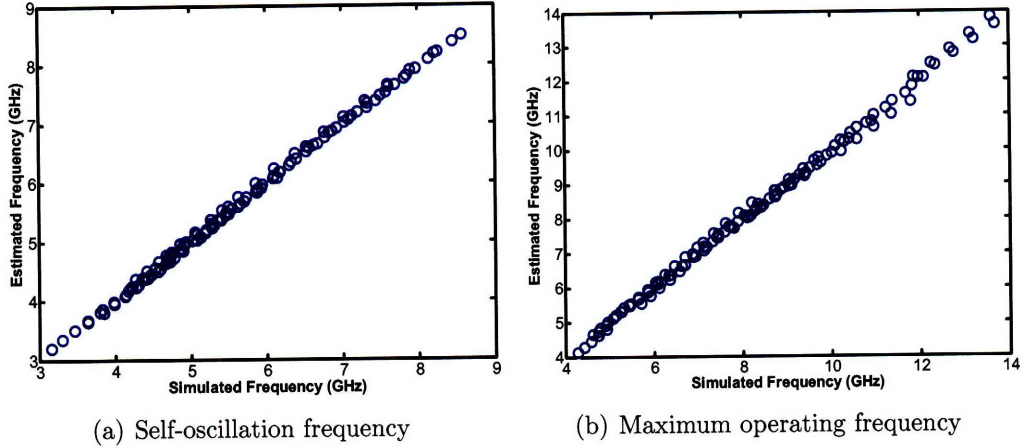


Figure 4-15: Quadratic modeling fitting of the oscillation frequency of a CML buffer-based ring oscillator.

4.3.2 Estimation of Parametric Yield of PLL Front-End

Figure 4-16 shows the general concept of statistical analysis of circuit performance of the frequency divider. The design parameters to be considered are device sizes, load resistance, and bias conditions (e.g., V_{DD}, and V_{BIAS}). The variation parameters are sheet resistance R_{SH}, threshold voltage V_{TH}, and channel length deviation ΔL. The performance variables of interest are self-oscillation frequency, maximum operating frequency, and voltage swing of the output signal. For statistical analysis of circuit performance, the design and variation parameters must be provided to a simulation model for full performance evaluation. The values of the variation parameters are sampled from pre-defined distributions and correlation models. The accuracy of the yield estimation is dependent of the number of Monte Carlo runs including the variation parameter sampling and performance evaluation.

As described in Figure 4-9, the maximum operating frequency evaluation of the frequency divider is a time-consuming task. Instead, we use the proposed quadratic RSM developed in Section 4.3.1 for estimation of the maximum operating frequency and its statistical distribution. The quadratic RSM of the maximum operating frequency is fully based on DC circuit parameters such as transconductance, bias current, parasitic capacitance, and resistance. Thus, using the quadratic RSM can accelerate the yield estimation of the frequency divider significantly compared to the full SPICE

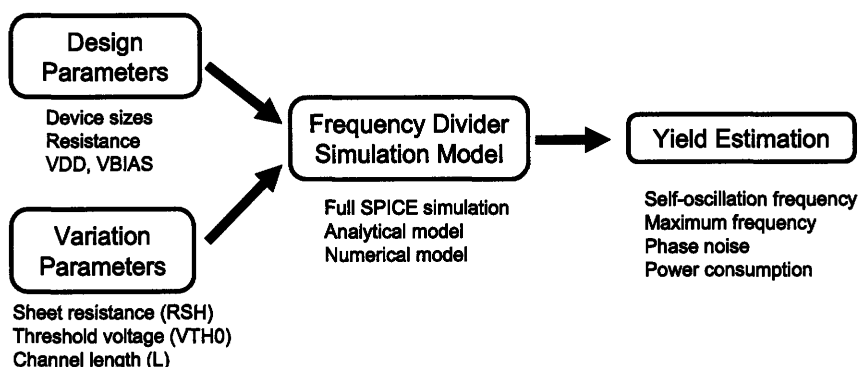


Figure 4-16: Estimation of the parametric yield of the frequency divider based on the statistics of variation parameters.

simulation-based estimation requiring transient analysis.

Figure 4-17 shows the procedure of the frequency divider yield estimation based on Monte Carlo simulation and DC analysis. First, a routine for the evaluation of the maximum operating frequency at sample design points is developed by a SKILL script in Spectre RF. We choose 125 design points to evaluate the self-oscillation and maximum operating frequencies and DC circuit parameters R_L, $g_{m,DIFF}$, $g_{m,LATCH}$, $g_{m,TAIL}$, I_{TAIL}, and C_L. The time delay components $(t_1, \ldots, t_4)$ and their quadratic terms are calculated from the DC circuit parameters. The coefficients of the quadratic RSM are calculated from the evaluated self-oscillation and maximum operating frequencies at the sample design points. The tolerance for the pseudo-inversion is set to achieve minimum fitting and estimation RMS errors. Using the fitted RSM, the statistics of the self-oscillation and maximum operating frequencies are calculated from statistics of the DC circuit parameters, and the parametric yield of the divider can be estimated. The statistics of the DC circuit parameters are gathered from Monte Carlo simulation of DC analysis which is computationally efficient.

Figure 4-18 shows the experimental results of the self-oscillation and maximum operating frequency evaluation using the quadratic RSM. We introduce 20% $3\sigma/\mu$ variation for the threshold voltage of the devices, 15% for channel length, 21% for sheet resistance variation, and 21% for parasitic capacitance variation (interconnect to substrate capacitance). The $3\sigma/\mu$ variation of the self-oscillation and maximum

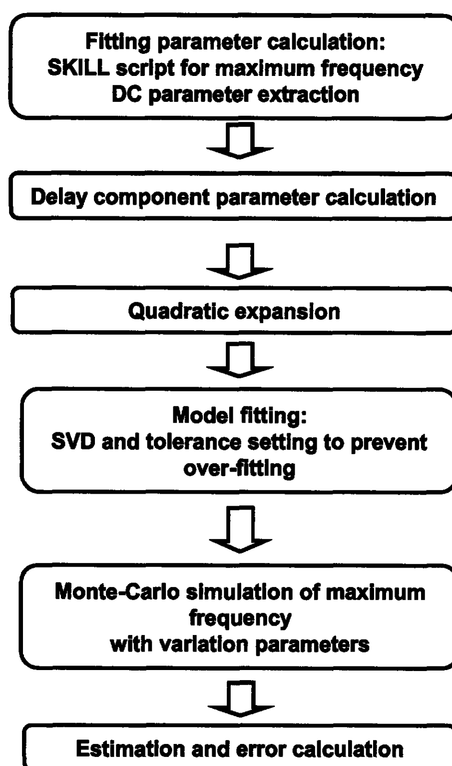
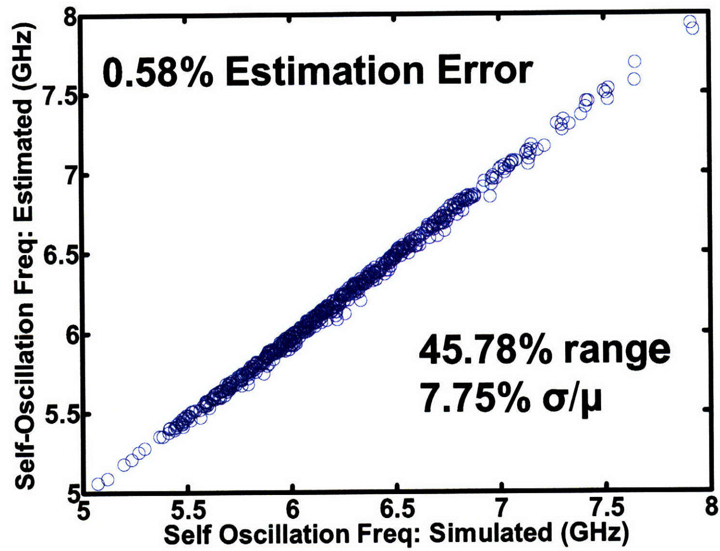


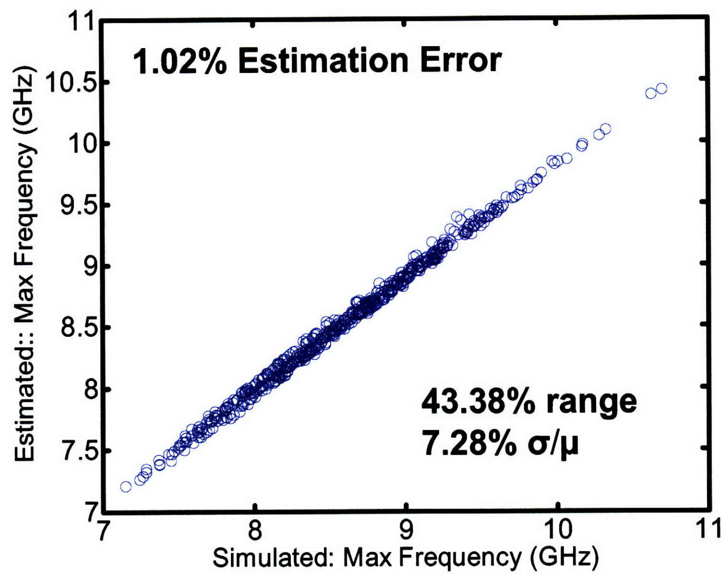
Figure 4-17: Procedure of yield estimation using DC Monte Carlo simulation results and functional approximation.

operating frequencies are 23.25% and 21.84%, respectively. The estimation errors are 0.58% and 1.02% for the self-oscillation and maximum operating frequencies, respectively, which are much smaller than the actual performance variation. This result verifies that the RSM-based yield estimation is fairly accurate enabling us to avoid full SPICE simulation.

The entire design space can be explored to investigate the design point with maximum yield by iterating the procedure in Figure 4-17 at a large number of design points. The design variables to be decided from the yield optimization are bias condition V_{BIAS}, load resistance R_L, and the size of differential pair devices W_1. For each design point, we run 500 Monte Carlo runs to obtain a sufficiently small confidence interval of the estimated yield value. From experiments, the size of the 99% confidence interval for the estimates of μ and σ from Gaussian distribution is 0.01% and 0.09%, respectively. Figure 4-19 validates an approximately Gaussian assumption for



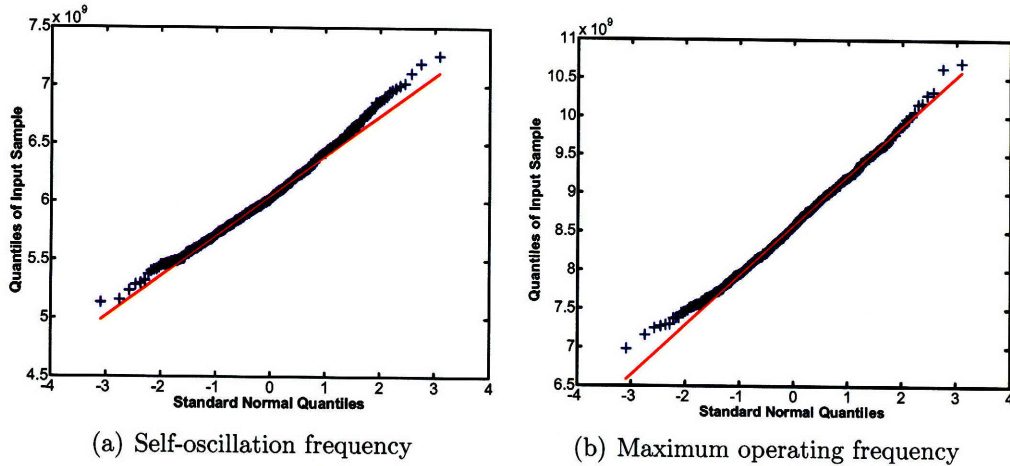
(a) Self-oscillation frequency



(b) Maximum operating frequency

Figure 4-18: Scattering plot of estimated and simulated self-oscillation and maximum operating frequencies in 500 Monte Carlo runs.

the self-oscillation and maximum operating frequency distributions.



(a) Self-oscillation frequency (b) Maximum operating frequency

Figure 4-19: Quantile-quantile normal plots of the simulated self-oscillation and maximum operating frequencies from 500 Monte Carlo runs.

In total, all possible combinations of nine different resistance values, six device sizes, and five bias conditions are simulated. For yield estimation at each combination, 500 Monte Carlo runs are performed. The elapsed time for the total simulation is less than five hours. Figure 4-20 shows the estimated parametric yield of the divider circuit over the design space for the given specifications in Table 4.2. Figure 4-20(a) shows the 3D yield surface of the yield over R_L and W_1 space at $V_{BIAS} = 1.05V$. The size of the latch and tail devices are adjusted based on W_1. Figure 4-20(b) shows the yield surface estimated at $V_{BIAS} = 1.20V$. From the experimental results, 97% parametric yield can be achieved at $V_{BIAS} = 1.05V$, R_L=450 Ω, and W_1=17μm. The yield surface shows that the parametric yield is highly sensitive to the change of R_L.

Maximum Operating Frequency (F_{MAX})	13GHz
Minimum Operating Frequency (F_{MIN})	6GHz
Output Voltage Swing (V_{SW})	300mV (0 dBm)

Table 4.2: Performance constraints of a 10GHz frequency divider in 0.18μm CMOS

4.3.3 Comparison of Dynamic and Static Yield Optimization

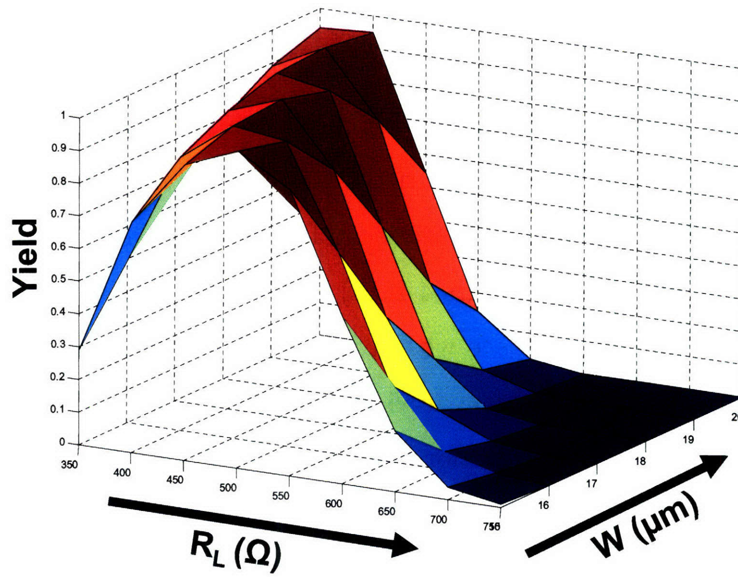
The parametric yield of the frequency divider has been optimized using dynamic and static methods in the previous sections. For the dynamic optimization, we showed

that the bias condition of the frequency divider can be tuned for an individual die sample to maximize the number of dies satisfying given performance constraints. The design parameters can be optimized at design time to maximize the parametric yield by statistical yield analysis of circuit performance for given parameter uncertainties.

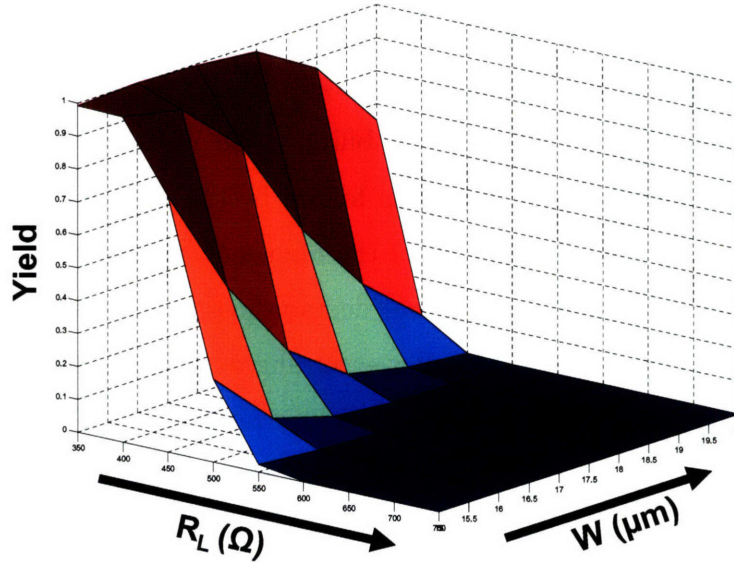
Both dynamic and static optimization methods can be combined to obtain additional yield benefit. From the simulation results of the static optimization in Section 4.3, the tunability of the bias condition can be adapted to observe the additional benefit on the parametric yield. Figure 4-21(a) shows the parametric yield of the frequency divider over the design space with dynamic tuning of V_{BIAS}. Figure 4-21(b) shows the comparison of the parametric yield with and without V_{BIAS} tuning. The dynamic V_{BIAS} tuning gives 2% additional yield benefit at the optimum design point obtained in Section 4.3.2. The benefit of dynamic V_{BIAS} tuning becomes large as the design point is further away from the static optimal point.

4.4 Summary

In this chapter, we discussed robust optimization methodologies for analog circuit design. We analyzed the performance variability of the VCO and frequency divider to investigate the main cause of functional failure by the variability. The trade-off in tuning the frequency operating range of the frequency divider was investigated in terms of parametric yield and performance degradation such as output phase noise. We showed how the parametric yield varies according to the change of the bias condition to validate the concept of dynamic yield optimization in the PLL front-end. We proposed an efficient numerical model for the evaluation of the maximum operating frequency of the frequency divider. Using the functional approximation of the frequency divider performance, the parametric yield of the PLL front-end circuit can be explored over the entire design space to optimize the parametric yield for the given parameter uncertainty. The static and dynamic optimization methods were jointly combined to evaluate additional yield benefit.

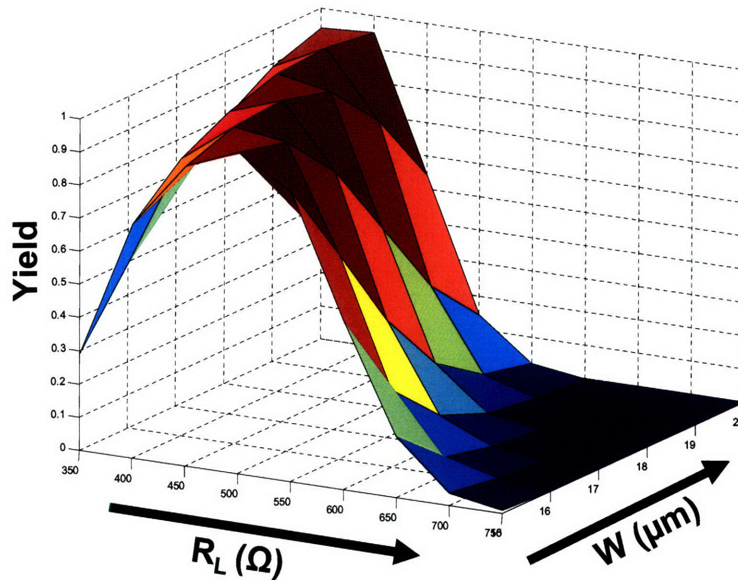


(a) $V_{BIAS} = 1.05V$

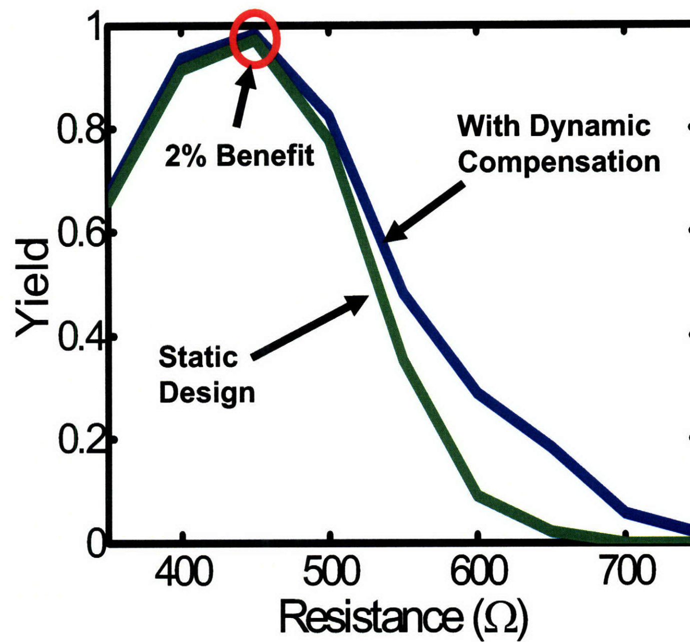


(b) $V_{BIAS} = 1.20V$

Figure 4-20: Functional yield of the frequency divider over the design space for the given specifications at $V_{BIAS} = 1.05V$ and $V_{BIAS} = 1.20V$.



(a) Yield surface at V_{BIAS}=1.05V



(b) Comparison of w/ and w/o dynamic compensation

Figure 4-21: Parametric yield of the frequency divider over the design space with dynamic V_{BIAS} tuning.

Chapter 5

Conclusion and Future Work

This thesis focuses on the design, analysis, and implementation of manufacturable mm-wave analog building blocks in a deeply scaled CMOS technology. We provided statistical measurement of circuit performance variation and robust optimization strategies to improve parametric yield. In this chapter, we summarize this thesis in Section 5.1. Ideas for future work as extensions of some of these contributions are discussed in Section 5.2.

5.1 Summary of Thesis

As the operating frequency of CMOS analog circuits reaches the mm-wave regime at 50GHz frequencies and beyond through the continuous scaling of MOS transistor feature size, parametric yield loss in analog circuit design by aggravated process variability becomes a serious concern. Multiple manufacturing steps contribute to the variation of CMOS device and interconnect parameters and overall circuit performance. A benchmarking task to characterize the performance-level variation properties of complex analog circuits is now required, in order to provide useful guidelines to the analog designer to build high yielding designs. To optimize parametric performance yield, statistical design methodologies have been suggested, whose goal is not only to meet the design specifications for nominal circuit performance, but also to achieve desired parametric yield in the face of process variability.

In this thesis, we have contributed the design and implementation of a mm-wave PLL front-end circuit, containing a VCO and frequency divider as high-speed building blocks of a PLL. A 77GHz LC-VCO is designed to achieve a wide frequency tuning range for improved manufacturability by employing design features including a complementary topology for phase noise improvement and power reduction, an accumulation-mode varactor for a wide capacitance tuning ratio, relaxed pitch devices for reduced parasitic capacitance, and a high-Q inductor for good phase noise. A 2:1 frequency divider is designed to operate up to 90GHz of input frequency, using a ring-ILFD architecture for a wide frequency locking range. The self-oscillation frequency and frequency locking range of the divider are analyzed to obtain analytic forms of the divider performance, which are used for statistical optimization of the divider performance. The PLL front-end circuit is implemented in 65nm SOI CMOS with various technology features for high-speed analog circuit design.

The statistical measurement results of the VCO and frequency divider circuits were shown from a large number of high frequency measurements over multiple wafers. The measurement data for 12 wafers and 76 dies from each wafer reveals trends of variation in the VCO and frequency divider. The statistics of VCO measurement data show an improved frequency tuning range and parametric yield by the device and circuit optimization. A strong systematic wafer-level pattern of the variability in the performance of the frequency divider is observed. The performance variability of the VCO and frequency divider was analyzed to investigate the main cause of functional failure by the variability.

An extraction scheme to obtain circuit parameter variation from the frequency divider measurement data was proposed. The extraction method is based on the sensitivity analysis of the divider self-oscillation frequency to the deviation of critical circuit parameters such as threshold voltage, load resistance, and lumped parasitic capacitance. Experimental results show the statistics of each circuit parameter and the important correlation between the parameters. Furthermore, process variation in electrical parameters of circuit components can be decomposed into die-to-die and wafer-to-wafer variation using a constrained principal component analysis. Calcu-

lated constrained principal components from primitive test structures can explain a significant amount of variance in the self-oscillation frequency of the divider, showing that the variation of complex circuit performance in a new technology can be predicted by the measurement data of a primitive test structure set.

We discussed general robust optimization methodologies for analog circuit design, and specialized static and dynamic optimization schemes for the VCO and frequency divider. As an example of dynamic optimization, we verified that the parametric yield of the PLL front-end can be improved by tuning the bias condition of the frequency divider, while there exists a trade-off between the parametric yield and phase noise performance. To enable static optimization, we propose functional approximation of the maximum operating frequency of the frequency divider. Using the functional approximation, the parametric yield of the PLL front-end circuit can be estimated over the entire design space within a reasonable amount of simulation time, and the optimal design point can be investigated.

5.2 Future Work

As noted in the ITRS road map, sub-100nm CMOS technologies have become one of the viable solutions for the implementation of mm-wave applications [8]. Compared to SiGe and III-V technologies which have been conventionally used for mm-wave applications, CMOS has a strong advantage in low cost and high density integration. However, there are negative scaling impacts on analog circuit design as well, and in particular, aggravated process variability of the device and interconnect performance causing parametric yield loss becomes one of the main design concerns [77].

To achieve high yielding analog circuits as building blocks of high frequency mixed-signal applications, parametric yield of such analog circuits must be predicted at the design stage and proper variability mitigation techniques must be utilized. In this thesis, we showed successful integration of mm-wave analog building blocks in a CMOS technology and verified their manufacturability based on high frequency measurement data over multiple wafers. Among the contributions of this thesis, the

methodology used for extraction of important circuit parameters could be extended to provide a general benchmarking scheme for fast characterization of analog design aspects of new technologies. Furthermore, an abundant resource of digital processing in scaled CMOS technologies can provide opportunities for the dynamic compensation of performance variability in analog circuits. Here, we discuss the future trend of process variation in analog circuits, and suggest analog technology benchmarking and digitally-assisted robust analog design as future work for robust analog circuit design.

5.2.1 Future Trend of Process Variation in Analog Circuits

The enhancement of performance and power consumption in CMOS circuits driven by the feature size scaling will continue in analog and digital circuits. Together with increasing manufacturing cost in high-end CMOS processes, process variability and corresponding parametric yield loss will continue to be an increasingly challenging issue in future process nodes. In digital circuit design, it is well known that the leakage power consumption will be a dominant factor in the variation in total power consumption, due to the exponential dependency of leakage current to threshold voltage variation. However, it is difficult to define a general future trend of variation in analog circuits since analog circuits have a large number of performance variables to be considered, and the variation of each performance is a mixture of multiple sources of variation with different physical characteristics and statistical properties.

Generally, the physical sources of variation can be categorized into systematic and random components. From the measurement results and statistical analysis of the VCO and frequency divider in Chapter 3, we verified that the performance variation has a large systematic component. Typically, wafer-level variation in critical dimension (CD) of transistor gates and back-end variation by etching and CMP non-uniformity are primary causes of the systematic variation in circuit performance. While the amount of systematic variation is largely determined by the quality of manufacturing control, various design-level regularization techniques have been used to reduce the systematic variation significantly (e.g., etch and CMP dummies in lay-

out). Restrictive design rules (e.g., uni-directional poly-silicon gates, layout density rules, etc.) also help to improve the regularity of the active and passive device performance across dies and between wafers. As a result, together with the improvement in physical manufacturing control, one can expect that the absolute amount of die-to-die variation of passive component oriented circuits (e.g., LC-VCO) will be reduced by the regularization techniques. Also, the reduction of wafer-level CD variation can mitigate the die-to-die variation of channel length dependent device and circuit characteristics (e.g., frequency divider performance when $V_{BIAS} \gg V_{TH}$). However, as the operating frequency and required precision of analog circuits increases in advanced applications, the relative impact of the systematic variation can also increase.

On the other hand, the random portion of process variation generally keeps increasing as geometric feature size shrinks down. Typically, threshold voltage variation by random dopant fluctuation and line-edge roughness in transistor gates and metal wires are major sources of the random variation in circuit performance. The theoretical degradation of threshold voltage matching between two devices with smaller feature size is well predicted in Pelgrom's model. The impact of the line-edge roughness will become more significant as the physical dimension of the device and metal wire shrinks, because the gap between the wavelength of photo-lithography and actual feature size has increased since the 180nm process node and likely will keep increasing [102]. The portion of the random variation in total performance variation has increased significantly and the trend will continue in future process nodes [81]. Therefore, the parametric yield loss of match sensitive analog circuits (e.g., SRAM cells, analog-to-digital converters, phase noise of ring oscillators, etc.) will become an increasingly challenging issue in future process nodes.

Alternatively, the process variability of circuit performance can be improved dramatically by the introduction of new technologies. For example, the introduction of metal gates in a CMOS technology reduces threshold mismatch due to variations in gate doping, while improving the maximum oscillation frequency F_{MAX} by reduced gate resistance. The measurement results in [56] show that the process variability of CMOS ring-oscillator performance has been reduced in 45nm high-k metal gate

technology compared to 65nm poly-silicon gate technology. Metal wire resistance variation after CMP has also been significantly mitigated by the improvement of process control in etching and CMP in the 45nm technology. Though new technologies will be able to provide discrete improvement in variation trends, the feature size scaling based variation trend will continue after each introduction of the new technology.

5.2.2 Technology Benchmarking for Analog Circuit Design

The demand for rapid time-to-market of high performance mixed-signal applications has become more stringent and challenging due to the fast evolution of technology. Though innovative circuit ideas are still a considerable contributor of circuit performance enhancement, the improvement in the device and interconnect performance by technology evolution (e.g., scaling, or stress-induced mobility enhancement) becomes a more dominant factor in today's semiconductor manufacturing.

Conventionally, designers need model parameters for active and passive devices to verify performance benefits and re-optimize previous circuit designs in a new technology. However, characterizing a complete set of the model parameters (e.g., in BSIM4 or PSP compact models) is an extremely time-consuming task, and it can be highly costly given the shortened life cycles of today's process nodes. Instead, in advance of the complete characterization of the model parameters, the new technology can be benchmarked by using well-designed test structures whose measurement data can enable early and accurate prediction of circuit performance enhancement. Furthermore, potential problems such as aggravated process variability in certain circuit performance variables can be characterized in advance and feedback can be provided for fine-tuning of the manufacturing process.

Technology benchmarking has been conventionally used in digital circuit design. Table 5.1 shows common metrics used in the characterization of a digital microprocessor manufacturing process. An array of test devices in different configurations in terms of size, device option, and bias condition are implemented in test fabrication runs to measure the DC performance of devices. For test of delay and power consumption in digital logic, ring oscillators are commonly used as a benchmarking unit.

	Parameter	Description
Devices	$I_{DS,LIN}$	Drain current in the linear region
	I_{GATE}	Gate leakage current
	I_{OFF}	Off current (subthreshold leakage)
	I_{ON}	Saturation current when)
	$V_{TH,\ LIN}$	Threshold voltage in the linear region
	$V_{TH,\ SAT}$	Threshold voltage in the saturation region
Ring oscillators	I_{DDA}	Active current
	I_{DDQ}	Quiescent current
	Frequency	Oscillation frequency

Table 5.1: Common metrics for the characterization of a digital microprocessor manufacturing process.

The oscillation frequency of the ring oscillator for different configurations indicates the time delay of logic gates, including the interconnect impact. Active and quiescent currents of the ring oscillator provide information to calculate the active and leakage power consumption of digital logic and microprocessors.

In contrast to digital circuits, analog circuits have a more diverse set of performance variables, as discussed in Chapter 4. Even though some of the metrics in Table 5.1 can be shared for analog benchmarking, a unique set of metrics to compare the benefits of new technology nodes in analog circuit design are strongly required since there are more performance variables beyond delay and power to be considered in analog circuit design. Traditionally, cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}) are the metrics used to compare the performance capability of analog manufacturing processes. RF performance defined by f_T and f_{MAX} of CMOS devices and interconnects in 65nm and 45nm SOI CMOS was reported in [61] and [60], respectively.

The list below shows several important metrics for analog circuit design.

- Cut-off frequency f_T and f_{MAX} of the devices
- Transconductor efficiency g_m/I_D
- Available voltage swing
- Intrinsic gain g_m/g_{ds}

- Noise figure NF
- Input offset ΔV_{IN}
- Temperature coefficient

For benchmarking of the metrics above, well-designed test structures for efficient measurement of the analog performance metrics are needed. Several example test structures to measure the metrics above were suggested in [91]. In this thesis, we showed that the self-oscillation frequency of the divider can be used as a variation probe for high frequency circuit parameters. As shown in Section 2.3.2, the analytic form of the divider self-oscillation frequency g_m/C_P implies the cut-off frequency of the device (f_T=g_m/C_{gs}) while C_P is a lumped sum of the C_{gs} of differential pair and latch devices and C_{wire}. While direct measurement of multi-hundred gigahertz f_T is extremely difficult, the variability of f_T can be extrapolated from the self-oscillation oscillation frequency measurement statistics.

In addition, we verified in Section 3.4.1 that the variability of critical circuit parameters can be extracted by using the self-oscillation frequency measurement data at multiple divider bias conditions. The number of parameters to be characterized can be increased by using multiple configurations of the divider circuit to reduce the co-linearity between the deviations of some parameters, which introduces a singularity problem during the matrix inversion in Equation (3.4).

Obtaining performance characteristics and their variation statistics using mm-wave measurement equipment is still a costly task. To reduce the cost of measurement, on-chip digital measurement interfaces are needed for efficient characterization of mm-wave circuit performance. In this work, the oscillation frequency can be divided down further by using deep sub-dividers until it can be measured by conventional digital counters. Such digital interfaces can enable an array of mm-wave test structures to characterize within-die variation of the VCO and frequency divider performance; understanding this within-die variation is likely to be important in the implementation of mm-wave imaging system which use an array of PLLs within each chip for fine-resolution of images.

5.2.3 Digitally-Assisted Robust Analog Design

Before it became a critical problem in digital circuit design, process variability was a well-known problem in analog circuit design. A wide range of analog circuits are highly matching sensitive, and within-die variation in active and passive components can cause serious performance degradation such as a voltage offset and non-linearity. Various techniques have been proposed and used to reduce the variability impact on analog circuit performance (e.g., symmetric layout, analog or digital calibration, dynamic element matching, larger device area).

While the speed and power performance of CMOS devices have been continuously improved, the matching property has been degraded by technology scaling. On the other hand, as the cost of complex digital functionality has been reduced by scaling, the design-overhead of utilizing digital calibration in analog circuits has also decreased. As a result, digitally-assisted analog design becomes a substantial trend in high performance and high precision analog circuit design [47]. In precision oriented analog circuits such as analog-to-digital converters, digital calibration techniques for the mismatch between devices and capacitors have been intensively studied for decades [58] [78].

In the PLL front-end circuit in this work, we verified that adaptive tuning of the bias voltage (V_{BIAS}) of the frequency divider can improve overall parametric yield. For actual implementation of the adaptive bias tuning, digital calibration is a promising design option for its low cost and versatile usage. Figure 5-1 shows the concept of digital calibration of V_{BIAS} using in-situ frequency measurement circuitry, a digital processor, and digital-to-analog converters (DACs). The digital processor must be equipped with an efficient algorithm to find an optimal V_{BIAS} by measuring the VCO and divider characteristics at different conditions of V_{BIAS}. The output frequency of the frequency divider must be deeply divided down using a chain of frequency dividers to be measurable using a digital counter. Thermal and flicker noise of DAC outputs must be carefully considered, since these are directly related to the phase noise of the divider output. Digital calibration can provide additional benefits such as the

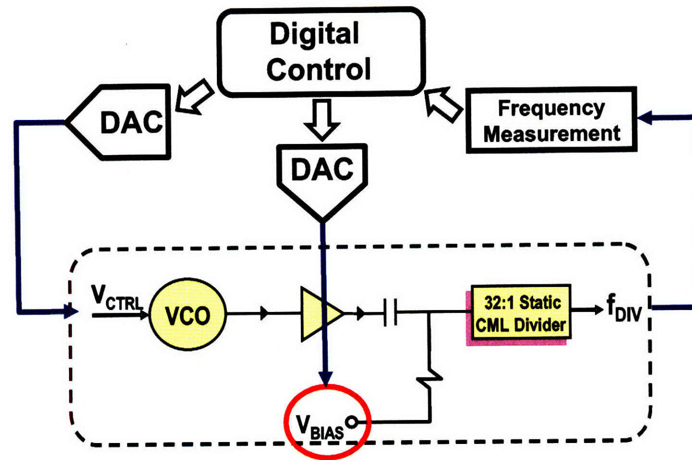


Figure 5-1: Digital feedback control of V_{CTRL} and V_{BIAS} and divided frequency measurement to set optimized V_{BIAS} voltage.

compensation of aging impact on circuit performance by low frequency calibration. The output performance variables to be tuned by digital calibration can be extended to phase noise, power consumption, I/Q mismatch.

Appendix A

Process Variability and Statistical Yield Analysis of High-Speed Ring Oscillators

The design and test of analog RF building blocks in SoC applications have been challenging due to the high-frequency operation and broad specifications of analog RF circuits. Considering the *chip-limited yield* (CLY) failure due to analog performance shortfall, analog *design-for-test* (DFT) methodologies for RF test are essential to improve testability and yield estimation of analog building blocks.

The main difficulty of analog design for RF DFT lies in signal speed. In a mixed-signal SoC, analog and RF function blocks are driven to the maximum speed to provide clocks in digital systems and carrier frequencies in communication channels. The operating frequency of the analog front-end circuits is higher than the affordable speed of digital interfaces. Therefore, analog RF circuits are unlikely to have systematic on-chip assistance to measure the performance variables accurately. Severe signal attenuation in high frequency bands is another reason for the difficulty of measurement unless proper RF buffering is provided. In total, it is difficult to have a standardized digital interface as used in digital DFT, and the test equipment and cables for RF test must be highly customized depending on circuit operating conditions and output variables.

Furthermore, as CMOS scaling continues to enhance the system performance and power, process variation in the performance of nano-scale device and interconnect becomes a serious issue [79]. In particular, for SoC applications, analog and RF building blocks can be a critical reason for limited overall system yield since the analog and RF blocks are operating at the highest frequency of the system, as they are sensitive to die-to-die and within-die variations in the deeply scaled CMOS process [14]. Therefore, the variation of analog and RF circuit performance must be fully characterized using dedicated test structures for accurate yield learning [91]. Systematic approaches are needed to test the various output performance variables (e.g., gain, noise, power, frequency range, and etc.) of analog and RF circuits over a number of samples within a short period of time.

The main contributions of the RF DFT in this chapter are as follows.

- The integration of the analog design and automated RF test and measurement plan for multiple performance variables at an early design stage.
- Implementation of assistance circuitry for reliable automated RF measurements over a number of analog circuit samples.
- Characterization of the variability of phase noise and output frequency over the

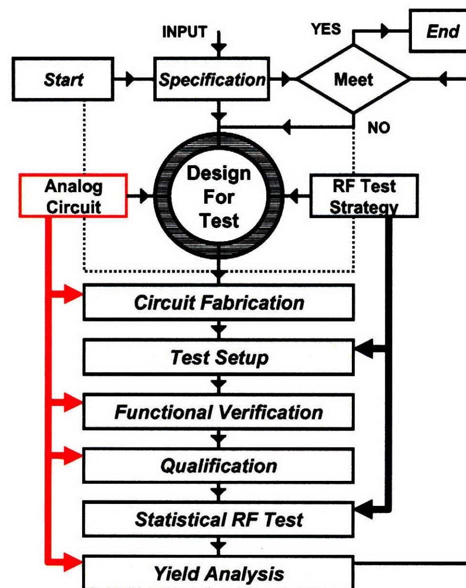


Figure A-1: Process flow diagram of analog design for RF test platform.

Table A.1: Digital DFT vs. RF DFT

	Digital DFT	**RF DFT**
Motivation	Structural test	Test feasibility
Problem	Complexity	Speed
Design	System	Ckt.+Env.
Test setup	Standard	Custom
Test process	Test and verify	Verify while test
Test case	Automatic	Manual
Pass/fail	Binary	Continuous

entire wafer.

- Yield analysis of a high-speed VCO based on measured statistics of phase noise and output frequency.

The RF DFT process flow in Figure A-1 captures the framework and methodology that produce test-friendly RF circuits and reliable measurements. The circuit design, test setup, verification, and qualification to prepare scalable statistical tests are described in Section A.2. The statistical test of the performance of a 6GHz widely tunable VCO is demonstrated as an example in Section A.3. The yield model of the VCO in a 130nm CMOS technology is developed, and the circuit yield in the presence of phase noise and frequency variability is estimated in Section A.4. The analog design and test plan are interactively used through the whole RF DFT process.

A.1 Analog Design for RF Test

Digital DFT and RF DFT have common and distinct characteristics as depicted in Table A.1. The digital DFT is focused on the functional test of logic blocks or the characterization of maximum operating frequency and power consumption. The analog DFT mainly considers feasibility of circuit performance measurement by using on-chip test circuitry or off-chip equipment.

Previously, analog DFT has been considered to focus on detecting soft failures

in analog circuits by using various fault sensors, or measuring specific performance variables using on-chip test circuitry. In [6], oscillation-based fault detection is implemented. The variation sensor outputs must be efficient to measure, and the decision is based on perfect correlation between the sensors and actual circuits. However, recent characterization results show that the within-die variation of threshold voltage is spatially uncorrelated, and therefore, the sensor cannot provide accurate estimation of circuit performance. Dedicated on-chip measurement circuitry can provide efficient measurement of analog performance (e.g., phase noise measurement of PLL in [51]). However, the measurement circuit must be highly customized and cannot be applied to multiple performance variables.

The RF DFT engages analog circuit design, specifications, and test strategies at an early design stage. The design must include circuit schematic, layout, interface, and test environment. For testability, the interfaces are customized using output buffers, pad sets, RF+DC probes, cables, and measurement equipment. The test case is manually generated according to the design specifications and test environment. The pass or fail of functional measurements is determined by pre-defined performance parameter ranges.

The RF DFT is applied to the design and test of a VCO for a phase-locked loop (PLL) in microprocessors as illustrated in Figure A-2. The VCO has an 11-stage delay chain to reduce process-induced variability by averaging. Each delay stage consists of a current-mode-logic (CML) differential amplifier with tail current control for frequency tuning. The VCO has been implemented in 130nm CMOS on a 200mm wafer. The oscillation frequency is controlled by the reference current input I_B. The VCO determines the CLY of the entire chip, and the *frequency tuning range* (FTR) must be wide enough to meet the specification frequency in the presence of process variation. Also, the phase noise of output signals needs to be lower than a specification limit.

The VCO specifications are listed in Table A.2. The specifications include static power consumption, FTR, dynamic power consumption, phase noise, and *figures-of-merit* (FoM). The FTR and phase noise are the most critical performance variables

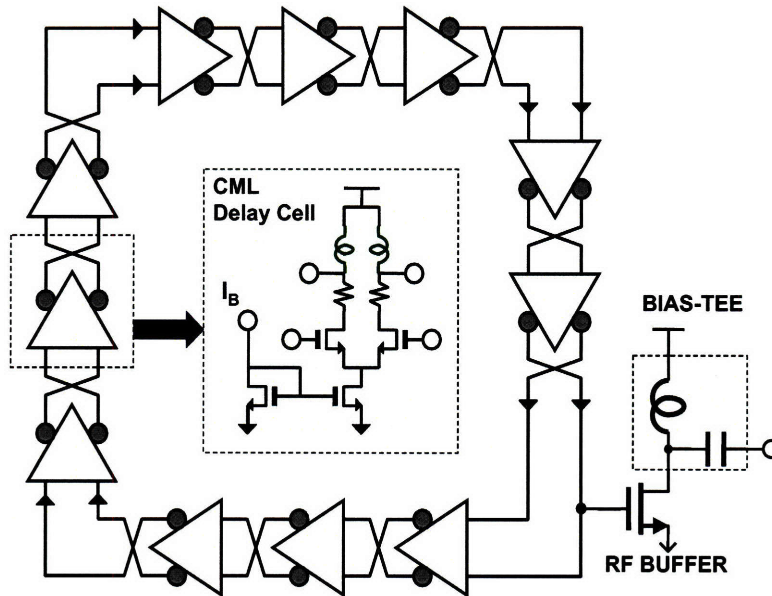


Figure A-2: A schematic diagram of 11-stage CML VCO implemented in 130nm CMOS.

for the VCO and overall system operation. The FOM is used for fair comparison of the VCO phase noise.

In the RF DFT, several design modifications and environmental variables must be applied to support automated quality measurements: 1) RF and DC interfaces, 2) pad pitch and size, 3) probe set, 4) RF buffer circuit, 5) on/off-chip DC decoupling, 6)

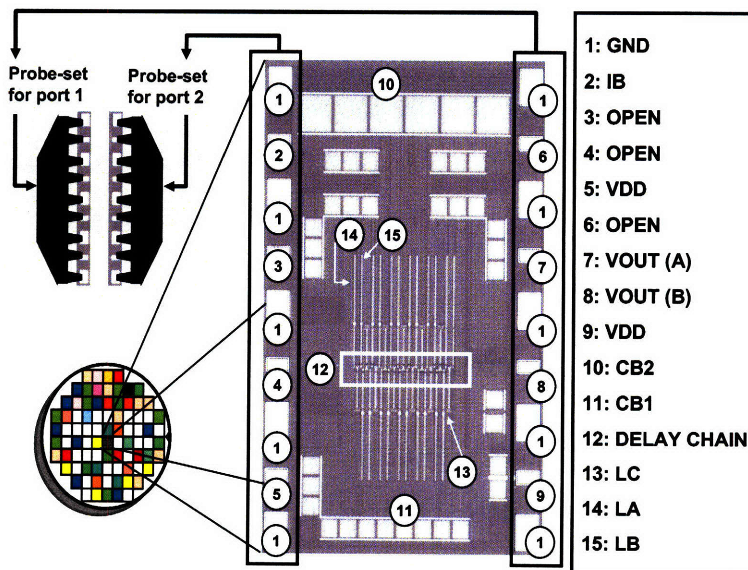


Figure A-3: VCO layout with testing environment considering RF DFT.

Table A.2: VCO Performance specification for RF DFT

Entity	Unit	Equipment	Specification
Active current	mA	SMU	40mA
Quiescent current	mA	SMU	1mA
Frequency	GHz	Spectrum	f_0=5.5GHz
FTR (%)	%	analyzer	FTR=40%
Output power	dBm		-20dBm
Phase noise	dBc/Hz	PLL	-120
FoM	@1MHz	analyzer	-160

cable connection, 7) measurement equipment and system, and 8) test code for automatic measurement. Especially, RF buffer and DC decoupling are important for phase noise and FoM measurements. This is because the *circuit-under test* (CUT) is surrounded with and connected to noise sources, such as a DC *source-and-measurement unit* (SMU), a control PC, and a wafer stepping tester.

Figure A-3 shows the layout and pad assignment and design assistants for efficient automated probing of the VCO circuit. The CUT requires two DC inputs and one RF output, and 150μm-pitch pads and probe sets are used. All RF pads are assigned on the right side to reduce the number of high-frequency probe sets. Since the contact between automatically-controlled probes and pads are not as solid as wire bonding, on-chip high-density bypass capacitors (CB1 and CB2) were inserted extensively to reduce the power supply noise induced by the weak contact. A common source RF buffer is added to improve output signal power. The VCO CUT is testable at the M3 level, reducing the RF DFT process cycle time for circuit debugging.

A.2 Measurement Setup

There are several practical issues to match the CUT well with the external test environment, and the issues must be resolved in the design stage. The instrument measurement ranges must be carefully inspected to meet the circuit specifications from simulation results. The availability of test instrument must be checked in time.

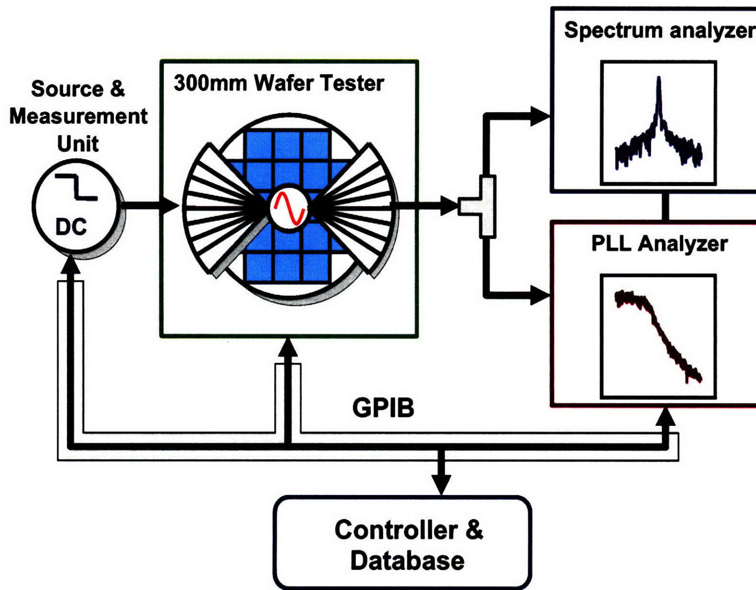


Figure A-4: Measurement setup diagram for the VCO.

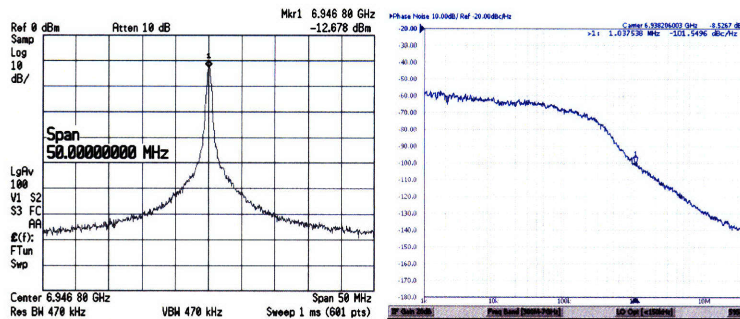


Figure A-5: Manual screen captures of VCO output spectrum with 50MHz span and the phase noise at 6.94GHz.

Estimated signal losses in on-chip interconnects, probe contact resistance, probe sets, cables, and a bias-T must be considered. Custom probes are fabricated if necessary, and the wear-out of the probe set, RF connector, cable, adapter, and bias-T must be checked in advance. Having spares of fragile RF test equipment is recommended since delayed yield learning of product designs can be costly. The automated test code must be prepared and debugged based on the simulation results.

Figure A-4 shows a test setup diagram for the VCO. DC SMUs provide operating conditions to the CUT through cable and probe set. The probe set is held by a wafer tester, and the tester performs robotic movements across the wafer. The RF output of the CUT is collected by the RF probe and bias-T. The power splitter divides the

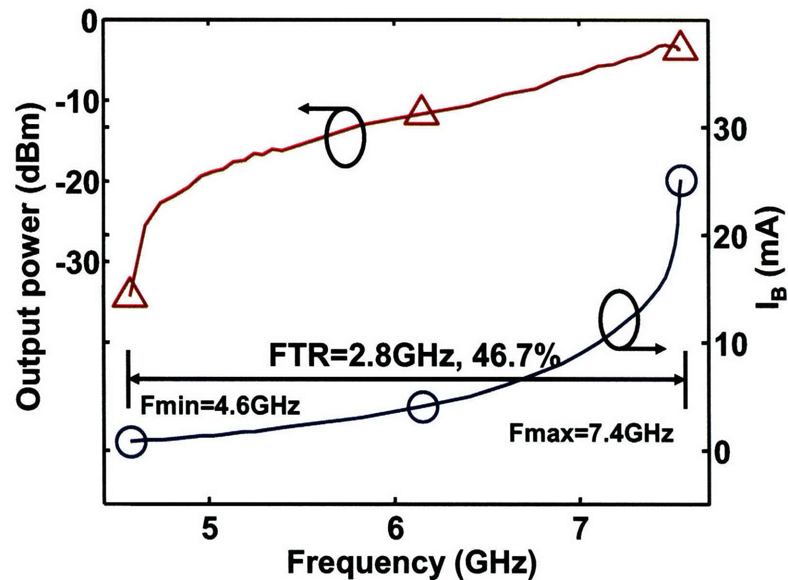


Figure A-6: VCO output frequency for input current I_B and the output signal power.

signal to the spectrum analyzer and the PLL analyzer. The PLL analyzer shows faster and more accurate phase noise measurement in real time than a spectrum analyzer. A spectrum analyzer is used for signal verification and oscillation frequency measurement. All of the instruments are connected through GPIB, and a PC controls instrument operations. The measurement results are transferred to the PC and their validity is evaluated with algorithms based on the VCO spectrum and phase noise models. For example, an accurate oscillation frequency is reliably determined by zooming in the measuring frequency range iteratively. The test results are recorded in a central test database, containing wafer and site information, and test conditions.

The measured VCO output spectrum and phase noise screen shots are shown in Figure A-5. The initial test shows that the VCO and the test setup are functional. The phase noise plot does not show noticeable noise modulation. In practice, several factors such as the tester condition and global ground should be modified to isolate noise sources. Once the minimal circuit function is verified, a set of repetitive tests are performed based on the pre-determined test plan. The FTR and the RF output power of the VCO are obtained with automated test code as plotted in Figure A-6. The plots show the VCO output frequency versus input current I_B and RF output power, all sampled by a spectrum analyzer. The measured VCO minimum frequency is 4.6GHz

at I_B=1mA, and the maximum is 7.4GHz at I_B=25mA. The FTR is 2.8GHz, or 46.7% around a center frequency.

The other important CUT specification is phase noise, and the phase noise curves at different I_Bs are shown in Figure A-7. The plot shows that the phase noise curves have regular slope overall. At the minimum oscillation frequency, the VCO output tends to have worse phase noise as plotted in Figure A-8. There are more abnormalities involved at 1MHz offset in the mid-I_B region as in Figure A-8. The plots suggest that the phase noise should be sampled at larger offset frequencies such as 2, 5, and 10MHz for reliable measurement. The PLL analyzer noise floor is below the minimum phase noise at 10MHz, verifying that the measurement result at 10MHz offset is actual VCO phase noise, not the instrument noise. Moreover, the phase noise must be measured at both the highest and lowest frequencies, as in Figure A-9, to verify that the VCO meets the phase noise specification over the operating range. The phase noise is assumed to change monotonically with I_B. The phase noise measurements tend to have a noisy curve, and there is a trade-off between the measurement time and the averaging, with respect to the test scalability.

The test procedure must be iterated to modify the parameter capturing algorithm and to improve the reliability of the measurement against environmental variation

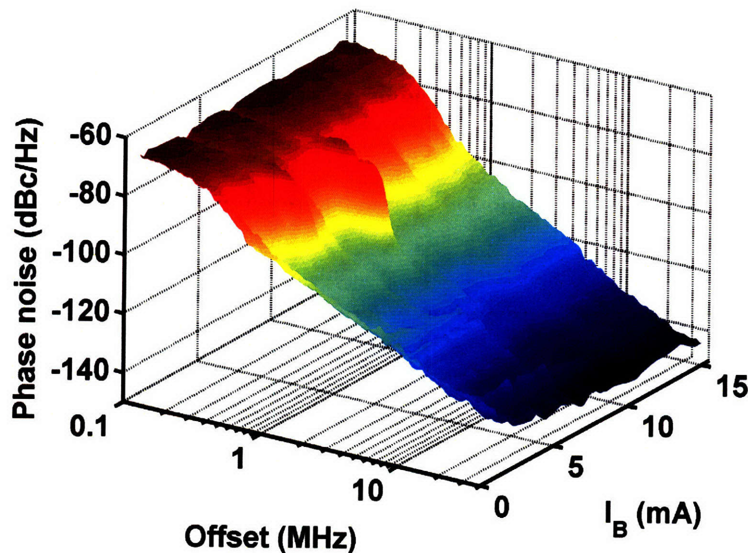


Figure A-7: VCO phase noise output with input current I_B sweep.

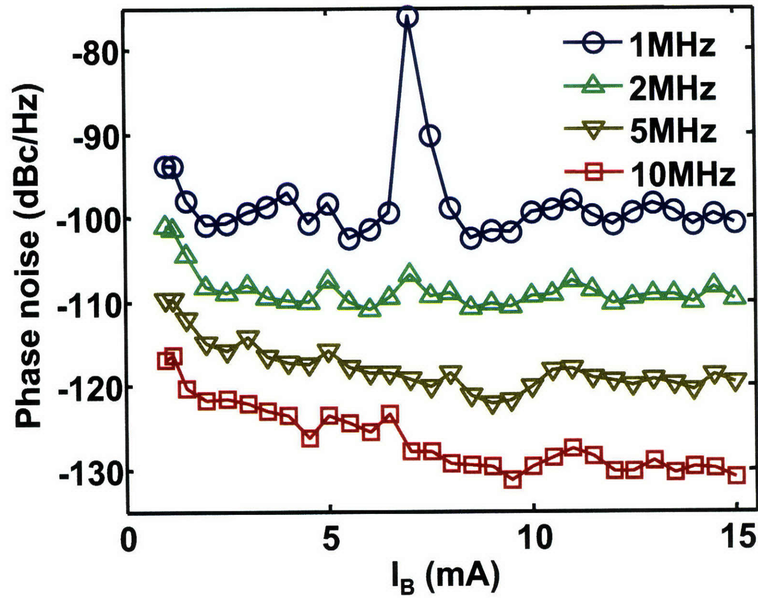


Figure A-8: VCO phase noise at 1, 2, 5, and 10MHz offset with I_B sweep.

and anomalies. When confidence is established in the circuit operation, environment, control, and algorithm, the test set up is qualified for statistical tests.

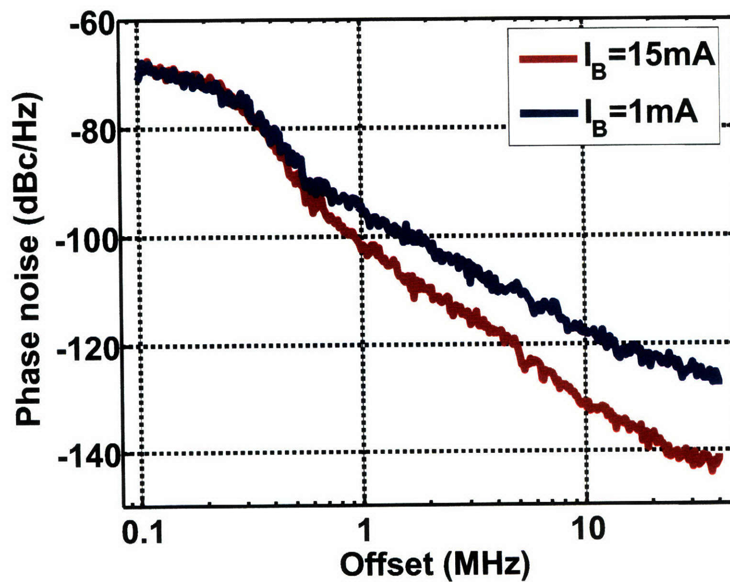


Figure A-9: VCO phase noise at I_B=1mA and 15mA.

A.3 Statistical RF Test

The test qualification for statistical measurement must be conducted on several sampled sites on a single or multiple wafers, before proceeding to massive (high data volume) measurements over a number of wafers. The test results must be qualified based on acceptance criteria assuming possible errors during the large number of measurements. The statistical tests were performed on a 200mm wafer including 46 dies.

Figure A-10 shows maximum and minimum tunable frequencies (F_{max} and F_{min}) of all 46 dies. The data is sorted on a descending order of the calculated FTRs. This measurement result shows the statistics of F_{max} at I_B=12mA and F_{min} at I_B=2mA including mean, standard deviation, and correlation between each other. The size of a common FTR over all dies is also estimated. The VCO yield defined by the minimum FTR specification (40%) can be calculated based on the measurement data and suggested yield model in Section A.4.

The measured phase noise values at 10MHz offset when I_B=2 and 12mA over all dies are shown in Figure A-11. The site index is the same as in Figure A-10.

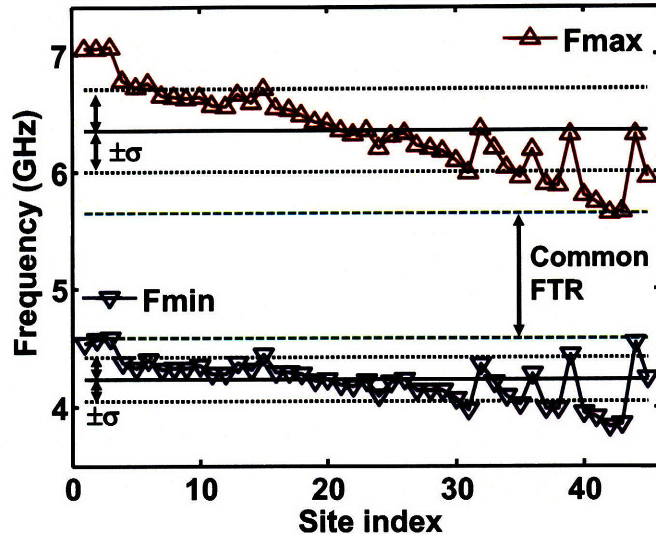


Figure A-10: Statistical measurement on VCO maximum and minimum tunable frequency.

Table A.3: CML VCO RF Performance Statistics

Entity	Average	σ/μ (%)	Median	Minimum	Maximum
I_A@F_{max} (mA)	53.2	5.86	53.6	39.8	56.8
I_Q (mA)	1.61	15.8	1.55	1.44	2.85
F_{min} (GHz)	4.23	4.33	4.24	3.83	4.58
F_{max} (GHz)	6.35	5.58	6.35	5.65	7.06
FTR (GHz)	2.12	9.76	2.14	1.71	2.50
FTR (%)	40.0	6.09	40.7	32.5	43.3
P_{RF}@F_{max} (dBm)	-4.40	15.7	-4.24	-6.90	-3.50
Phase noise (dBc/Hz@10MHz, I_B=2mA)	-123.5	2.88	-124.3	-129.5	-113.0
Phase noise (dBc/Hz@10MHz, I_B=12mA)	-129.8	1.20	-129.7	-132.6	-126.9
FoM (dBc/Hz)	-166.1	0.91	-165.9	-169.1	-163.3

The phase noise at I_B=2mA shows stronger fluctuation and the phase noise variation does not show strong correlation to the variation of FTR at both I_B conditions. The mean and standard deviation are used to construct a phase noise yield model. The statistical RF test result is summarized in Table A.3.

A.4 Yield Analysis

We consider the frequency tuning range and phase noise to define sound samples for yield calculation. Figure A-12 shows the distribution of phase noise at 10MHz offset and output frequency variations at F_{min} and F_{max} of the VCO. At F_{min} (I_B=2mA), the yield is limited by the phase noise specification since the phase noise shows a wide spread. On the other hand, at F_{max} (I_B=12mA), the output frequency variation shows a wide spread and becomes a critical concern for yield estimation.

We provide the estimation of circuit yield against frequency variation at F_{max} as an example. To estimate the circuit parametric yield in manufacturing, the variation must be decomposed to within-die, die-to-die, wafer-to-wafer, and lot-to-lot variation. For most mixed-signal SoC applications, the die area consumed by analog building blocks is extremely small compared to digital circuits. Therefore, the within-die

variation is not considered to be a serious issue in analog circuits, unless the circuit is a repetitive large array and the performance is highly sensitive to device mismatch, such as in SRAM cells.

The die-to-die variation over a wafer is one of the main concerns in overall variation. The slowest and fastest dies in a 200mm wafer in our example show 22.2% range of F_{max}, and the $3\sigma/\mu$ of F_{max} is 16.74%. The die-to-die frequency variation over a wafer is seen to be highly systematic; the cross-correlation between different wafers is more than 90% in most cases [67]. We model the variation such that there is a mean-shift between wafers caused by the wafer-to-wafer variation, while σ/μ of each wafer is preserved.

The cause of wafer-to-wafer variation can be either temporal or spatial. The temporal wafer-to-wafer variation is caused by the drift of process conditions in single wafer processing. While the wafer-level variation is likely to be systematic, the wafer-to-wafer variation is time and equipment dependent and we assume it as random in this analysis.

By using the RF DFT, the variation pattern of the VCO output frequency tuning range over a 200mm wafer has been fully characterized as in Table A.3. Figure A-13

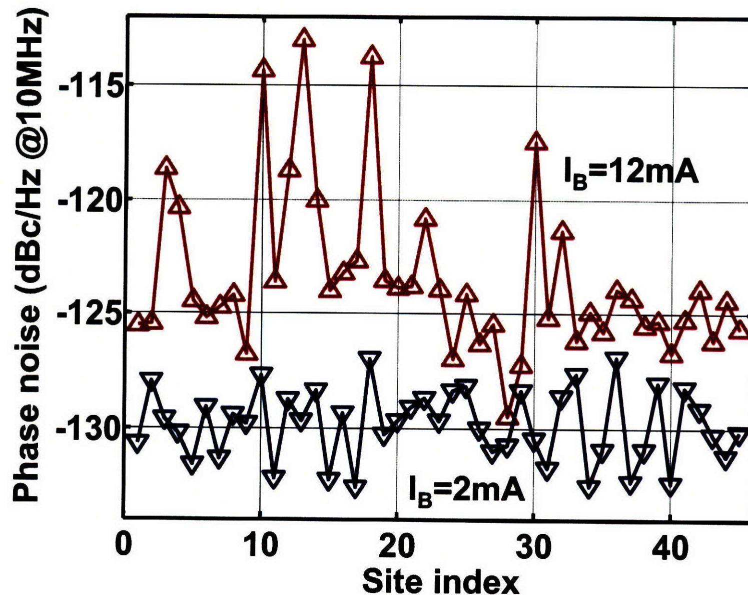


Figure A-11: Statistical measurement on VCO phase noise with I_B=2mA and 12mA @10MHz offset.

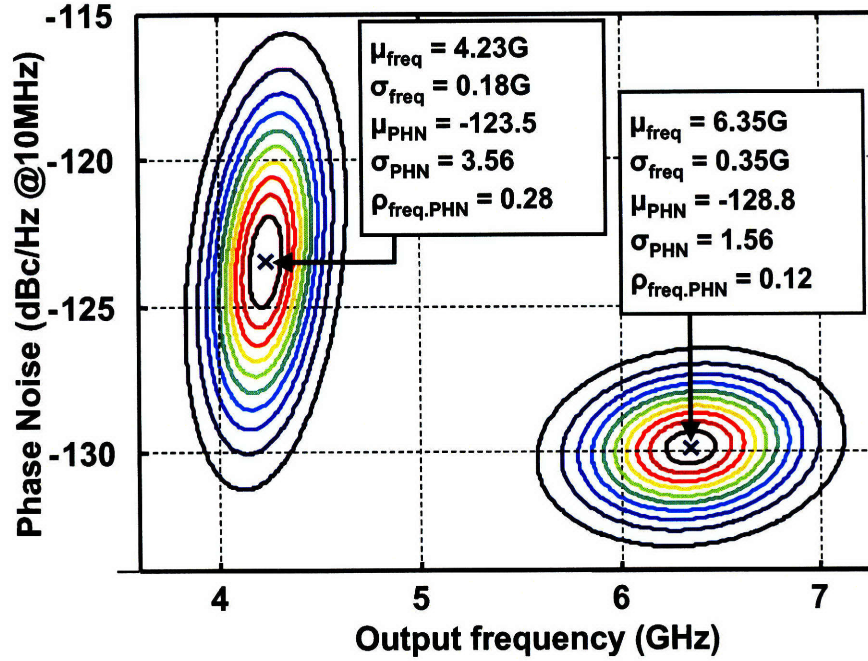


Figure A-12: VCO F_{max} (I_B=12mA) and F_{min} (I_B=2mA) versus phase noise distribution.

shows our variation model including die-to-die variation over a single wafer and wafer-to-wafer variation. For each wafer, $3\sigma/\mu$ is preserved at 16.74%. The mean shift of each wafer is assumed to come from a normal distribution with zero mean and σ_{W2W} standard deviation, and is added to all dies in a wafer to model the wafer-to-wafer variation.

The probability of the VCO maximum tunable frequency (F_{max}) not satisfying the minimum requirement $\mathrm{F_{MAX,\,MIN}}$ can be calculated as follows.

$$P(f < \mathrm{F_{MAX,\,MIN}}) = \int_{-\infty}^{\infty} Q(\frac{\mathrm{F_{MAX,\,MIN}} - m(w)}{\sigma(w)}) f_{\sigma_{w2w}}(w)dw \tag{A.1}$$

where $Q(x) = \int_{-\infty}^{x} \frac{1}{\sqrt{2\pi}} e^{-\frac{x^2}{2}} dx$, $f_\sigma(w) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{w^2}{2\sigma^2}}$, $m(w) = m_{ref} - w$, and $\sigma(w) = m(w) \cdot \frac{\sigma_{ref}}{m_{ref}}$. Here, m_{ref} and σ_{ref} are the mean and standard deviation of the reference wafer with zero mean shift. The yield can be calculated numerically using the characterization results from the measurement. Assuming the minimum $\mathrm{F_{MAX,\,MIN}}$ specification is 6.35GHz for 40% FTR, the calculated circuit yield is 51%. Similar analysis can be applied to the phase noise constraint at F_{min}.

A.5 Summary

A framework for analog design for RF test has been developed for the statistical measurement of yield-limiting analog building blocks in mixed-signal SoC applications. A systematic measurement plan for high-speed analog circuits is critical for fast and accurate yield learning. A 6GHz ring-based CML VCO was implemented in a 130nm CMOS technology with circuit assistance for automated measurements. The frequency tuning range, phase noise, and power consumption of the VCO and their statistical properties were characterized over a 200mm wafer. The measurement results show an important trade-off between the variability of phase noise and output frequency at different bias conditions of the VCO. The yield of the VCO circuit for given phase noise and FTR specifications is estimated based on the proposed variation model.

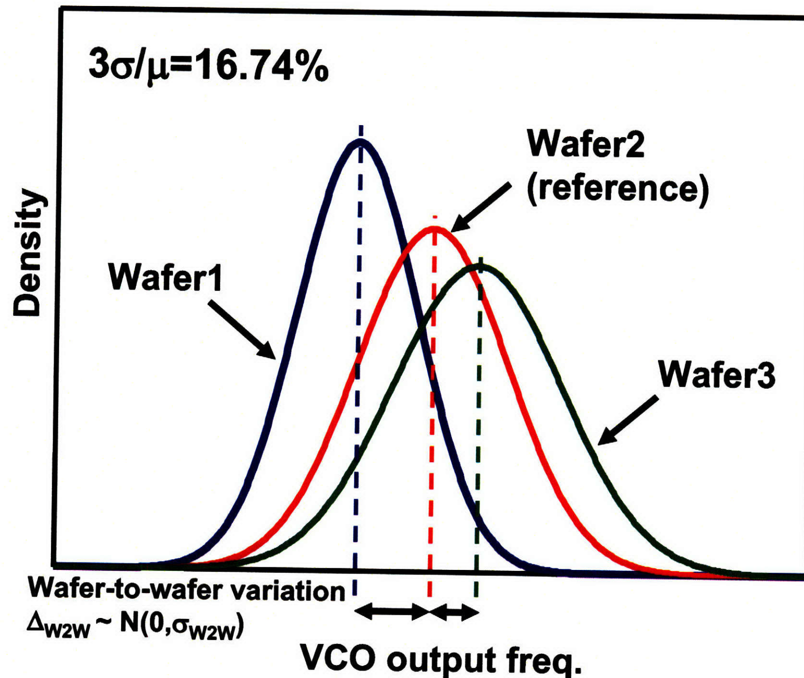


Figure A-13: Variation model including wafer-level die-to-die variation and random wafer-to-wafer variation.

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