Designing an Ultra Low Quiescent Current Buck Switching Regulator

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by

John Underhill Gardner

S.B. EE, M.I.T., 2007

Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degree of

Master of Engineering in Electrical Engineering and Computer Science

at the MASSACHUSETTS INSTITUTE OF TECHNOLOGY

May 2008

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Abstract

The new buck regulator proposed in this thesis was designed to operate with only a few micro-amps of supply current during no load output conditions, while maintaining low output voltage ripple. The regulator also has high efficiency for current loads above an amp to make the converter useful in a variety of applications. The specifications will be achieved by implementing a control scheme similar to the one used in the LT3481 buck regulator. The converter will use burst mode, pulse frequency modulation, and pulse width modulation to achieve control over the entire load range. The capabilities of a full BiCMOS process technology will be taken advantage of to enable implementation of good control dynamics at low currents. This micropower buck regulator was designed, fabricated, and tested in silicon to measure its characteristics as compared to simulation and desired specifications.

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Chapter 1

Introduction

There are many applications which require step-down DC-DC conversion in the milli-watt to several watt range. Among these applications are portable electronic systems, automotive applications, and wall transformer regulators. Battery life is a critical component for portable systems and automotive applications, thus power management must be as efficient as possible. In particular, efficiency over a range of loads can become critical. If a portable system is powered on, but the functionality requiring the regulated DC voltage is not being used, the efficiency of the converter can significantly decrease. A specific example is modern CMOS memory and microcontrollers, which need a DC bias to hold state, but do not consume appreciable current. In such cases, efficiently plummets when no current is being drawn from the output of the converter because all the power used by the converter to regulate the unused output voltage is wasted. This supply current can often be in the milliamp range. Therefore, there is a need to decrease the supply current necessary to operate the converter as the output current decreases. This has lead to the creation of a series of micropower switching regulator parts which only require ten to hundreds of micro-amps of current to operate during no load conditions. The aim of this thesis is to describe the design of a buck switching regulator circuit which only consumes a few micro-amps with disconnected load.

The Linear Technology Corporation presently sells several micropower products. The thesis work proposed here is done through Linear Technology taking advantage of the work they have done designing and fabricating micropower products. This thesis is supported by Linear Technology through the VI-A program.

1.1 Micropower

It is important to understand how a micropower regulator is different than a non-micropower regulator. Many switching regulators will require a substantial static component of supply current regardless of the output load. However, micropower regulators refer to converters which require less supply current when operating at lower output loads as shown in Fig. 1-1.

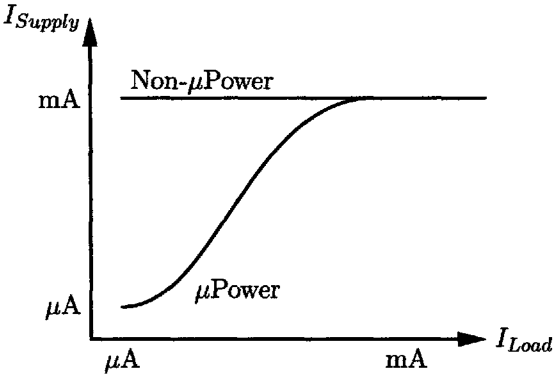


Figure 1-1: Generalized Supply Current vs. Load Current curve for a micropower and a non-micropower converter.

The efficiency of a power converter is defined as the output power divided by the input power. When milli-amps of supply current are used to generate micro-amps of output current, the input power is much larger than the output power resulting in poor efficiency. However, when the supply current is comparable to the output current at small output current levels, the input and output powers are comparable, which results in significantly higher efficiency. The higher efficiencies realized by micropower parts operating at a small percentage of their total output power is depicted in Fig. 1-2.

The efficiency advantage of micropower parts is most pronounced when there is no output load, in other words when the regulated voltage is not being used. The converter supply current during conditions of no output load is referred to as quiescent current. The quiescent current is one of the primary quantities used to characterize micropower parts.

1.2 Prior Work

The efficiency advantages of micropower parts are only part of the story. Achieving low quiescent current is difficult because there are trade-offs which often have to be made. Many

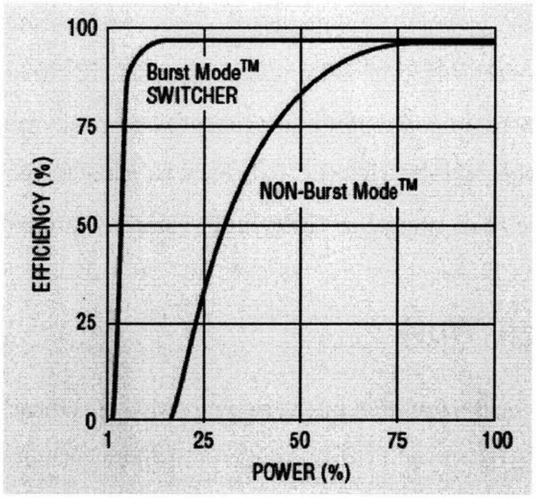


Figure 1-2: Increased efficiency of a micropower part at low output current loads.[3] (Used with permission)

control schemes are such that output voltage ripple is quite large in micropower operation when compared to full frequency operation, independent of the output capacitance. Users can tolerate ripple voltage of ten or twenty milli-volts, but larger amounts of output ripple become unacceptable. Also, typically the maximum load current the regulator is able to provide is smaller when micropower operation is incorporated because control and stability of the converter becomes difficult when the load range spans several orders of magnitude.

The trade offs in designing micropower buck parts can be seen by examining a list of several Linear Technology micropower buck regulators shown in Table 1. The parts which can supply the highest amount of output current also have the largest quiescent current (LT1977 and LT3435). The converse is also true; the parts with low quiescent current also have low maximum output current (LT1934 and LT3470).

Part	$V_{in,max}$ (V)	$I_{out,max}(A)$	I_{supply} (μA)	Burst V_{out} Ripple (mV)
LT1934	34	0.3	12	40
LT1977	60	1.24	100	40
LT3435	60	2.4	100	80
LT3437	80	0.4	75	20
LT3470	40	0.2	25	20
LT3481	36	2	50	10
Proposed	**36**	**2**	**1-10**	**10**

Table 1.1: Specifications for several current Linear Technology Buck Regulators compared to the proposed buck regulator specifications.[1]

The output ripple in burst mode is listed. This specification is difficult to cite because it depends on the exact current load and the type/size of the output capacitor used. The values listed in the table correspond the the peak-to-peak values in switching waveform plots contained in the part data sheets. It is hard to make a comparison between them, but it is clear that more than twenty or thirty milli-volts is quite common.

1.3 Proposed Work

The new proposed buck regulator has very aggressive specifications, as listed in Table 1.1. It builds upon the LT3481, which has better performance than the other parts listed. The LT3481 has increased output load range with low current ripple, while maintaining low supply current. However, a part with these qualities, but even lower quiescent current is very desirable. The LT1934 was very popular and sold in the millions because of its very low quiescent current, even though it has undesirable voltage ripple and non-fixed frequency control. Therefore, the proposed part will be of interest to many customers with many different applications.

1.4 Applications

There is little reason to redesign a regulator without considering whether there will be need for new features and more impressive design specifications. A buck regulator with a quiescent current of only a few micro-amps does have several interesting applications.

The first of these applications are systems where the regulated voltage is necessary, but current is not always being drawn from the output. For example, modern CMOS memory and microcontrollers need a regulated voltage and almost no current when remembering or holding a certain state, but when switching state will require more power. The user does not want the regulator to drain the battery unnecessarily and would like good efficiency during idle states, so a low quiescent current regulator would be desirable. This is especially true in laptops and other portable applications where battery life is a big issue and every little bit of efficiency counts.

The second set of applications are systems where the product is not being used a vast majority of the time and the battery cannot be discharged during this time period. One specific example of this kind of system is a fire alarm. A majority of the time it is simply waiting to detect a situation where it needs to respond and start fully operating. An ultra low quiescent current regulator would be good in this scenario because the battery needs to survive reliably for a long time in such a product without being depleted by the converter when idling with no load.

The third set of applications are energy harvesting systems. Energy harvesters collect energy from the environment in the form of vibrations, light, or thermal gradients. The difficulty with these systems is that only small amounts of energy can be collected and the energy does not come in a constant form. Therefore, an energy storage system has to be set up like the one in Fig. 1-3.

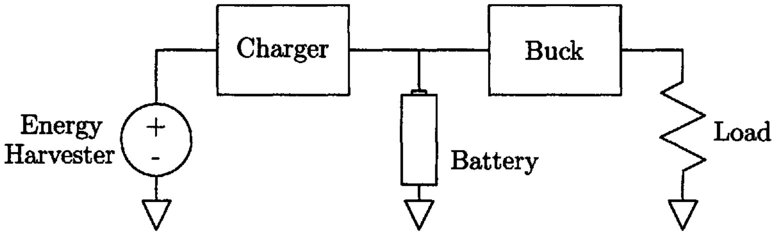


Figure 1-3: Example System Utilizing Energy Harvesting

The voltage from energy harvesters is usually too low to store and needs to be interfaced with a charger or boost converter to charge a battery or similar energy storage device. Then the stored energy needs to be regulated before it can be used to power a load device. Since the energy harvester is only able to gather small amounts of power into the battery, the system is only capable of operating loads with small power requirements. Therefore, the regulator used to source the load needs to be efficient at light loads to make the system viable. The ultra low quiescent current regulator described in this thesis is such a candidate.

1.5 Batteries

While discussing the effect the converter will have on draining the battery, one also has to consider the natural self-discharge of the battery. Batteries have a finite shelf-life as their charge is slowly drained over time. The self-discharge of a battery depends on battery chemistry, temperature, and whether the battery is a primary or a secondary (rechargeable) battery.

Rechargeable batteries have significant self-discharges. Nickel Cadmium (NiCd) and

Nickel Metal Hydride (NiMH) are the worst with 15% to 20% and 30% per month, respectively. Lead acid and lithium chemistries are better with lead acid discharging 4% to 6% of their charge per month and lithium secondary battery discharge being half that of lead acid batteries. Primary batteries are significantly better than rechargable batteries in terms of self-discharge. Alkalines can have shelf-lives of around 5 years, while lithium primaries can have 10 to 15 year shelf-lives.[12]

Battery	Chemistry	Voltage	Capacity	Self-Discharge Rate	Leakage
Panasonic LC-R122R2P	Lead-Acid	12V	2.2Ah	5yrs	50.2μA
Panasonic 6AM-6PI	Alkaline	9V	500mAh	5yrs to 85%	1.7μA
Energizer NH22	NiMH	9V	175mAh	21days to 70%	104.2μA
Energizer X22	Alkaline	9V	655mAh	5yrs to 80%	3.0μA
Energizer L91	Lithium	1.2V	3000mAh	15yrs to 90%	2.3μA

Table 1.2: Self discharge of several different battery chemistries at room temperature.[2][4]

The self-discharge characteristics of several specific batteries are shown as examples of self-discharge for different battery chemistries in Table 1.2. The superior performance of primary alkaline and lithium batteries to secondary lead-acid and NiMH batteries is clear. It is important to note that battery discharge is specified as a percentage of total capacity. Therefore, batteries with larger current capacities will have more leakage even for the same battery type. This means that NiMH are even worse, while lead-acid and lithium are better when comparing them based on leakage per Ah, than just leakage current. All the values listed in the table are for room temp (25°C). The self-discharge will approximately double for every additional 10°C of temperature.

When using a primary 9V battery, as might be used in a fire alarm application, there are only two to three micro-amps of self-discharge current. This is comparable to the quiescent current of the proposed buck converter. If the quiescent current were larger, as in presently available regulators, the converter itself would be the limiting factor in battery lifetime. However, if the target quiescent current of the proposed converter was significantly lower than a few micro-amps, there would be diminished increase in battery life because the battery self discharge would be the limiting factor. Therefore, the chosen quiescent current goal of one to ten micro-amps for the project is a good one.

Even for systems with greater battery self-discharge rates, such as with rechargeable lithium-ion batteries in laptops, lowering the quiescent current of the regulator below the self-discharge rate of the battery can be desirable. Minimizing the converter quiescent current still improves battery life, even if the battery self-discharge is greater than the quiescent current, one just observes diminishing returns because the battery self-discharge rate is limiting the battery life, not the converter. However, perhaps the most important aspect of a low quiescent current regulator is that the user does not have to worry about the power consumption of the converter during no load conditions because the quiescent current is much lower than the battery self-discharge rate.

1.6 Thesis Overview

Chapter 2 will cover the basics of the buck switching regulator operation and control. Then, the merits of low current circuits will be described in relation to the project in Chapter 3. Chapter 4 will examine the modeling of the control loop, so that a compensation network can be devised. Next, the design of each low current sub-circuit of the regulator will be detailed in Chapter 5. Chapter 6 will review the results of the bench tested silicon. Finally, the issues discussed in the thesis will be summarized in Chapter 7.

Chapter 2

System Overview

This chapter describes the basics of buck switching regulators and buck switching regulator integrated circuits. It then outlines the control scheme used in the proposed project, including how burst mode is used to achieve micropower operation.

2.1 Buck Switching Regulator

The circuit topology of a basic buck switching regulator is shown in Fig. 2-1.

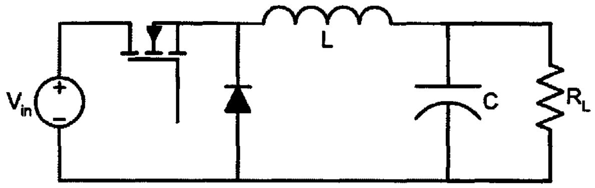


Figure 2-1: Basic Buck Switching Regulator Topology

This circuit does not show any of the feedback circuitry which is used to control and drive the switch. The feedback circuitry and the choice of switch are two of the most difficult parts of designing a buck regulator system. The switch and the feedback circuitry are the aspects of the regulator which are integrated in the proposed IC, and the other elements are discrete, external components.

The typical application circuit for the proposed part is shown in Fig. 2-2. The internal switch is connected between the V_{in} and SW pins. The diode D1, inductor L1, and capacitors C_{out} and C_{in} are the same as shown in the basic topology. The resistors R1 and R2 form a divider which measures the output voltage and inputs it to the feedback pin FB. The other

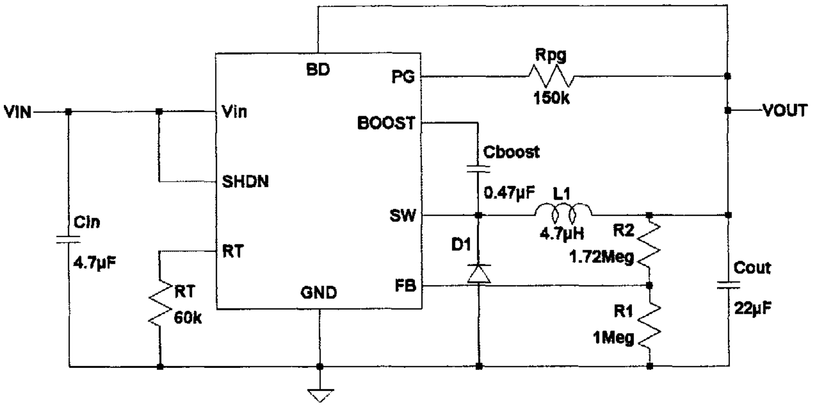


Figure 2-2: Typical Application Circuit for Proposed Part

external components help implement useful features of the IC. The shutdown pin (SHDN) can be tied low to stop the part from switching and is connected high, usually to V_{in}, for normal operation. A resistor is connected to the RT pin to program the switching frequency of part to be anywhere from 200kHz to 2.4MHz. A capacitor is connected to the BOOST pin, which is used to generate a voltage higher than V_{in}, which is needed to more efficiently drive the internal switch. Finally, the resistor connected to the PG, or Power Good, pin acts as a pull up resistor and the output of the PG pin goes high when V_{out} comes within 10% of its regulated value.

2.2 Control Scheme

Now that the basic system has been outlined, the operation of the control scheme will be explained. The primary job of the IC is to properly control the internal switch. The control scheme for the new buck IC is the same as the control scheme used in the LT3481 buck converter. The LT3481 is a recently designed buck converter, which has low quiescent current, low output ripple voltage, and a large range of current loads, while maintaining good efficiency. The block diagram for the LT3481 is shown in Fig. 2-3.

The control scheme uses both voltage and current mode feedback. The voltage is sensed

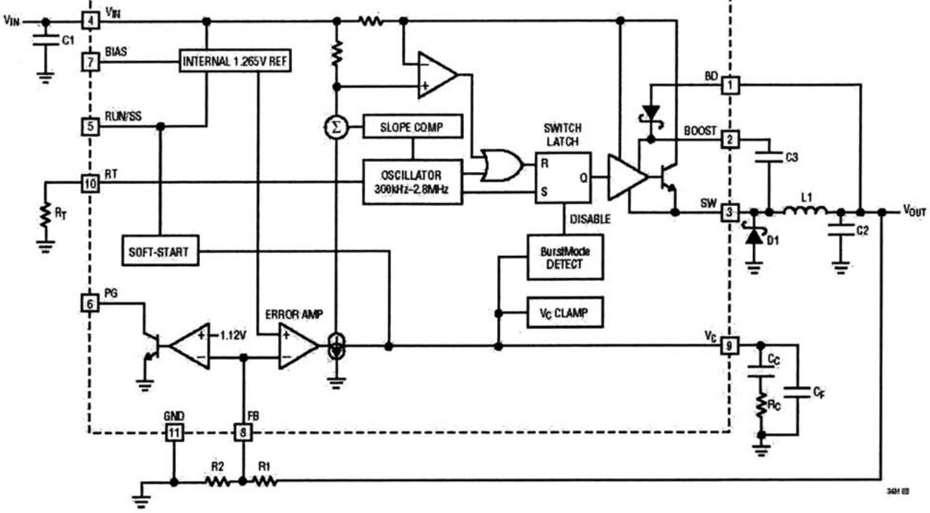

VIN
C1
4
VIN
7
BIAS
INTERNAL 1.265V REF
5
RUN/SS
10
RT
RT
SOFT-START
6
PG
1.12V
ERROR AMP
11
GND
8
FB
R2
R1
SLOPE COMP
OSCILLATOR
300kHz-2.8MHz
SWITCH
LATCH
R
S
Q
DISABLE
BurstMode
DETECT
VC CLAMP
BD
1
BOOST
2
C3
SW
3
L1
VOUT
C2
D1
VC
9
CC
CF
RC

Figure 2-3: Block Diagram for LT3481 Buck Converter showing internal control scheme, as well as external component connections.[10] (Used with permission)

through the FB pin using an external resistor voltage divider. The voltage on the FB pin is compared to an internal reference voltage using an error transconductance amplifier. The voltage error signal is one input to the internal control system. Since the controller is trying to reduce the voltage error to zero, the resistor divider ratio is used to set the desired output voltage of the converter.

The switch current is measured by the resistor between the V_{in} pin and the collector of the internal power switch. This current is monitored by an amplifier and comparator, and is the second input to the internal control system. Using these two feedback signals, the output voltage for different loads is regulated through Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM) or Burst Mode operation.

2.2.1 Pulse Width Modulation

PWM is the dominant control method during normal operation, namely medium to large current loads. During PWM the frequency of the drive applied to the base of the power switch remains constant. However, the duty ratio, or time the switch is driven such that it is on, changes to control the buck regulator. This control scheme implements current mode control, meaning it controls both the output voltage and inductor current. In a peak current controlled converter, which we are considering, the duty ratio is established implicitly by setting current limits. Namely, the switch is turned off when the switch current ramps to a peak current limit [20]. This leads to the generation of a particular duty ratio. The current limit is based upon the voltage error signal from the transconductance amplifier. The error signal provides a DC shift to a sawtooth slope compensator waveform, which when compared to the measured switch current, trips a comparator turning off the switch drive. When the error is large and the output voltage is low the current limit is increased, so the output capacitor can charge to the desired output voltage. Conversely, when the output voltage is too high the current limit is decreased, so the capacitor can discharge to achieve the desired output voltage. In this way, both the inductor current and output voltage are controlled by PWM.[10] The slope compensator, error amp, summing junction, comparator, and power switch driver can all be seen on the block diagram in Fig. 2-3.

In a buck topology, the average inductor current is equal to the average output current, since the inductor is always connected to the output and the capacitor draws no average current. The average input current is equal to the average switch current, which will be zero when the switch is off and equal to the positively ramping inductor current when the switch is on. The relationship showing how duty ratio controls the input and output current and voltage ratios under ideal conditions in continuous conduction mode is summarized below.[14]

$$I_{out} = \frac{I_{in}}{D} \tag{2.1}$$

$$V_{out} = DV_{in} \tag{2.2}$$

Even though these equations will not be exact in real converters with less than perfect efficiency, they show the general trends between duty ratio and output current and voltage. The controller will adjust the operating point duty ratio to achieve proper DC voltage conversion. The system will be compensated such that when output transients and perturbations in input, output, and load conditions occur the system can quickly and accurately return the output voltage and inductor current to the desired regulated levels.

PWM control can be seen in the LT3481 switching waveforms in Fig. 2-4. The current in the inductor ramps up when the switch is on and ramps down when the switch is off.

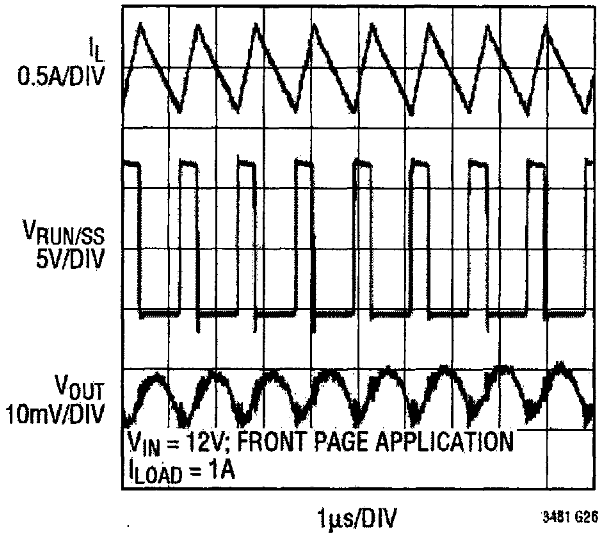


Figure 2-4: LT3481 Full Frequency Continuous Mode Operation[10] (Used with permission)

2.2.2 Burst Mode and Pulse Frequency Modulation

Burst Mode is a part of the control scheme which takes over at low current loads. A converter can use on the order of milli-amps of supply current during normal operation. However, during light load operation, in the limit of zero load current, the supply current can contribute significant loss in efficiency. Burst mode strives to decrease the necessary supply current down to the tens of micro-amps level to increase light load efficiency. This functionality is implemented by shutting down all the control circuitry, except for the error amplifier, during light load conditions when the output voltage is high. Then, as low amounts of current from the output capacitor are supplied to the load, the output voltage will drop. When the error amplifier senses the drop in output voltage, it will turn on, or "wake-up," all the control circuitry and drive the switch, thus recharging the output capacitor and restoring the output voltage. Then, all the control circuitry will be put back to "sleep" again, namely the control circuitry will be shut off until it needs to turn on again to drive the switch.

This method for light load control is good for significantly reducing the supply current and increasing the converter efficiency. However, swings in output voltage are inherent to the process, so large amounts of output voltage ripple can result. One way to reduce the output voltage ripple is to burst frequently with small charge impulses. Therefore, the output capacitor will have less negative ramping time, thus reducing the peak-to-peak output voltage swing. Bursting more frequently, however, will most likely require more supply current, so a trade-off must be struck between voltage ripple and quiescent current.

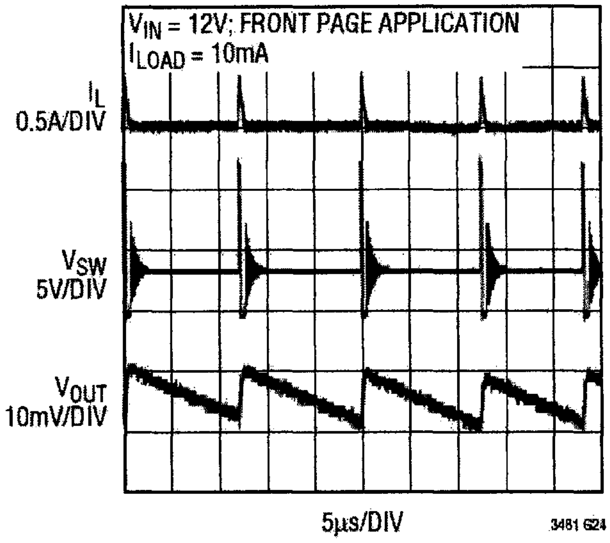


Figure 2-5: LT3481 Burst Mode Switching Waveforms[10] (Used with permission)

Fig. 2-5 shows the switching waveforms for the LT3481 in burst mode operation. One observes the inductor current pulses, which are used to charge the output capacitor. Also, the linearly decreasing output voltage as the output capacitor discharges can be seen. It is interesting to note that when the control circuitry "wakes up" the power switch is only turned on once. If the switch turned on multiple times the output ripple would be increased, because the output capacitor would be charged to a higher voltage and would take a longer time to discharge to the same control turn-on trip point. The output voltage ripple in this example is only 10 mV. This is the same as the ripple during normal operation in Fig. 2-4 and smaller than the burst mode ripple voltages for the other parts in Table. 1. This level of ripple voltage will be the goal of the new buck regulator.

2.3 Optimizing the Circuit for Ultralow Quiescent Current

The goal of this project is to minimize the current consumption of the circuit when in sleep mode. This means that only about a third of the circuit needs to be optimized for low power operation because the other two-thirds will be powered down. However, the current consumption of the part while switching will necessarily be larger than the sleep current, because when all the circuitry wakes up there will be brief moments of high current consumption. Even though it is beyond the scope of this project to design the circuitry which "wakes up" to be low power, there are ways the system can be optimized so that the effects of the high power circuitry can be minimized to keep the quiescent current during switching as close as possible to the current consumption during sleep.

There are two ways in which the influence of the high power circuitry can be minimized. The first is to minimize the number of times the part has to wake-up by maximizing the period between pulses when in burst mode. The part has to pulse after the output capacitor has been sufficiently discharged. The primary discharge paths for the capacitor when there is no output load are the DC current in the feedback resistor divider and DC reverse leakage current through the catch diode. Therefore, the simple, yet important, steps of maximizing the total resistance of the feedback divider and selecting a low leakage diode will maximize the period between pulses.

The second way to minimize the influence of the high power circuitry to is minimize the total time that the high power circuitry is awake each time it turns on. This time period is controlled by a sleep timer, which keeps all the high power circuitry on after a current pulse until the timer expires and the high power circuitry is then powered down. When the high power circuitry is powered down, the part can immediately switch once the error amplifier signals the need for a current pulse. If the part went to sleep immediately after a current pulse, then the next current pulse could come very quickly and the part could end up switching faster than the programmed switching frequency.

The plots in Fig. 2-6 show how the chip transitions between Burst Mode and PWM. When in burst mode, to provide increased load current the switching frequency is increased and the current limit is held constant. When in PWM mode, the switching frequency is constant and the current limit is increased to provide increased load current[21]. The sleep timer in the upper plots (Fig. 2-6 (A)) is $5\mu s$, which corresponds to the minimum programmable switching frequency of 200kHz. Therefore, there are smooth transitions between Burst Mode and PWM. However, the lower plots (Fig. 2-6 (B)) show the result of a shorter sleep timer. When transitioning from Burst Mode to PWM, the part can burst faster than the programmed switching frequency. Therefore, there is a range of load currents where the part can regulate in either burst or PWM mode. There is hysteresis in

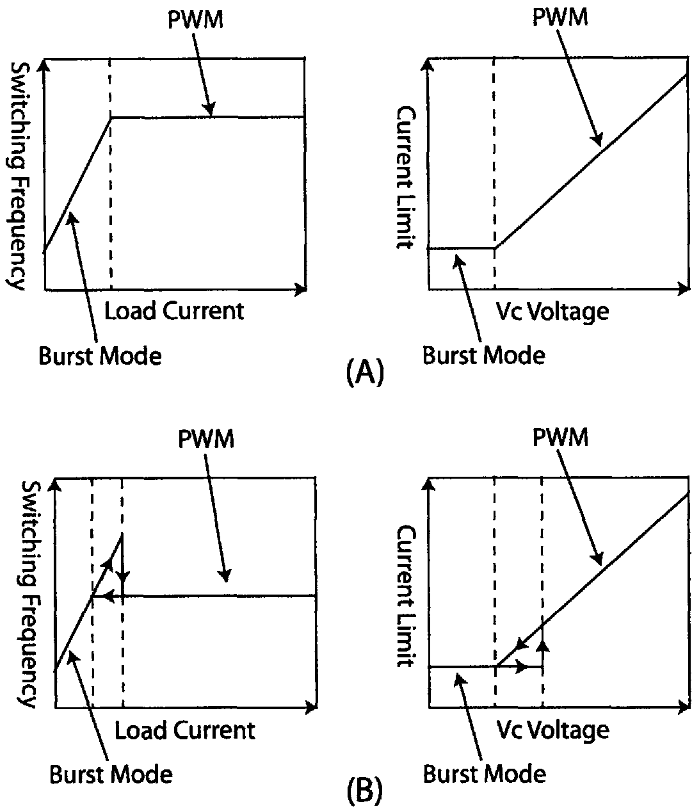

PWM
Switching Frequency
Load Current
Burst Mode
PWM
Current Limit
Vc Voltage
Burst Mode
(A)
PWM
Switching Frequency
Load Current
Burst Mode
PWM
Current Limit
Vc Voltage
Burst Mode
(B)

Figure 2-6: (A) Transition between Burst Mode and PWM when the sleep timer is slower than the programmed switching frequency. (B) Transition between Burst Mode and PWM when the sleep timer is faster than the programmed switching frequency

the load current where the transition between modes occurs and this hysteresis increases for smaller sleep timer durations.

Small sleep timer periods may lead to instabilities in the control loop of the regulator. However, the hysteresis between mode transitions is not necessarily detrimental. Since there is considerable hysteresis, as long as the part is able to regulate around a narrow control voltage range for a given load current, then there should not be erratic transitioning between modes, even when operating in the load range where two different regulation points exist. This means that decreasing the sleep timer to help minimize the quiescent current is worth investigating.

Chapter 3

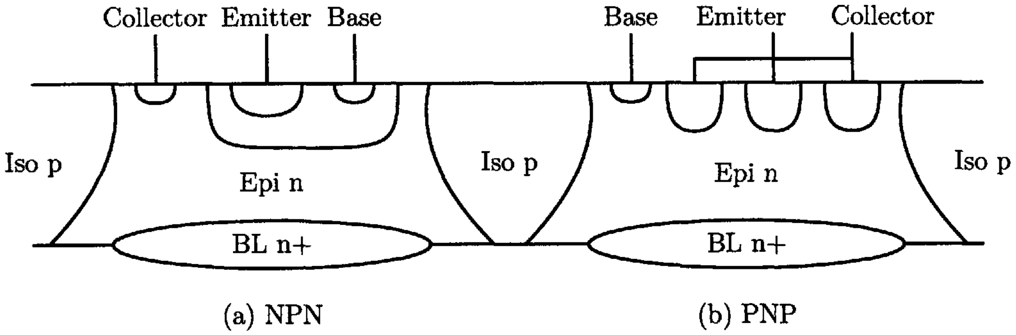
Low Power Circuits

The design work in this thesis is based around the idea of redesigning sub-circuits within the switching regulator to operate with low power consumption. The goal of a buck regulator requiring only a few micro-amps of quiescent current can only be realized if the individual sub-circuits require hundreds or even tens of nano-amps of DC current. This chapter describes the general approach to designing circuits for low current operation. It focuses on the differences between bipolar and MOS devices, in terms of capacitance, gain, leakage, and transitioning between different modes of operation. Understanding the advantages and disadvantages of the devices available in the process is essential to designing circuits capable of taking advantage of the full BiCMOS process used for this thesis project.

3.1 Device Capacitance

Speed is an important characteristic of many analog circuits. Amplifiers and comparators are often speed critical and need to be fast. In switching regulators there are often nodes which need to slew over several volts quickly. Parasitic capacitances need to be charged as a node is slewing. Charging such capacitances becomes more difficult when dealing with small currents and speed can be limited by parasitic capacitances. The best way to avoid these problems when operating with small currents is to minimize the capacitance of the devices one is using or to use devices with the smallest capacitances.

The structure of an NPN and a PNP device are shown in Fig. 3-1. There are three capacitances inherent in the NPN structure. The base-to-emitter capacitance (Cje), the base-to-collector capacitance (Cjc), and the collector-to-substrate capacitance (Cjs). These



(a) NPN

(b) PNP

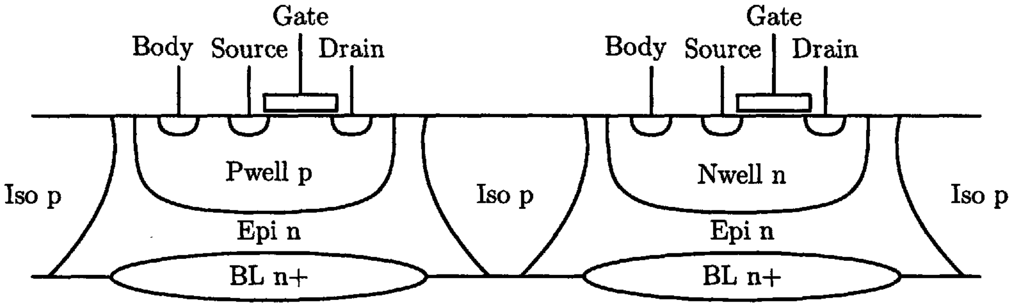
Figure 3-1: NPN and PNP Structures

three capacitances exist in the PNP device as well, except that the PNP has a base-to-substrate rather than a collector-to-substrate capacitance. All of these capacitances are junction capacitances, which are the sum of the sidewall capacitances, which scale with the perimeter of the junction, and the vertical junction capacitance, which scales with the area of the junction. The capacitances with the substrate are more complicated because it consists of both the capacitance with the walls of the iso and the buried layer to the substrate.

	NPN Normal Epi	NPN Light Epi	PNP Normal Epi	PNP Light Epi
Cje	16.3fF	25.5fF	16.3fF	16.3fF
Cjc	55fF	14.5fF	128fF	40.4fF
Cjs	226fF	226fF	309.9fF	309.9fF

Table 3.1: NPN and PNP junction capacitances for two different values of epi-doping. These capacitances are the values with zero volts of applied DC junction bias (C_{jo}).

The values of each of these capacitances for a few minimum sized bipolar devices in this process are listed in Table 3.1. The values listed are for zero volts of applied junction bias. For increasing bias the capacitances will decrease according to the equation $C_j = \frac{C_{jo}}{\sqrt{1+\frac{V_{bias}}{\Phi_o}}}$ [7]. There are a few characteristics to notice from the table. First, the collector junction capacitance is usually larger than the emitter junction capacitance because the collector junction is larger than the emitter junction. Second, the light epi devices have smaller collector junction capacitance. Junction capacitances are always smaller for lighter junctions because lighter junctions can deplete further. The edges of the depletion region act as plates in a parallel plate capacitor and the capacitance of such a structure is inversely proportional to the distance between the "plates". Third, the substrate junction capacitance is much larger than the other junctions due to the significantly larger size of the junction. The PNP device is larger than the NPN device, so sits in a larger tub having a larger substrate capacitance.



(a) NMOS (b) PMOS

Figure 3-2: NMOS and PMOS Structures

The structures of NMOS and PMOS devices are shown in Fig. 3-2. The device capacitances present here are the gate-to-source (C_{gs}), gate-to-drain (C_{gd}), source-to-body (C_{sb}), and drain-to-body (C_{db}) capacitances. The gate-to-body capacitance exists, but it is so small that it will not be considered. The gate-to-source capacitance includes the capacitance intrinsic to charging the gate to turn on the transistor. This is the oxide capacitance, which is inversely proportional to the oxide thickness used in the process. Overlap capacitance contributes to the gate-to-source and gate-to-drain capacitances. This is the capacitance with the drain and source regions which diffuse underneath the gate. The source and drain capacitance to the body are junction capacitances, which include sidewall and vertical junction components, just like the bipolar capacitances.

	NMOS		PMOS	
Cox	1.33	$\frac{fF}{\mu m^2}$	1.33	$\frac{fF}{\mu m^2}$
Cj	0.644	$\frac{fF}{\mu m^2}$	0.304	$\frac{fF}{\mu m^2}$
Cjsw	0.57	$\frac{fF}{\mu m}$	0.46	$\frac{fF}{\mu m}$
Cgdo,Cgso	0.1	$\frac{fF}{\mu m}$	0.315	$\frac{fF}{\mu m}$
Cgs	7.1	fF	8.0	fF
Cgd	0.4	fF	1.3	fF
Csb,Cdb	17.6	fF	11.2	fF

Table 3.2: NMOS and PMOS device capacitances for minimum sized devices, $4\mu m$ wide and $2\mu m$ long. These capacitances are the values with zero volts of applied DC bias.

The capacitances in this process for the basic NMOS and PMOS devices are listed in Table 3.2 for zero volts of applied bias. The top of the table shows the capacitances used in the transistor models, which are a function of transistor sizing. The values in the lower half of the table are capacitances between the device nodes calculated for a minimum device size of 4μm width and 2μm length.

It is easy to see that the device capacitances are much smaller for the MOS devices. Comparing the gate-to-source versus the base-to-emitter capacitances, the MOS parameters are two to three times smaller. Comparing the drain-to-gate versus the collector-to-base capacitances, the MOS parameters are more like thirty times smaller. Finally, if we assume that the body is tied to an incremental ground, the capacitance to ground is thirteen times smaller for the NMOS drain than the NPN collector.

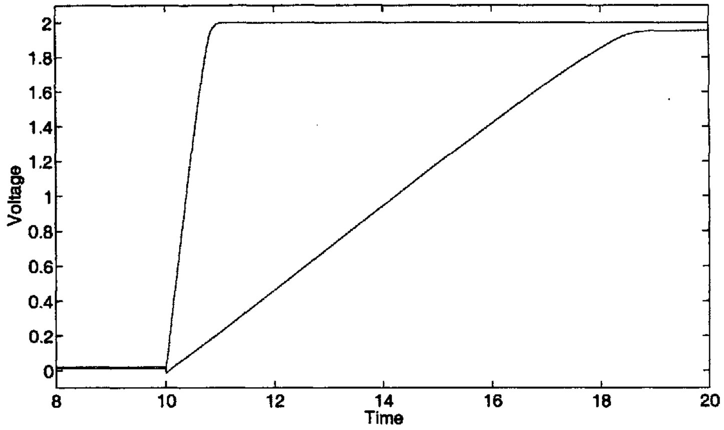


Figure 3-3: Comparison of slew rates for a MOS and bipolar transistor each loaded by a 100nA current mirror.

The difference between these device capacitances can be seen in a simple slew rate circuit. A NMOS transistor, with a PMOS current mirror load attached to its drain, is turned off, causing the NMOS drain to slew. A NPN is similarly set up with a PNP current mirror load and when the NPN is turned off, its collector will slew. This simulation was conducted with a two volt upper rail and a current mirror running 100nA of current. At any moment in time during the simulation, the output node of the bipolar transistor receives slightly more current from its load than does the MOS transistor output node from its load. Therefore, a slew rate comparison between the two devices is a fair comparison. The resulting output node voltage waveforms are shown in Fig. 3-3. The NMOS reached 90% of its final value in 0.74μs, while the NPN reached 90% of its final value in 7.53μs. The MOS circuit slews 10 times faster than the bipolar circuit. The total capacitance on the NPN collector is the NPN substrate capacitance, plus the NPN and PNP base-to-collector capacitances, which total 409 fF. The total capacitance on the NMOS drain is the combination of the drain-to-body and drain-to-gate capacitance for both the NMOS and PMOS, which equals 30.5 fF. Therefore, based on the models, the MOS circuit is expected to be about thirteen times faster.

3.2 Subthreshold Operation

Another important characteristic of analog circuits, including amplifiers and feedback loops, is gain [7]. Both voltage gain and current gain can be important depending on the circuit. The transconductance of both bipolar and MOS transistors will be considered. We will also consider the voltage gain of a transistor with an active load, which often occurs in basic differential-pair amplifiers.

$$BJT \ : \ g_m = \frac{I_c}{V_{th}} \quad r_o = \frac{V_A}{I_c} \tag{3.1}$$

$$MOS \ : \ g_m = \sqrt{2k\frac{W}{L}I_D} \quad r_o = \frac{1}{\lambda I_D} \tag{3.2}$$

The basic equations for the transconductance and output resistance of a bipolar transistor and a MOS transistor are listed in Eqn. 3.1 and 3.2, respectively. These equations hold when the the bipolar is in the forward active region where the base-to-emitter junction is forward biased and there is more than about 100 mV of collector-to-emitter bias, so that the collector-base junction is reversed biased. The MOS is in the active region where the gate-to-source voltage is above V_T and the drain-to-source voltage is above about 100 mV.

There is another useful region of MOS operation, which occurs at low currents. When the drain current is low, the gate-to-source voltage is nearly equal to V_T or even slightly below V_T. This region is called subthreshold, or alternatively referred to as weak inversion, while the normal MOS operation described above is called strong inversion. The drain current is a exponential function of V_{gs} (Eqn. 3.3) rather than a square-function of V_{gs} as in operation with normal current levels.

$$I_D = I_o e^{\frac{V_{gs}}{nV_{th}}} (1 + \lambda V_{ds}) \tag{3.3}$$

$$n = 1 + \frac{C_B}{C_{ox}} \tag{3.4}$$

The relationship between gate voltage and drain current changes because the basic mechanism behind the transistors' operation changes. Under normal operation, a channel is formed between the source and drain, and current flows due to the potential difference between the source and drain. The drain current is a drift current. In subthreshold, however, a channel does not completely form between the gate and source, and the charge flow that occurs is because of diffusion. The drain current is a diffusion current. It is no coincidence that the current equation looks similar to the current equation for a bipolar transistor, a device exhibiting current diffusion. Unlike the bipolar equation, the subthreshold current equation has an additional factor n. The voltage of the silicon between the gate and the source is less than the transistor gate voltage. It is smaller based on the capacitive divider between the oxide capacitance and the body capacitance of the device (Eqn. 3.4).

Based on the subthreshold current equation, the transconductance and output resistance can be calculated (Eqn. 3.5). The transconductance is the same as that for a bipolar except for the factor of n. The output resistance is the same as it is in strong inversion. Empirically, the quantity lambda is the same as it is in strong inversion.

$$g_m = \frac{I_D}{nV_{th}} \quad r_o = \frac{1}{\lambda I_D} \tag{3.5}$$

The transconductance (gm) versus current plot in Fig. 3-4 summarizes the transistor properties explained above. The MOS transistor g_m is proportional to current when operating is subthreshold and so has a linear curve on the plot as does the NPN transistor. At higher currents the MOS transistor comes out of subthreshold and the g_m exhibits a square root of current dependence. The length of the MOS transistor has no effect on g_m when in subthreshold, but g_m decreases with increasing length in strong inversion[9]. It is good to note that the transconductance is always greater for larger bias currents, regardless of whether it is in weak inversion or strong inversion. However, the transconductance per unit of bias current is largest when in subthreshold. Regardless of how the MOS transistor is

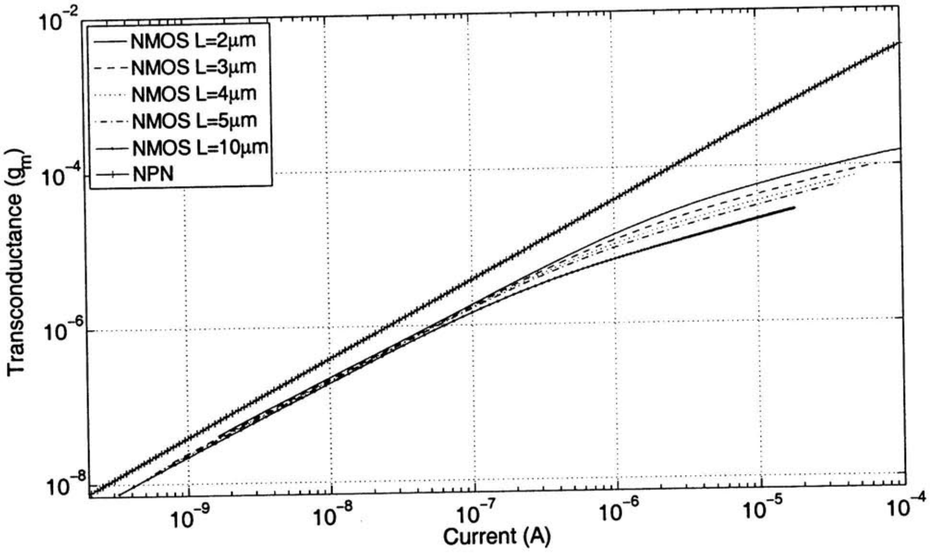


Figure 3-4: Transconductance versus current for NPN and NMOS devices. When the MOS devices are in subthreshold their transconductance is proportional to current, as are the NPN devices.

operated, the bipolar has larger g_m for a given current consumption.

It is interesting to note that the transistor is in subthreshold for larger currents when the gate length is smaller. This makes sense because the gate voltage is smaller for a given current when the device length is smaller. For a minimum size device, the subthreshold cutoff occurs around current densities of about $250\frac{nA}{\mu m}$.

The plot of intrinsic gain ($g_m r_o$) versus current in Fig. 3-5 is also instructive. The gain is independent of current when the MOS is in subthreshold because g_m is proportional to current and r_o is inversely proportional to current. When the MOS transistor enters strong inversion, the gain decreases because r_o is decreasing faster than g_m is increasing. The length of the transistor increases the gain when in subthreshold because the length is inversely proportional to λ, which increases the output resistance for larger gate lengths[9]. The bipolar gain is flat for the majority of the plot for the same reason the MOS subthreshold gain is flat with current. The NPN with a lighter doped epi has increased gain than its higher doped counterpart, because the early voltage (V_A), and thus the output resistance, is larger. At very small currents the bipolar gain falls off as the output resistance and early voltage decrease with beta degradation. As for the previous plot, the bipolar transistor gain is always larger than that of the MOS transistor for a given current consumption.

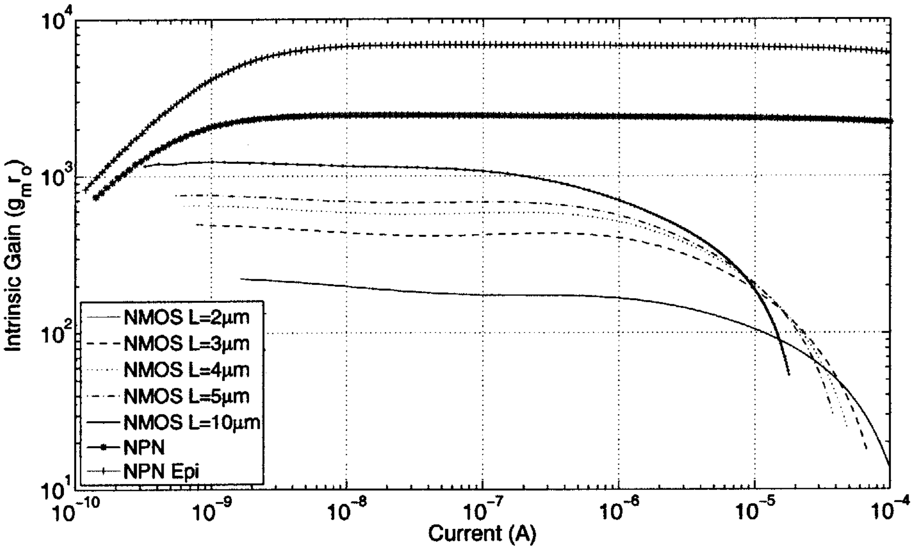


Figure 3-5: Intrinsic gain ($g_m r_o$) versus current for NPN devices with different epi dopings and NMOS devices with different gate lengths. When the MOS are in subthreshold threshold their intrinsic gain is maximized and independent of current.

These plots show that bipolar transistors have superior small signal parameters when compared to MOS transistor operating with the same bias current. However, if one needs to use MOS transistors for their superior capacitance, speed, and size, it is advantageous to operate them in subthreshold when current is at a premium. In subthreshold, MOS transistors have better intrinsic gain and g_m per unit of current than when in strong inversion. Therefore, for the low current circuits being designed in this thesis, the trade off in current gain and voltage gain when switching from bipolar to MOS devices is not as bad as it might be when using larger bias currents.

3.3 Base Currents and Saturation

When designing low current circuits, the existence of base currents must be kept in mind. Beta from the transistors in this process are typically greater than one hundred. However, beta is a process parameter, which can vary considerably. So for the sake of making conservative calculations, a beta value of one hundred will be used. If a sub-circuit is operating with 100nA, a base current of equal value will be generated by a collector current of 10μA. Therefore, the subcircuit current would be altered by 10% if connected to the base of a transistor operating with only 1μA of collector current. This means that when interfacing circuits, base current must be taken into careful consideration, and if possible, MOS transistors should be used to avoid the effect of DC base current altogether.

Another characteristic of bipolar transistors which must be considered is PNP transistors in saturation. The PNP transistors in this process are lateral transistors, meaning carriers travel across the wafer near the surface from p-type diffusion to p-type diffusion (Fig. 3-1(b)). When the collector is not reversed biased because the transistor is operating in the saturation region, minority carriers in the base are not readily swept up by the collector. Therefore, the minority carriers are able to get past the collector and get swept up by the substrate, which is strongly reverse biased. In this scenario, the PNP transistor will not be supplying any current through its collector, but current will flow to ground through the substrate. This current is being wasted, which is unacceptable in a part striving for low current consumption.

PMOS transistors operating in a similar regime, namely the linear or cutoff regions, does not suffer from this same problem. If the drain-to-source voltage goes to zero, current will not flow across the formed channel and no current will be wasted to the substrate.

3.4 Leakage

Normally leakage currents are small enough compared to transistor bias currents that they can be ignored. However, when transistors operate with tens of nano-amps at high temperatures, leakage currents become significant compared to the bias levels. The temperature dependence of the leakage current will be described so that estimates of the magnitude of the leakage current and the parameters which affect it can be understood.

$$I_D = AJ_S\left(e^{\frac{qV_D}{kT}} - 1\right) \tag{3.6}$$

The typical diode equation is shown in Eqn. 3.6. When the diode voltage (V_D) is negative the diode current is approximately equal to the saturation current ($-AJ_S$). This reverse current is typically on the order of femto-amps at room temperature, but it has significant temperature dependence.

$$J_S = \frac{qD_h n_i^2}{N_D L_h} + \frac{qD_e n_i^2}{N_A L_e} \tag{3.7}$$

$$J_S \propto n_i^2 \propto T^3 e^{-\frac{E_g}{kT}} \tag{3.8}$$

The equation for the saturation current density in Eqn. 3.7 is comprised of diffusion coefficients (D), doping concentrations (N), non-depletion region length (L), and the intrinsic carrier concentration (n_i). Only the intrinsic carrier concentration has a strong temperature dependence, which leads to the temperature dependence of the saturation current (Eqn. 3.8)[8, p. 469-71].

The leakage current at room temperature is observed to be larger than that predicted by the saturation current. This is the result of a second reverse current mechanism. Thermally generated electron-hole pairs in the depletion region, which are quickly swept apart generate a significant current during reverse bias. This recombination-generation (R-G) current is not factored into the normal diode equation. The equation for the R-G current is shown in Eqn. 3.9, where τ is the carrier lifetime in the depletion region and W is the width of the depletion region[19, p. 270-3].

$$J_{R-G} = \frac{qWn_i}{\tau} \tag{3.9}$$

Since the R-G current is only proportional to n_i, not n_i^2, it increases more slowly than the saturation current as temperatures rise. Therefore, although the R-G current is dominant at lower temperatures, the saturation current dominates at elevated temperatures.

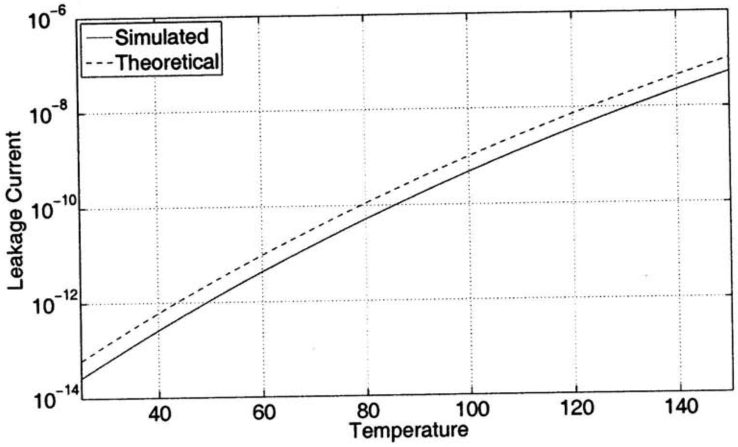


Figure 3-6: Simulated leakage current plotted against $T^3 e^{-\frac{E_g}{kT}}$, the theoretical temperature dependence.

The temperature dependence used in circuit simulation is shown in Fig. 3-6 to match the temperature dependence of the saturation current and n_i^2. It is acceptable to ignore R-G current because we only care about leakage current at high temperatures where the R-G current is less significant.

In a transistor device the diode between the buried layer (BL) and substrate, and the diode between the p doped isolation (Iso) and n doped well, generate the most leakage because they are of the largest size. The BL-substrate diode leakage is proportional to device area, while the Iso-well diode leakage is proportional to device perimeter. For a standard size NPN device the leakage current at 125°C is calculated to be about 3.6nA, 1.3nA coming from the BL-substrate diode and 2.3nA coming from the Iso-well diode. For larger devices, for example an NPN with 16 emitters, the leakage is calculated to be about 7.4nA with 3.6nA coming from the BL-substrate diode and 3.8nA coming from the Iso-well diode (Fig. 3-6 is calculated using a 16 emitter sized NPN device).

Even at elevated temperatures the leakage currents are small. However, they are not negligible when bias currents are on the order of tens of nano-amps. Therefore, the potential effects of leakage currents should be considered during circuit design, in particular when accuracy and matching is necessary. For example, a current mirror with one extra leakage component will result in a 3.6% error for 100nA currents and 7.2% error for 50nA currents.

Chapter 4

Control Loop Modeling for Frequency Compensation

The primary function of a buck switching converter is to properly regulate the output voltage over a range of loads and transients. Therefore, the control loop must be modeled so that the frequency characteristics of the regulator can be understood. Then the loop can be compensated to ensure stability and good transient response for all loads and load steps. This chapter describes the modeling of a current mode buck converter and its frequency compensation. This will lead to constraints, which will influence the design of the error amplifier.

4.1 Voltage Mode Model

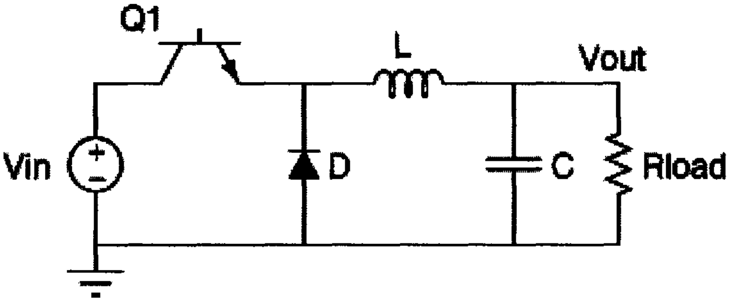


Figure 4-1: Basic circuit for a buck switching regulator.

To generate a set of equations to model the dynamics of a basic buck converter we need to use an average circuit model. We replace the switching elements of the circuit with current or voltage sources to abstract their switching behavior into averaged behavior[8]. The transistor switch is on for a fraction of the switching period based on the duty cycle, d. When the switch is on, it supplies the inductor current and when the switch is off, it runs zero current. Therefore, we can average the behavior of the switch by replacing it with a current source providing a local average current, $d\bar{i}_L$. Similarly, the voltage across the diode is equal to V_{in} when it is off and equal to zero when it is on. Therefore, we can average the behavior of the diode by replacing it with a voltage source providing a local average voltage, $d\bar{v}_{in}$. The complete average circuit model for the buck converter is shown in Fig. 4-2.

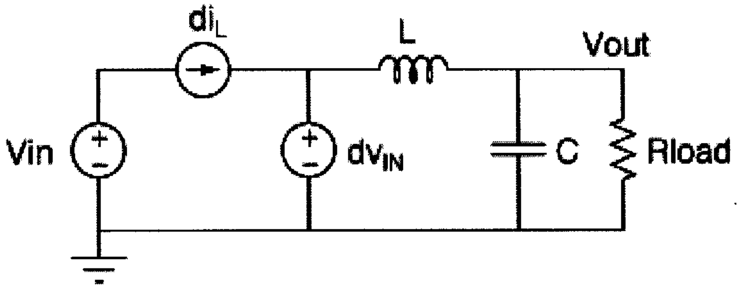


Figure 4-2: Basic average circuit model for a buck switching regulator. The NPN switch has been replaced with a current source of value di_L and the diode has been replaced with a voltage source of value dv_{IN}.

Now we can examine the current and voltage across the inductor and capacitor using the averaged circuit model.

$$L\frac{\partial \bar{i}_L}{\partial t} = d\bar{v}_{in} - \bar{v}_o \tag{4.1}$$

$$C\frac{\partial \bar{v}_o}{\partial t} = \bar{i}_L - \frac{\bar{v}_o}{R} \tag{4.2}$$

Next, we want to replace each averaged variable by the sum of its DC and AC components, so that we can find the small signal AC behavior of the converter. For example, $\bar{i}_L$ becomes $I_L + \tilde{i}_L$, where the variable with the tilde represents the AC component. We do this for the inductor current, input voltage, output voltage, and duty cycle. After approximating the AC component of the input voltage as zero ($\tilde{v}_{in} = 0$) and canceling the DC bias point components in each equation, we get the following result:

$$sL\tilde{i}_L = \tilde{d}V_{in} - \tilde{v}_o \tag{4.3}$$

$$sC\tilde{v}_o = \tilde{i}_L - \frac{\tilde{v}_o}{R} \tag{4.4}$$

Combining these two equations to eliminate $\tilde{i}_L$, we can get the transfer function relating an incremental change in duty cycle to the incremental change in output voltage[16].

$$\frac{\tilde{v}_o}{\tilde{d}} = \frac{V_{in}}{s^2LC + s\frac{L}{R} + 1} = \frac{\frac{V_{in}}{LC}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}} \tag{4.5}$$

This transfer function shows that the system has two complex poles. Therefore, this system can exhibit poor damping or even instability under high-gain feedback control. Some sort of frequency compensation will be necessary to stabilize the voltage mode converter.

4.2 Current Mode Model

This part does not control the duty cycle directly because it is a current mode part. Rather, it servos the peak inductor current, which indirectly sets the duty ratio. This can be easily seen in a block diagram of the control loop (Fig. 4-3)

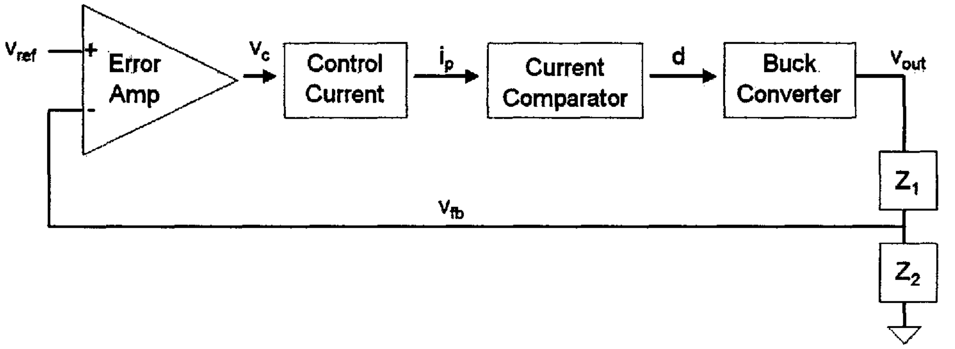


Figure 4-3: Block diagram of the current mode control loop. The inherent buck converter system regulates an output based on the duty cycle of the switch. The feedback through the error amplifier generates a control voltage, which sets the peak current control signal. The peak current control signal determines the duty cycle; thus the control voltage only indirectly sets the duty cycle.

This means that to find the transfer function of the system we need to find the relation between the peak inductor current and the duty ratio. By examining the interaction between the inductor current and the slope compensated peak current level (Fig. 4-4), one can use geometry to find the relationship between duty cycle and peak inductor current[17].

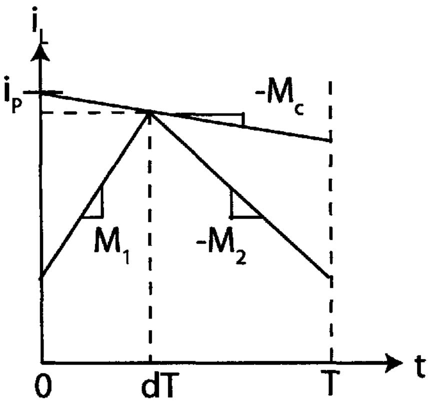


Figure 4-4: The inductor current over one switching period. Geometry is used to find the average inductor current as a function of the peak inductor current.

Take the peak inductor current value and subtract the average current delivered per unit time during one cycle to find the average current.

$$\bar{i}_L = (i_p - M_c dT) - \frac{1}{T}\left[\frac{1}{2}M_1 d^2 T^2 + \frac{1}{2}M_2 (1-d)^2 T^2\right] \tag{4.6}$$

$$\bar{i}_L = i_p - M_c dT - \frac{1}{2}M_1 d^2 T - \frac{1}{2}M_2 (1-d)^2 T \tag{4.7}$$

The slopes M_1 and M_2 are the ramp rates of the inductor and are equal to $\frac{V_{in}-V_o}{L}$ and $\frac{V_o}{L}$, respectively. Using the expressions for the ramp rates, we can linearize the equation around a DC operating point[17][18].

$$\bar{i}_L = i_p - M_c dT - \frac{1}{2L}(v_{in} - v_o) d^2 T - \frac{1}{2L} v_o (1-d)^2 T \tag{4.8}$$

$$\tilde{i}_L = \tilde{i}_p - M_c \tilde{d} T - \frac{1}{2L}(\tilde{v}_{in} - \tilde{v}_o) D^2 T - \frac{1}{2L} \tilde{v}_o (1-D)^2 T \tag{4.9}$$

The bias points for I_L, I_p, V_{in}, and V_o cancel, and the $\tilde{v}_{in}\tilde{d}$ and $\tilde{v}_o\tilde{d}$ terms are approximated as zero, which yields Eqn. 4.9. Finally, we can solve for the incremental change in duty cycle ($\tilde{d}$) in terms of the control variable $\tilde{i}_p$, which will allow us to convert the voltage mode model into a current mode model.

$$\begin{aligned} \tilde{d} &= \frac{1}{M_c T}\left(\tilde{i}_p - \tilde{i}_L\right) - \frac{D'^2 - D^2}{2LM_c}\tilde{v}_o && (4.10) \\ \tilde{d} &= A\left(\tilde{i}_p - \tilde{i}_L\right) - B\tilde{v}_o && (4.11) \end{aligned}$$

Eqn. 4.11 has been simplified by ignoring the incremental change in input voltage and substituting the variables A for $\frac{1}{M_c T}$ and B for $\frac{D'^2 - D^2}{2LM_c}$. By plugging the expression for $\tilde{d}$ into the buck linearized model (Eqn. 4.4), we can get the equations for the current mode linearized model.

$$\begin{aligned} sL\tilde{i}_L &= \left[A\left(\tilde{i}_p - \tilde{i}_L\right) - B\tilde{v}_o\right] V_{in} - \tilde{v}_o && (4.12) \\ sC\tilde{v}_o &= \tilde{i}_L - \frac{\tilde{v}_o}{R} && (4.13) \end{aligned}$$

With some algebra, we can find a transfer function for the incremental change in output voltage in response to an incremental change in the peak current limit.

$$\begin{aligned} \frac{\tilde{v}_o}{\tilde{i}_p} &= \frac{AV_{in}}{(sL + AV_{in})\left(sC + \frac{1}{R}\right) + BV_{in} + 1} && (4.14) \\ &= \frac{\frac{Av_{in}}{LC}}{s^2 + \left(\frac{AV_{in}}{L} + \frac{1}{RC}\right)s + \left(\frac{AV_{in}}{LRC} + \frac{BV_{in}+1}{LC}\right)} && (4.15) \end{aligned}$$

The resulting transfer function shows that we still have a two pole system, but some numerical work is required to determine how the poles have changed from those in the voltage mode case. If $\frac{AV_{in}}{R}$ is much greater than $BV_{in} + 1$, then the system simplifies to having a pole at $-\frac{1}{RC}$ and a pole at $-\frac{AV_{in}}{L}$. We will consider a converter with parameters approximately in the middle of their possible range to get a sense for these variables. If the part is converting 12V to 3V at a switching frequency of 600kHz with a load of 6Ω, a 4.7μH inductor, and a 22μF capacitor we get the following values:

$$
\begin{aligned}
\frac{AV_{in}}{R} &= \frac{V_{in}f}{RM_c} \approx \frac{12*0.6*10^6}{6*0.3*10^6} = 4 && (4.16)\\
BV_{in}+1 &= \frac{V_{in}(1-2D)}{2LM_c}+1 \approx \frac{12*0.5}{2*4.7*10^{-6}*0.3*10^6}+1 = 3.13 && (4.17)\\
\frac{1}{2\pi RC} &\approx \frac{1}{6.28*6*22*10^{-6}} = 1.21kHz && (4.18)\\
\frac{AV_{in}}{L} &= \frac{V_{in}f}{M_cL} \approx \frac{12*0.6*10^6}{0.3*10^6*4.7*10^{-6}} = 5.1MHz && (4.19)
\end{aligned}
$$

It turns out that rather than being much larger than $BV_{in}+1$, $\frac{AV_{in}}{R}$ is approximately equal to it. However, the two poles that would have resulted from such an approximation are separated by over three orders of magnitude. Therefore, since we want to double the product of the poles, while keeping their sum the same, the lower frequency pole will be twice as large and the higher frequency pole will stay about the same. This means that the system will have poles at about $-\frac{1}{\pi RC}$ and $-\frac{AV_{in}}{L}$. The smaller pole location will change depending on the load current and switching frequency as the ratio between $BV_{in}+1$ and $\frac{AV_{in}}{R}$ change. However, they will still be on the same order regardless of the parameters we choose.

4.3 Circuit Model for Compensation

The linear averaged circuit model for the current mode converter gives us a nice result with which to easily model and analyze compensation networks. The crossover frequency of the control loop is required to be about an order of magnitude below the switching frequency for the linear averaged circuit model to remain a good approximation. This means that we have only one system pole ($\frac{1}{\pi RC}$) because the other pole is higher than the switching frequency, which we are staying far away from anyway. The system pole is about twice the frequency of a pole generated by the output capacitor and load resistor. Thus, the system pole can easily be included in a test circuit by using an output resistor which corresponds to the desired current load, and an output capacitor half the size of what will actually be used in a typical application.

The combination of an error amplifier with a voltage gain of about 500, a 0.85 power stage transconductance, a 6.6 ohm load, and a 1:2.7 feedback voltage divider results in a loop gain on the order of a thousand. If the output pole is about 1kHz, then the converter will have a crossover frequency of about 1MHz. This is greater than the minimum possible programmable switching frequency of 200kHz, which is unacceptable. This simple calculation demonstrates the need to compensate the current mode converter.

Now we need to think about the best method of frequency compensation. Adding a dominant pole will work, but will restrict us to crossover frequencies below the $\frac{1}{\pi RC}$ system pole to achieve stability. We would hope to get a crossover frequency in the tens of kHz because that is about an order of magnitude below the lowest possible programmable switching frequency. In other words, tens of kHz crossover is the fastest, stable control loop we could hope for given the constraints. Therefore, a zero should be added above the system pole to get an enhanced phase margin at crossover frequencies above the system pole. Thus a pole-zero compensation scheme will achieve the desired control loop crossover frequency in the tens of kHz range. The desired frequency response after compensation is depicted in Fig. 4-5.

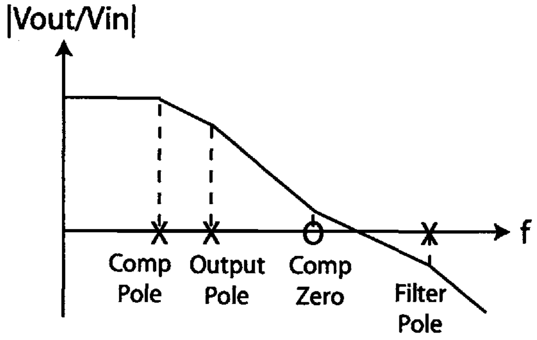


Figure 4-5: Bode plot showing the desired poles and zeros in the loop transfer function after proper compensation.

The pole-zero compensation is easily achieved physically in the circuit. A compensation resistor and capacitor in series on the output of the error amplifier will generate both a pole and a zero. It is also a good idea to add a shunt filter capacitor to filter as much high frequency content as possible from the sensitive error amplifier output. The shunt filter capacitor will be sized so that the pole it creates will be far enough above the crossover frequency to have minimal effect on the loop dynamics. The control loop can be modeled as in Fig. 4-6[10].

The control loop block diagram approximates the error amplifier with a certain transcon-

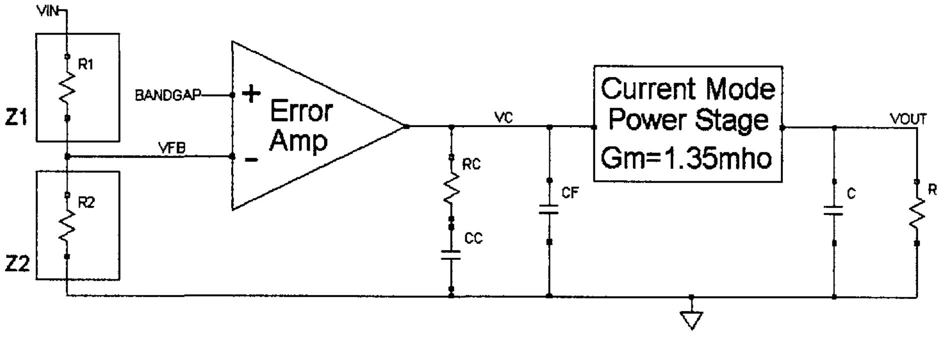


Figure 4-6: Diagram showing how the compensation scheme is achieved and modeled with a schematic.

ductance and output resistance, while the power stage is similarly approximated as a transconductance between the control voltage and the output current. Once the error amplifier is designed, it can replace the generic amplifier used in the block diagram. However, the power stage will always be approximated in this simple control loop model, which is used to analyze the frequency characteristics of the control loop. Later the dynamics of the real system can be studied by analyzing the step response of a full chip simulation. Those simulations are in the time domain and take significant time to run. Therefore, this simple block diagram approach is a good way to quickly adjust the compensation network in the frequency domain.

The transfer function for this control loop will consist of three factors:

$$\frac{V_{out}}{V_{in}} = \frac{V_{FB}}{V_{in}}\frac{V_c}{V_{FB}}\frac{V_{out}}{V_c} \tag{4.20}$$

The $\frac{V_{out}}{V_c}$ segment contributes one pole to our transfer function; the $\frac{1}{\pi RC}$ pole we have already discussed. The $\frac{V_{FB}}{V_{in}}$ segment contributes no poles or zeros if we are using a simple resistor divider network. This segment will be considered more in the next section on phase lead capacitance. The remaining $\frac{V_c}{V_{FB}}$ segment is where the compensation network is contained. Modeling the error amplifier output impedance as R_o, we can derive the transfer function for this segment.

$$\frac{V_c}{V_{FB}} = -g_m\left[\left(R_c+\frac{1}{sC_c}\right)||\left(\frac{1}{sC_f}\right)||R_o\right] \tag{4.21}$$

$$= \quad -g_m \left[\frac{R_o \left(1 + sC_cR_c\right)}{1 + s\left(C_cR_c + C_cR_o + C_fR_o\right) + s^2\left(C_cR_cC_fR_o\right)} \right] \tag{4.22}$$

This equation reveals that we have a zero at $\frac{1}{2\pi C_cR_c}$. It also reveals that we have two poles. The locations of these poles can be easily determined if a few approximations are made. First, the output impedance of the error amplifier is going to be on the order of a hundred mega-ohms because to get sufficient voltage gain with a small bias current, and thus small g_m, R_o must be huge. This means that C_cR_o is going to be much larger than C_cR_c. Second, the shunt filter capacitance is going to be approximately an order of magnitude smaller than the compensation capacitor. This will always be true because the shunt filter capacitor is not being used for compensation, but to filter the sensitive control node. Therefore, it will be selected to be as large as possible without interfering with the compensation network. With this in mind, it means that C_cR_o will be at least an order of magnitude greater than C_fR_o. The result when these approximations are implemented is shown in the equations below (Eqn. 4.25).

$$\begin{aligned} & 1 + s\left(C_cR_c + C_cR_o + C_fR_o\right) + s^2\left(C_cR_cC_fR_o\right) && (4.23) \\ \approx\ & 1 + s\left(C_cR_o\right) + s^2\left(C_cR_cC_fR_o\right) && (4.24) \\ \approx\ & \left(1 + sC_cR_o\right)\left(1 + sC_fR_c\right) && (4.25) \end{aligned}$$

Thus the compensation network provides two poles, one at $\frac{1}{2\pi C_cR_o}$ and one at $\frac{1}{2\pi C_fR_c}$. The pole contributed by the filter capacitor will need to be at a higher frequency than the zero or else the zero will not provide the extra phase margin needed to stabilize the system. This again limits the filter capacitor to be approximately an order of magnitude smaller than the compensation capacitor $\left(\frac{1}{2\pi C_C R_c} << \frac{1}{2\pi C_f R_c}\right)$.

The mathematics shows that the compensation network indeed generates a compensating pole and zero, and a higher frequency filter pole. The specific pole and zero locations for the compensated control loop are labeled in the ideal bode plot in Fig. 4-7.

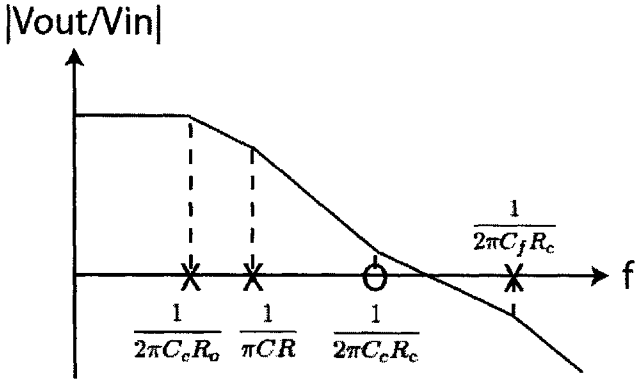


Figure 4-7: Bode plot showing the poles and zeros in the loop transfer function.

4.4 Phase Lead Capacitance

One caveat to this analysis is parasitic capacitance. On chip the parasitics will be insignificant, especially since most of the important nodes already contain some capacitance to ground. The one exception to this is the feedback node, which will have significant capacitance since it is connected to an external pin and has been modeled without shunt capacitance. As a result, the $\frac{V_{FB}}{V_{in}}$ segment of the control loop transfer function will no longer be flat with frequency.

First, lets examine the response of the feedback divider to a parasitic shunt capacitance, C_2.

$$\frac{V_{FB}}{V_{in}} = \frac{\left(R_2 || \frac{1}{sC_2}\right)}{R_1 + \left(R_2 || \frac{1}{sC_2}\right)} \tag{4.26}$$

$$= \frac{R_2}{R_1 + R_2 + sC_2 R_1 R_2} \tag{4.27}$$

The parasitic capacitance will generate a pole at $\frac{1}{2\pi C_2 (R_1 || R_2)}$. For 5pF of parasitic capacitance with 1MΩ and 1.7MΩ feedback resistors, this pole will be at 50.5kHz. This will be very close to the crossover frequency of our control loop and destroy the phase margin of the system. Smaller feedback resistors will alleviate this problem, but the largest possible feedback resistor are desirable to maximize the quiescent current performance of the switcher.

The use of a phase lead capacitor corrects the problem, while allowing the use of large feedback resistors. A phase lead capacitor, C_1, is placed in parallel with the upper feedback resistor and will have the following effect on the frequency response of the feedback divider.

$$\begin{aligned}\frac{V_{FB}}{V_{in}} &= \frac{\left(R_2 || \frac{1}{sC_2}\right)}{\left(R_1 || \frac{1}{sC_1}\right) + \left(R_2 || \frac{1}{sC_2}\right)} && (4.28)\\ &= \frac{R_2\left(1 + sC_1R_1\right)}{R_1 + R_2 + s\left(C_2R_1R_2 + C_2R_1R_2\right)} && (4.29)\end{aligned}$$

This setup results in a zero at $\frac{1}{2\pi C_1 R_1}$ and a pole at $\frac{1}{(C_1+C_2)(R_1||R_2)}$. If C_1 is much larger than C_2 and the feedback resistor ratio is 1:1.7, then the pole will be at a frequency 2.7 times higher than that of the zero. If a large enough phase lead capacitor is used to place both the pole and zero well below the crossover frequency, the pole-zero combination will increase the crossover frequency of the control loop, without contributing any phase at crossover.

Chapter 5

Chip Design

This thesis describes the design of a complete integrated circuit. The goal of realizing ultra low quiescent current could only be realized through a design fabricated in silicon. This project required transistor level design in addition to design on a block or sub-circuit level, so a board design with discrete blocks for each subcircuit would not have been useful. It also would have prohibited low current design because as traces and nodes get large, parasitics would significantly influence low currents.

This chapter describes the circuit blocks which were designed. Each sub-circuit is described individually, included the trade-offs and requirements inherent to each one. Since this project included the layout of the circuit so it could be fabricated and tested in silicon, a few of the key issues concerning the layout have also been described.

5.1 Circuits

The LT3480 was used as a basis for the design of this thesis project. The part only needed to operate off a small supply current during burst mode operation. Therefore, only the circuits which were powered on during burst mode needed to be redesigned for low current operation. These subcircuits encompassed about a third of the existing chip and are circled in the LT3480 block diagram shown in Fig. 5-1.

The circuits include the bandgap reference, the error amplifier, the power good (PG) comparator, the burst mode logic, the Vc clamp, and a shutdown circuit.

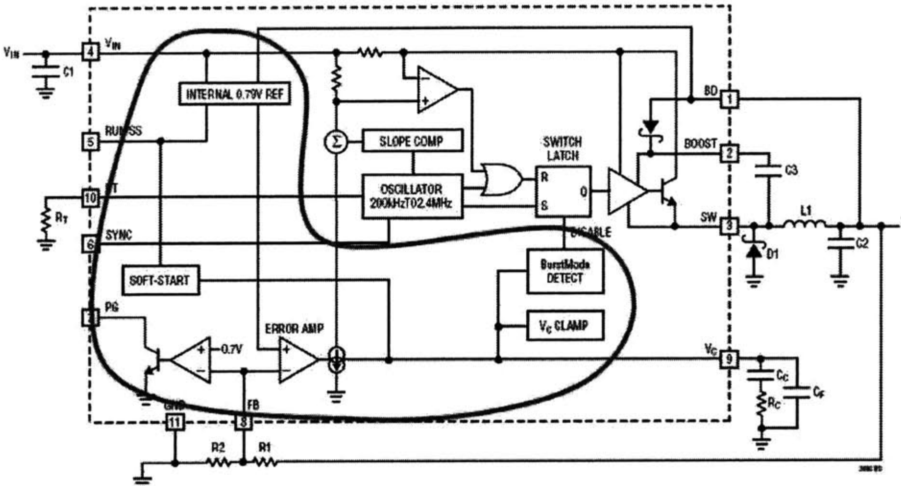

V_IN
C1
4
V_IN
INTERNAL 0.79V REF
5
RUN/SS
10
RT
R_T
6
SYNC
SOFT-START
7
PG
0.7V
ERROR AMP
Σ
SLOPE COMP
OSCILLATOR
200kHz TO 2.4MHz
SWITCH
LATCH
R
S
Q
DISABLE
BurstMode
DETECT
V_C CLAMP
BD
1
BOOST
2
C3
SW
3
L1
V_OUT
D1
C2
V_C
9
C_C
R_C
C_F
GND
11
FB
8
R2
R1

Figure 5-1: Block Diagram for LT3480 Buck Converter. The blocks which remain powered on during burst mode are circled.[11] (Used with permission)

5.1.1 Bandgap

The bandgap reference is one of the two most important micropower circuits in the voltage regulator. The bandgap circuit is the reference for the regulated output voltage and thus has to be accurate and constant across temperature.

A bandgap reference is the combination of a V_{be}, which had a negative temperature coefficient (tempco) and a positive tempco voltage. Often a delta V_{be} is used as the positive tempco voltage because it is proportional to absolute temperature (PTAT). When these two voltages are combined in the proper proportion, the temperature coefficients cancel to yield a voltage which is constant across temperature.

The desired bandgap circuit needs to be as current efficient as possible. Therefore, a Brokaw bandgap topology was used as in Fig. 5-2 because it is a simple topology and only requires two legs of current. Transistor Q2 is larger than transistor Q1, which creates a ΔV_{be} across R1. The emitter ratio of Q2 to Q1 and the value of R1 sets the current level through Q2. The current mirror established by M1 and M2, biases Q2 and Q1 with identical collector currents. The PTAT voltage across R1 also appears across R2 and is scaled by $2\frac{R2}{R1}$. Then, the PTAT voltage across R2 is added to the negative tempco V_{be} of Q1 to create the nearly constant tempco bandgap voltage at the base of Q1 and Q2.

The Brokaw topology is a good choice for a low current bandgap because Q1 is used

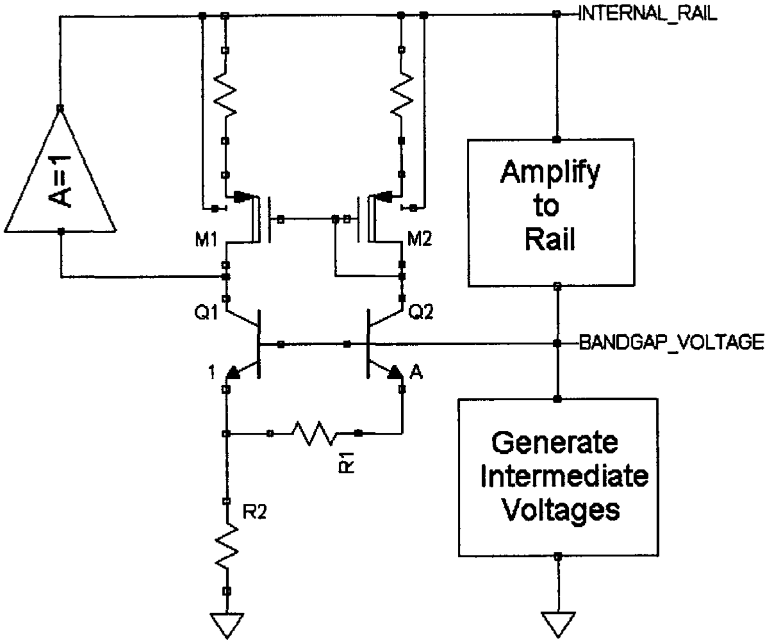


Figure 5-2: Block Diagram of the Brokaw bandgap circuit

for both the V_{be} and ΔV_{be} parts. Therefore, there are only two current legs, while other bandgap circuits might use three or more legs to generate the V_{be} and ΔV_{be} terms separately and then combine them.

The basic bandgap circuit also needs a feedback leg to set the voltage of Q1's collector. When Q1's collector voltage increases, the feedback loop causes the bandgap voltage to also increases, which means that Q1 has to run more current due to an increased base-to-emitter voltage. For M1 to supply more current to Q1, Q1's collector voltage decreases. Therefore, the feedback is negative. The feedback leg from the collector of Q1 to the internal rail has an AC gain of one. This is acceptable because the gain from the bandgap node to the collector of Q1 is high, so the loop gain is large. The feedback leg just needs to consist of level shifting to set the collector of Q1 to a DC level to properly bias Q1 and M1 in active regions.

The basic bandgap circuit has another segment which sets the internal rail voltage based on the bandgap voltage. It also generates a series of voltages less than bandgap to be used elsewhere in the regulator. This circuitry is doing double duty by providing a current which can be mirrored to all the other micropower circuits.

Leakage Considerations

Since the goal of this project is to decrease the quiescent current as much as possible, it is interesting to consider what the potential limitations are on the lower current limits of the bandgap reference. The bandgap reference is a DC circuit; it does not have to be fast. Therefore, good DC accuracy can be achieved using large capacitors to filter out high frequencies. The feedback loop will have a bandwidth of only a few hundred hertz to a few kilohertz, so should not be affected by the use of filter capacitors. Therefore, the tradeoff between current and speed does not have to be considered when lowering the current consumption of the bandgap because the bandgap circuitry does not need to be fast.

The most important consideration is leakage currents. At elevated temperatures the leakage of large junctions can become significant. As the bandgap operating current is decreased, the leakage current becomes larger in proportion and could potentially degrade high temperature performance. At 125°C the leakage in a standard transistor is about 2.8nA, but for the larger bipolar transistors used in the bandgap the leakage can be 7.0nA at 125°C.

The Brokaw bandgap is well suited to deal with leakage. The only sizable leakage comes from the NPNs forming the ΔV_{be}, which have sizable leakage between their large collector tubs and the substrate. The transistor emitter currents are set by the resistor R1, so leakage will not affect the NPN collector currents. Rather, it will cause the current mirror (M1 and M2) to source more current to supply both the collector current and the collector leakage. Therefore, if the leakage in both legs is matched, the leakage effects will be canceled. The current mirror is implemented with MOS transistors to minimize leakage effects. PNP devices have large base to substrate leakage, which would add leakage to the right leg of the bandgap and not to the left leg of the bandgap, if used for the current mirror. MOS devices leak from the body, which is connected to the internal rail. Therefore, the MOS leakage in the current mirror will not influence the bandgap.

The leakage effects on the bandgap voltage were simulated. The change in bandgap voltage was -6.14 mV per nA of leakage out of the left leg and 5.70 mV per nA of leakage out of the right leg. When current leaks out of the left leg, the voltage drop across R2 and the V_{be} of Q1 decrease, lowering the bandgap voltage. On the other hand, when current leaks out of the right leg, more current is mirrored to the left leg resulting in more voltage across R2 and the V_{be} of Q1 increasing, thus raising the bandgap voltage. These figures seem to indicate that the bandgap voltage will decrease by 0.44 mV per nA of matched leakage. However, this is erroneous because the V_{be} and ΔV_{be} terms are not a simple superposition of what is happening to Q1 and Q2 separately. In simulation, 10nA of matched leakage from each leg simultaneously resulted in a -0.2mV change in the bandgap voltage, which is not very significant when compared to predicted noise levels. Therefore, the key to good bandgap performance is to match the leakage.

The high temperature performance has been examined, but what about the low temperature performance? The most significant potential problem is beta degradation for temperatures reaching -40°C and below. The collector currents in the bandgap circuit are PTAT, so they will decrease significantly at low temperatures. The resulting decreased current density will cause the beta of the NPNs to plummet. Therefore, the base currents will increase relative to the collector currents, but the collector currents will be so small, on the order of nano-amps, that the base current should never be more than a few nano-amps. The bandgap node will be able to supply this base current, thus beta degradation should have little effect on the bandgap performance at low temperatures.

Resistor Tempco Effects

The bandgap voltage is not completely constant over temperature. The first order tempco of a V_{be} is canceled by a scaled PTAT voltage. However, a V_{be} has second-order effects, which lead to a parabolic curving in the bandgap voltage across temperature. The second order effects can be seen in Eqn. 5.1 as the $Hln(H)$ term (See Appendix A for derivation)[5].

$$V_{be} = E_{go} - \left\{ E_{go} - V_{ber} - V_R ln\left(\frac{I_C}{I_{CR}}\right)\right\} H - \sigma V_R H ln(H) \tag{5.1}$$

In this equation, H is the ratio of the temperature to a reference temperature, and V_{ber}, I_{CR}, and V_R are the measured V_{be}, collector current, and thermal voltage ($\frac{kT}{q}$) at the reference temperature.

In this process, the high resistance thin film resistors used have a significant temperature coefficient. The tempco of the resistors factors into the calculation of the bandgap voltage because the transistor collector current will change with temperature differently than it will for resistors with no temperature coefficient. Therefore, the ratio of the collector current to that at the reference temperature in the V_{be} equation will reflect resistor tempco.

$$\frac{I_C}{I_{CR}} = \left(\frac{T}{T_R}\right)^{\tau} = H^{\tau} \tag{5.2}$$

The variable τ represents the tempco of the transistor collector currents. If the resistors have no tempco, τ will be equal to one because a PTAT voltage across resistor R1 sets the collector currents, thus the collector currents will be PTAT. If the resistors have a positive tempco, τ will be less than one and if the resistors have a negative tempco, τ will be greater than one.

Substituting the collector current temperature dependence into the V_{be} equation still yields a first-order and parabolic temperature terms.

$$\begin{aligned} V_{be} &= E_{go} - \{E_{go} - V_{ber} - V_R ln\left(H^{\tau}\right)\} H - \sigma V_R H ln\left(H\right) & (5.3)\\ &= E_{go} - \left(E_{go} - V_{ber}\right) H + \left(\tau - \sigma\right) V_R H ln\left(H\right) & (5.4)\end{aligned}$$

Now the effects of the resistor tempco on the bandgap voltage and the variation in the bandgap voltage across temperature can be calculated[5].

$$\begin{aligned} V_{bg} &= V_{be} + \gamma H & (5.5)\\ \frac{\delta V_{bg}}{\delta H} &= \left(\gamma + V_{ber} - E_{go}\right) + \left(\tau - \sigma\right) V_R \left(1 - ln\left(H\right)\right) & (5.6)\\ \gamma &= E_{go} - V_{ber} + \left(\sigma - \tau\right) V_R & (5.7)\\ V_{bg} &= E_{go} + \left(\sigma - \tau\right) V_R \left(1 - ln\left(H\right)\right) H & (5.8)\end{aligned}$$

The variable γ represents how much PTAT voltage is necessary to counter-balance the first-order tempco of the V_{be} term. The equation indicates that for larger τ, less PTAT voltage is needed. In other words, less PTAT voltage is needed for more negative tempco resistors. More importantly, the equations indicate that the parabolic term in the V_{be} voltage is smaller when resistors with more negative tempco are used. Therefore, using negative tempco resistors makes the bandgap voltage more accurate across temperature and positive tempco resistors make it less accurate across temperature[13, p. 636].

$$\Delta V_{bg} = (\sigma - \tau)\, V_R \left(\frac{\Delta T}{T_R}\right)^2 \tag{5.9}$$

We will use high resistance-per-square SiCr resistors, which have a negative tempco of -2600 ppm, in this bandgap reference circuit. This means that τ will increase from 1 to 1.76. The first-order approximated equation for the change in bandgap voltage with temperature in Eqn. 5.9 can be used to estimate the bandgap performance. For a room temperature reference temperature of 298K, a temperature change of 100K, and a sigma value of 3, a change of 5.78mV is calculated for a bandgap with resistors with zero tempco[5]. When the negative tempco SiCr resistors are taken into account, the change in bandgap voltage between room and 125°C is calculated as 3.58mV. This is a 40% reduction in the parabolic bandgap error due to the effects of resistor tempco.

$$V_{bg} = E_{go} + (\sigma - \tau)\, V_R \tag{5.10}$$

The equation for the bandgap voltage at room temperature (Eqn. 5.10) shows that the bandgap voltage decreases for resistors with more negative tempco. This is important to consider when the bandgap voltage is going to be trimmed to a specific value at room temperatûre because if the wrong voltage is trimmed to at room, than the curvature of the voltage over temperature will be skewed. Based on Eqn. 5.10, the negative tempco resistors used in this process are expected to decrease the bandgap voltage at room by about 19.8mV.

5.1.2 Error Amplifier

The error amplifier is the other of the two most important micropower circuits in the part. The error amplifier is the heart of the control loop. It needs to have the proper tradeoff between gain, transconductance, slew rate, and frequency compensation.

The first system parameter to consider is output voltage accuracy at steady state. The bandgap voltage and feedback resistor accuracy are the primary factors for determining output voltage accuracy. However, the extent to which the output voltage changes as a function of the output load is determined by the voltage gain of the error amplifier. The control voltage Vc, which is the output of the error amp, has a range of 2V. This two volt range divided by the voltage gain of the error amp, sets how much the feedback pin must move when transitioning from no load to maximum load. The change in the feedback pin as a percentage of the 1.2V input to the error amp, gives one a measure of the percentage that the DC output voltage will change across the load range. It would be undesirable, however, to make the voltage gain larger than is necessary because it makes the amplifier more difficult to compensate. This in turn is because lowering the frequency of poles means making compensation components larger. Therefore, a voltage gain of four to five hundred is desirable because it yields a 0.4% to 0.33% error in the DC output voltage over load.

The second system parameter to consider is the response to load transients. The system needs to be stable across temperature, input voltage, and output load, plus have quick response to large system perturbations. This means we want to maximize the slew rate and transconductance of the amplifier while operating at a very low bias current. The choice of topology that will work best with the compensation scheme discussed in the previous chapter is our first concern. Minimizing the operating current will directly limit the maximum current the error amplifier can source or sink to drive the compensation capacitor. Therefore, to achieve a good slew rate with little current, the compensation capacitor must be as small as possible. A small compensation capacitor will increase the crossover frequency of the control loop, so the compensation capacitor can only be minimized to a certain limit. These trade-offs led to a compensation capacitor of about 4pF.

Selecting an amplifier topology with multiple stages means that the current used in the initial stages can not be used to charge the compensation capacitor. Therefore, a single stage amplifier topology was chosen because for a given current consumption the maximum amount of current to drive output capacitance is achieved with a single stage. The error amplifier has differential inputs so a simple source coupled differential pair with a current mirror load was used for this stage. Since the MOS transistors are operating is sub-threshold, the length of the devices can be increased to increase the amplifier output resistance until the desired voltage gain is obtained with a single stage. If we want the output voltage due to a sizable transient response to peak after no more than $10\mu s$, this means we want a slew rate on the order of $0.1\frac{V}{\mu s}$. A slew rate of this magnitude means the error amplifier needs 400nA of bias current. Each input device operating at 200nA yields an ideal transconductance in sub-threshold of about $3.85\mu S$.

The setup shown in Fig. 5-3 is used to quickly simulate the frequency and transient response of the system. The differential pair with active load is used as the error amplifier, as shown in the figure. The error amplifier is biased with 400nA of tail current and the

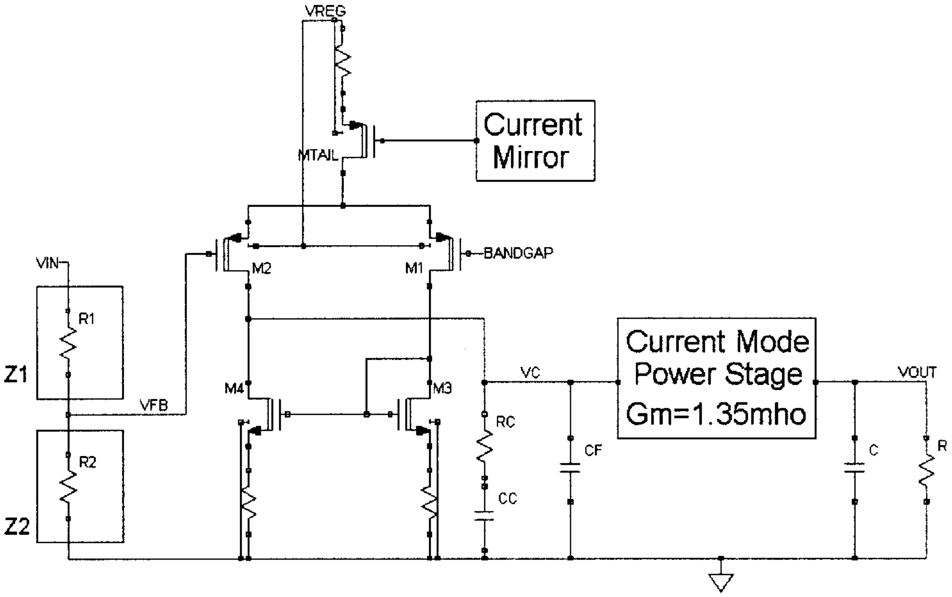


Figure 5-3: Block diagram of control loop with error amplifier circuit explicitly included. This diagram is used to simulate frequency and transient response of regulator.

devices are sized to provide a voltage gain of four to five hundred. The compensation component sizes were determined experimentally based on this simulation. Typical output components were used, namely a 22μF output capacitor and a 6.6Ω load resistor, which corresponds to a current load of 0.5A since the feedback resistor divider is set for a 3.3V output. A nice frequency response is achieved when the compensation capacitor (C_C) is 4pF, the compensation resistor (R_C) is 3MΩ, and the shunt filter capacitor (C_F) is 0.1pF. The resulting bode plot is shown in Fig. 5-4 with a crossover frequency of 43.2kHz and a nice phase margin of 69.7 degrees. It is important that the phase margin is well above the desirable 60 degrees because high order poles and proximity to the switching frequency, which are not taken into account with this simple simulation model, will lead to decreased phase margin.

The simulated results to a load step from 0.5A to 1A and 1A to 0.5A are shown in Fig. 5-5. A load step is a much easier control loop test to conduct on the complete circuit than a frequency response measurement. Furthermore, a transient simulation will include the time variation and switching characteristics of the system, which are lost in the frequency response simulation due to the approximation of circuit averaging. Therefore, a load step simulation was made with both the complete buck regulator circuit and the simplified

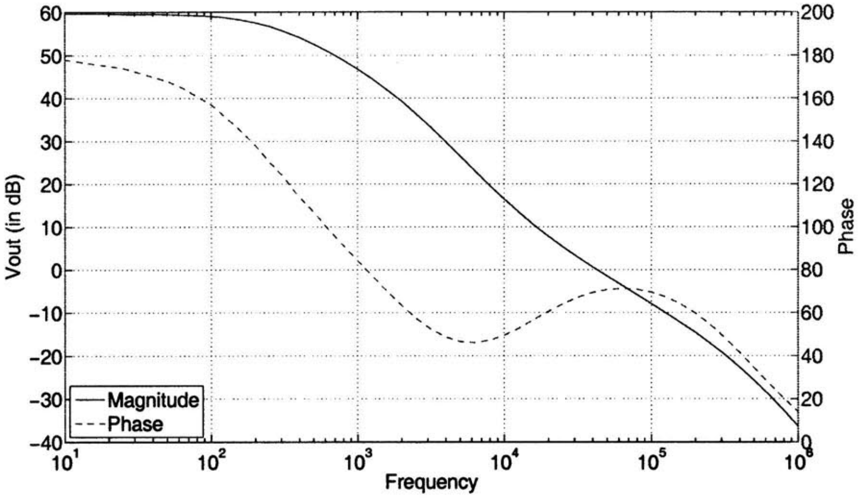


Figure 5-4: Bode Plot of the compensated control loop. The crossover frequency of 43.2kHz with 69.7 degrees phase margin is labeled.

control loop circuit, which was used to simulate the frequency response. Both these circuit experienced an step in the output load from 0.5A to 1A at 600μs and a step back from 1A to 0.5A at 650μs, as seen in the figure. Both simulations return to regulation in about 40μs with less than 80mV overshoot in either direction. The lack of ringing in both waveforms demonstrates good phase margin. The frequency and transient simulations show that the choice of error amplifier and compensation network are working well.

5.1.3 PG Comparator

The power good (PG) comparator is used to flag the user when the power has reached 90% of the desired regulated value. Whenever the output voltage is below 90% of the set voltage the PG pin will pull current and if the output is above the 90% threshold than zero current will be drawn by the PG pin. By connecting a pull-up resistor between the PG pin and the output voltage, a logic level can be created at the PG pin where it is high if the voltage is in regulation and low if the voltage is not in regulation.

The PG comparator consists of a simple comparator connected to an inverter, which drives a large NMOS device, as shown in Fig. 5-6. The comparator does not have to have large gain or be fast. Therefore, it is designed as a simple differential pair of MOS devices operating in subthreshold with a small amount of current, in this case about 50nA total.

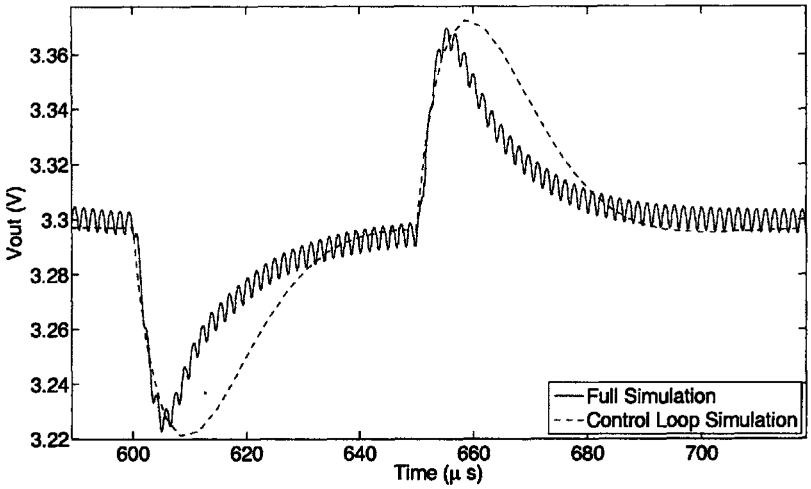


Figure 5-5: Bode Plot of the compensated control loop. The crossover frequency of 43.2kHz with 69.7 degrees phase margin is labeled.

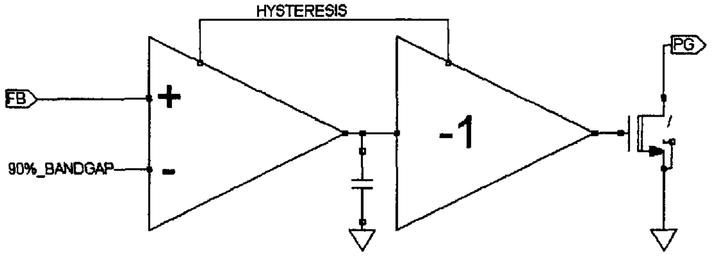


Figure 5-6: Block diagram for PG comparator circuit

A gain of a few hundred provides sufficient accuracy, especially when combined with the inverter, which will drive the NMOS hard. Running the comparator at small currents does not matter because the comparator does not have to be fast, in fact, it will be compensated to be slow. The comparator will be compensated to have a crossover frequency of about 150kHz to be below the minimum possible operating frequency of 200kHz, so that switch coupling is rejected. The slew rate will be set at about 0.1 $\frac{V}{\mu s}$, so that it will take at least $10\mu s$ for the output to toggle, so that during normal load transitions the PG comparator will not trip. The pg comparator is designed with about 27mV of hysteresis to prevent jitter near transition. It will also be able to sink about 1mA when the output NMOS is on with 400mV of drain-to-source voltage.

5.1.4 Burst Logic

During light load operation, the output capacitor will charge quickly with a current pulse, then it will discharge very slowly. When the output voltage remains well above the regulated value for a period of time significantly longer than the full frequency switching period, the Vc control voltage (the output of the error amplifier) will decrease to values near the bottom of its range. When the Vc voltage is below a certain threshold, the part will enter into burst mode, also known as pulse frequency modulation (PFM).

PFM burst mode is achieved by comparing the Vc value to an exponentially decaying threshold waveform which decreases from an upper voltage limit to a lower voltage limit. As the output capacitor slowly discharges, the Vc voltage will creep up. When the Vc voltage becomes larger than the threshold waveform, a comparator will trigger the switch to turn on for the minimum possible duration to provide a small current pulse. The threshold waveform will be reset and the jump in the output voltage as a result of the current pulse will cause the Vc voltage to decrease sharply.

When the Vc voltage crosses the threshold waveform while it is still decaying, the comparator acts as a voltage controlled oscillator (VCO). When the output load is small, the output capacitor discharges slowly, the average Vc value is near the lower threshold voltage limit, and the pulse frequency is low. When the load is slightly larger, the output capacitor discharges faster, the average Vc value increases, and thus the pulse frequency increases. The change in pulse frequency for a given change in average Vc level is determined by the decay rate of the threshold waveform.

When the Vc voltage crosses the threshold waveform when its has fully decayed to its lower voltage limit, this represents the lightest of loads, such as no load. The frequency of the switching pulses is controlled completely by the Vc voltage slowly increasing to the lower threshold voltage limit, then sharply decreasing in response to the current pulse, and then slowly increasing back to the lower threshold voltage. Arbitrarily low pulse frequencies can be achieved when the converter is operating in this regime. A decaying threshold voltage is implemented rather than a constant threshold voltage, so that after one pulse the difference between the Vc and the threshold voltages is large to prevent extra pulses from being accidentally triggered.

The burst mode logic circuitry needs to be both fast and low current, so will be realized using MOS devices. Multiple stages will be used to get sufficient gain. The circuit uses minimum sized devices and no compensation capacitors to maximize speed. The gain of the amplifier is $g_m R_o$ and the major pole is $\frac{1}{2\pi C R_o}$, where C is the parasitic capacitance on the output node. The crossover frequency is thus equal to $\frac{g_m}{2\pi C}$. The output node has three drain-to-body capacitances and two gate-to-source capacitances. This values along with the transconductance of the input devices operating at 50nA each, yields a crossover frequency of 3.3MHz. In simulation the amplifier has a crossover frequency of about 2.4MHz with 60 degrees of phase margin. The simulation bandwidth is smaller than the hand calculated version due to the crossover frequency being near the f_T of the transistors.

5.1.5 Regulator Buffer

The micropower circuitry operates with only a few micro-amps total, while the non-micropower circuitry operates with hundreds to thousands of micro-amps. Furthermore, the micropower circuitry always stays on, while the non-micropower circuity turns on and off when the part transitions between burst mode operation and full frequency operation. Due the different needs between these two sets of circuitry, each is operated from separate internal voltage rails. This way, as the load on the non-micropower rail changes from a few milli-amps to zero current, the fluctuations will not affect the sensitive micropower rail. This is particularly critical because jitter on the micropower rail will directly couple into the bandgap reference. A buffer is designed to accomplish the task of isolating these two internal supply rails.

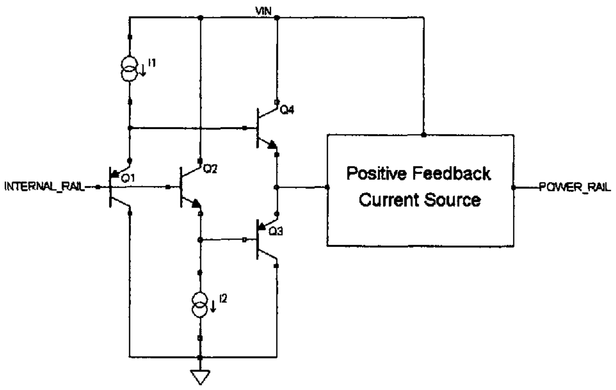


Figure 5-7: Block diagram of buffer between micropower and power internal rails.

The basic setup of the buffer is shown in Fig. 5-7. A positive feedback current source is used to source the wide range of current needed by the power rail, which can require anywhere from 2mA to zero current. When the power rail load changes between its load extremes, the positive feedback circuit input can source or sink about $2.2\mu A$. Even this amount of current would disturb the micropower rail, which is supplying a current of only a few micro-amps. Therefore, two additional buffering stages are established. A push-pull buffer (Q3 and Q4) sources or sinks as much current as needed by the positive feedback stage. The push-pull stage is preceded by Q1 and Q2, which properly level shift the signal so that both the micropower and power rails have the same DC value and the same tempco. The current sources which supply Q1 and Q2 run about 65nA of current, which is more than twice the maximum base current needed by both Q3 and Q4. With collector current of less than 65nA, the base currents of Q1 and Q2 should be less than a nano-amp. Therefore, the buffer will keep the switching of the high power internal rail from having anything but the most minimal effect on the micropower rail.

5.1.6 Startup Circuit

When the part first powers on, a fairly accurate current needs to be generated to start biasing all the rest of the circuitry. This current needs to be small to keep the quiescent current low. It would also be preferable to keep the current independent of input voltage, especially since the acceptable input voltage can range from several volts up to about forty volts. A JFET can be used for voltage blocking, but that buffered voltage can still range up to a maximum of 10 to 12 volts. A resistor would have to be about $100M\Omega$ to run 100nA from 10V into a node near ground. This resistor is excessively large and its current would be very dependent on the input voltage.

A self-bias circuit, such as one of those shown in Fig. 5-8, is a good way to generate an accurate current with less supply dependence. The circuits create a desired current by placing a V_{be} or ΔV_{be} across a resistor. This current is mirrored to keep the current in both legs the same. The problem with these circuits is they have two steady states, a state where both legs are operating at the desired current and a state where both legs of the circuit are running zero current. Therefore, these circuits need a startup circuit to ensure that they do not get stuck in the zero state. If even a small amount of current is drawn from one of the legs, the self bias loop will force the currents to the desired levels.

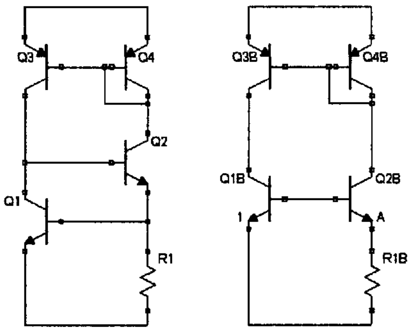

Q3
Q4
Q2
Q1
R1
Q3B
Q4B
Q1B
Q2B
1
A
R1B

Figure 5-8: Two self biasing circuits

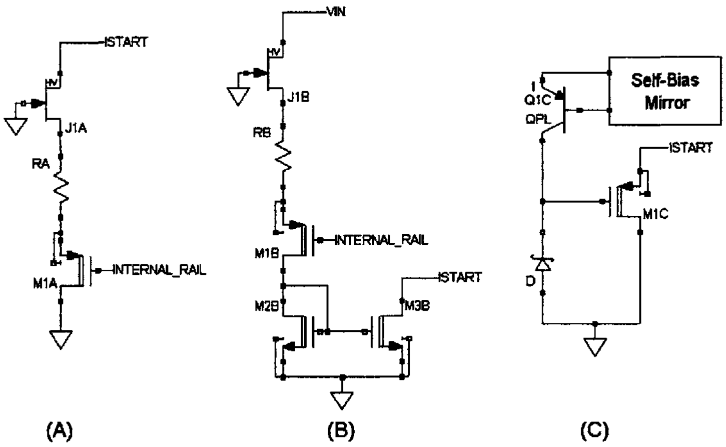

ISTART
HV
J1A
RA
INTERNAL_RAIL
M1A
VIN
HV
J1B
RB
INTERNAL_RAIL
M1B
ISTART
M2B
M3B
1
Q1C
QPL
Self-Bias Mirror
ISTART
M1C
D
(A)
(B)
(C)

Figure 5-9: Example startup circuits. Istart connects to the self-bias circuit and draws current to prevent the zero current state.

Several circuits were tried as startup circuits. The first two (Fig. 5-9 A and B) depend on a rising node to try and turn off the startup circuit after the part starts running. The internal rail starts at zero and rises to its final value of about 3V. If the internal rail was high enough and the JFET pinch was low enough, then the resistor between them could be turned off after the circuit started up. However, this is not the case in these circuits and so the resistor would have to run DC current even after startup. Either the resistor or the DC current is large in these cases. The DC current through the resistor is wasted in these circuits because it flows straight to ground. Another idea (not shown) was to build a ring oscillator, which would turn on a transistor to provide startup current and then the oscillator would be turned off once an internal node reached its non-zero voltage. This system was deemed unreliable, overly complex, and would take up comparable die space to a large resistor.

Another startup idea was to rely on leakage currents for startup (Fig. 5-9 C). In this circuit a leaky Shottky diode is used to ensure that when no current is running, the PMOS gate is low. This causes the PMOS to run a startup current and once the self bias circuit is running, the PMOS will be turned off by the PNP mirror from the self-bias circuit. This circuit runs no DC current after startup and its only downside is that it would be hard to test to make sure it works.

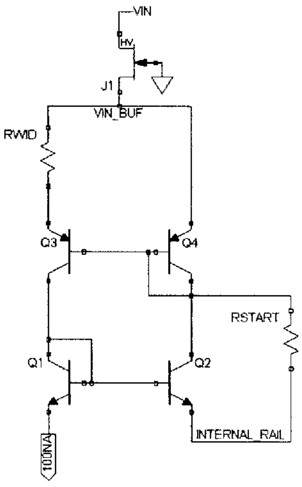


Figure 5-10: Final startup circuit which provides current to the micropower circuitry.

The circuit which was used as the startup circuit works based on a load defined current. The current through Q2 and Q4 is determined by the current load on the internal rail. This current load is independent of the regulator load and the input voltage, but will change over temperature. The current in Q1 and Q3 is about ten times smaller than that in Q2 and Q4 as dictated by the Widlar current mirror of Q3 and Q4. It is important to notice that no quiescent current is wasted with this scheme. Furthermore, the minimum input voltage is only a v_{be} plus a saturation voltage greater than the rail. This yields a minimum input voltage of about 3.7V at room temperature.

A resistor between Q4 and the internal rail is used for startup. The resistor current is used by the micropower circuitry, so the resistor current can be larger than when we first considered a resistor for startup. If the input voltage is 10V and the internal rail is about 3V, then a $30M\Omega$ resistor can be used to run about 210nA. This resistor is still large, but about a third the size of the one previously considered and there was sufficient die space in which to include it.

As the input voltage changes, the startup resistor current decreases from 210nA to only a few nA. As the resistor current falls, transistor Q2 will compensate by running more current. However, the current in Q4 changes by one-sixth the value the resistor current changes. Therefore, by increasing the resistor value, one can minimize the current change in Q4, and thus in Q3, over supply voltage. There was enough die space to increase the resistor to $60M\Omega$. With this resistor value, the current in Q4 changes about 1.3% over supply voltage at all temperatures and the current in Q3 changes about 4% over supply at cold and 2.7% over supply at hot. If the startup resistor were half the size, the change is Q4 current would double to 2.5% over supply, while the Q3 current percentage change across supply would not change.

5.1.7 Shutdown Circuit

The shutdown circuit is used to turn off the part when the shutdown pin is pulled low. During normal operation the shutdown pin is held high, typically by connecting it to the input voltage. The important parameters of the shutdown circuit are how much current the part consumes when in shutdown, how much current the shutdown circuit consumes when the part is on, what the voltage thresholds are between shutdown and normal operation, and the accuracy in those threshold voltages.

The shutdown circuit designed for this project can have several unique features. Normally the current consumed by the part when in shutdown is less than 1μA. The bandgap reference in this project only consumes about 350nA when each leg is running 100nA. Therefore, the bandgap can be left running even during shutdown. When the part starts back up, regulation can begin immediately without waiting for the bandgap capacitors to charge back up. More importantly, however, is that the bandgap voltage can be used in an accurate shutdown comparator. This is not normally possible because during shutdown there are no accurate voltages available.

A block diagram of the shutdown circuit is shown in Fig. 5-11. A comparator is used to compare the shutdown voltage to an accurate voltage from the bandgap reference. The part will shutdown when the SHDN pin is below 1V. This threshold was selected so that the circuit will work well with any type of logic which may be used to control the SHDN pin. This input to the comparator is connected to MOS gates and thus not able to withstand

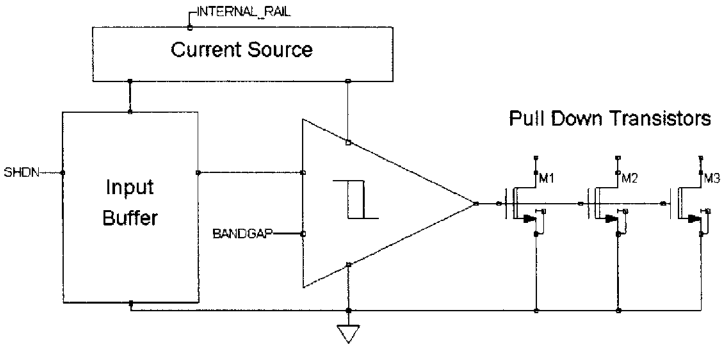


Figure 5-11: Block diagram for shutdown circuit

large input voltages, which may occur when the shutdown pin is connected to V_{in}. Therefore, an input buffer is required to allow the shutdown pin to be rated to 80V.

The functionality of the shutdown circuit will not be in use most of the time. Therefore, it would be preferable for the shutdown circuit to run zero current when the shutdown pin is held high, to eliminate any contribution to the quiescent current when not being used. This goal was achieved by designing the circuit such that the PMOS current sources to the buffer and comparator stages are cut off when the shutdown pin is sufficiently high. When the shutdown pin is above 2.6V, the current sources will be off and the entire circuit will consume zero power. When the shutdown pin is below 2.6V, the current sources will come out of cutoff and will each run 100nA. Therefore, the entire shutdown circuit consumes at maximum 200nA, only when the shutdown voltages are sufficiently low that the shutdown functionality will be used.

5.1.8 Current Limit

A current limit is used to turn off the switch when the switch current has ramped to a desired maximum value. The current limit changes based on the output load and controls the duty cycle of switching during full frequency operation. The current limit is increased as Vc is increased. Therefore, when the output voltage sags, the Vc and the current limit increase to source more current to the output. Likewise, the current limit decreases when the output voltage is too large. The output voltage and current limit could change to reach a stable duty cycle or in reaction to a load transient.

When the part is in PFM or burst mode operation the current limit needs to stay constant. Therefore, the current limit is disconnected and defaults to its minimum value during these modes. On the other end of the spectrum, the maximum current limit is set to about 2.7A. The maximum current limit is set to ensure the protection of the switch from power levels greater than it can handle and to prevent the part from entering an unstable operating regime. The current limit is clamped by placing a clamp on the upper limit of the Vc node. The effective Vc to current limit transconductance changes across temperature. Therefore, the Vc clamp compensates for these temperature effects by clamping the Vc node to a smaller voltage at cold and a larger voltage at hot.

5.1.9 High Power Interfacing

Besides the buffer between the micropower and non-micropower rails, there is additional interfacing between micropower and higher power circuitry. The most important of these is the buffering of intermediate voltages. Several voltages less than the bandgap voltage are needed as references in non-micropower circuitry. These voltages are connected to the bases of bipolar transistors, which can source or sink several hundred nano-amps. When the circuitry connected to the bandgap operates with only 100nA per leg, these base currents are enough to overwhelm the circuits generating the intermediate voltages. Therefore, buffers are required to isolate the high power and micropower circuits.

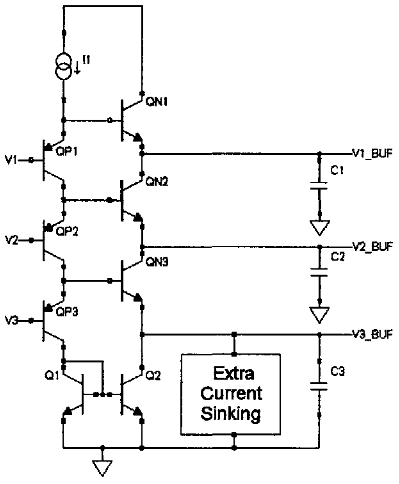


Figure 5-12: Block diagram for buffering intermediate voltage references from high power circuit base currents.

The intermediate voltages are buffered as shown in Fig. 5-12. The voltages need to be level shifted up and then shifted down so that they have a flat temperature coefficient, like the bandgap voltage used to generate them. To be current efficient, all the buffers are stacked, so only two legs of current are used. To sink several hundred nano-amps of current, the current in each of the buffer legs has to be at least several hundred nano-amps. However, the buffer only has to sink that much current when the non-micropower circuitry is powered on. Therefore, a small circuit is used to sink extra current only when the non-micropower circuitry is operating. This allows the buffers to function with only 100nA of bias current in each leg. Large capacitors are used to steady the buffered voltages as switching the non-micropower circuity on and off can cause them to fluctuate.

5.1.10 Internal Options

During no load situations, the advantages of the low quiescent current of this part are maximized. When there is no load current, the only dominant discharge path for the output capacitor is through the feedback resistors. If feedback resistors of tens or hundreds of kΩs are used, tens to hundreds of micro-amps can be drawn from the output capacitor. By maximizing the size of the feedback resistors, the time between switching pulses is maximized, which minimizes the supply current consumed in no load situations.

However, there are limits to the practical size of resistors which can be used on printed circuit boards. Therefore, including large feedback resistors on-chip is beneficial because it enables and ensures the use of properly sized resistors. There was room on the chip to include a total of $27.2M\Omega$ of resistance to be used as feedback resistors for a 3.3V output application. The inclusion of internal feedback resistors simplifies the application of the part by further reducing the number of external components (the part is already simplified by being internally compensated). The problem with internal feedback resistors is that the output voltage of the part cannot be adjusted. However, such an option still might be desirable to some users.

Another internal option which can be included is a phase lead capacitor. A phase lead capacitor is connected between the output and the feedback pin. This capacitor can be added externally, except when internal feedback resistors are used. Therefore, this internal option is a necessary compliment to the internal feedback resistors. The phase lead capacitor increases the crossover frequency of the converter as described in Chapter 4. By boosting the gain of higher frequency signals, the converter is able to better respond to load transients.

5.2 Layout

There are many real world effects not all of which can be included in SPICE simulations. Potential problems may arise if care is not taken in the layout of analog circuitry. Some of these effects include thermal gradients, current injection between devices, matching, and process variation. In switching regulators there are nodes which are rapidly changing, thus coupling between switching and sensitive nodes is a potential issue. This is especially a concern with the low current circuits designed in this project.

5.2.1 Bandgap Layout

The bandgap is the most sensitive part of the circuit because it is the accurate voltage reference for the entire IC. The components in both legs of the bandgap need to match as well as possible, this means that the NPN transistors need to have a layout that is identical in every way except that one device will have many more emitters than the other. The matching is shown in the bandgap layout in Fig. 5-13. Since the devices will have the same maximum dimensions, both devices will have the same collector leakage, which as shown previously in Section 5.1.1, is critical to good temperature performance.

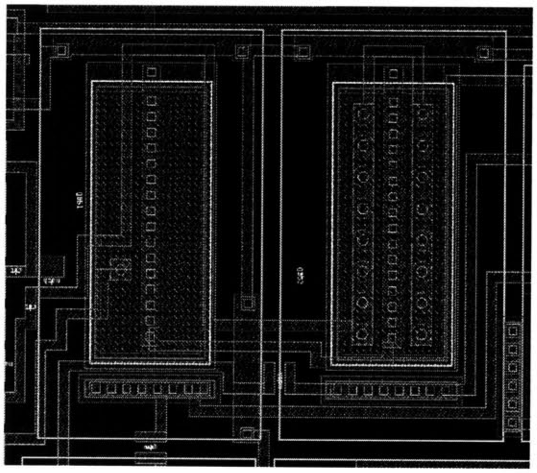


Figure 5-13: Layout of the two bandgap NPN transistors. Their layout is identical except for the number of emitters.

An active leakage compensation option will be included in the layout. It consists of a single PNP with a three-way split collector. One collector is connected to its own base and the other two collectors are connected to each of the two legs of the bandgap circuit. When the PNP base leaks current to the substrate at high temperatures, it will be mirrored to the other collectors. Essentially, the leakage current is being measured by the diode connected collector and then added back into the bandgap legs. This active leakage compensation option should not be necessary because the mismatch in the bandgap should only be a function of the leakage difference between the two legs, not the absolute leakage in the legs. However, the option to incorporate active leakage compensation will be made available in case it is needed.

The standard layout conventions of not placing sensitively matched circuits near edges or corners of the die, or near power devices, will apply to the bandgap more than any other circuit element in this project[6]. The other positioning problem is where to place the single emitter within a device layout sized for many more emitters. The single emitter is placed such that the thermal gradient from the power switch will not cause thermal mismatch between the two NPNs. Therefore, we imagine that there is a radial thermal gradient emanating from the center of the power switch and place the single emitter such that a line of constant temperature will pass through the center of the single emitter and the centroid of the emitters in the other NPN. In Fig. 5-13, the switch it to the upper left, so the single emitter is placed slightly below center. Although it is impossible to perfectly predict how to best layout the bandgap circuitry, by considering all the potential layout issues we can at least minimize the influence of the mismatch sources.

5.2.2 Coupling Effects

A switching regulator has nodes that are switching very quickly with high powers over large voltage ranges. This makes the coupling of electric and magnetic fields through parasitic capacitance and inductance a potentially significant problem. Circuits operating with low currents will be overwhelmed by even small amounts of inductively coupled current or suffer voltage fluctuations by being unable to adequately charge parasitic capacitance. These effects will have to be managed by properly considering them during layout.

One strategy is to identify sensitive nodes and minimize their size to reduce the effects of coupling. The internal Vc node is a perfect example of a node which needs to be as small as possible. Not only is the accuracy of the Vc node essential because it is the voltage controlling the regulator feedback loop, but it is also a very large impedance node as a result of the low current consumption error amplifier having a large voltage gain. The devices connected to this node were brought as close as possible to each other, as seen in Fig. 5-14, so that this trace could be made small.

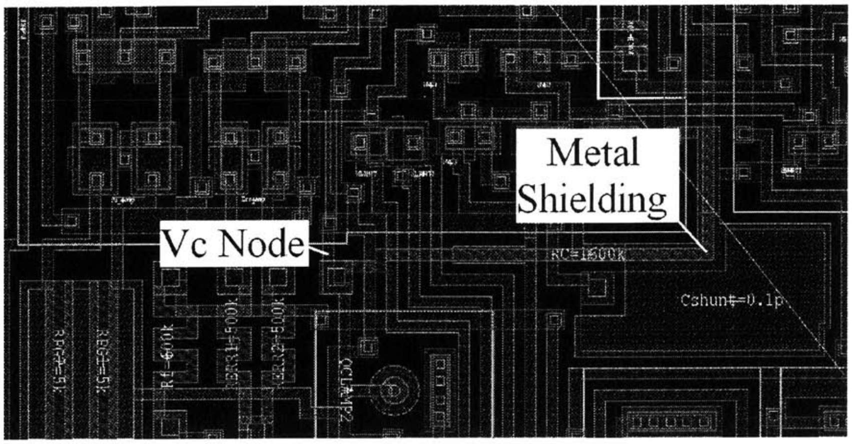


Figure 5-14: Layout showing the size of V_C node. Notice that QCLAMP2 and the series compensation resistor are placed close to the MOS to limit the node size. The picture also shows the metal shielding of the compensation resistor.

Sometimes it is impossible to make certain nodes physically small. For example, sensitive circuits connected to large bond or trim pads can be susceptible to parasitic coupling. However, when these signal are DC or slowly changing as in the case of the feedback and bandgap voltages, these nodes can be low pass filtered to prevent unwanted interference from higher frequency switching nodes.

As one would imagine, some circuits cannot be low pass filtered because their operation would be changed drastically. In these cases it is sometimes possible to shield the circuits. The main place this is used is for large resistors, which could end up acting like large antennas. By covering the thin film with a grounded metal layer, they are at least somewhat protected from coupling effects. The series compensation resistor is shielded in this way as illustrated in Fig. 5-14.

5.2.3 Matching

Matching is always something to consider during analog circuit layout. The most important areas where matching will be important, outside of the bandgap circuit, is in the current mirrors and error amplifier input pair. It was convenient to select PMOS for both these areas, which exhibit better matching than NMOS devices. In this process, a 10μm by 10μm

NMOS device will have about 3mV of V_T mismatch and a PMOS of the same dimensions will exhibit 1mV of V_T mismatch. The V_T mismatch of a MOS device is inversely proportional to the square root of its area $(\frac{1}{\sqrt{WL}})$[22]. Therefore, smaller devices will have more mismatch than larger devices.

When considering mismatch between the error amplifier input pair, even devices of minimum size will only have 3mV to 4mV of V_T mismatch. This will be slightly smaller than the bandgap voltage variance that might be expected from die to die. Plus, since the bandgap voltage is trimmed by measuring the voltage on the feedback pin, any mismatch in the error amplifier will be trimmed out. Therefore, the mismatch of the error amplifier input pair is not expected to be a significant issue.

The mismatch in the current mirror is another story. In this case, we are concerned with the matching of the drain current being mirrored, rather than the V_T mismatch directly. A detailed derivation of the equations showing the relation between the device mismatch sources and the mirror output current is included in Appendix B. The resulting equations from that analysis will be discussed in this section.

The equation for the current mismatch of two MOS devices (Eqn. 5.11) is minimized when the gate is driven as far above the threshold voltage as possible[22]. V_{OD} is the over drive voltage, which is $V_{GS} - V_T$, ΔV_T is the threshold voltage mismatch, $\frac{\Delta\beta}{\beta}$ is the percent mismatch in the device transconductance, and $\frac{\Delta I_{OUT}}{I_{OUT}}$ is the percent difference in the mirrored output current as a result of mismatch factors.

$$\frac{\Delta I_{OUT}}{I_{OUT}} = \sqrt{4\left(\frac{\Delta V_T}{V_{OD}}\right)^2 + \left(\frac{\Delta\beta}{\beta}\right)^2} \tag{5.11}$$

The equation for the percent change in mirrored current when the devices are in subthreshold (Eqn. 5.12) in unaffected by biasing.

$$\frac{\Delta I_{OUT}}{I_{OUT}} = \sqrt{\left(\frac{\Delta V_T}{nV_{th}}\right)^2 + \left(\frac{\Delta\beta}{\beta}\right)^2} \tag{5.12}$$

We can improve the accuracy of the current mirror by employing source degeneration (Eqn. 5.13). Although degeneration is typically only a bipolar technique, it is helpful when the MOS devices are in subthreshold because their drain current is an exponential function of gate bias as is the case with bipolar devices.

$$\frac{\Delta I_{OUT}}{I_{OUT}} = \frac{nV_{th}}{nV_{th} + I_{IN}R}\sqrt{\left(\frac{\Delta V_T}{nV_{th}}\right)^2 + \left(\frac{\Delta\beta}{\beta}\right)^2} \tag{5.13}$$

If we use 4μm by 4μm PMOS devices, they will have 2.5mV of V_T mismatch and 2% transconductance mismatch. This will result in 5.2% error in current mirroring when in subthreshold. If 100mV of source degeneration is used for devices of the same size, the current mirror error is 1.8%; almost three times as good. To get a current mirror error of that size without source degeneration, one would need PMOS devices about 11.5μm by 11.5μm. It is important to note that about 10% error in all the current mirrors would be perfectly acceptable, except for the device providing current for the error amplifer, which would preferably only have an error of about 3%.

Although it usually constitutes more space to use source degeneration rather than making the mos devices larger, there are additional advantages to using degeneration. One is that you gain some immunity to fluctuation in the voltage rail from which the PMOS mirror is sourcing current. One also has the ability to build in resistor options to be able to easily adjust the bias current in any of the mirrors, which is helpful when trying to analyze the low current performance of the circuits in this project.

About 100mV of source degeneration was used in this design because the extra space to do so existed. It is good to note that if space is not available and the size of the MOS devices needs to be increased, it is better to increase the length of the device rather than its width. This is because output resistance of the mirror is greater for larger gate lengths, which minimizes the effect of drain-to-source voltage on the mirror current. It also increases the gate-to-source voltage for a given drain current, which increases the signal to noise ratio in the case of noise on the supply rail.

5.3 Total Quiescent Current Consumption

Now that the design and layout of the project has been described, how far was the quiescent current consumption of the part able to be lowered? Based on simulation we expect that the total current consumption of the design when in sleep mode will be 60 times smaller than the LT3480 on which it is based.

The breakdown of the 98.48μA current consumption of the LT3480 is shown in Fig. 5-15. The breakdown of the 1.56μA current consumption of the thesis project part is shown in Fig. 5-16.

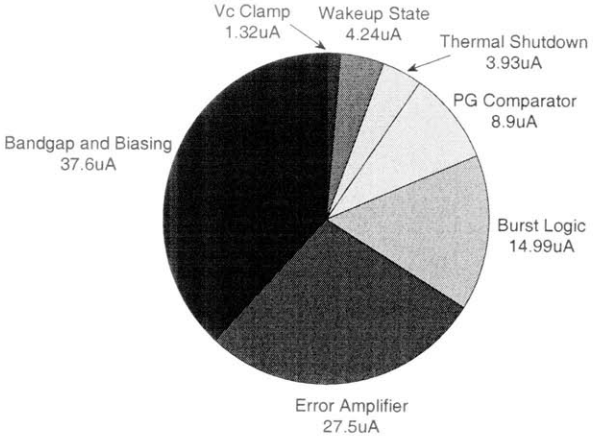


Figure 5-15: LT3480 quiescent current consumption. The total Iq is 98.48μA.

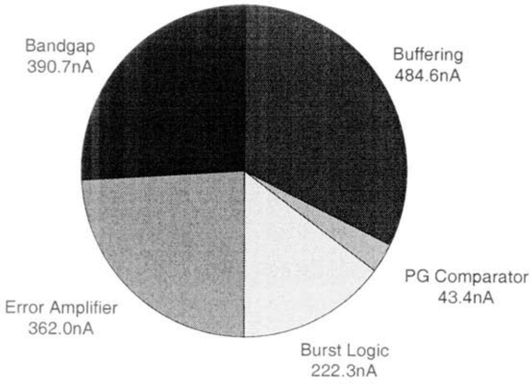


Figure 5-16: Thesis Project quiescent current consumption. The total Iq is 1.56μA.

Chapter 6

Measured Data

After completing design and layout, the project was fabricated so that proper operation and performance of the project could be assessed and verified. The first aspect to be examined was the quiescent current of the part, since that was the primary design focus of this project. However, it is important that the part be versatile, so a wide range of input voltages and output currents were examined, including performance across temperature. The other caveat to low current operation was the output ripple, which needs to measured. A brief discussion of double pulsing is included. Each individual system was compared to what was predicted by simulation, particularly the bandgap and error amplifier blocks. The overall system response was assessed in terms of transient and frequency response. Finally, the efficiency across the entire output load range is measured, which is very important since the job of the part is to efficiently convert power. The results of all these tests are included in this chapter to demonstrate how effectively the design described in this thesis achieved the desired specifications.

6.1 Test Setup

After the chips were fabricated, they needed to be packaged into parts for testing. The packaging process can take about a week to complete. Therefore, a probe insert was made so that the chips could be tested immediately by probing the wafer itself.

A picture of the probe insert is shown in Fig. 6-1. The small probes clustered in the center of the card are lowered on to a wafer and make contact with the exposed pads on each product die. The external components needed to build a complete switching regulator circuit are built right onto the probe card. The copper ring seen in the image is a ground ring, which enables external components to be soldered radially between the pins and ground.

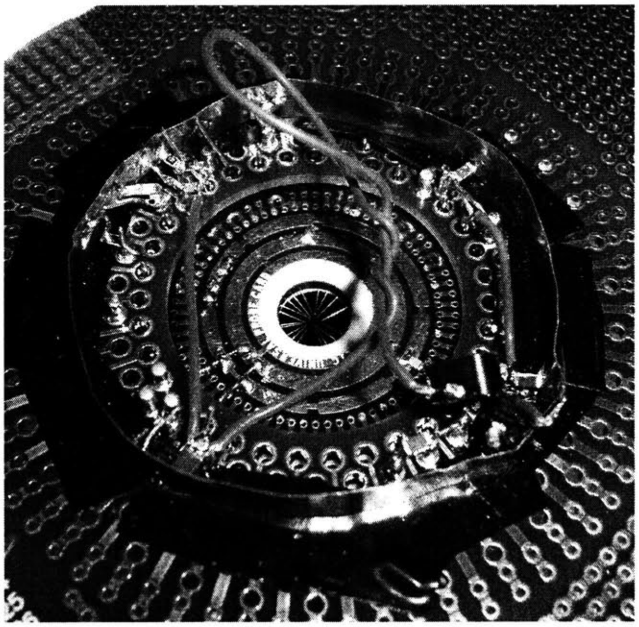


Figure 6-1: Picture of the probe insert used to directly probe die on a wafer. The switching regulator circuit is built onto the board so that chips can be tested while on wafer. The copper ring is a ground ring.

There are a number of internal nodes which needed to be accessed and several internal options with which to tinker. Hand probing can be difficult and parts can easily be damaged. Therefore, the probe card system was quite helpful, because if a part was damaged during testing, the probe card simply needed to be lifted and moved over to the next die. This greatly facilitated the early testing process.

The most significant disadvantage to the probe card insert is that the probes introduce parasitic inductance and resistance into the system. It is also easy for fast moving nodes, such as the switch node (SW), to couple to sensitive nodes, such as the feedback node (FB). The additional resistance in ground paths leads to susceptibility when the switch node is pulled below ground right after the switch turns off and the catch diode runs current. Despite these issues, the part was able to switch and properly regulate the output. However, the part had a major problem with multiple pulsing. The combined effects of switch coupling and poor grounding would cause the internal reference voltage to increase, which would keep the Vc node high, so that the part would switch 6 to 10 times before returning to sleep mode. As the load current was increased, this problem caused the output voltage to ratchet up resulting in output voltage ripple which could be greater than a volt!

Due to the multi-pulsing and ratcheting problems, the probe insert could not be used for large loads or measuring accurate switching data. However, the probe card was significantly valuable in gathering DC current and voltage data when the part was in sleep mode, and for measuring the characteristics of the error amplifier, both of which required a lot of internal probing.

The packaged parts were tested on normal copper boards, as shown in Fig. 6-2. The packages are open and the die unpassivated so that in this setup internal nodes may be accessed.

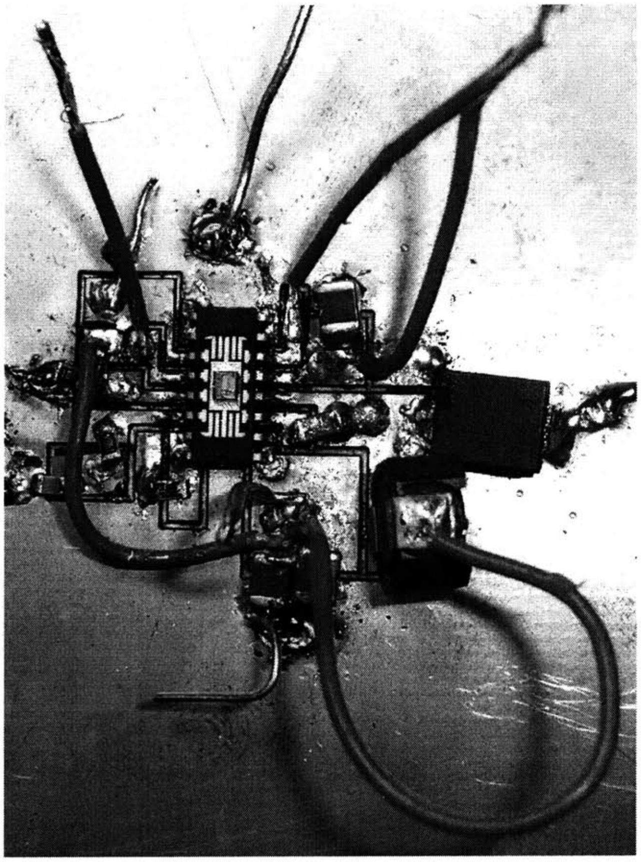


Figure 6-2: Picture of the board layout used for testing. The packaged die is open and unpassivated so that internal nodes can be probed and options can be accessed.

It was necessary to test the parts in open packages, but as a result the bond wires coming from the center of the die would sometimes drape on the edge of the die. This

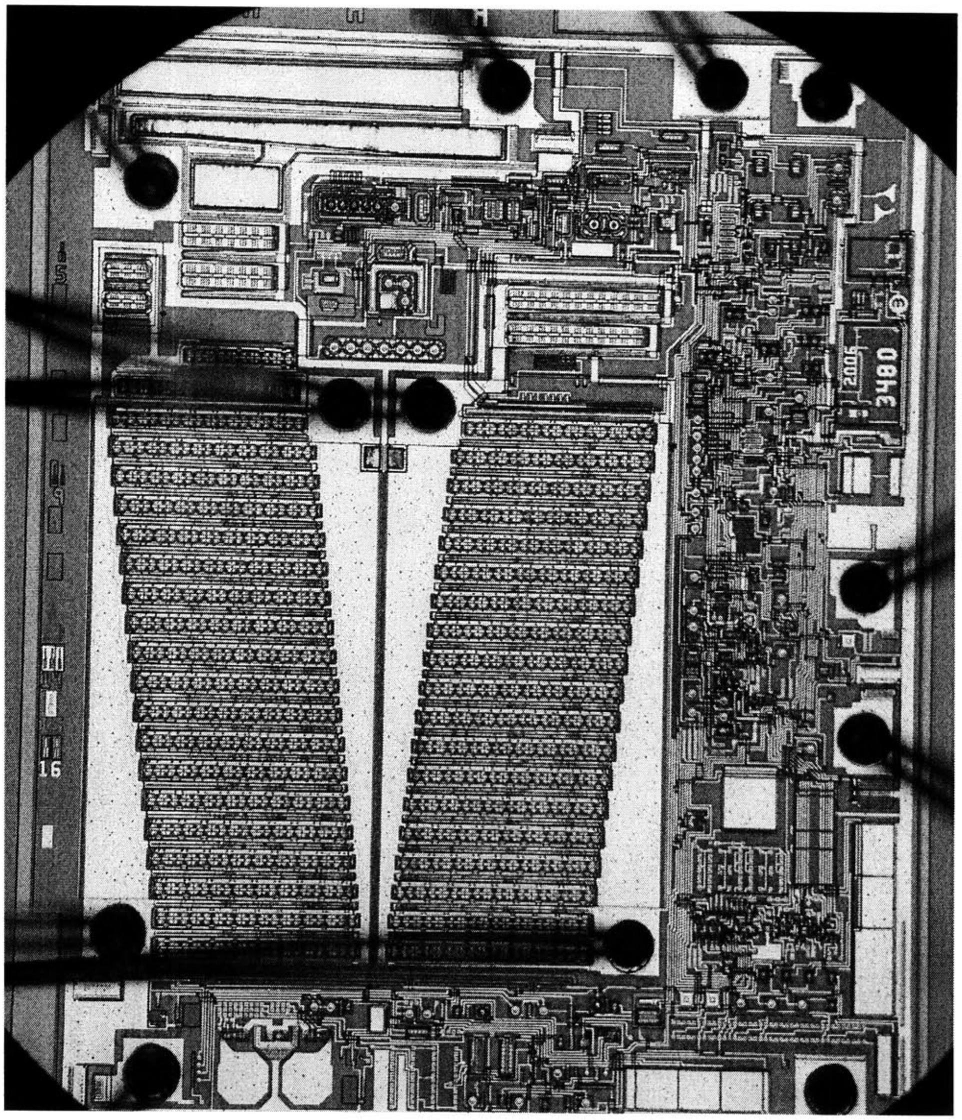


Figure 6-3: Picture of the fabricated part. A majority of the MOS devices can be seen in the clump of traces near the lower right corner of the die.

caused leakage current between the input node and switch node to ground, which would ruin the quiescent current measurement. Therefore, these bond wires would have to be manually lifted with probes. The die and the bond wires coming from central pads can be seen in Fig. 6-3.

6.2 Quiescent Current

Achieving a low quiescent current was the main goal of this project. In simulation, the quiescent current consumed by the part when in sleep mode was $1.5\mu A$ to $1.6\mu A$. By holding the feedback pin high to keep the part in sleep mode, the quiescent current was measured to be $1.4\mu A$ to $1.5\mu A$ depending on the test setup and measurement accuracy. The part was operating at such low current that light sources, such as microscope lights, bench lights, or skylights would affect the currents measured on the unpassivated die. Therefore, during all quiescent current measurements the die was shielded from light.

Current	Measured	Simulated
Error Amp	298nA	339nA
PG Comparator	47.2nA	47.8nA
Bias Buffer	94.8nA	96.7nA
Burst Logic	89.3nA	95nA
Vc Comparator	90.3nA	96.6nA
Vc Threshold	48.0nA	50.4nA
1x Bandgap Leg	95nA	98.7nA
16x Bandgap Leg	87nA	98.9nA
Total Iq	1.295uA	1.55uA

Table 6.1: Measurements of the current consumption of some of the main circuit blocks as compared to simulated values.

Measurements of the most important areas of current consumption were conducted with an HP meter with more than $10G\Omega$ of impedance and are recorded in Table 6.1. The measured values were a few percent less than the simulated predictions in some cases and up to about ten percent less in other cases, which corresponds to the difference between the simulated and measured total quiescent current. The primary reason for the measured values being smaller than the simulated values is due to differences in the simulated versus measured bandgap voltage. The bandgap voltage is used to establish a constant current, which is mirrored to the other major circuit blocks listed in the table. The bandgap voltage is difficult to simulate accurately due to the many factors which influence matching and temperature characteristics, which go into selection of the proper room temperature bandgap voltage. The simulated bandgap voltage was 1.26V, while the untrimmed bandgap voltage was measured to be 1.22V. This is a three to four percent difference, which would lead to similar differences in the mirrored currents.

Another potential source of error is that the drain of the current source being measured could have been imprecise. Care was taken to correctly bias the current sources during measurement, but the bias was established by using the simulated voltage values. The change in the output current of the current source for different bias voltages was found to be 10n-mho (10nA per V) for the error amplifier current source, 2n-mho for the current sources supplying slightly less than 100nA, and 1n-mho for the current sources supplying slightly less than 50nA. These values correspond to about two to three percent current variation per volt of bias.

The extent that the DC current values for the part during sleep mode matched simulated expectations was very satisfying. However, the value of the quiescent current during regulation will certainly be larger than that measured during sleep. The current pulses, even though they are infrequent, will increase the quiescent current because the part has to wakeup and operate with large supply current. The measured quiescent current during regulation is plotted versus input voltage in Fig. 6-4.

The quiescent current will increase the more often the part has to pulse during burst mode. This frequency is dependent on two factors, how much power is delivered to the output capacitor per pulse and how quickly the capacitor is drained between pulses. In a no load situation, the output capacitor primarily discharges due to the current through the feedback resistors and the catch diode reverse leakage.

In Fig. 6-4, the three curves represent different feedback resistors and catch diodes. The upper curve uses 270kΩ of total feedback resistance, while the middle and lower curves use 2.7MΩ and 27MΩ of total feedback resistance. This means that for the 3.3V output the feedback resistors draw 12.2μA, 1.22μA, and 0.122μA, respectively. It is important to note that all three setups use a SMC 3100 (3A, 100V) diode, which has lower leakage than smaller voltage diodes, as seen in Table 6.2.

Therefore, the total discharge current from the output capacitor will be 12.7μA, 1.72μA, and 0.622μA for the three plotted curves. When using mega-ohms of feedback resistance, a

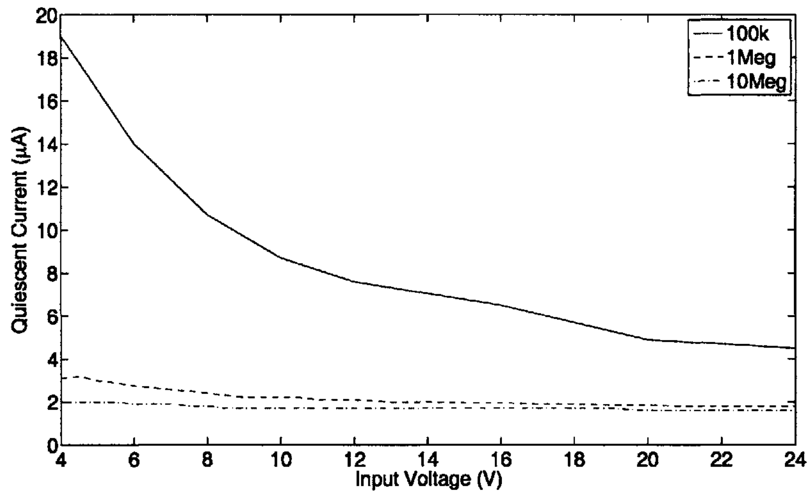


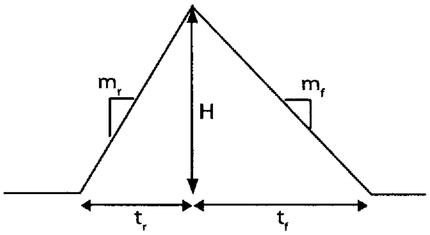
Figure 6-4: The quiescent current measured during switching for a range of input voltages. The feedback resistor divider remained in a ratio of 1:1.7, but for each curve the smaller resistor was either 100kΩ, 1MΩ, or 10MΩ. As shown, the quiescent current decreases for larger feedback resistor values.

Type	Max Current	Max Voltage	Leakage at 5V	Leakage at 10V
SMA 230	2A	30V	1.75uA	2.7uA
SMA 360	3A	60V	1.9uA	2.2uA
SMB 360	3A	60V	2.45uA	3.3uA
SMC 3100	3A	100V	0.5uA	0.6uA

Table 6.2: Reverse leakage currents for several different current and voltage diodes.

low leakage diode needs to be selected so that the current remains resistor limited, but for tens of mega-ohms of resistance the leakage is diode limited even with a low leakage diode. However, the tens of mega-ohm resistors are implemented on-chip due to the difficulties of using large external resistors, so it would be difficult to increase the feedback resistor sizes beyond tens of mega-ohms. Therefore, if the user chooses the largest reasonable external feedback resistors and a low leakage diode, the power performance of the part with no load is maximized. However, if care is not taken, then all the design work that went into making a low quiescent current part is wasted.

The second factor determining quiescent current during switching is the size of the current pulse. This effect is what causes the quiescent current to be larger for lower input voltages in Fig. 6-4. The current pulses are larger for higher input voltages, so more power is delivered to the output capacitor per pulse. The characteristics of the pulses for different input voltages is shown in Table 6.3.



Vin	H (mA)	t_r (ns)	t_f (ns)	$m_r \left(\frac{A}{\mu s}\right)$	$m_f \left(\frac{A}{\mu s}\right)$	Calc. m_r	Calc. m_f	Calc. H
6	175	312	204	0.56	-0.86	0.57	-0.83	175
8	218.8	228	260	0.96	-0.84	1	-0.83	212.69
10	250	188	296	1.33	-0.84	1.43	-0.83	247.66
12	275	164	328	1.68	-0.84	1.85	-0.83	280.46
16	331.2	136	392	2.44	-0.84	2.7	-0.83	352.14
20	381.2	112	452	3.4	-0.84	3.55	-0.83	443.64
24	425	108	500	3.94	-0.85	4.4	-0.83	493.88

Table 6.3: Characteristics of current pulses for different input voltages.

Each current pulse has a triangular shape, so can be described by the rise time, fall time, and height as labeled in the figure above Table 6.3. The rise time corresponds to the time when the switch is on, so the current is ramping up through the inductor at a rate equal to $\frac{V_{in}-V_{out}}{L}$. On the other hand, the fall time corresponds to when the switch is off and the current in the inductor is ramping down at a rate equal to $\frac{-0.6-V_{out}}{L}$. One can see from the table that the calculated and measured slopes are nearly equivalent.

However, the more important factor is why the height of the current pulses increases with input voltage. The peak current in the inductor is controlled by a current comparator, which compares the switch current measured through a sense resistor to a programmed current limit. During burst mode, the current pulse ramps to the minimum possible peak current, which is established by adding offset to the current comparator. However, the current comparator is not infinitely fast, so there is a fixed time, once the switch current reaches the limit set by the comparator offset, before the comparator output will toggle and turn off the switch. The faster the rising ramp rate of the current, the more the switch current will overshoot the minimum limit during the comparator delay time period. Therefore, since larger input voltages have faster rising current ramp rates, they will generate larger current pulses.

The last column in Table 6.3 shows the calculated height of the current pulse based on the comparator delay model. A rough calculation of the minimum current pulse was made by calculating the comparator offset and determining the corresponding switch current limit. The comparator offset is generated by a 1.1 to 1 emitter ratio between the input pair devices. Using the exponential equation for bipolar transistors, the emitter ratio leads to $V_{th}ln(1.1) = 2.48mV$ of offset at room temperature. The switch current sense resistor is a difficult quantity to measure. In simulation a 40mΩ sense resistor value was used. This gave a 3.32A peak current limit, while the actual current limit was found to be about 1.7A. This leads one to believe that the sense resistor is actually about 20.5mΩ. Therefore, a 2.48mV offset would be generated by 121mA as measured by the sense resistor. Using this current limit and fitting the comparator overshoot model to the measured data, the comparator delay was calculated to be about 94.5ns. This means the comparator has a bandwidth of about 10MHz.

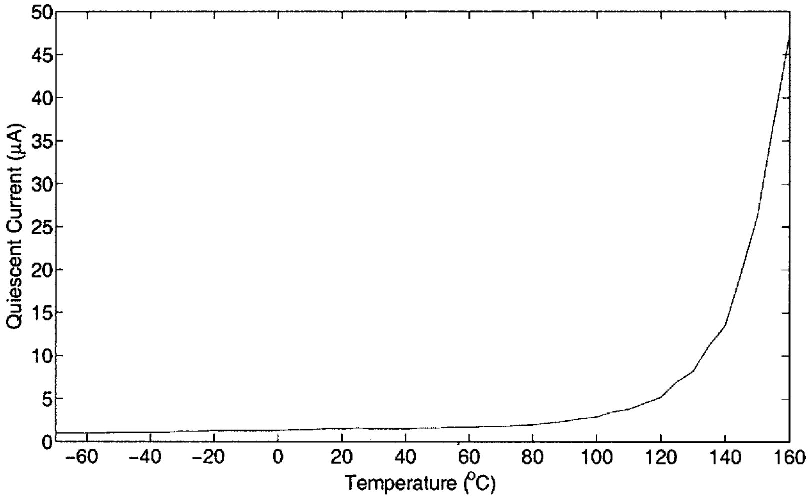


Figure 6-5: The quiescent current is shown to increase with temperature. The increase is exponential, which seems to indicate it is caused by diode leakage.

Another important aspect of the quiescent current is how it changes over temperature. The quiescent current should not have a temperature coefficient because a majority of the currents are established from the bandgap voltage, which should be flat across temperature. However, the quiescent current increases exponentially at high temperatures. This is the result of leakage currents as all the diodes to substrate in the circuit begin to have significant leakage. This quiescent current does not even double until above 100°C and remains below $10\mu A$ up to 130°C, so is not a factor for most applications.

6.3 Current Limit and Minimum Input Voltage

Not only must the part have excellent quiescent current at no load, but we also wanted the part to be able to provide an output current into the range of amps. The first measure of the output range is to look at the current limit of the converter.

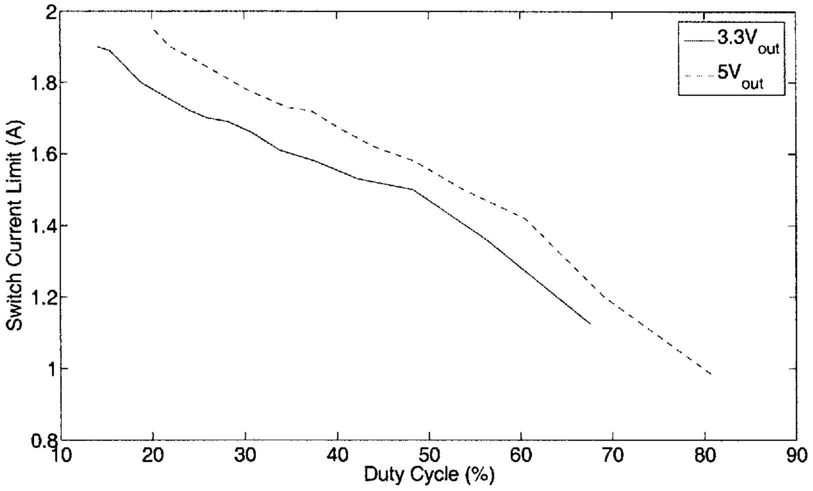


Figure 6-6: The current limit plotted against duty cycle for both 3.3V and 5V outputs.

The curve in Fig. 6-6 is a plot of the current limit versus duty cycle. The current limit decreases linearly with duty cycle. This is what one would expect because slope compensation is used to control the peak current. The use of slope compensation is necessary to achieve stability in a current mode controlled converter. Slope compensation causes the current threshold, which sets where the current comparator will trip, to decrease linearly over time. Therefore, a smaller duty cycle will trip higher up on that negative slope than a larger duty cycle, resulting in a larger measured value for the current limit at smaller duty cycles.

The current limit for an input voltage of 12V and an output voltage of 3.3V was found to be 1.7A. The simulated value is 3.32A, which leads one to believe that the sense resistor is actually $20.5m\Omega$, rather than the $40m\Omega$ used in simulation. This difference is reasonable because the sense resistor is a complex shape of metal incorporated into the power switch and its value is difficult to predict accurately. However, once the value is known, it should not change from die to die due to process variation.

The current limit is a measure of the peak switch current. Therefore, the maximum output current able to be sourced by the IC will be smaller than the current limit. The maximum output current is shown in Fig. 6-7 for a range of input voltages for both 3.3V and 5V outputs.

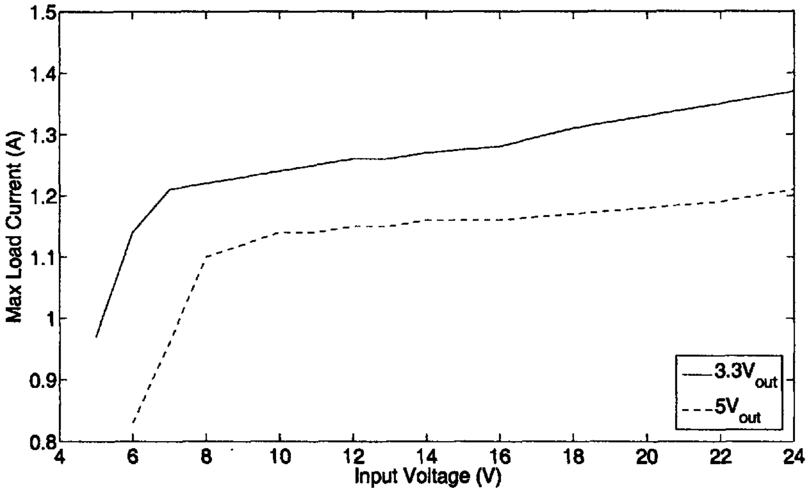


Figure 6-7: The maximum load current plotted against the input voltage while regulating a 3.3V or 5V output.

The maximum load is larger for increasing input voltages. This is simply because larger input voltages correspond to smaller duty cycles where the current limit will be larger. The maximum load is the average of the inductor current waveform. Therefore, if there is less inductor current ripple, the maximum load current will be closer to the value of the current limit. So for a given current limit, a user could increase the maximum output current by using a larger inductor to decrease the current ripple.

Another measure of the versatility of the regulator is the minimum allowable input voltage. The minimum input voltage of the part for 3.38V and 4.84V outputs is shown in Fig. 6-8. This graph shows two different factors which effect the minimum input voltage. The 3.38V output needs at least 800mV of additional voltage to supply a V_{be} plus a V_{sat} above the internal rail. When the output is well above the internal rail, the limiting factor on the output becomes the drive stage. The drive stage needs at least $2V_{sat}$s above the output,

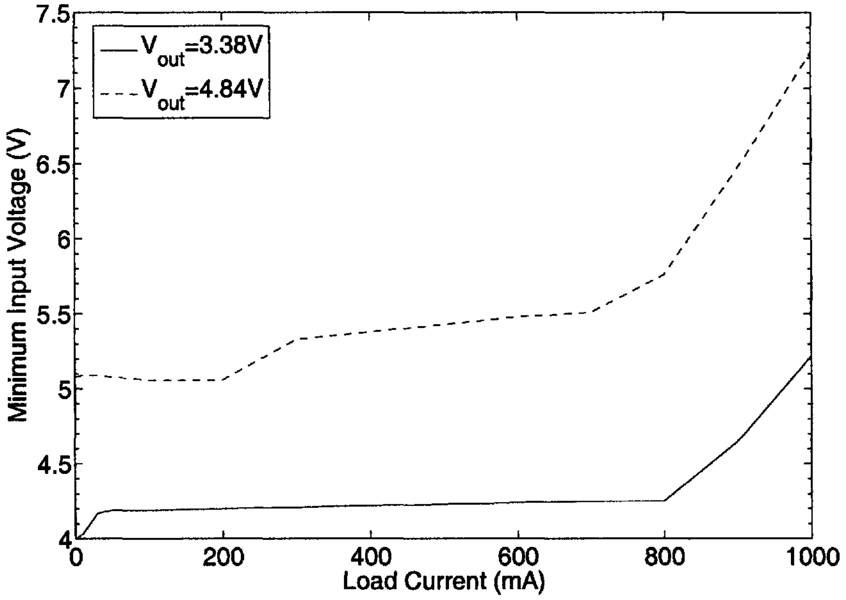


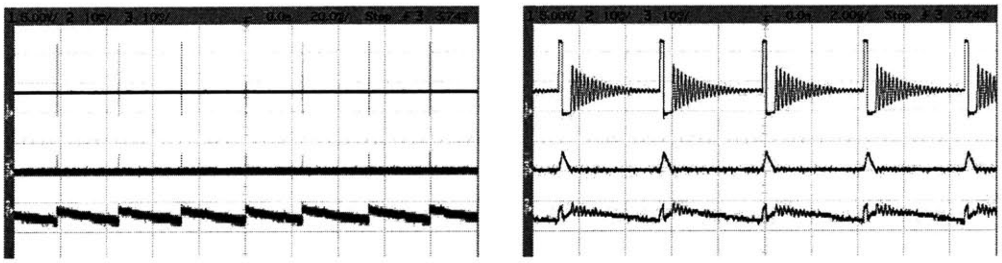
Figure 6-8: The minimum input voltage across load to maintain a regulated 3.38V or 4.84V output.

which is equivalent to the 200mV of difference between the input and output voltages for the minimum input voltage curve for the 4.84V output. At larger load currents the drain-to-source voltage of the switch increases leading to higher minimum input voltages.

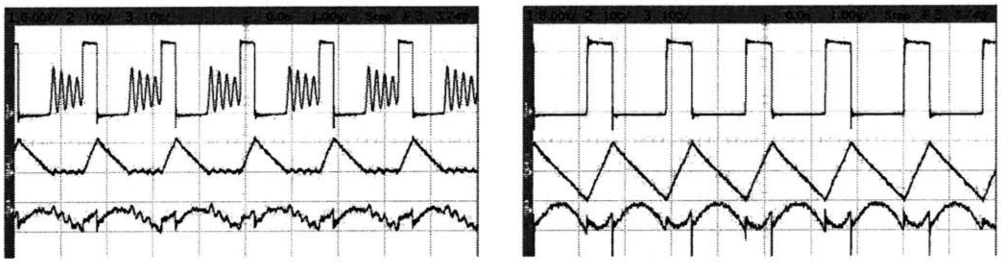
6.4 Low Output Ripple

The regulated output voltage needs to have low ripple. If the regulator is designed to have large current pulses, burst mode operation becomes more efficient, but the output ripple increases. Therefore, it is important to have limitations on the acceptable level of output ripple when designing a burst mode part. Usually one wants no more than 20mV to 30mV of ripple, however, the ultra-low quiescent current regulator designed here has less than 10mV of ripple for both burst mode and full frequency operation.

The four oscilloscope shots in Fig. 6-9 were taken at four different load current levels, all with a 22μF ceramic output capacitor. Each figure shows the voltage on the switch node as the top waveform, the current through the inductor as the middle waveform, and the voltage ripple on the output as the bottom waveform. The first setup (Fig. 6-9(a)) shows



(a) $I_{load} = 0$ (b) $I_{load} = 15\text{mA}$



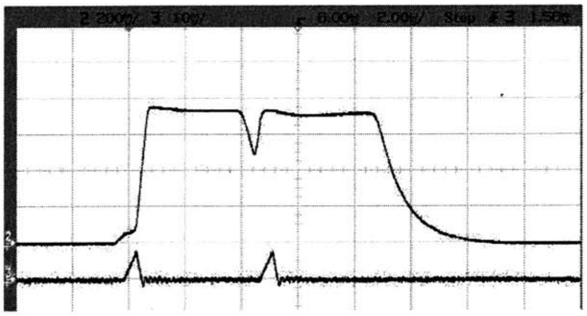
(c) $I_{load} = 150\text{mA}$ (d) $I_{load} = 1\text{A}$

Figure 6-9: Switch voltage (top trace), inductor current (middle trace), and output ripple (lower trace) for four different output loads. Even though the four oscilloscope shots show the converter operating in different modes, the output voltage ripple is always less than 10mV. The output capacitor was 22μF in all cases.

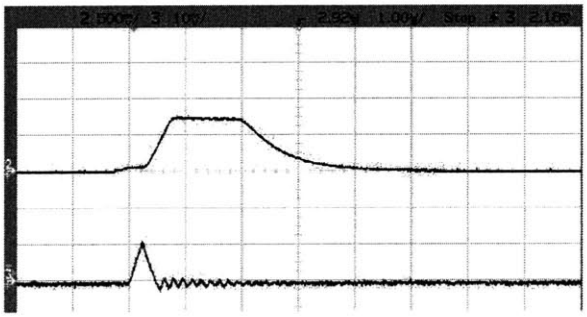
the converter operating with no load. The part bursts very infrequently with a frequency of about 37.5 Hz. The output ripple is shown as a sawtooth waveform as the output capacitor is quickly charged by a current pulse and then slowly discharges. The second setup (Fig. 6-9(b)) shows a 15mA load where the part is still operating in burst mode, but the pulse frequency has increased to about 225kHz. The output ripple still has a sawtooth waveform shape, but has some coupling from the switch waveform, which can clearly be seen. The coupling is a result of measuring the SW node and the output ripple simultaneously. The third setup (Fig. 6-9(c)) shows a 150mA load where the part is operating at full frequency of about 600kHz, but the inductor current is still discontinuous. The output ripple looks more sinusoidal, but still has significant switch coupling. The fourth setup (Fig. 6-9(d)) shows a 1A load where the part is operating at full frequency and the inductor current is continuous. The output ripple is clearly sinusoidal in this case. All four traces, regardless of the shape of the output ripple, demonstrate an output ripple of less than 10mV.

6.5 Double Pulsing

Very few problems were found with the initial silicon for this project. However, for input voltages less than 12V, the part double pulsed in burst mode instead of producing clean single pulses. This is not a significant problem in terms of stability or regulation, but increases the output ripple and effects the quiescent current performance. Therefore, this issue was worth investigation.



(a) Double pulsing with sleep timer set at about 4μs



(b) Single pulsing with sleep timer shortened to about 1.4μs

Figure 6-10: The voltage on the R_T pin (top trace) and the inductor current (lower trace) for a long sleep timer with double pulsing and a short sleep timer with single pulsing.

An example of the double pulsing behavior can be seen in the waveform shown in Fig. 6-10(a). The lower trace is the inductor current waveform, which shows two pulses in succession. The upper waveform is the voltage on the R_T pin. Probing the R_T pin can be instructive because the R_T pin will be high when the high power circuitry is powered on and it will be low when the high power circuitry is off. A resistor is placed on the R_T pin to set the value of a current source, which controls the oscillator. The oscillator is part of the high power circuitry which shuts off during burst mode. Therefore, probing the voltage on the R_T pin allows one to compare high power circuitry transitions to other waveforms.

One observes in Fig. 6-10(a) that the high power circuitry turns on with the current pulse and then turns off about 4μs later when the sleep timer expires. However, a second pulse occurs at about the same time the sleep timer expires. This leads one to believe that the double pulsing is caused by either the sleep timer expiring or the high power circuitry turning off.

It was found that when the high power circuitry turns off or turns on, there is a jitter in the control voltage at the output of the error amplifier. This is most likely a direct result of jitter on the internal voltage rail and the bandgap reference as a result of the high power rail transitioning. The comparator that indicates when the next pulse in burst mode should fire compares the control voltage to a decaying exponential. The decaying exponential reaches about 90% of its final value in about 4μs, which is the same period as the sleep timer. Therefore, the small jitter in the control voltage occures when the decaying exponential has nearly reached its final value, which can result in the comparator signaling a premature current pulse. To alleviate this problem, the sleep timer was shortened to about 1.4μs. This causes the jitter in the control voltage to occur while their is still plenty of margin in the comparator. Therefore, there is no risk of causing a premature current pulse as a result of turning off the high power circuitry. The shorter sleep timer and the resulting single pulse burst mode behavior is shown in Fig. 6-10(b).

6.6 Bandgap

The regulated output voltage is only as good as the internal bandgap reference. The bandgap reference circuitry must be examined to ensure it operates properly at low currents. The bandgap voltage was measured over temperature by sweeping the feedback pin voltage until a switch transition was observed. The state of the switch will toggle when the error amplifier output switches from high to low, or low to high, due to the feedback pin transitioning past the bandgap reference voltage. The values of the bandgap reference extracted in this manner are plotted versus temperature in Fig. 6-11 for a trimmed reference.

This bandgap circuit is operating with 100nA per leg. However, it exhibits less than 4mV of variation over the -55°C to 125°C temperature range; this is better than 0.33%. Furthermore, the bandgap voltage remains good for temperatures outside this range. We

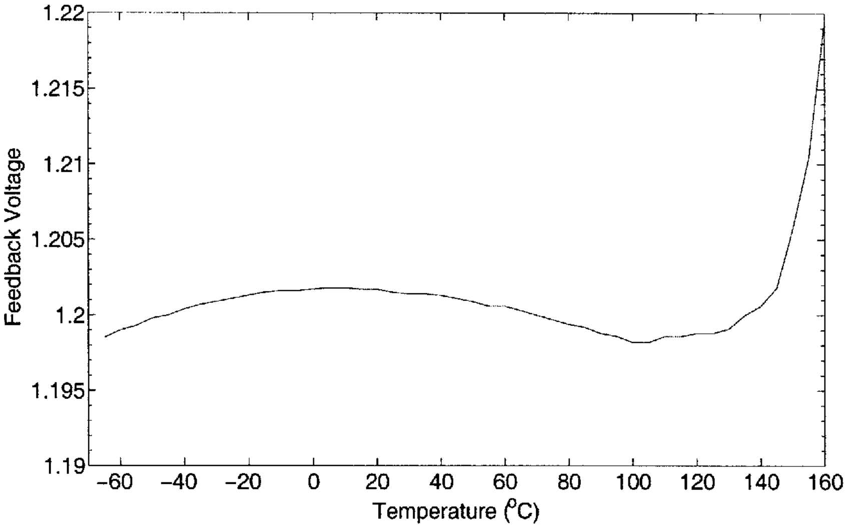


Figure 6-11: The feedback pin (or bandgap voltage) measured over temperature for a trimmed bandgap reference operating with 100nA per leg. For the temperature range typically specified for ICs (-55°C to 125°C) the voltage varies by less than 4mV.

observe that the reference noticably increases at temperatures of 160°C and higher. This phenomena is due to leakage imbalance, but is benificial because it compensates for the negative curvature in the temperature coefficient in the 100°C to 150°C temperature ranges, so enhances the bandgap performance. One also notices that the trimmed room temperature value of the bandgap voltage is just above 1.2V. This is smaller than expected based on hand calculations. However, due to the resistor tempco, the bandgap voltage is expected to be less than the typical value of around 1.22V. There are also differences observed in the reference voltage due to packaging and passivation stresses.

The bandgap voltage was also tested when the bandgap circuitry was operating with only 50nA per leg. The measurements for an untrimmed reference with 50nA per leg are plotted in Fig. 6-12. Even untrimmed, the reference voltage only varies about 1%. Based on the untrimmed data, if the reference were trimmed, one might expect about 4 to 5mV of variation, which is the same that was found when operating with 100nA per leg. These results are very promising and seem to indicate the leakage is not a problem at high temperatures and beta degradation is not a problem at low temperatures for the Brokaw topology used for this bandgap reference.

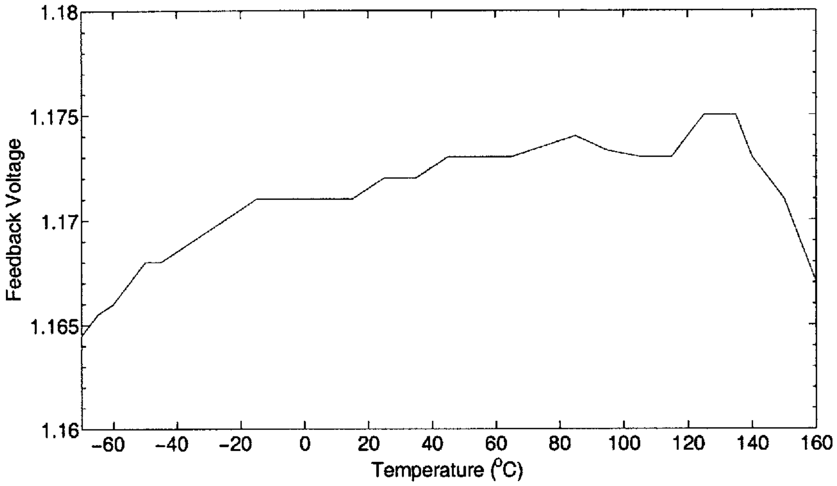


Figure 6-12: The feedback pin (or bandgap voltage) measured over temperature for an untrimmed bandgap reference operating with 50nA per leg. The reference continues to work properly at high and low temperatures, despite operating at low currents. These curve indicates that the reference voltage should vary by less than 5mV once trimmed.

6.7 Error Amplifier

The error amplifier is the other subcircuit, besides the bandgap reference, which necessitates specific scrutiny since its operation is directly coupled with frequency and load transient performance. The error amplifier characteristics were measured directly. Achieving such a measurement required probing of the internal error amplifier output node (V_C node). The output current of the error amplifier with the output node fixed at 1V was measured over a range of feedback pin voltages. A nice, smooth curve was found as seen in Fig. 6-13. This curve clearly demonstrates that the maximum current the error amplifier can source or sink when driving the output node is 300nA. This is much smaller than the 400nA of tail current desired for the error amplifier. This is acceptable, however, because the system will still be stable and operate well, but the error amplifier will have a smaller transconductance and slew rate than it would have with a larger bias current.

The output current curve can be differentiated to find the transconductance versus feedback voltage curve as plotted in Fig. 6-14. This curve shows that the g_m of the amplifier is only about 2.25μS at maximum. Given a 300nA tail current, hand calculations for transconductance using $g_m = \frac{I_D}{nV_{th}}$ for subthreshold, with I_D equal to 150nA, n set to 2, and the thermal voltage equal to 26mV at room temperature, one calculates a transconductance

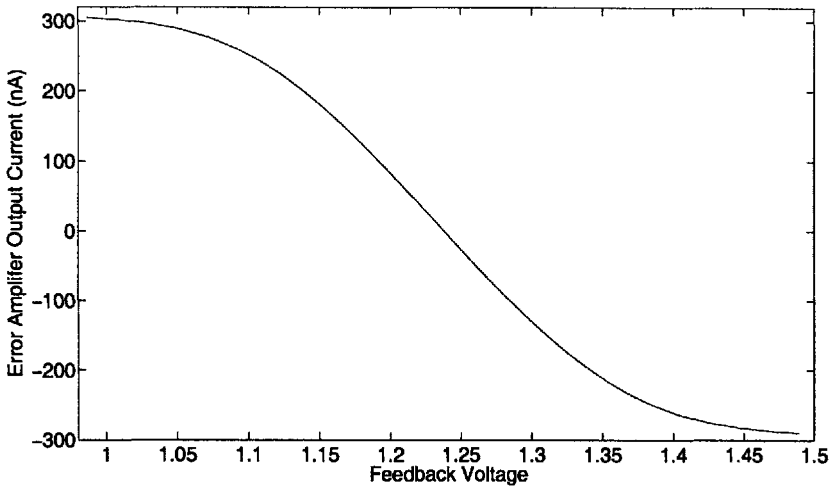


Figure 6-13: Measured error amplifier output current when Vc is fixed at 1V.

of 2.88μS. Therefore, the measured value is more than 20% less than the calculated value, even after taking into account the smaller error amplifier tail current. This difference seems to indicate that the MOS devices are not deeply enough in sub-threshold. Decreasing the current density of the input devices by increasing their widths will help the devices operate more ideally in the sub-threshold regime.

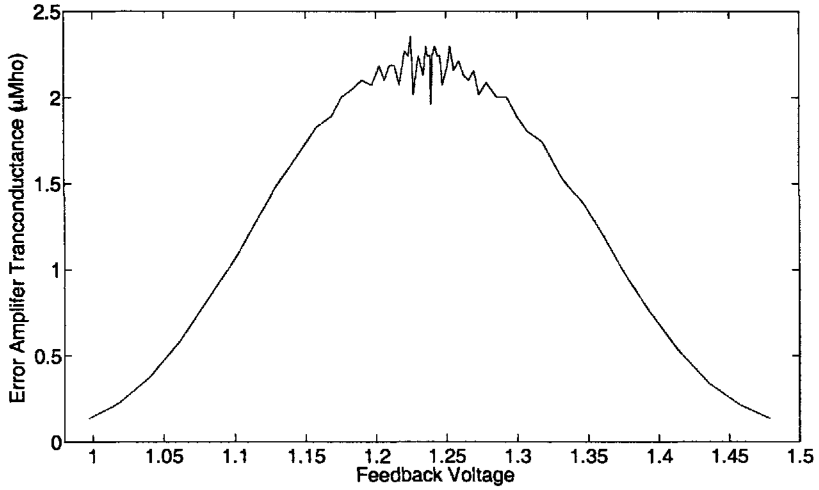


Figure 6-14: Measured transconductance of error amplifier.

The last important characteristic to measure is the voltage gain of the error amplifier.

This measurement was done by changing the regulator output voltage and observing the voltage change on the error amplifier output node. The output voltage of the regulator was changed, rather than the feedback pin voltage, because the input change has to be very small for the change in the error amplifier output node voltage to fit within its 2V range. One makes the input voltage to the feedback pins smaller by the feedback resistor divider ratio when driving the regulator output. A voltage gain of 364 was found for the error amplifier. This is smaller than the gain of 460 predicted by simulation, but is still quite acceptable.

6.8 Frequency and Transient Response

The control loop was analyzed in both the frequency and time domains. To measure the frequency response of the fabricated converter the closed loop was broken between the top of the feedback divider and the regulator output, and a measurement device was inserted, which would inject a small signal and measure the resulting output signal. In this way a magnitude and phase relationship could be plotted over frequency to generate a bode plot for the control loop. The crossover frequency and phase margin were measured for different compensation capacitor, compensation resistor, feedback resistor, phase lead capacitor, and output capacitor values. The transient response of many of these setups to a load step from 0.5A to 1A was measured. The peak overshoot in the output voltage, as well as the approximate time it took for the output voltage to settle back to its regulated value, is listed in Table. 6.4 along with the frequency response data.

There were three sets of compensation component sizes which were examined, a 6pF comp capacitor with a 2.4MΩ series resistor, a 6pF comp capacitor with a 3MΩ series resistor, and a 4pF comp capacitor with a 3MΩ series resistor. It was determined based on simulation that the 4pF comp cap with the 3MΩ resistor would be the best compensation setup, but the other setups were measured as a comparison. A smaller comp capacitor and larger comp resistor should both increase the crossover frequency because they increase the frequency of one of the poles and decrease the frequency of one of the zeros, respectively. This trend was seen experimentally, for example, the crossover frequency increased from 37.1kHz to 43.8kHz to 44.7kHz as the comp resistor value was increased from 2.4MΩ to 3MΩ and then the comp capacitor was decreased from 6pF to 4pF (these values are for the

C_C	R_C	R_{fb1}	R_{fb2}	C_{lead}	C_{out}	f_c	ϕ_M	Overshoot	t_{settle}
6p	2.4M	10k	17.4k	0	30μ	16.8k	54.4^o	-	-
6p	2.4M	10k	17.4k	0	20μ	21.8k	58.8^o	-	-
6p	2.4M	1M	1.7M	0	30μ	14.5k	46.8^o	100mV	40μs
6p	2.4M	1M	1.7M	0	20μ	18k	51.7^o	-	-
6p	2.4M	1M	1.7M	22p	30μ	31.7k	63.0^o	70mV	60μs
6p	2.4M	1M	1.7M	22p	20μ	45.8k	57.3^o	-	-
6p	2.4M	1M	1.7M	100p	30μ	37.1k	51.3^o	60mV	40μs
6p	2.4M	1M	1.7M	100p	20μ	51.9k	46.3^o	-	-
6p	2.4M	10M	17.2M	1p	30μ	16.0k	49.7^o	110mV	40μs
6p	2.4M	10M	17.2M	1p	20μ	22.2k	54.1^o	-	-
6p	3M	1M	1.7M	0	30μ	15.7k	50.2^o	100mV	40μs
6p	3M	1M	1.7M	0	20μ	19.3k	54.1^o	-	-
6p	3M	1M	1.7M	100p	30μ	43.8k	50.8^o	50mV	35μs
6p	3M	1M	1.7M	100p	20μ	62.3k	45.1^o	-	-
4p	3M	1M	1.7M	0	30μ	17.0k	43.0^o	90mV	35μs
4p	3M	1M	1.7M	0	20μ	21.0k	48.2^o	-	-
4p	3M	1M	1.7M	100p	30μ	44.7k	45.9^o	50mV	30μs
4p	3M	1M	1.7M	100p	20μ	62.1k	41.6^o	-	-

Table 6.4: Frequency and transient response characteristics for different compensation settings. The crossover frequency and phase margin were measured directly with a machine, while the peak overshoot and time to settle back to regulation for the load steps were recorded manually based on captured oscilloscope traces.

100pF phase lead capacitor with 30μF output capacitor case).

The phase of the control loop depends on where the crossover frequency falls relative to the phase bump created by the compensation resistor zero. For all the compensation component values tested, the frequency with the maximum phase margin seemed to be between 25kHz and 35kHz. The crossover frequencies without a phase lead capacitor were always below 25kHz and the crossover frequencies with a 100pF phase lead capacitor were always above 35kHz. Therefore, with neither the 0pF, nor the 100pF, phase lead capacitor was the region of maximum phase margin reached. This is why the 0pF phase lead capacitor cases had maximal phase margin with a smaller output capacitor because a smaller output capacitor increases the crossover frequency. On the other hand, the 100pF phase lead capacitor cases always had maximal phase margin with a larger output capacitor because a larger output capacitor decreases the crossover frequency. In either case, the converter had more phase margin near the frequency where the compensation zero yielded the most phase bump.

Based on the frequency and phase analysis alone, it seems that none of the compensation component choices which were explored really achieved the best results. However, we are more interested in the response of the converter to load transients because such a response is important when the voltage regulator is used in real systems. The frequency response yields good insight into the response of the converter to a load step, but is itself not of primary importance. When looking at the load step response, setups with a higher crossover frequencies performed better than those with smaller crossover frequencies. Furthermore, of the setups with high crossover frequencies, the ones with the smaller 4pF compensation capacitor performed best. This makes sense intuitively since fast systems can respond quickly to output load changes and a smaller compensation capacitor is easier for the error amplifier to drive.

This analysis shows that the best setup for this particular converter is a 4pF comp capacitor, a 3MΩ series resistor, and a 100pF phase lead capacitor. The step response of this setup with a 30μF output capacitor is shown in Fig. 6-15. The frequency response of this setup with a 30μF output capacitor is shown in Fig. 6-16.

Now one thinks about how the control loop could be further optimized for even better performance. The 50mV overshoot in the step response is quite nice. Furthermore, the inductor current responds in about 3 to 8 switching cycles, which is very fast. However,

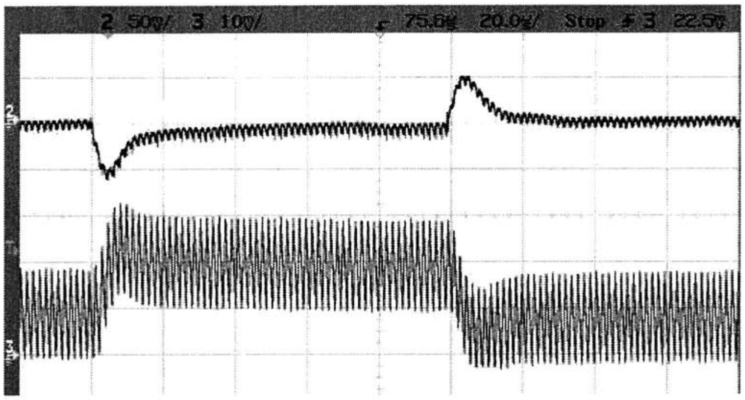


Figure 6-15: Response to a 0.5A to 1A and then a 1A to 0.5A step in the output load. The upper trace is the output voltage of the regulator and shows a 50mV peak overshoot in response to the load step. The lower trace is the inductor current where the 10mV per division corresponds to 500mA per division.

the one concerning characteristic of the step response seen in Fig. 6-15 is the long tail on the voltage waveform as it settles back to its regulated value. This indicates a poor transconductance to compensation capacitor ratio. We always knew this would be a problem area because the error amplifier transconductance is tiny due to its small bias current. To improve this ratio without increasing the current, one could increase the width of the error amplifier input devices to decrease their current densities and get more ideal subthreshold behavior, which would increase the transconductance. One could also decrease the compensation capacitor further, to perhaps 2pF. Each of these techniques would yield a factor of two improvement in the g_m to C_C ratio. However, as it stands, the long tail on the voltage waveform is not a huge issue.

In terms of better optimizing the frequency response, the crossover frequency we achieved was the same as desired, but the phase margin is lower than optimal. High frequency behavior diminishes the phase margin as can be seen for both the phase lead and no phase lead cases in Fig. 6-16, neither of which has as pronounced a phase bump as seen in simulation. Two tests were conducted to see if the phase could be improved. The first test was to increase the switching frequency from 600kHz to 1MHz, which increases the phase margin by about 3^o. The second test was to remove the shunt filter capacitor from the error amplifier output node, which improved the phase margin by about 5^o. The problem with high frequency behavior influencing the phase is that it is difficult to remedy it without lowering the crossover frequency. However, removing or lowering the value of the

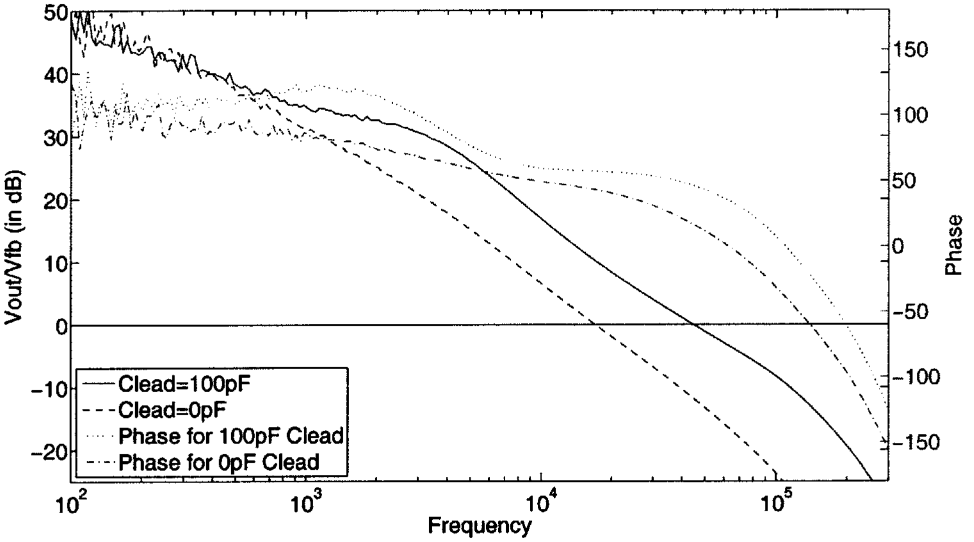


Figure 6-16: The measured bode plot with C_C = 4pF, R_C = 3MΩ, C_{out} = 30μF for the case when no phase lead capacitor is used and the case when a 100pF phase lead capacitor is used.

shunt filter capacitor does seem like one useful step to increasing the phase margin without compromising speed.

6.9 Efficiency

The goal of switching regulators is to convert one voltage into another as efficiently as possible; we want to transfer as much input power to our load as possible. Therefore, the efficiency of the ultra-low quiescent current buck regulator was measured over a huge load range from 1μA to 1A for a variety of conditions. The efficiency curves when converting to a 3.3V output are shown in Fig. 6-17 and the efficiency curves when converting to a 5V output are shown in Fig. 6-18.

The efficiency curves are plotted with the load current on the log scale so that the three different regions of efficiency can clearly be seen. The converter is most efficient for loads between 100mA and 1A, and efficiencies above 80% are observed. The second region is for loads ranging from 100μA to 10mA, where the efficiency is remains constant at about 65% to 70%. The third region is for loads below 100μA, where the efficiency linear decreases for smaller loads.

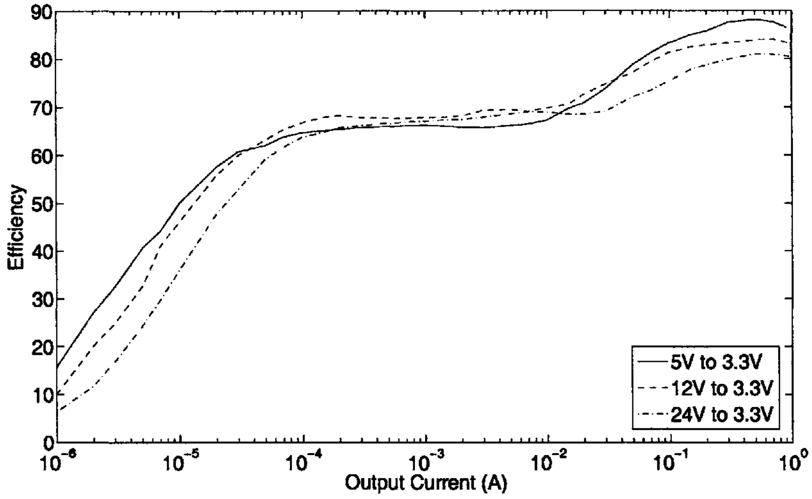


Figure 6-17: Measured efficiency for conversion from 5V, 12V, and 24V to 3.3V over a load range from 1μA to 1A.

The question of primary importance is how does the ultra-low quiescent current operation of the buck converter affect the efficiency in the different load regimes? For loads below 100μA, the converter is operating in burst mode. Therefore, the frequency of current pulses is increased as the load current is increased. The high current circuitry is powered on for a length of time proportional to the switching frequency because it only turns on during a switching pulse. For example, if the switching frequency is doubled, the output current is doubled, and the high power circuitry is powered on for twice as long on average. However, the quiescent current consumed by the part during sleep mode is constant for any period of time regardless of the switching frequency. In other words, the total quiescent current consumed between pulses decreases as the pulses become more frequent. Therefore, the efficiency will linearly increase for increasing load currents because the input power lost by supplying the quiescent current stays relatively constant as the output power increases.

For loads between 100μA and 10mA, the part is operating at full frequency, but in discontinuous mode. Therefore, as the load increases the period of time the switch is on during each cycle is increased. In this regime the quiescent current has a minor effect because the switch frequency is so high. Instead, the lost efficiency is dominated by the supply current when the high power circuitry is on. The length of time the high power circuitry is on each cycle increases as the switch is on for longer portions of each cycle.

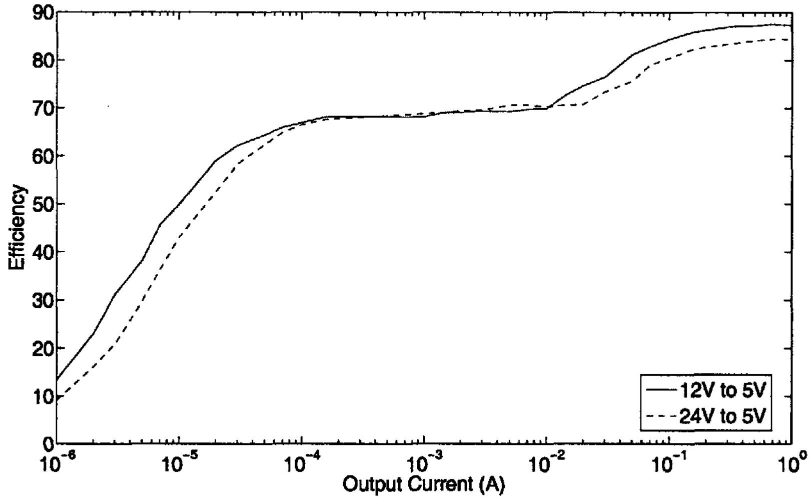


Figure 6-18: Measured efficiency for conversion from 12V and 24V to 5V over a load range from 1μA to 1A.

Therefore, the power lost as supply current increases as the output power increases, so the efficiency stays reasonably constant in this regime.

For loads above 10mA, the efficiency of the part increases because the supply current, even when the high power circuitry is on, is very small compared to the output power. Other efficiency loses unrelated to supply current come into play in this region.

The mechanisms limiting the efficiency in each region can be experimentally supported by observing the results when a few system parameters are changed. The efficiency when the sleep timer is shortened or when large internal feedback resistors are used is plotted in Fig. 6-19 along with the standard 12V to 3.3V curve for comparison. One sees that for loads less than 100μA, the efficiency is made noticeably larger with internal feedback resistors, while shortening the sleep timer only has minor gains in this region. This makes sense because larger feedback resistors will increase the burst frequency for a given load current because the output capacitor will not be drained as fast. However, as argued above, the efficiency in this regime is only minorly affected by the high power supply current because the burst frequency is large. This appear to be experimentally true because decreasing the time the high power circuitry is on by shortening the sleep timer has only a minor effect on efficiency.

For loads between 100μA and 10mA, the option that is more efficient switches. Larger

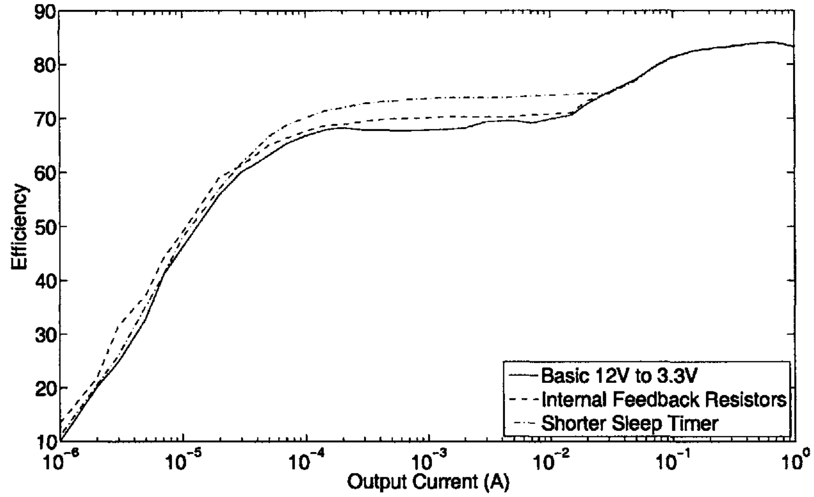


Figure 6-19: 12V to 3.3V efficiency for use with internal feedback resistors or a shorter sleep timer as compared to the efficiency without these options. The use of internal feedback resistors increases the efficiency by one to three percent for loads below 100μA, while the use of a shorter sleep timer increases the efficiency by about six percent for loads between 100μA and 10mA. Note that the shorter sleep timer curve uses external 1 MΩ and 1.7 MΩ feedback resistors and internal feedback resistor curve used the standard sleep timer length.

feedback resistors have only a minor effect on efficiency because the part is operating a full frequency. On the other hand, shortening the period of time the high power circuitry is on will significantly enhance the efficiency because the supply current when the high power circuitry is on is the efficiency-limiting factor in this load region. The efficiency increases about 6% in this region when the sleep timer is shortened.

Lastly, the efficiency for loads above 10mA is identical for all three setups. This demonstrates that the supply current has negligible effect for these high output powers.

Chapter 7

Conclusion

The goal of this thesis project was to realize an ultra low quiescent current buck switching regulator. The micropower circuitry in the LT3480 was redesigned to operate on tens to hundreds on nano-amps of current. The resulting converter consumed 1.5μA when in sleep mode and 1.7μA to 2.2μA when regulating with no load. This is about sixty times less quiescent current than consumed by the original LT3480. As a result, the converter has efficiency even for micro-amp loads. A linear regulator will have a maximum efficiency of 27.5% efficiency for a 12V to 3.3V application. This regulator has a greater efficiency for loads as low at 3μA.

The design did not compromise any other specifications in order to achieve low current operation. The output ripple is less than 10mV in both burst mode and full frequency operation when using reasonable output capacitors sizes of at least 22μF. Current loads of over an amp are able to be sourced by the part. The regulator also has a well compensated control loop, which is able to return to regulation in about 30μs with 50mV of overshoot on the output in response to load transients of 500mA. The control loop was able to be fast and stable over the entire load range, while consuming little current, by using internal compensation. This method not only simplifies the use of the converter by reducing the number of external components, but is also the only way to use capacitances small enough to get acceptable slew rates with less than a micro-amp of current.

It is certainly possible to lower the quiescent current even further than was achieved with this IC. The bandgap circuitry had about 5mV of variation across its temperature range from -55^{o}C to above 125^{o}C. The bandgap current was even halved without any noticeable reduction in performance. Therefore, it seems possible to push it to even lower currents. The error amplifier could also function well with less current by using an even smaller compensation capacitor to maintain acceptable slew rates. Based on the measured results, any coupling between the high current and low current circuits was never detrimental to performance, except for the double pulsing observed as a result of fluctuations on the V_C node generated by the high current circuitry turning off. This issue was easily remedied by readjusting some time constants. Therefore, there seems to be no reason why the subcircuits which are not speed critical, could function properly with less bias current.

However, lowering the quiescent current of the integrated circuit to levels below one micro-amp would only be marginally more useful than the converter designed in this thesis. The self-discharge of batteries and leakages of components is already on the order of micro-amps. Therefore, an even lower quiescent current converter would not as significantly increase battery life because the converter is no longer the limiting factor. Yet, a lower quiescent current would increase the efficiency for loads up to 100μA. If efficiency in this output load region is important for a certain application than an even lower quiescent current regulator might prove useful.

Only the subcircuits which are on during sleep mode were redesigned. The next step would be to redesign the other two-thirds of the part, the non-micropower circuitry, for low current operation. This would increase the efficiency of the converter for output loads between 100μA and 10mA. Several circuits were designed in this thesis to interface the low current circuitry with the high current circuitry. If all the subcircuits in the part were designed for low current operation, than the buffers that make up that interfacing would not be necessary. The simplifications of a more unified system would lead to further lowering the quiescent current.

It is essential that the individual using this part is knowledgeable about the low current operation. If small feedback resistors or diodes with micro-amps of reverse leakage are used on the output, then the low quiescent current operation will be washed out. However, it the user uses the proper external components, the effects of the high current consumption circuitry will be slight, and the ultra low current operation will be achieved.

Appendix A

V_{be} Temperature Dependence

The temperature dependence of a transistor base-to-emitter junction was used in the bandgap analysis in Section 5.1.1. The derivation of that equation is included in this appendix [5].

The basic equation for V_{be} comes from the classic bipolar collector current equation.

$$V_{be} = \frac{kT}{q} ln\left(\frac{I_C}{I_S}\right) \tag{A.1}$$

This equation makes the V_{be} voltage look PTAT. However, we know that a V_{be} has a negative tempco in the following form.

$$V_{be} = E_g - \alpha T \tag{A.2}$$

The key is that I_S is significantly temperature dependent.

$$I_S = BT^{\sigma} e^{-\frac{qE_g}{kT}} \tag{A.3}$$

We can plug this into the original V_{be} equation.

$$\begin{aligned} V_{be} &= \frac{kT}{q}\left[ln\left(I_C\right) - ln\left\{BT^{\sigma}e^{\left(\frac{-qE_{go}}{kT}\right)}\right\}\right] \quad &(A.4) \\ &= E_{go} + \frac{kT}{q} ln\left(\frac{I_C}{BT^{\sigma}}\right) \quad &(A.5) \end{aligned}$$

To eliminate the factor B, we can measure V_{be} at a specific reference temperature, T_R, and collector current, I_{CR}, which will be V_{ber}.

$$B = \frac{I_{CR}}{(T_R)^{\sigma}} e^{\frac{E_{go}-V_{ber}}{kT_R/q}} \tag{A.6}$$

Substituting this value for B into the prior V_{be} equation, we get the V_{be} equation used in Section 5.1.1[5].

$$\begin{aligned} V_{be} &= E_{go} + \frac{kT}{q} ln\left(\frac{I_C}{I_C R\left(\frac{T}{T_R}\right)^{\sigma} e^{\frac{E_{go}-V_{ber}}{kT_R/q}}}\right) && \text{(A.7)} \\ &= E_{go} - (E_{go} - V_{ber})\frac{T}{T_R} + \frac{kT}{q} ln\left(\frac{I_C}{I_{CR}}\right) - \frac{\sigma kT}{q} ln\left(\frac{T}{T_R}\right) && \text{(A.8)} \\ &= E_{go} - \left\{E_{go} - V_{ber} - V_R ln\left(\frac{I_C}{I_{CR}}\right)\right\} H - \sigma V_R H ln\,(H) && \text{(A.9)} \end{aligned}$$

In this equation, H equals $\frac{T}{T_R}$, which is a measure of the relative 'Hotness', and V_R is the thermal voltage at the reference temperature, T_R. The equation shows the negative tempco of a base-emitter junction (the $-H$ term) and it also shows the parabolic second order effect (the $-Hln\,(H)$ term)[5].

Appendix B

MOS Current Mirror Matching

Matching of MOS devices is characterized by two parameters: ΔV_T which is the mismatch in the threshold voltage and $\frac{\Delta\beta}{\beta}$ which is the percent mismatch in the transconductance. When analyzing current mirrors, we have to derive how these two MOS mismatch parameters affect the accuracy of the output current in a MOS current mirror such as that shown in Fig. B-1 [22].

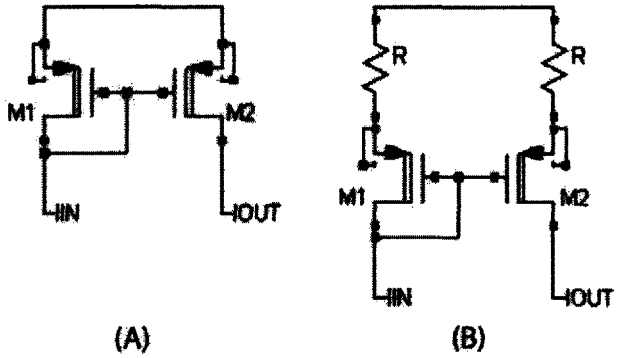


Figure B-1: (A) PMOS current mirror analyzed for matching. (B) PMOS current mirror with source degeneration analyzed for matching.

First, we will derive the equation for typical PMOS devices in the saturation region by adding the error factors to the equation for the drain current. Then the equation is simplified from step 1 to step 2 by using a first order approximation.

$$I_{OUT} = K'(1+\beta_{OFF})\frac{W}{2L}(V_{GS1} - V_T + V_{T,OFF})^2 \qquad \text{(B.1)}$$

$$I_{OUT} = K'\frac{W}{2L}(V_{GS1} - V_T)^2\left(1 + \beta_{OFF} + 2\frac{V_{T,OFF}}{V_{OD}}\right) \tag{B.2}$$

$$I_{OUT} = I_{IN}\left(1 + \beta_{OFF} + 2\frac{V_{T,OFF}}{V_{OD}}\right) \tag{B.3}$$

$$\sigma\left(\frac{\Delta I}{I}\right) = \sqrt{4\left[\frac{\sigma(\Delta V_T)}{V_{OD}}\right]^2 + \sigma\left(\frac{\Delta\beta}{\beta}\right)^2} \tag{B.4}$$

The final equation (Eqn. B.4) comes from the fact that the transconductance and threshold voltage offsets will add as the root mean square because they are statistically independent. The overdrive voltage, V_{OD}, is equal to $V_{GS} - V_T$. Its appearance in the mirror accuracy equation means that a larger gate-to-source voltage is necessary for improving current matching[22].

The current mirror matching for PMOS devices in subthreshold can be derived in the same fashion. A first order Taylor expansion is used to simplify step 1 to step 2. Again, the errors add as a root mean square as shown in the final step (Eqn. B.7)

$$I_{OUT} = I_o(1 + \beta_{OFF})\, e^{\frac{q\left(V_{GS1} + V_{T,OFF}\right)}{nkT}} \tag{B.5}$$

$$I_{OUT} = I_{IN}\left(1 + \beta_{OFF} + \frac{qV_{T,OFF}}{nkT}\right) \tag{B.6}$$

$$\sigma\left(\frac{\Delta I}{I}\right) = \sqrt{\left[\frac{\sigma(\Delta V_T)}{nV_{th}}\right]^2 + \sigma\left(\frac{\Delta\beta}{\beta}\right)^2} \tag{B.7}$$

This equation (Eqn. B.7) has no dependence on biasing, so the devices must be sized to achieve the desired mirror accuracy.

The third interesting mirror matching case is when the MOS devices are in subthreshold and resistor degeneration is added. First, the gate-to-source voltage of the output device is found in terms of the input device gate-to-source voltage and the error terms (Eqn. B.9).

$$V_G = V_{GS1} + I_{IN}R \tag{B.8}$$

$$V_{GS2} = V_{GS1} + V_{T,OFF} - R\Delta I \tag{B.9}$$

Now we can continue as before by plugging the error terms into the gate-to-source voltage term in the output current equation. A first order Taylor expansion approximation is again used in step 1 to step 2. Then, the ΔI term on the right side of the equation needs to combined with the left side of the equation.

$$
\begin{aligned}
I_{OUT} &= I_o\left(1+\beta_{OFF}\right)e^{\frac{qV_{GS2}}{nkT}} && \text{(B.10)}\\
I_{OUT} &= I_{IN}\left(1+\beta_{OFF}+\frac{V_{T,OFF}-\Delta IR}{nV_{th}}\right) && \text{(B.11)}\\
\frac{I_{OUT}}{I_{IN}}-1+\frac{\Delta IR}{nV_{th}} &= \beta_{OFF}+\frac{V_{T,OFF}}{nV_{th}} && \text{(B.12)}\\
\frac{\Delta I}{I_{IN}}\left(1+\frac{RI_{IN}}{nV_{th}}\right) &= \beta_{OFF}+\frac{V_{T,OFF}}{nV_{th}} && \text{(B.13)}\\
\frac{\Delta I}{I_{IN}} &= \frac{nV_{th}}{nV_{th}+I_{IN}R}\left(\beta_{OFF}+\frac{V_{T,OFF}}{nV_{th}}\right) && \text{(B.14)}\\
\sigma\left(\frac{\Delta I}{I}\right) &= \frac{nV_{th}}{nV_{th}+I_{IN}R}\sqrt{\left[\frac{\sigma\left(\Delta V_T\right)}{nV_{th}}\right]^2+\sigma\left(\frac{\Delta\beta}{\beta}\right)^2} && \text{(B.15)}
\end{aligned}
$$

The final result when adding source degeneration (Eqn. B.15) is the result for the subthreshold case without degeneration multiplied by a $\frac{nV_{th}}{nV_{th}+I_{IN}R}$ term. Therefore when more source degeneration is used, the current mirror accuracy improves.

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