Low-Power Amplifier Chopper Stabilization For A Digital-to-Analog Converter

by

Keith Jordy

S.B., Applied Mathematics (2007)
S.B., Electrical Engineering and Computer Science (2007)
Massachusetts Institute of Technology

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Author .....
Department of Electrical Engineering and Computer Science
August 8, 2008

Certified by .....
Joel Dawson
Carl Richard Soderberg Professor of Power Engineering
Thesis Supervisor

Accepted by .....
Arthur C. Smith
Chairman, Department Committee on Graduate Students

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Abstract

Modern portable media devices demand low-power and low-noise performance from the internal digital-to-analog converter. CMOS design has allowed for oversampling sigma-delta modulation to achieve these goals. However, noise is typically limited by the kT/C noise in the switched capacitor filter following the digital modulation. These filters also require a large amount of on-chip capacitance. The goal of this project is to design a continuous-time output stage for a DAC. A continuous-time output requires much less capacitance than the SC filter. Chopper stabilization is applied to the amplifier to reduce the low-frequency noise. The challenge of this architecture is maintaining amplifier harmonic performance and transient performance. In simulations, chopper stabilization improved signal-to-noise ratio by 11dB while maintaining system level harmonic distortion performance.

Thesis Supervisor: Joel Dawson
Title: Carl Richard Soderberg Professor of Power Engineering

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Chapter 1

Introduction

New consumer digital media players are pushing the performance requirements of digital-to-analog converters. There is a demand for very low cost DACs that also have very high dynamic range. Sigma-delta modulation is a technique that can be easily realized using low-cost CMOS processes to achieve these goals. However, the converters are still limited in their flicker noise performance by the analog filters following the digital modulation. Typical methods to reduce the noise of the amplifiers within in the filter include increasing device sizes or decreasing bias currents. While decreasing bias currents seems to reduce flicker noise as well as power consumption, it may not always be possible given the gain and bandwidth performance objectives of the design.

Chopper stabilization can be applied to the amplifiers in the analog portion of the DAC. This modulation technique converts the frequency range of the input to a higher range far above the dominant $1/f$ noise. After the low-frequency noise is added to the signal, a demodulator brings the desired output back to the baseband and moves the noise to the chopping frequency. The noise can then be removed with a low-pass filter. Improvements in the signal-to-noise ratio can be traded for smaller device sizes in the amplifiers resulting in a smaller and cheaper design.

1.1 Previous Work

There are two techniques classically used to reduce noise in amplifiers. The first, autozeroing, samples the noise during a null input and then subtracts the effect of the noise from the input signal using a sample and hold circuit. The principle behind autozeroing is that the noise will not change much between sampling. As long as the null input noise is sampled often enough, the dc-offset can be effectively measured and removed. This method is best suited for switched capacitor circuits when a null input can be applied during a period that the output is held on a capacitor. Autozeroing has the effect of increasing the baseband noise floor by aliasing the wideband noise when sampling [9].

Chopper stabilization, first introduced over 50 years ago, converts the input signal into a frequency region far above the $1/f$ corner before entering the amplifier. The amplifier noise consists of $1/f$ noise which has a high low-frequency content and thermal noise which has a white spectrum. It is then demodulated after amplification which has the effect of bringing the desired signal back down to baseband and pushing the low frequency noise up to the chopping frequency. Only thermal noise with foldover effects are present at baseband signal range after demodulation. Thermal noise cannot be removed since it is present in the entire frequency spectrum. However, baseband noise is reduced significantly since $1/f$ noise is no longer present.

Typically chopping is achieved by switching voltages between balanced halves of an amplifier to have the effect of changing the sign of the signal. While most of the previous work referenced implements voltage chopping, current chopping is also possible as long as the signal is contained within the path of the current in the equal sides of the amplifier. Both methods will be investigated within this thesis.

1.2 Continuous-time DACs

Common sigma-delta DACs use a digital modulator followed by a switched-capacitor (SC) analog filter. However, the noise in this design is limited by the thermal kT/C

noise. SC filters also require a larger amount of on-chip capacitance. For cutoff frequencies below 100kHz, the total capacitance can be on the order of nanofarads [1]. For these reasons, a continuous-time (CT) output stage is used as seen in Figure 1-1.

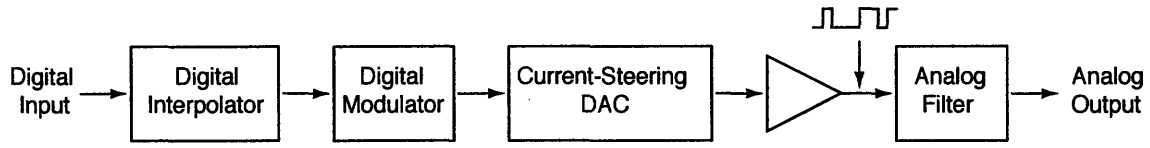

Figure 1-1: Sigma-delta DAC with CT output stage and filter

The converter has digital core that translates the digital input into a 3-level sigma-delta stream that is passed to the analog portion of the chip. A current steering DAC translates the 2-bit digital input into a differential pair of currents. This pair of currents is then passed to a fully-differential op-amp configured as an inverter with a single pole LPF. Next, an active higher order filter is used to remove the modulator steps leaving only the analog output. The purpose of the first LPF is to prevent the active filter from seeing full-scale steps which can cause distortion due to the nonlinear settling of the filter [1]. This thesis only considers the CT analog output seen in Figure 1-2.

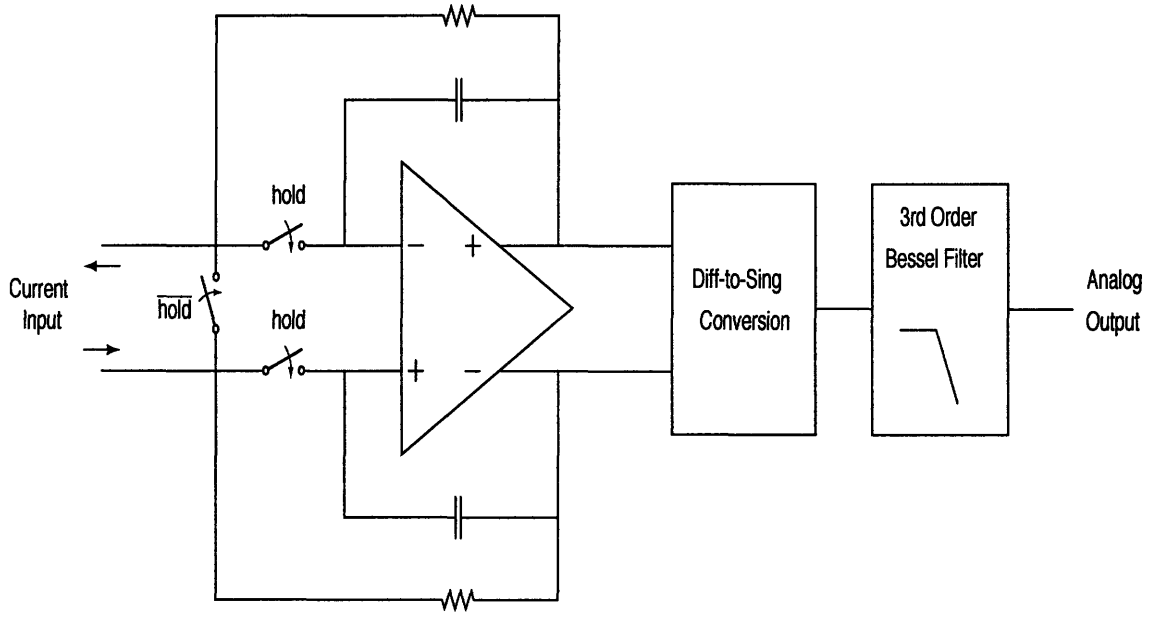

Figure 1-2: Continuous-time analog output stage

The hold switches before the amplifier are used to eliminate inter-symbol interfer-

ence. While the current steering DAC is switching, the amplifier is disconnected and the inputs are tied together. This makes the amplifier intolerant to the DAC. The last value is held on the capacitors until the current switching has settled.

1.3 Baseline Comparison

The new DAC design will be compared against the ADAU1361 low-power codec. This is a sigma-delta converter designed by the Digital Audio Group at Analog Devices Inc. Its design uses a CT analog output stage similar to the one presented in this thesis. It is fabricated in the standard TSMC 0.18μm CMOS process. At a nominal supply voltage of 1.8V, the chip uses only 2.5mW of power and achieves greater than 95 dB of signal-to-noise ratio.

A majority of the power is dissipated in analog portion of the chip. And half of the current is used for the op-amp in the integrator immediately following the current steering DAC.

The goal of this thesis is to design an amplifier that has improved noise performance. It must have similar AC performance to the amplifier used in the ADAU1361 for use in the converter's architecture. The stand-alone amplifier has a SNR of 107dB with chopping; a 9dB increase over the amplifier used in the baseline model. Chopping results in more distortion reducing the total harmonic distortion. However, a THD of greater than -85dB will be considered acceptable for comparison with other DAC amplifiers currently on the market.

1.4 Thesis Outline

Chapter Two describes the theory of chopping and shows the restrictions that the amplifier must work within for effective noise shifting. The implementation of two chopping amplifiers is presented in Chapter Three. This chapter uses chopping with both voltages and currents on identical single-ended amplifiers and discusses the performance of both methods. It also contains the design of the modulation blocks and

device sizing requirements. Chapter Four shows the design of the fully-differential amplifier used in the inverter stage of the DAC. It shows the amplifier, biasing, and clock designs as well as the simulated results. In Chapter Five, the complete analog back-end for the the DAC is simulated to compare the performance of the design presented in the thesis with that of the ADAU1361. Conclusions are drawn in Chapter Six.

Chapter 2

Theory of Chopping

Chopper stabilization is a technique used to reduce the effects of low frequency noise and offset. Similar methods such as autozeroing and correlated double sampling use sample and hold circuitry to measure and subtract the sampled noise from the input single. It relies on the high correlation between samples for good noise reduction. However, the undersampling of thermal noise results in noise folding. Therefore, sampling techniques result in lower offset and $1/f$ noise at the cost of higher thermal noise at baseband frequencies. Similar noise folding occurs with chopping but harmonics decay with the square of the frequency so noise folding from high frequencies is small.

Chopping does not require sample and hold circuitry and requires less on-chip capacitance. It works by multiplying the noise by a square wave resulting in copies of the noise spectrum at odd multiples of the chopping frequency. Chopping can be applied to low-power op-amps to push the $1/f$ noise spectrum to a very high frequency away from the signal baseband resulting in higher signal-to-noise ratios. However, the limit to very high chopping frequencies is charge injection. As the frequency increases, the charge injection occupies a larger percentage of the duty cycle. This increases the offset.

2.1 Application to Amplifiers

The principle of the chopper stabilization is shown in Figure 2-1; feedback resistors and capacitors are neglected for simplicity. Chopper stabilization eliminates low frequency noise by first shifting the input signal to a high frequency where the predominant noise is thermal. This modulation can be accomplished by switching the input signal between the to terminals of the amplifier. Thermal and $1/f$ noises are added to the signal. The signal is then demodulated after amplification. This simultaneously moves the signal back to the baseband frequencies and modulates the amplifier's low frequency noise to odd multiples of the chopping frequency.

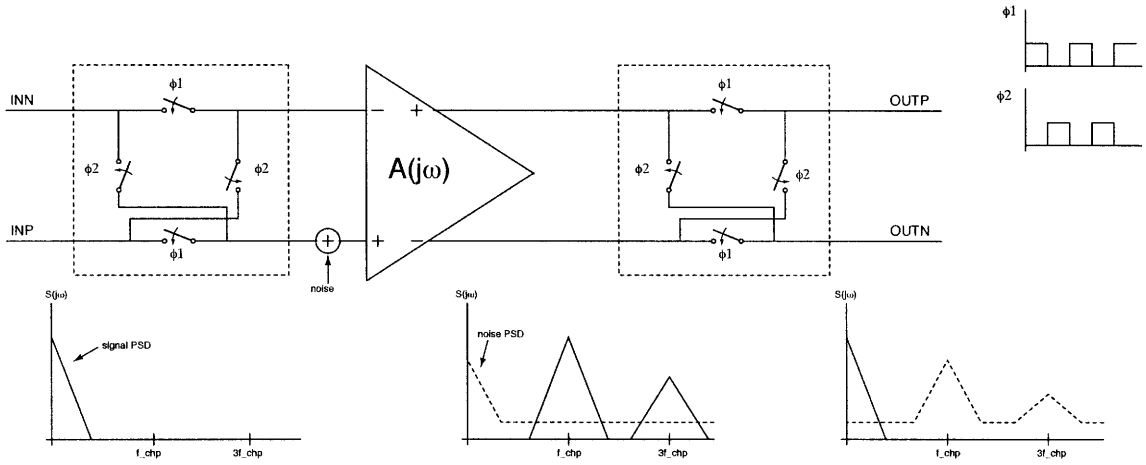

Figure 2-1: Chopper stabilization results in the noise power being shifted around odd multiples of the chopping frequency.

Modulation of the noise, as pictured in Figure 2-2, occurs by multiplying the signal by alternating values of $+1$ and -1 as denoted by $m(t)$.

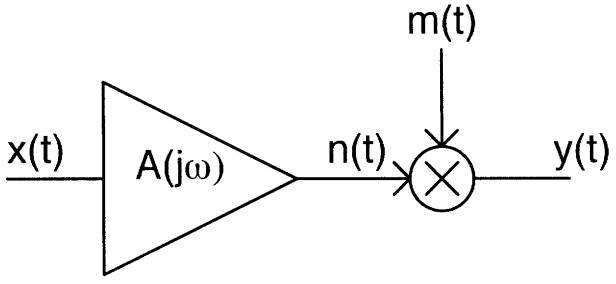

Figure 2-2: Noise modulation occurs by multiplying the noise by a square wave.

The signal $m(t)$ has a frequency equal to the that of the chopping frequency. It is the same signal that is used in Figure 2-1 to modulate the input signal to the chopping frequency. The modulator signal can be expanded into the Fourier Series:

$$m(t) = \sum_{\substack{k=1 \\ k\ odd}}^{\infty} \frac{4}{\pi k} \sin \omega_s k t \tag{2.1}$$

$$M(j\omega) = \sum_{\substack{k=1 \\ k\ odd}}^{\infty} \frac{2}{\pi k} \left(\frac{-1}{j} \delta(\omega + k\omega_s) + \frac{1}{j} \delta(\omega - k\omega_s) \right) \tag{2.2}$$

$$P_m(j\omega) = |M(j\omega)|^2 = \frac{4}{\pi^2} \sum_{\substack{k=1 \\ k\ odd}}^{\infty} \frac{1}{k^2} \left(\delta(\omega + k\omega_s) + \delta(\omega - k\omega_s) \right) \tag{2.3}$$

$$= \frac{4}{\pi^2} \sum_{\substack{k=-\infty \\ k\ odd}}^{\infty} \frac{1}{k^2} \delta(\omega - k\omega_s) \tag{2.4}$$

The power spectral density of the noise seen after chopping is equal to the convolution of the PSD before chopping with $|M(j\omega)|^2$. This results in shifted copies of the noise power at odd harmonics of the chopping frequency. Thermal noise is relatively flat over the spectrum and summing the shifted copies of the thermal noise results in noise folding. Noise folding occurs when the spectrum extends past half of the chopping frequency and the modulation causes noise to stack at baseband.

$$S_{yy}(j\omega) = S_{nn}(j\omega) * |M(j\omega)|^2 \tag{2.5}$$

$$S_{yy}(j\omega) = S_{nn}(j\omega) * \frac{4}{\pi^2} \sum_{\substack{k=-\infty \\ k\ odd}}^{\infty} \frac{1}{k^2} \delta(\omega - k\omega_s) \tag{2.6}$$

Since the input signal sees two modulating blocks, one before the amplifier and one after, the desired signal is at the baseband at $y(t)$. However, the noise only goes through one modulation block and left at odd multiples of the chopping frequency.

The chopping frequency should be chosen such that it is much greater than the

sum of the bandwidth of the input signal and the $1/f$ corner frequency. This will ensure that the noise is modulated to a sufficiently high enough frequency that $1/f$ power does not interfere with the signal and can be removed without a high-order filter.

2.1.1 Effects on Fully Differential Amplifiers

The ADAU1361 uses a fully differential amplifier immediately following the current-steering DAC. Since only a single output is required for the line drivers to follow in subsequent stages, the designers decided to drop the negative output of the amplifier. However, this architecture imposes problems when combined with chopping.

Consider the input referred noise at positive terminal of the amplifier as shown in Figure 2-3. During periods where ϕ_2 is high, the noise from $n(t)$ is seen at the output, V_{out}. However during the other phase when ϕ_1 is high and ϕ_2 is low, the noise from the negative input terminal is not seen at the single output of the inverter.

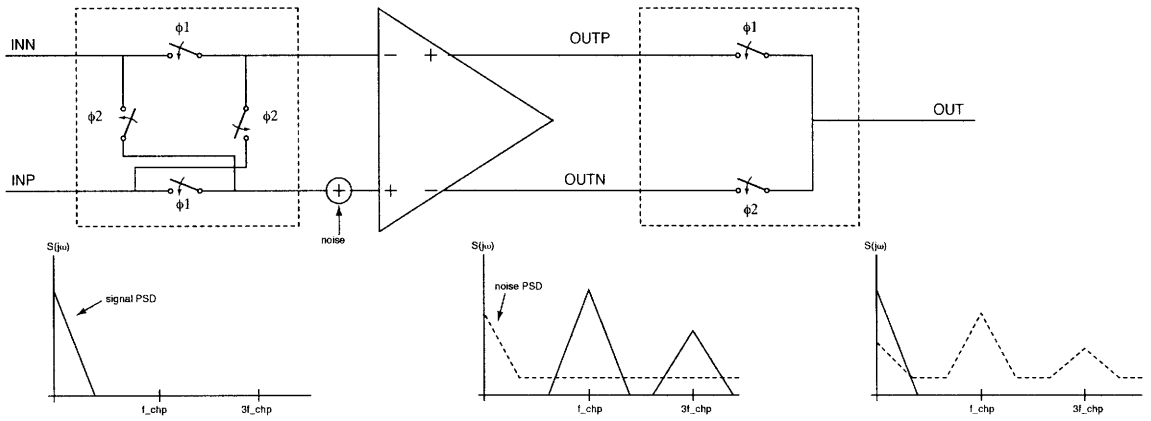

Figure 2-3: Chopper stabilization of a fully differential amplifier considering only a single output: The noise is sampled instead of modulated leaving $1/f$ at the baseband. Adding noises at both inputs will result in same baseband $1/f$ noise.

In the case of a fully-differential amplifier with only a single-ended output, the noise is multiplied by a square wave with the values of 0 and +1. Due to a DC offset in the modulator signal, a scaled copy of the noise power spectrum remains at baseband frequencies.

This type of chopping clock will be referred to as the sampling chopping clock,

$m_s(t)$, because it has the effect of scaling the noise and creating shifted copies of the noise power spectrum at odd multiples of the chop frequency. As with the standard chopping theory above, there will be some noise folded over from the higher frequencies. However since the chopping frequency is much higher than the $1/f$ corner and the contributions from odd harmonics decrease by the frequency squared, noise folding will be negligable. The chopping clock, $m_s(t)$, can be expanded with the following Fourier Series:

$$M_s(j\omega) = \frac{1}{2} + \sum_{\substack{k=1 \\ k\ odd}}^{\infty} \frac{1}{\pi k}\left(\frac{-1}{j}\delta(\omega + k\omega_s) + \frac{1}{j}\delta(\omega - k\omega_s)\right) \tag{2.7}$$

$$P_{ms}(j\omega) = \frac{1}{2} + \frac{1}{\pi^2}\sum_{\substack{k=1 \\ k\ odd}}^{\infty} \frac{1}{k^2}\left(\delta(\omega + k\omega_s) + \delta(\omega - k\omega_s)\right) \tag{2.8}$$

$$= \frac{1}{2} + \frac{1}{\pi^2}\sum_{\substack{k=-\infty \\ k\ odd}}^{\infty} \frac{1}{k^2}\delta(\omega - k\omega_s) \tag{2.9}$$

The power spectral density of the noise seen at the output due to the input referred noise at the negative terminal is reduced by a factor of two at the baseband and shifted copies appear at odd harmonics of the chopping frequency. These copies also decay by the square of the harmonic and therefore the folding of thermal noise reaching the baseband is minor.

A fully differential amplifier contains two identical half circuits. When only one output is considered, only one of the half circuits contributes to the noise. However, chopping switches the signal path between both sides equally. Each half circuit will contribute to the noise at the output. The noise at the output due to the input referred noise at the negative terminal is reduced by a half. After chopping, the noise at the positive input, which was not seen before chopping, appears at the output with the same strength as the other noise. Therefore, the noise at the single output after chopping can be approximated by:

$$S_{yy}(j\omega) \simeq S_{nn}(j\omega) * 2 \left\{ \frac{1}{2} + \frac{1}{\pi^2} \sum_{\substack{k=-\infty \\ k\ odd}}^{\infty} \frac{1}{k^2} \delta(\omega - k\omega_s) \right\} \tag{2.10}$$

The above equation predicts that the output noise, $S_{yy}(j\omega)$, will be larger than the noise seen at the output before chopping, $S_{nn}(j\omega)$. In practice, the power of the two noises are about equal. While the noise from the input is reduced by half from sampling, noise from both inputs add to the single output. Summing the noise from the two inputs results in total output noise that is equal to that of the non-chopping amplifier. However, the amplifier's common mode feedback circuit sees the chopping and will have its noise contribution decreased. A more detailed noise analysis will be discussed in Chapter 4.

Chapter 3

Implementation

Chopping can be implemented on most circuits with two mirrored paths. Switching the signal between paths with opposite signs will result in modulation. It is important that these paths are identical so that the output is not dependent, other than the sign, on the path taken.

3.1 Chopping Blocks

Four switches are used for each modulator block seen in Figure 3-1. This is the basic chopping block that has two inputs and two outputs. However, a similar one can be made with two inputs and one output to be used in single-ended amplifiers. During the first phase of the clock cycle, both signals are passed straight through the modulator. And the signals switch outputs for the second stage.

Special attention must be paid to the timing of the two phases. In general, they should be driven with a non-overlapping clock to prevent noise leakage. This clock contains a short period of time where neither signal is propagated through the chopping block to prevent noise leakage during switching. The phases should also be close to a 50% duty cycle for proper modulation. The types of clocks used will be discussed further for specific cases in Section 3.2 and in the design of the non-overlapping in Section 4.4.

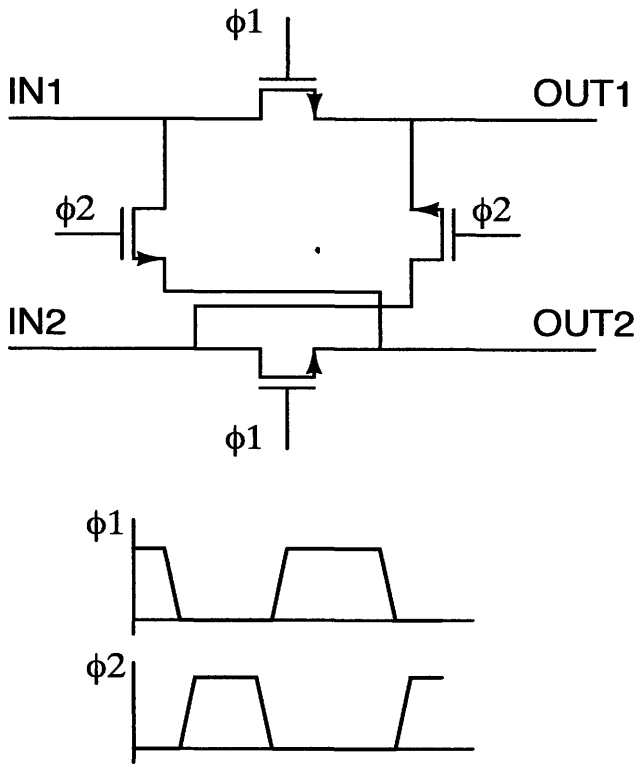

Figure 3-1: Modulation Block with Non-Overlapping Phase Clock

3.1.1 Device Sizing

There are two considerations for the size of the switches. First, the switches should be as small as possible to keep the gate-source capacitance, C_{gs}, to a minimum. Charge stored on the parasitic capacitances will cause spikes during switching. Second, the on-state resistance (R_{on}) of the devices must be chosen properly so the capacitances following the chopping block can be driven quickly enough. Also, a large on resistance will cause noise when voltages are being passed due to the voltage drop across the device.

Consider a typical placement of a single switch before the gate of an output stage device in Figure 3-2. The sizing of the output device is determined by the performance requirements of the amplifier; its length and width can not be modified. For small charge injection, the width of the switch should be as small as possible to keep it's C_{gs} to a minimum. However in order to charge and discharge the output device's parasitic capacitances quickly, the width of the switch must be large to make the on

resitance small.

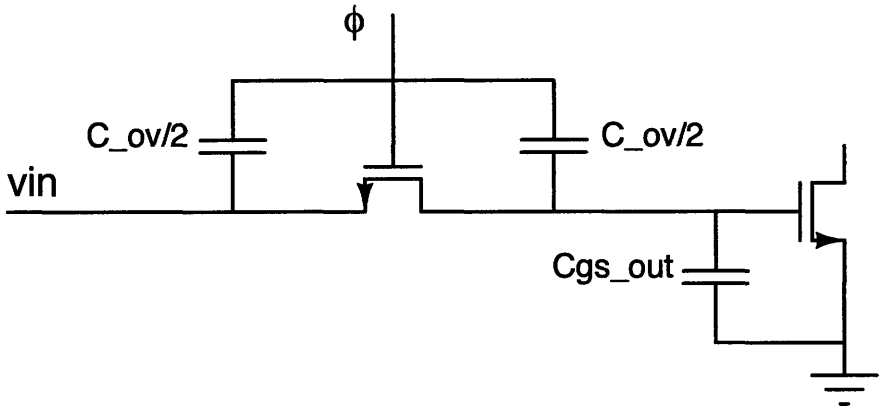

Figure 3-2: Charge injection from the chopping switches is caused by charge stored on the overlap capacitance.

The time constant for the charging and discharging of the output device's parasites is approximated by the following equations:

$$\tau = R_{sw} C_{out} \tag{3.1}$$

$$R_{sw} = \frac{1}{\mu_n C_{ox} \frac{W_{sw}}{L_{sw}} (v_{GS} - V_T)} \tag{3.2}$$

$$C_{out} = \frac{2}{3} W_o L_o C_{ox} \tag{3.3}$$

$$\tau = \frac{2}{3} \frac{W_o L_o}{\mu_n \frac{W_{sw}}{L_{sw}} (v_{GS} - V_T)} \tag{3.4}$$

When a MOSFET turns off, charge errors occur from the channel charge flowing out to the drain and source and from the charge due to overlap capacitances. The channel charge usually dominates and if v_{DS} is zero, it is given by [5, p. 309]

$$Q_{CH} = WLC_{ox} V_{eff} = WLC_{ox} (V_{GS} - V_t) \tag{3.5}$$

From equations 3.4 and 3.5 above, it is obvious there are conflicting requirements for the width of the chopping switches. However in practice, charge injection usually

dominates the error within the circuit and switches are kept as close to minimum sizes as possible.

3.2 Types of Chopping

There are two types of chopping: current chopping and voltage chopping. Both have the same effect except one swaps voltage between the circuit halves and the other swaps currents. Voltage chopping is the simplest method and has been traditionally used because there is less risk of crashing the bias points of devices [3]. However, voltage chopping will have slightly worse noise performance because of the voltage drop across the modulator devices. Current chopping requires proper timing to prevent the crashing of bias points during switching.

3.2.1 Voltage Chopping

Voltage swapping is commonly used to implement modulation within the amplifier. Such configurations have been proven successful in the design of low noise CMOS amplifiers [10]. Input modulation is almost always voltage chopping since the switching occurs at the gates of the input devices. However, there is flexibility on where the output chopping can occur. For voltage chopping, the ideal placement for the demodulation block is at the gates of the output devices.

Voltage chopping occurs at high impedance nodes. These nodes are very sensitive to thermal noise and placing switches here will increase this noise [7]. However, a small increase in thermal noise is acceptable since it is significantly less than the predominant $1/f$ noise.

It is desirable for the voltage swing at the switches to be small. Large deviations in voltage will require more time for the voltage to settle since the parasitics must charge or discharge accordingly. The voltage swing at the output stage gates is typically a few millivolts, while the output swing is over a volt. Ripple during the settling period, due to both charge injection and the time constant from parasitics, increases the distortion at the output of the amplifier. In addition to distortion and

settling time, the voltage drop across the source and drain of the switches cause offset errors from biasing. Generally, voltage chopping will result in a slightly worse noise performance than if current chopping were used due to losses and parasitics of the switches in voltage paths.

A design for a single-ended voltage-chopping amplifier can be seen in Figure 3-3. This is a folded-cascode amplifier with a class AB output stage. The two pairs of devices, mp6 with mn6 and mp8 with mn12, setup the bias points for the two devices of the output stage. Their gate voltages are set by a separate bias circuit. The threshold voltage drop from the gate of the PMOS device biases the top half of the output stage and the threshold drop of the NMOS device biases the lower half.

Modulation of the signal chopping occurs at the gates of the two input devices, mn20 and mn21. Native NMOS devices are used for this chopping block. A minimum length of $1.2\mu m$ is used for both a minimum settling time and charge injection. The width is set at $2\mu m$ which is slightly above the $0.34\mu m$ minimum for appropriate on resistance to drive the input gates. The second modulation block swaps the voltages just above and below the bias circuitry for the output stage between the two mirror halves of the cascode. Chopping transfers the signal between the two halves of the amplifier. This is why switching is required at the gates of both output devices.

A non-overlapping clock as seen in Figure 3-4 drives the two phases of the chopping blocks. The non-overlap period is set to be about $5ns$ to reduce the noise leakage between the two chopped halves.

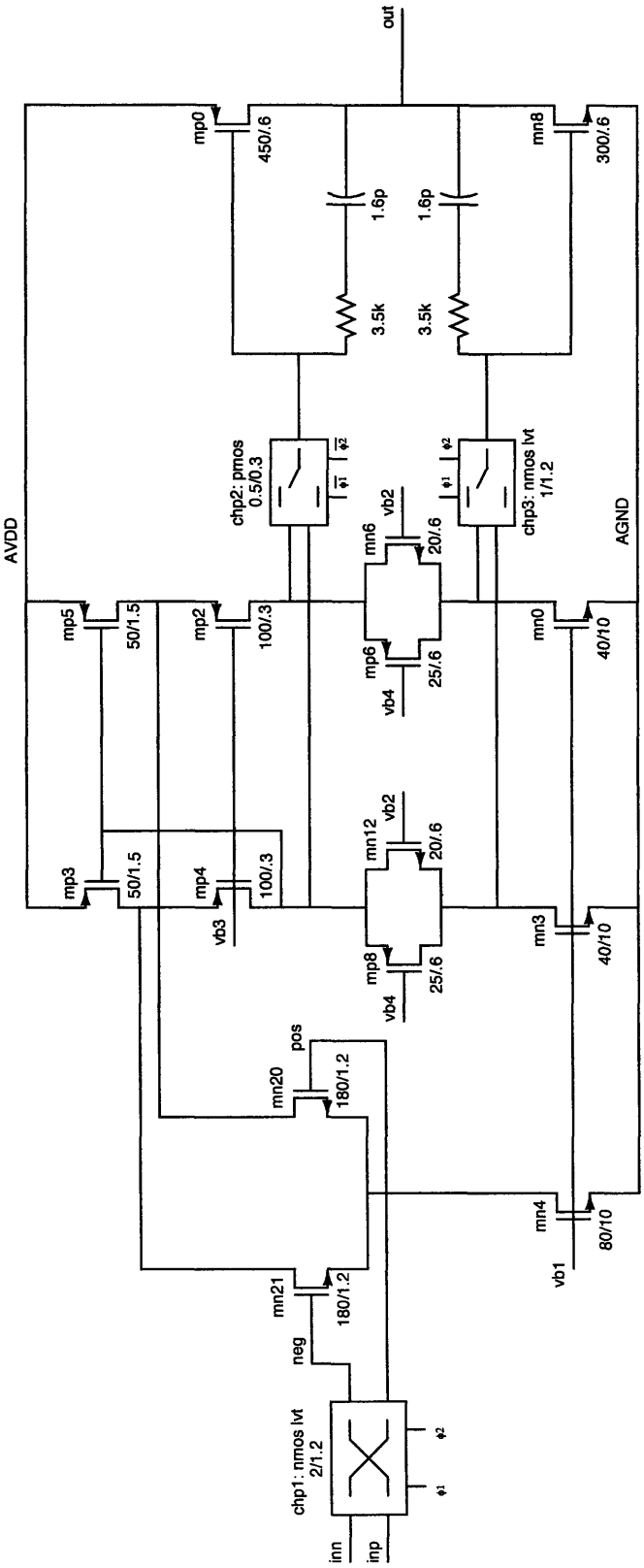

Figure 3-3: Single-ended amplifier with voltage chopping. Chp1 modulates the input signal while chp2 and chp3 demodulate it and move the noise up to the chopping frequency.

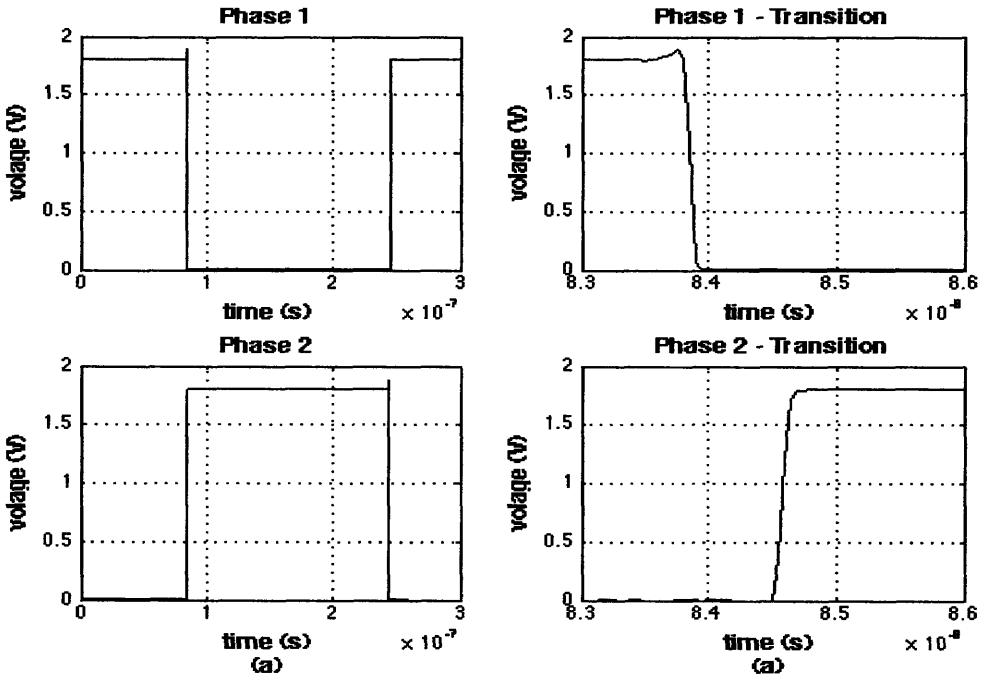

Figure 3-4: Two-phase non-overlapping clock. (a) The two phases clock the switches of the chopping block such that each signal goes to each output for 50% of the period. (b) The two clocks are non-overlapping to prevent noise leakage while switching. The non-overlap time is 5ns.

3.2.2 Current Chopping

Current chopping is more difficult to implement than voltage chopping. Since the switching blocks must be placed in the current path through devices, there is a risk of crashing the device's bias point when current is switched off. However, these topologies result in better noise and distortion performance than the previous amplifiers [7].

Demodulation occurs at the low impedance node in the middle of the cascode. This node is less sensitive to charge injection because it is not directly coupled to the output and the amount of charge injection is much less than the quiescent bias current through the path. As a result, the chopping switches can be very large to achieve a small resistance. The devices are over ten times larger than the switches used in the voltage chopping amplifier in the last section.

The same amplifier topology used in the previous section is shown in Figure 3-5 with current chopping. Input modulation still swaps the voltages on the gates of the input devices while demodulation occurs in the current signal path between the two PMOS devices in the cascode. These two chopping positions eliminate the noise from the four major noise contributors: mn21, mn20, mp3, and mp5. The next two major sources of noise, after the input devices and two top MOSFETs in the cascode, are the NMOS current sources, mn3 and mn0. A third chopper is added above the current sources, mn3 and mn0, of the folded cascode. This modulates the $1/f$ noise of these two devices. Chp3 does not lay in the signal path thus its switching does not affect the spectrum of the amplified signal.

Two switches, mn1 and mn5, at the gates of the output devices disconnect the two stages while the chopping switches settle. Figure 3-6 shows the clock timing for the four phases used in the circuit. When phase 4 goes low output stage is disconnected, the voltage is held on the parasitic capacitances of mp0 and mn8. This ensures that the output is insensitive when currents are swapped. If these switches were not present, charge would be pulled quickly off of the output device gates during the non-overlap portion of the clock when the current sources get disconnected.

The two switches between the stages are located at a high impedance node. Their

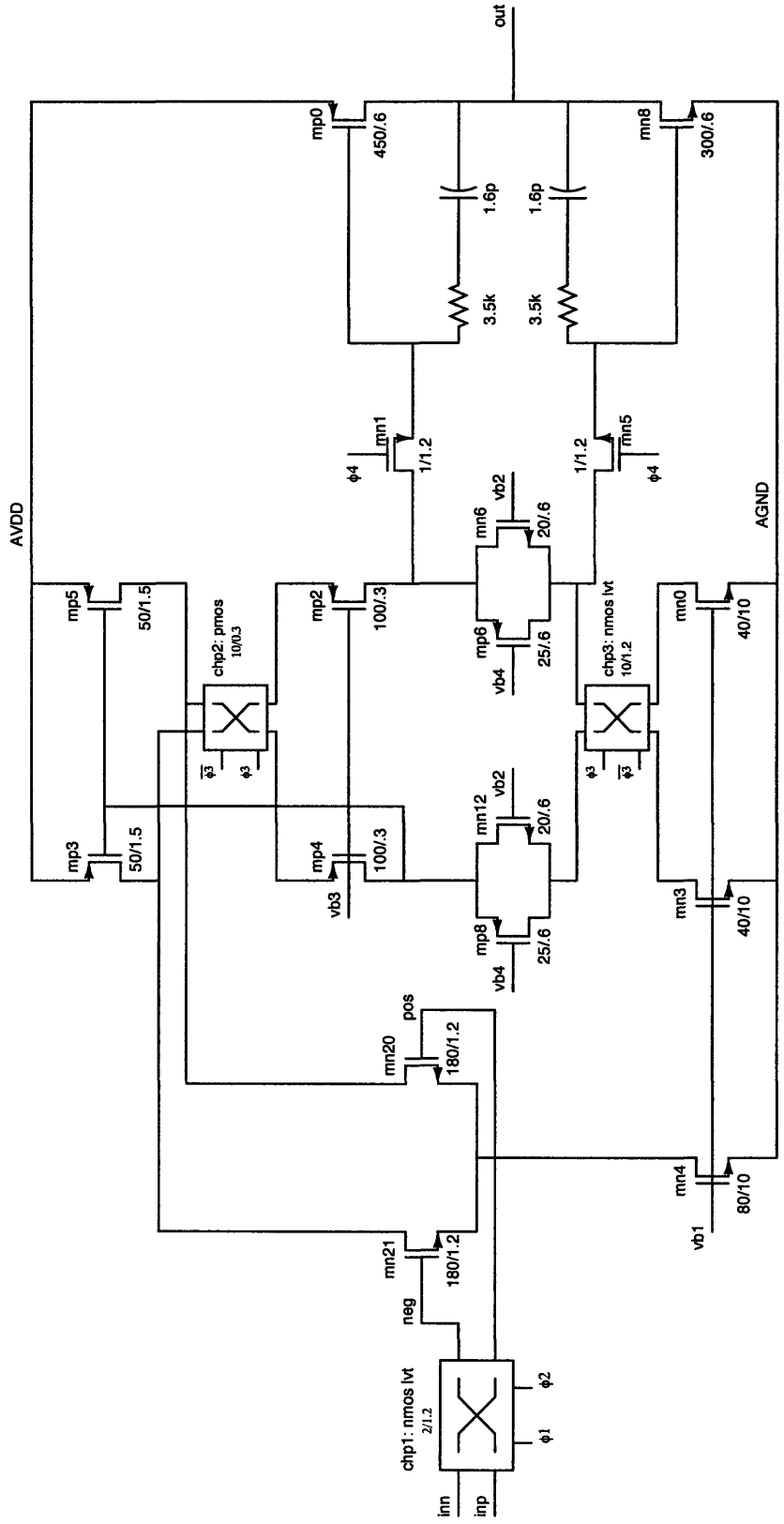

Figure 3-5: Single-ended amplifier with current chopping. Chp1 modulates the signal with voltage chopping. Chp2 and chp3 use current chopping to demodulate the signal.

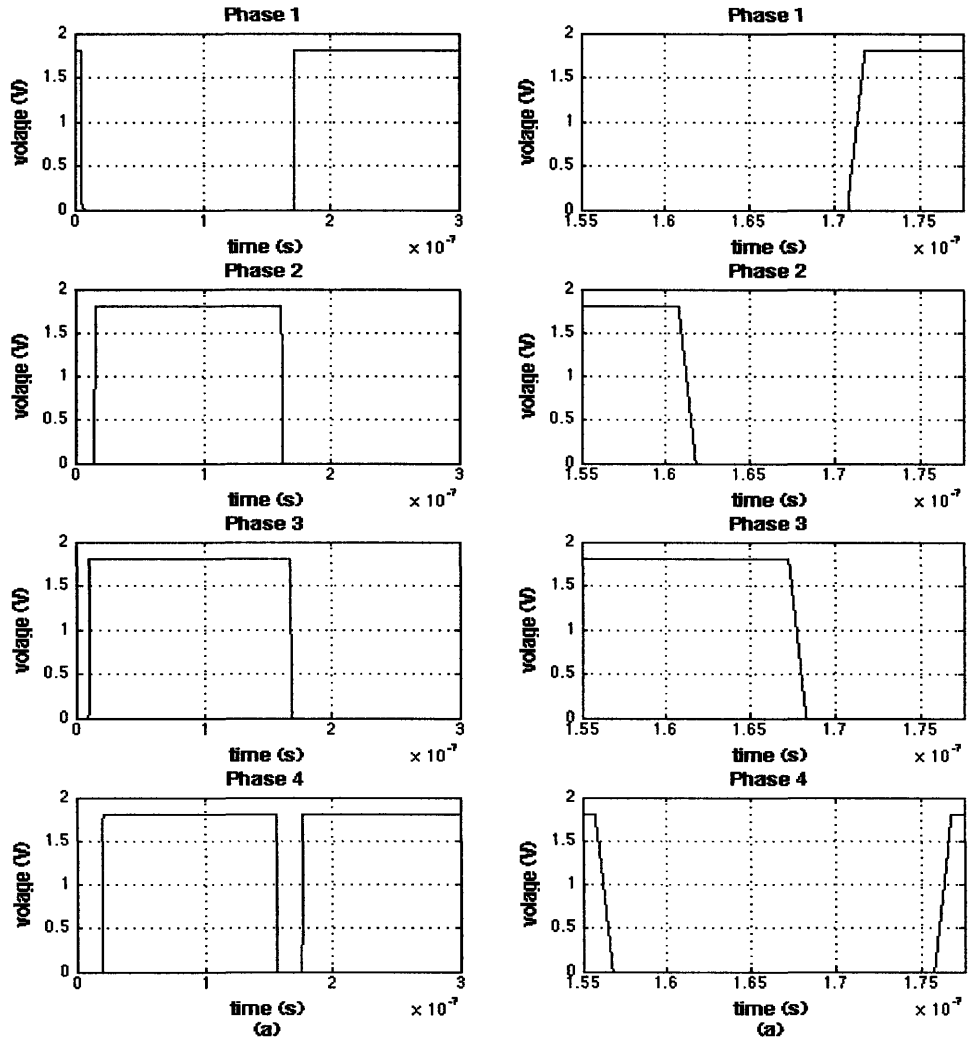

Figure 3-6: Four-phase non-overlapping clock. (a) Phase 1 and 2 are non-overlapping and drive the input chopper. Phase 3 controls the current switching between the two paths of the cascode. This phase does no need to be non-overlapping since noise leakage will not propagate to the output. Phase 4 disconnects the output before any of the other phases change. (b) The transitions of the clock show that the output stage is first disconnected. Next the non-overlapping period for the input chopper begins and the current chopping in the cascode begins. Finally the non-overlapping period ends and the output stage is reconnected.

charge injection is directly coupled to the output and will have a significant effect. However, since the switches are at high impedance nodes, their channel resistances will not cause much offset error once the voltage has settled. Minimum sized devices

are used to keep charge injection small.

Before any chopping occurs, the phase 4 clock disconnects the output stage. The non-overlapping portion of phase 1 and 2 connected to the input chopper begins. Current through the cascode returns to its nominal values and the phase 3 clock with its complement swaps the current through both chp2 and chp3. This demodulates the signal and moves the noise of the major contributors, the two input devices and the four current sources, to the chopping frequency. Finally, the non-overlap period for the input chopper ends and the output is reconnected.

3.2.3 Single-Ended Amplifier Performance

The performance of all three single-ended amplifiers can be seen in Table 3.1. AC characteristics are identical because chopping switches the signal between two balanced paths in the circuit. Since each path by itself would have the same AC response, chopping will not effect these characteristics. Signal-to-noise ratio (SNR) was increased significantly while total-harmonic distortion (THD) up to 20 kHz of a 1 kHz sine wave input was reduced with the addition of chopping. Canceling noise contributions of the major devices caused the increase in SNR. However every time there was switching, a small ripple appeared at the output due to charge injection. This ripple worsened the THD.

Table 3.1: Single-ended Amplifier Performance

Spec	No Chopping	Voltage Chopping	Current Chopping
Gain	106 dB	106 dB	106 dB
UGF	32.4 MHz	32.4 MHz	32.4 MHz
PM	55.8°	55.8°	55.8°
GM	21.1 dB	21.1 dB	21.1 dB
Power	0.315 mW	0.315 mW	0.315 mW
THD	-100.94 dB	-85.6 dB	-87.3 dB
SNR	-101.5 dB	-106.0 dB	-107.1 dB

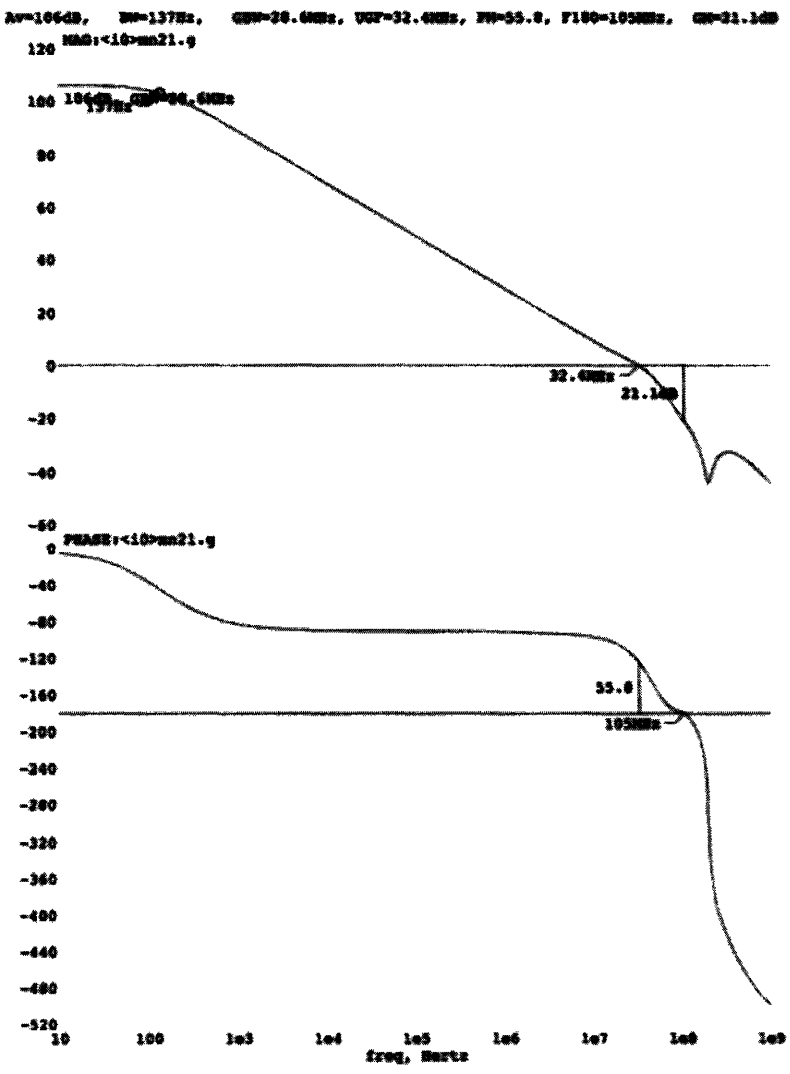

Figure 3-7: AC response for the single-ended amplifier: Chopping does not change the AC response of the amplifier.

Chapter 4

Amplifier Design

This chapter will discuss the design of the amplifier used in the inverter stage of the DAC. Its performance will be compared to the that of the ADAU1361. For now, only the specific stage will be discussed and the system around the amplifier will be ignored so a more in depth analysis of the performance can be studied. Validation of the amplifier design within DAC will be carried out with different simulation tools used in Chapter 5.

4.1 Consequences of Noise Sampling

In Chapter 2, it was shown that when using only one output of a fully differential amplifier, chopping does not reduce the noise power seen at the output. Therefore, the simple addition of chopping circuitry to the ADAU1361 architecture will not improve performance. There are two potential solutions to this problem. First, the DAC architecture can be changed to use single-ended chopping amplifiers as seen in Chapter 3. However, the requirement for very fast common-mode correction of the output of the current steering DAC makes the design of a new architecture difficult. Second, the inverter stage of the chip can use both outputs of the fully-differential amplifier and have a differential-to-single ended conversion follow. This allows for a slower common-mode correction since the differential output resolves linearity problems with drifting current sources. However, extra power is required for the differential-to-single ended

conversion. The latter solution will be implemented in the remainder of the thesis.

4.2 Circuit Details

The fully-differential folded-cascode amplifier is chosen for the DAC is shown in Figure 4-1. The design is similar to that used in the previous chapter but identical output stages are connected to both half circuits of the main amplifier. It uses a class AB output stage biased the same way that the single-ended amplifiers were biased in Chapter 3. Another single-ended folded cascode amplifier is used for common-mode feedback.

4.2.1 Common-Mode Feedback

Common-mode feedback is used to keep the mean output voltage at half of the supply voltage, 0.9V. The two outputs are averaged using a passive network seen in Figure 4-1. The resulting value, *cmfb*, is compared with the desired common-mode value, *cm*, that is supplied to the amplifier by an external source. The comparison happens within the single-end folded-cascode and adjusts the gain of the main amplifier to raise or lower the common-mode voltage of the outputs.

When the observed common-mode is above the desired voltage, more current is pulled through the left input to the feedback amplifier and less current flows down the left branch of the cascode. This lowers the voltage at the gates of mp8 and mp11, *vb_cmbf*, to supply more current to the input device which is reflected over to the gates of cascode devices, mp3, mp5, mp13, and mp14, of the main amplifier. Increasing the current from the cascode pushes more charge onto the gates of the output devices than the NMOS current source and pull off. The effect is to decrease the common-mode voltage to match the desired value.

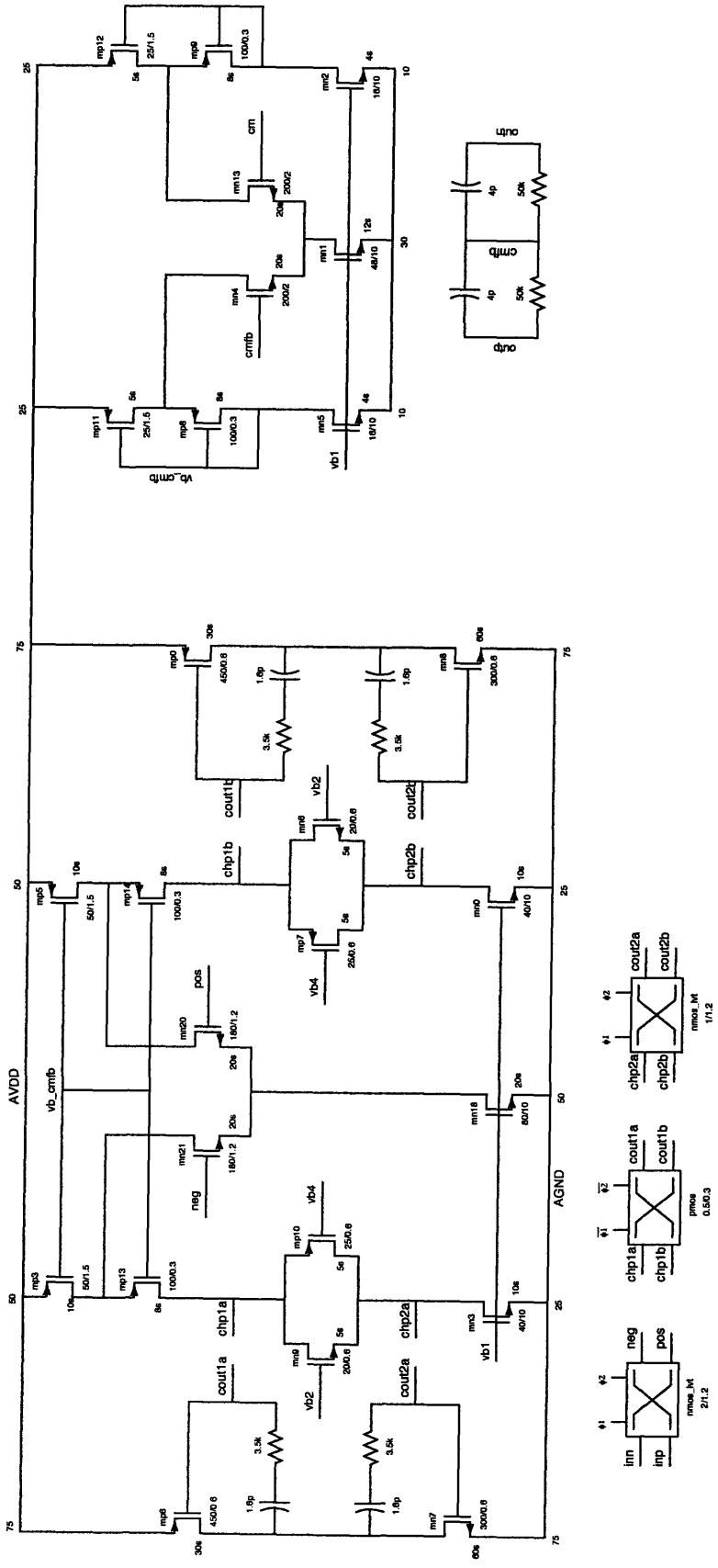

Figure 4-1: Fully differential amplifier with voltage chopping

4.2.2 Biasing

The amplifier is biased by a external circuit as seen in Figure 4-2. The same biasing circuitry is used for all the amplifiers presented in this thesis. Voltages *vb2* and *vb4* are used to set the gate voltages for NMOS and PMOS devices, respectively, biasing the gates of the output stage. These values are set for the proper biasing of the current though the class AB output.

Internal biasing is used to setup the PMOS devices in the cascode of the main amplifier. For the proper biasing, mp3 and mp5 must be matched to mp11 of common-mode feedback in Figure 4-1.

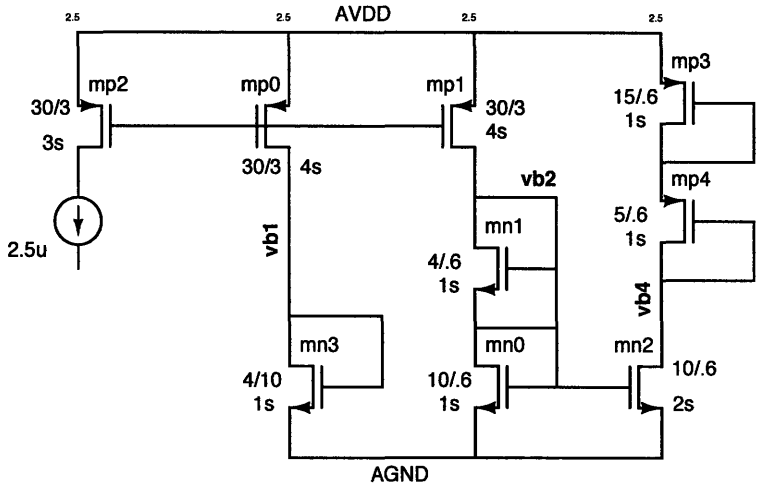

Figure 4-2: Bias circuitry

4.3 Chopping Locations

Chapter 3 described the two types of chopping that could be implemented. Although the current chopped amplifier provided better noise performance, it requires a more complicated switching scheme. Switching should occur within the 20ns that the hold switches are open. Once the hold switches close, the amplifier should be settled and ready to accept the new input. Current switching requires the extra step of disconnecting the output stage before the circuit halves are swapped. This reduces the time for the amplifier to settle. There is also the risk of crashing devices when

the current is stopped during switching. Because of these reasons, voltage chopping is implemented.

The demodulation blocks are located at the gates of the output devices. As seen in Chapter 3, each of the two output devices requires its own set of choppers. Swapping output stages, changes the output from negative to positive resulting in multiplication of the signal by a square wave from -1 to $+1$.

The chopper for the top output device uses standard PMOS switches while native NMOS switches are used in the lower chopper. This design choice comes from the ability to turn the switches on and off quickly and the bias points of the two nodes. The upper and lower gate voltages are biased at 1.1V and 0.4V, respectively. The supply voltage is only 1.8V. Even with a low threshold voltage for an NMOS device, it may not be able to turn on completely if placed at the top node. Thus a PMOS switch is used and clocked with the opposite phase of the NMOS device. Native switches can be used at the lower node. These devices require a negative v_{GS} to turn off. The bias point of the lower node is large enough that v_{GS} is sufficiently small such that the device is completely turned off.

There is no need to chop the common-mode feedback circuit. Noise from the common-mode circuit enters the main amplifier between the input modulator and the demodulator. Therefore, its noise contribution will be modulated around the chopping frequency. Noise entering through *vb_cmfb* affects both halves of the main amplifier equally. Taking the differential output of the amplifier will further eliminate noise from the common-mode feedback circuit.

4.3.1 Device Sizing

In the $0.18\mu m$ process, the resistance for the minimum sized devices is about 5kΩ. This was determined to be slightly high for the application. Devices were sized for an on resistance of about 1kΩ.

The main concern when choosing the switch sizes was to minimize charge injection. From Equation 3.5, it is clear that both the length and width must be minimized. However, there is also a requirement in the settling time because the output must

be stable when the hold switches before the amplifier close. This requires that the widths be chosen slightly above minimum values. PMOS and NMOS switch widths are chosen to be $0.5\mu m$ and $1\mu m$, respectively, while the minimum allowed values are $0.22\mu m$ and $0.34\mu m$.

4.4 Timing

A two-phase non-overlapping clock with a fifty-percent duty cycle is used to drive the four devices in each modulation block. Since both PMOS and NMOS switches are used, complements of both phases are required for simultaneous switching. The chopping frequency is half of the DAC's sample frequency, 3.2MHz, and the non-overlap period is 5ns.

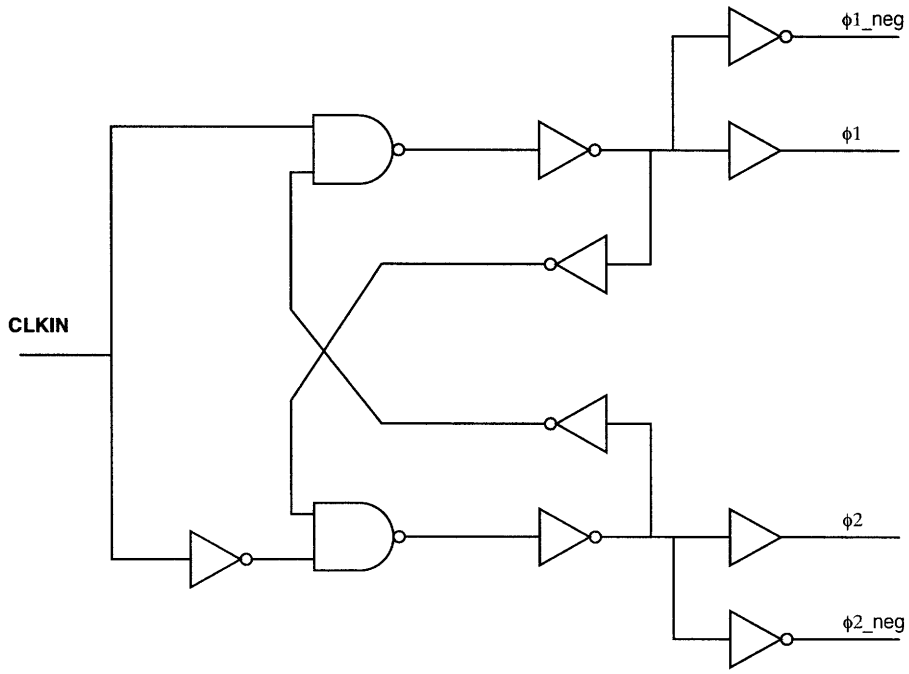

Figure 4-3: Non-overlapping clock generator. The two phases and their complement are created from a signal that is half the DAC clock frequency.

In order to create the non-overlapping clock, the 6.4MHz DAC sample frequency is first halved using a D-flipflop. The resulting clock is passed to the clock generator shown in Figure 4-3 which creates both phases and their complements. All four signals must be generated at the same time to ensure that the clock edges line up properly. If

the complements were created by simply inverting one of the phases, there would be an additional delay added by the inverter and the PMOS and NMOS switches would not turn on or off simultaneously.

4.5 Testing

Performance is specified by the ADAU1361's design requirements. The amplifier must work at a nominal supply voltage of 1.8V and have a differential gain of at least 75dB, a common-mode gain greater than 70dB, SNR greater than 97.5dB, and THD greater than 85dB.

For the application of the main integration stage in a digital-to-analog converter, the amplifier is placed in a similar configuration to its intended use with a 10kΩ load. The output will is measured as a differential signal. This section evaluates the stand-alone amplifier while Chapter 5 will discuss the system validation of the amplifier.

4.5.1 AC Response

The AC response is tested with the amplifier configured as an inverter with a single pole seen in Figure 4-4. The amplifier is placed in the inverter configuration with a single pole at 10MHz. Using a low-pass filter shoftens the sharp transition of the step inputs that will be seen from the digital input. This is important because abrupt transitions can cause errors within the DAC system [1]. Two load resistors are connected to the common-mode voltage to represent the approximate loading seen by the amplifier in the converter. Since chopping does not affect the frequency response of the amplifier, only one plot for the AC response is seen below.

The open-loop differential response is measured from the gates of the two input devices, mn21 and mn20, to the output. The common-mode AC response is taken from the inputs to the common-mode feedback, mn4 and mn13, to the output of the amplifier.

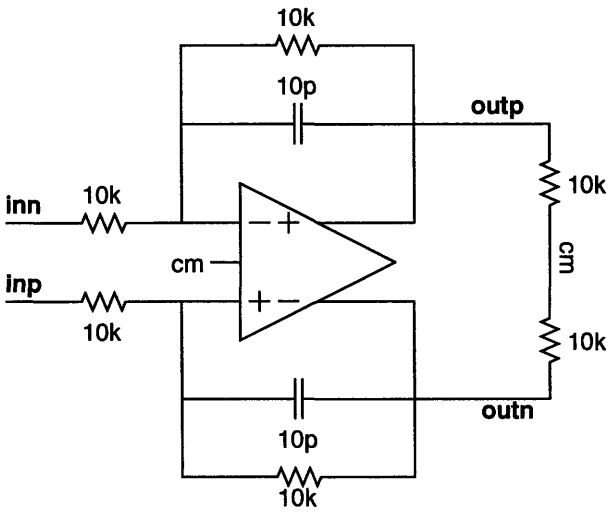

Figure 4-4: Amplifier configuration for AC analysis

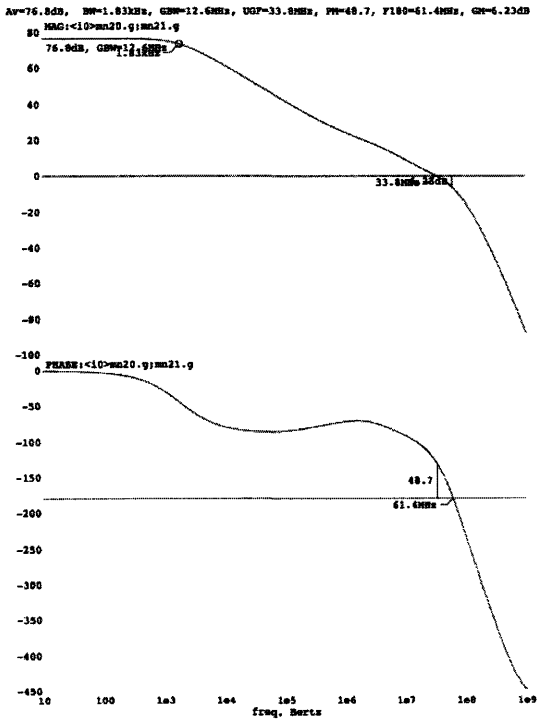

Figure 4-5: AC response for the fully-differential amplifier: Chopping does not change the AC response of the amplifier.

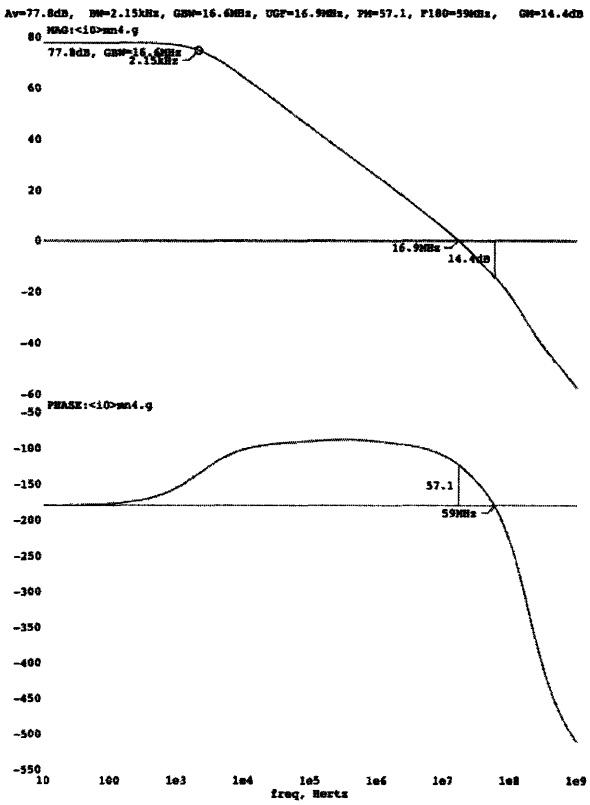

Figure 4-6: AC response for the common-mode of the differential amplifier

4.5.2 Noise Analysis

For the noise analysis, the amplifier was placed in the unity gain feedback configuration with no inputs as seen in Figure 4-7. This configuration gives the noise of only the amplifier without any effects due to the feedback resistors and capacitors.

The total noise power is shown in Figure 4-8. After chopping, the $1/f$ noise is reduced by two orders of magnitude. A spike in noise is seen around 3.2MHz from the modulation. The remaining $1/f$ noise seen comes from the devices of the output stage not enclosed by the two sets of chopping blocks. However, these devices are large and contribute a small percentage of the $1/f$ noise.

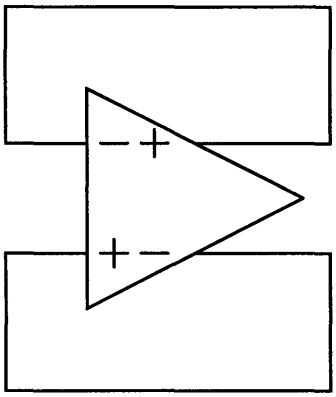

Figure 4-7: Amplifier configuration for noise analysis

4.5.3 Summary

Table 4.1 summarizes the performance of the amplifier with and without chopper modulation. As expected, the AC characteristics are identical and the signal-to-noise ratio has a 7dB improvement. The total harmonic distortion worsened by 13dB. However, it exceeds the minimum requirement of -85dB.

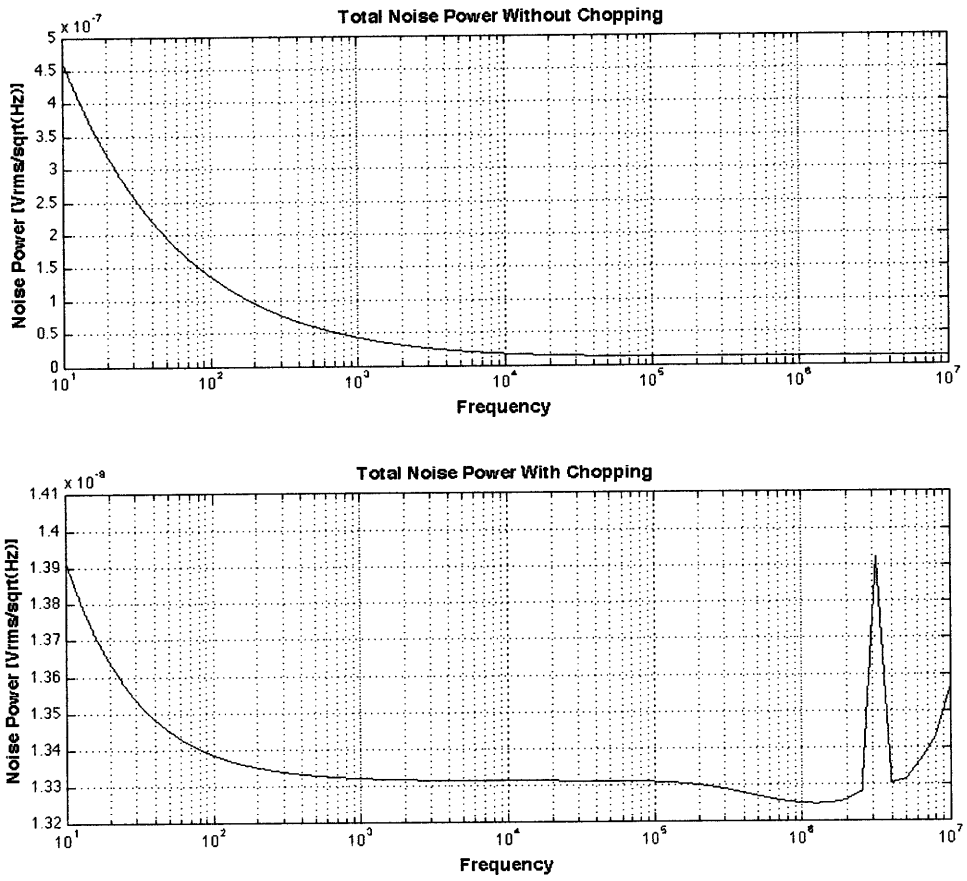

Figure 4-8: Noise spectrum for the differential amplifier. (a) The noise spectrum without chopping shows a clear $1/f$ noise and white noise. (b) Chopping results in a reduction of $1/f$ noise by two orders of magnitude. A spike in noise is seen around 3.2MHz due to the noise shifting.

Table 4.1: Fully-Differential Amplifier Performance

Spec	No Chopping	With Chopping
Diff Gain	76.8 dB	76.8 dB
CM Gain	77.8 dB	77.8 dB
UGF	33.8 MHz	33.8 MHz
PM	48.7°	48.7°
GM	6.23 dB	6.23 dB
Power	0.64 mW	0.64 mW
THD	-100.94 dB	-87.3 dB
SNR	-101.58 dB	-108.32 dB

Chapter 5

Design Validation

The amplifier discussed in Chapter 4 will be part of the analog back end for a three-level sigma-delta audio DAC. The back-end includes the current steering DAC, inverter stage, active filter, and line drivers for the outputs. A system level validation is used to determine the amplifier's performance relative to the ADAU1361. Chapter 4 proved that a fully-differential chopping amplifier will improve the SNR by 11dB. The system level simulation will be used to compare the harmonic distortion of the two designs.

The hold switches described in Chapter 1 filter the oscillations while the chopping switches settle since the output voltage will be held on the feedback capacitors. Harmonic distortion of the system will not be as dependent on the THD of the amplifier seen in the previous chapter as the SNR, which is directly related to the SNR of the system.

5.1 System Overview

Design of the analog back-end of the DAC created for this thesis can be seen below in Figure 5-1. The current steering portion decodes the digital input into a differential signal. Current steering is achieved through the use of two current sources. These sources can push current into or pull current from the input of the integrator. A null input is also available to create the third level of the DAC.

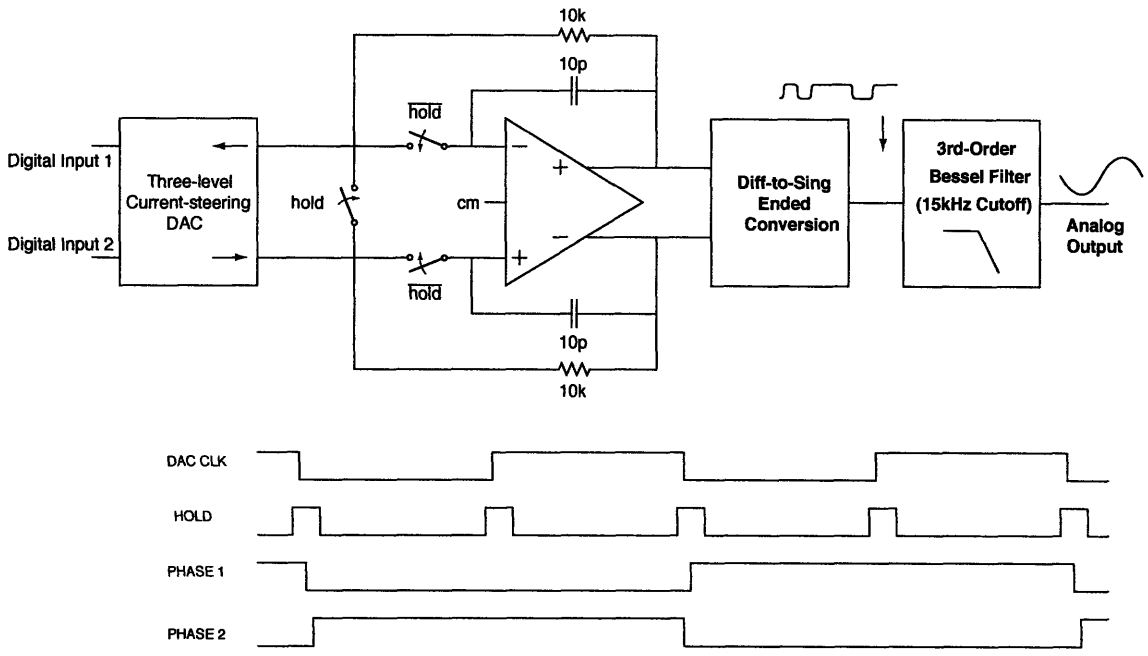

Figure 5-1: Analog back-end for the digital-to-analog converter

Two hold switches before the op-amp disconnect the current steering DAC during transitions. These give the DAC 20ns to settle before it is reconnected. The previous value is held on the feedback capacitors. During this period, the chopping switches change the signal path. The output of the chopper should also settle before the hold switches open. A major problem with a continuous-time output stage is that it suffers from errors caused by mismatches in rise and fall time. If there is a mismatch, the area under the sequence of bits will depend on the order of bits [1]. This intersymbol interference is reduced by the hold switches; allowing the slow current-steering DAC to settle before integration eliminates the errors from mismatched rise and fall times.

The inverter stage contains a single pole lowpass filter with a high cutoff frequency. This filter prevents the active filter later from seeing full steps at the clock frequency. Full steps cause errors due to the non-linear settling time of op-amps [1]. After the op-amp, the signal is converted from differential to single ended. The conversion uses the single ended chopping amplifiers seen in Chapter 3. Finally, a third order Bessel filter with a cutoff frequency of 15kHz filters the sigma-delta modulation leaving only the analog output.

The DAC used in comparison with this design, the ADAU1361, implements a

similar topology. However instead of using a differential-to-single ended conversion, it drops the negative output. As seen in Chapter 2, chopping can not be used when only one output is taken from a fully-differential amplifier. Dropping an output also wastes the benefit of the good common mode noise rejection of a differential output. The ADAU1361's inverter amplifier requires a very fast common-mode correction to ensure linearly over the three levels of the DAC. Common-mode correction resolves non-linearity caused by drifting current sources. This error is not present when a differential output is taken at all times. The new system topology does not require a fast common-mode correction and uses much less current because the correction speed can be much slower.

5.2 Performance Comparison

For the testing of the analog back end, both the ADAU1361 and the improved design were placed in their respective topologies. The same values where used for the cutoff of the frequencies. A three level digital input for a 2 kHz sine wave is applied to the current steering stage.

The distortion between the two designs are very similar. As seen in the previous two chapters, oscillations during switch settling increases harmonic distortion for chopping amplifiers. These oscillations are on the order of 500kHz and are easily filtered by the Bessel filter with a cutoff filter of 15kHz.

Table 5.1: System Performance Comparison

Spec	ADAU1361	New Design
THD	-35.96 dB	-38.72 dB
SNR	-97 dB	-108.32 dB
Power	1.17 mW	1.39 mW

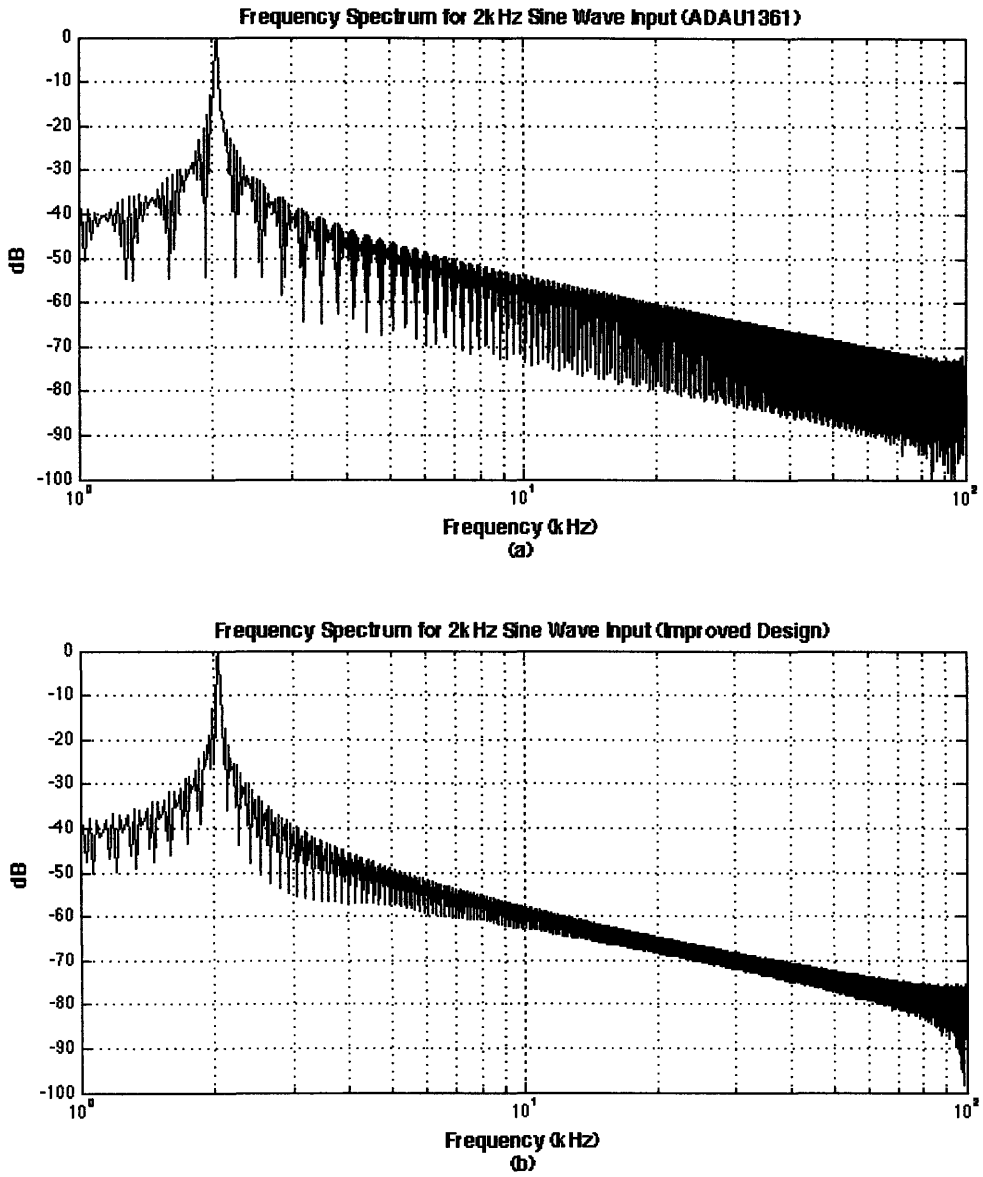

Figure 5-2: Frequency Spectrum for 2kHz Input. (a) Signal spectrum from the ADAU1361. (b) Signal spectrum for the proposed design.

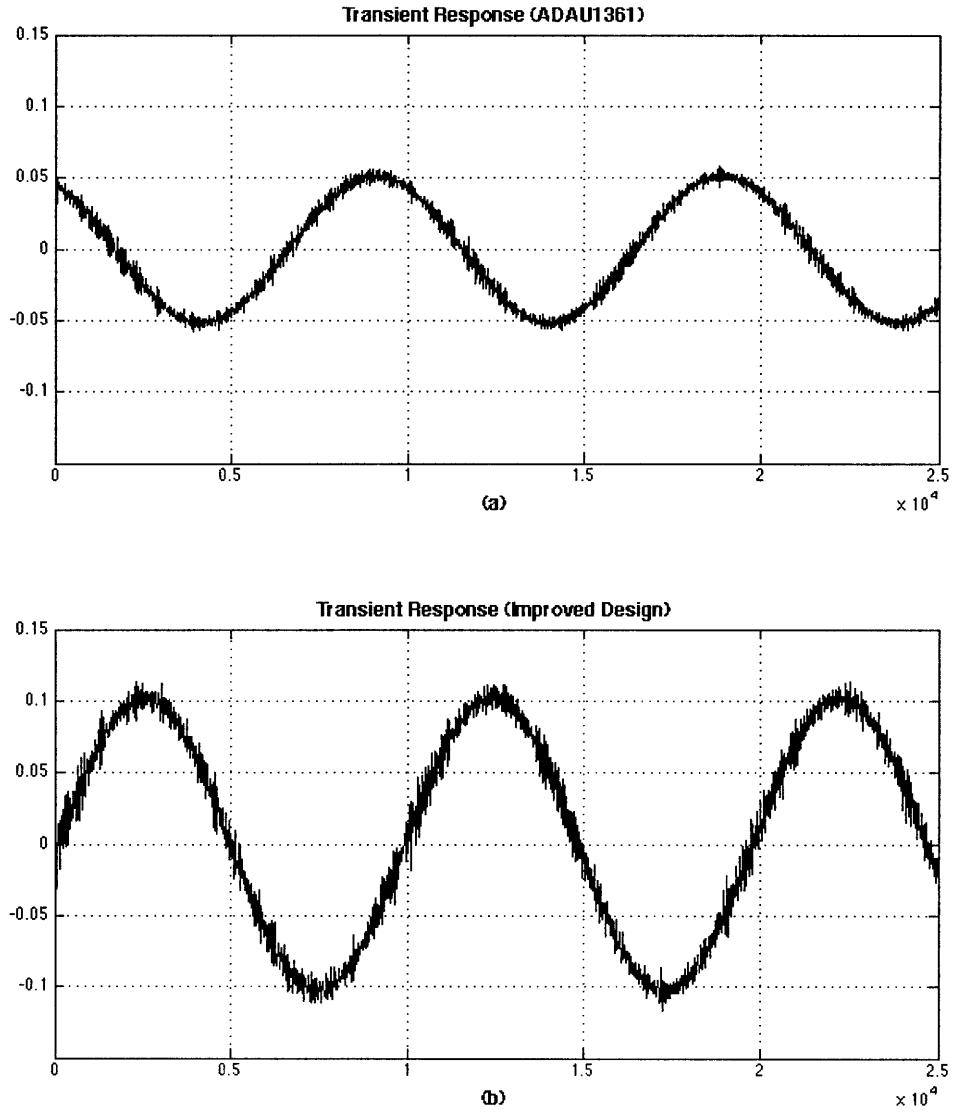

Figure 5-3: Transient Output for the DAC System. (a) Analog output from the ADAU1361. (b) Analog output from the proposed design. The signal magnitude is twice the magnitude of the ADAU1361 due to the differential-to-signal ended conversion.

Chapter 6

Conclusions

Low noise, low power circuits can benefit from the addition of chopper stabilization. At low voltage supplies, chopper modulation can effectively reduce noise levels without requiring extra bias current. This modulation technique was chosen to avoid aliasing of the amplifier broad-band noise and eliminate $1/f$ noise from the major contributors. However, modulation cannot be applied to all amplifier topologies. As seen in the baseline comparison, attempting modulation led to noise sampling and no net benefit with chopping.

To minimize the contribution of $1/f$ noise and allow for clean filtering without a very high order filter, the modulation frequency must be much greater than the sum of the signal band and the corner frequency. For the designed DAC, the chopping frequency of 3.2MHz is much larger than both the 20kHz signal range and the 10kHz corner frequency. Within the stand-alone amplifier, switching the signal caused oscillations during settling. In order to minimize the noise from charge injection and settling, the switches were designed to settle within 20ns, the length of the hold period for the DAC. These oscillations caused a large increase in the harmonic distortion of the amplifier. However when combined with an aggressive filter, the 500kHz oscillations were removed and the system level simulations showed no significant increase in distortion.

With the addition of chopping, the SNR improved by 7dB and the system level distortion was the same as the baseline comparison. A differential output from the

inverter stage keeps linearity without the need for a fast common mode feedback.

6.1 Future Research

As seen in Chapter 3, current chopping has better noise and distortion performance over voltage chopping. The differential amplifier used voltage chopping for simplicity: the timing circuitry is easier to create and there is no risk of crashing bias points during the non-overlap period. However, applying current chopping would result in better performance.

The DAC system uses a differential current steering decoder for the digital signal. This requires a fully-differential amplifier using twice as much current as the single-ended amplifier and a differential-to-single ended conversion stage. The system can be improved with a topology that uses only single-ended amplifiers while keeping linearity over the three level sigma-delta code. There is potential for the analog back-end to use significantly less current and have similar noise performance.

Bibliography

[1] Robert Adams, Khiem Nguyen, and Karl Sweetland. A 113-dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling. *IEEE Journal of Solid-State Circuits*, 33(12):1871–1878, December 1998.

[2] Christian Enz and Gabor C. Temes. Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization. *Proceedings of the IEEE*, 84(11):1584–1614, November 1996.

[3] Christian Enz, Eric Vittoz, and Franois Krummenacher. A CMOS Chopper Amplifier. *IEEE Journal of Solid-State Circuits*, 22(3):335–342, June 1987.

[4] Paul Gray, Paul Hurst, Stephen Lewis, and Robert Meyer. *Analysis and Design of Analog Integrated Circuits.* John Wiley and Sons, Inc, New York, fourth edition, 2001.

[5] David Johns and Ken Martin. *Analog Integrated Circuit Design.* John Wiley and Sons, Inc, Crawfordsville, Indiana, first edition, 1997.

[6] Eric Klumperink, Sander Gierkink, Arnoud van der Wel, and Bram Nauta. Reducing MOSFET $1/f$ Noise and Power Consumption by Switched Biasing. *IEEE Journal of Solid-State Circuits*, 35(7):994–1001, July 2000.

[7] Mihai A.T. Sanduleanu and A.J.M. van Tuijl. *Power Trade-offs and Low-power in Analog CMOS ICs.* Springer, Boston, Massachusetts, first edition, 2002.

[8] Mihai A.T. Sanduleanu, A.J.M. van Tuijl, R.F. Wassenaar, M.C. Lammers, and H. Wallinga. A low noise, low residual offset, chopped amplifier for mixed level applications. *IEEE Conference Proceeding*, 2:333–336, September 1998.

[9] Takeshi Yoshida, Yoshihiro Masui, Takayuki Mashimo, Mamoru Sasaki, and Atsushi Iwata. A 1V Supply 50nV/Hz Noise PSD CMOS Amplifier Using Noise Reduction Technique of Autozeroing and Chopper Stabilization. *IEEE Symposium of VLSI Circuits Digest of Technical Papers*, 2005.

[10] Takeshi Yoshida, Yoshihiro Masui, Mamoru Sasaki, and Atsushi Iwata. Low-Noise and Low-Voltage Circuit Techniques for CMOS Analog Design. *5th COE Workshop Proceeding*, 2005.