A Locally-Adaptive Imager

by

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Abstract

A high–performance imager suitable to be fabricated in a digital CMOS process is described. The design implements a column–parallel architecture, where each column of the pixel array has a dedicated analog–to–digital converter. Due to this added parallelism, slower ADCs can be used while still maintaining a significant frame rate.

Due to the large number of converters, the individual units need to have a tight layout pitch, occupy a small area and dissipate very little power. Moreover, these converters have to be accurately matched to avoid fixed pattern noise, a phenomenon that can occur if the signals of two or more pixels that receive the same light intensity are digitized to different binary combinations. These special requirements are addressed with a novel current–mode dual–slope distributed converter. This system is made of shared blocks that dissipate the most power and ultra–low power pseudo–converters that are present in all the columns of the imager. The matching issue is solved using switched–current cells to generate a precise reference current for each pseudo–converter. An active pixel with five PMOS transistors collects the photogenerated charge and delivers it to the converters as a current signal.

The imager response can be adapted locally depending on the light intensity distribution by modulating the clock frequency of a digital counter on a row–by–row basis. This process changes the shape of the converter array transfer characteristic, and thus several companding options can be obtained with different modulating functions.

The design and layout of a prototype ASIC is presented. The imager has a spatial resolution of 128 rows and 8 columns, the sensing array can be read 80 times per second and the pixel currents are digitized to 8 bits using the distributed converter previously described. The chip is designed for the Hewlett–Packard 0.5μm CMOS process that is offered through MOSIS.

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Pablo M. Acosta Serafini

August 28, 1997

Dedication

To my family

A mi familia

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Chapter 1

Introduction

1.1 Motivation

Solid–state imaging systems have been in service for a number of years in such high–tech devices as medical instruments, satellites and telescopes. Perhaps aided by the increasing popularity of personal computers and the Internet, the spotlight is now shifting to imagers in more "mainstream" applications like digital cameras, camcorders and scanners which, for the most part, are expected to follow the same cheaper/better paradigm that is so ubiquitous in the computer industry.

Since 1970 an array of charge–coupled devices (CCDs) [1] is the preferred way of building solid–state image sensors. Three decades of research in CCD technology have helped to overcome many of their initial technical problems, and as a consequence, CCD imagers nowadays have excellent spatial resolution, low noise and high light intensity resolution, so it seems fair to predict that these systems will continue to improve its performance thus meeting the demand for better products.

In spite of this positive perspective, some technical problems arise if CCD imagers are expected to dramatically improve their level of integration, cost and power dissipation. The main obstacle is that CCDs require at least two polysilicon layers and a buried–channel implant to achieve their high performance, and unfortunately these features cannot be found in standard CMOS fabrication processes. The consequences of this are twofold: first,

the manufacturing costs are higher because special fabrication processes are needed; and second, the level of integration that can be achieved in imagers is low because CCD processes generally do not include PMOS devices and because the NMOS transistors available are mostly of the depletion–mode type. Besides this lack of suitable devices, CCDs have an additional problem that diminishes their ability to achieve high levels of integration. As Geppert says,

> Most solid–state cameras now available use charged–coupled devices (CCDs) as image sensors. But the large capacitances of these devices hinder their integration with drive and image–processing circuits [2].

The currents associated with charging and discharging these capacitances are usually very significant, so CCDs are not particularly well suited for portable or battery–operated systems. In recent years CMOS technology has appeared as an alternative imaging solution that could present competitive advantages with respect to CCDs in specific areas. Certainly there are several categories in which CMOS imagers still have a significantly poorer performance than CCDs, but unquestionably CMOS technology can achieve such high levels of integration that a camera–on–a–chip is no longer a utopian goal belonging to a technology roadmap, but rather a certain design alternative. The 1996 IEEE Spectrum Technology Report confirms this observation:

> As line widths and other lithographic features of ICs shrink, and the number of transistors on a chip mushrooms, functions galore are being combined on a single die. The ultimate result of this trend will be the system–on–a–chip, in which all circuitry –for a computer, a cellular phone, a microelectomechanical actuator, or a *solid–state camera*– will be housed within a couple of square centimeters of silicon [...] Among the numerous devices riding the wave of integration are new image sensors that can be fabricated with "vanilla" CMOS. This technology will enable ICs to be built that contain the sensor array, analog–to–digital conversion, image processing, and other circuits required for still and video imaging [2].

In fact the first CMOS cameras–on–a–chip have already reached the marketplace; for example, the VM5402 module from VLSI Vision Ltd. [3] only needs a 9V input and some external passive components to produce a video output. There are also substantial cost savings that appear when standard CMOS fabrication processes can be used:

> The low cost of CMOS imagers derives from the *assumption* that the cost of technology development will have been amortized by the huge sales volume of "standard" CMOS logic and memory chips (for which the technology is developed) [4].

Other characteristics that can be expected from CMOS imagers include a good dynamic range, single power supply operation, easier implementation of an electronic shutter, low power dissipation and better radiation resistance than CCDs [5]. It is clear then that the main advantages of CMOS imagers are the following [5]:

- Production of highly miniaturized, low cost imaging systems.
- System power savings of 100x–1000x through on–chip integration.
- Integration of full digital interface that reduces system design time and improves reliability.
- Possibility of having window-of-interest readout and random access with faster frame rates.

These features make CMOS imagers particularly attractive for several applications such as industrial inspection systems, video phones, surveillance cameras and smart car navigation systems [5].

1.2 Imager Characteristics

The following is not a comprehensive list of imager characteristics but rather a review of the key features that illustrate the differences between the CCD and CMOS technologies.

These features are:

- Addressability: Random or sequential access. CCDs operate like an analog shift register, so they can only be read serially and the access time depends on the position of the pixel that needs to be read in the sensing array. On the contrary, CMOS imagers are very similar to random access memories (RAMs) in that it is possible to read any pixel in the sensing array with the same access time regardless of its location.

- Fill Factor: This metric is defined as the ratio between the photoactive area and the total pixel area [6]. The fill factor of CCD imagers depend greatly on their architecture but they go from about 40% for interline transfer (IT) imagers to nearly 100% for frame transfer (FT) imagers [7], where the sensing element also performs gating functions. On the other hand, the charge–output pixel is the design with the highest fill factor among CMOS imagers because it only requires a single transistor besides the photodiode but still its fill factor is only about 40% [8].

- Frame Rate: One of the most important features of an imager; it indicates how many times per second is possible to read the pixel array. Here CMOS imagers have a definite advantage over CCDs because of their random access nature, a feature that can be used to trade spatial resolution for frame rate; that is to say, it is possible to read only a window of interest in the sensing array at a rate significantly higher that the nominal frame rate of the imager.

- Light Intensity Resolution: The resolution of the converter(s) used to digitize the signals coming from the pixels, which can be thought of as dependent on the dynamic range of the system. State–of–the–art CCDs have noise levels of 3 e^- r.m.s. for full wells on the order of 200,000 e^- [9], while CMOS imagers have noise levels of about 13 e^- r.m.s. for comparable wells [5], so CCDs typically have a much higher signal–to–noise ratio (SNR) that CMOS imagers.

- Power Dissipation: One of the main advantages of the CMOS imagers is that it is possible to integrate the sensing array with the conversion, driving and digital processing

blocks. CCDs have recently achieved medium to high integration levels with specialized 5V CMOS/CCD processes that feature the buried channel capacitors used in the imager *and* the enhanced MOS devices used in the regular circuits [10]; however, these processes are expensive and there is still the need to supply large currents to the power electronics that drive the CCD capacitances. The CMOS imager architecture does not have any significant power block. The sensing array can be designed to operate with the same power supplies that the digital blocks use, nowadays 3.3 V or 2.5 V. Consequently the pure CMOS technology has an advantage in terms of power dissipation, both because of its lower voltage and current requirements and because the higher level of integration eliminates the need to drive the external pins and board capacitances present in multi–chip designs.

1.3 Sample Imager Applications

Solid–state imagers can be used in a variety of applications and each of them has different performance requirements, as proven by the three representative cases shown in Figure 1.1.

The first application is camcorders and other consumer electronics. Here the light intensity resolution is usually 8 bits per primary color to give the camera TrueColor capabilities, so these systems use analog–to–digital converters (ADCs) that are in the medium range of the resolution spectrum. The frame rate for these devices is around 30 $\frac{frames}{second}$ which is well above the roll-off frequency of the human eye but still in the medium range of frame rates. One particular characteristic of camcorders is that they usually have three imagers, so that with the aid of a dichroic prism it is possible to capture color images with excellent SNR and without color register problems [11]. However, this parallelism adds a new constraint to the imager, namely that they should be small to fit in the constantly shrinking volumes of new camcorders.

The second representative application is iris scanning, one of the new biometrics for personal identification [12]. It was found by Leonard Flom and Aram Safir that the iris, the colored disk that surrounds the pupil of the eye, is a richly detailed and unique texture that

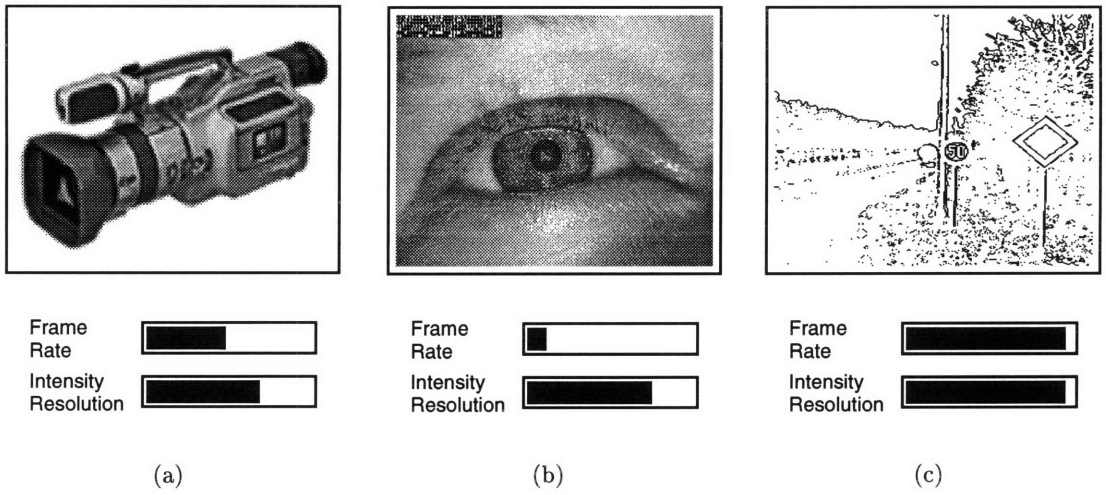


Figure 1.1: Sample applications of solid–state imagers and their requirements. (a) Camcorders and other consumer electronics, (b) iris scanning for personal identification and (c) machine vision.

stays remarkably stable over time [13]. Several commercial systems that use this discovery capture the iris with an imager to subsequently apply sophisticated pattern recognition algorithms to match the acquired image with the ones they have in storage. This procedure is so reliable that some manufacturers claim that the odds of an identification error is less than 1 in 10^{34} [14]. The accuracy of these systems rely on the recognition algorithms which in turn rely heavily on images with high intensity resolution (16 bits or more). On the contrary, the requirements in terms of frame rate are very lax as the systems usually take one still shot per person.

1.4 Machine Vision Requirements

Perhaps the most demanding and challenging application for imagers is machine vision because it usually requires both high frame rate and high light intensity resolution, a condition that puts the ADCs under a severe strain.

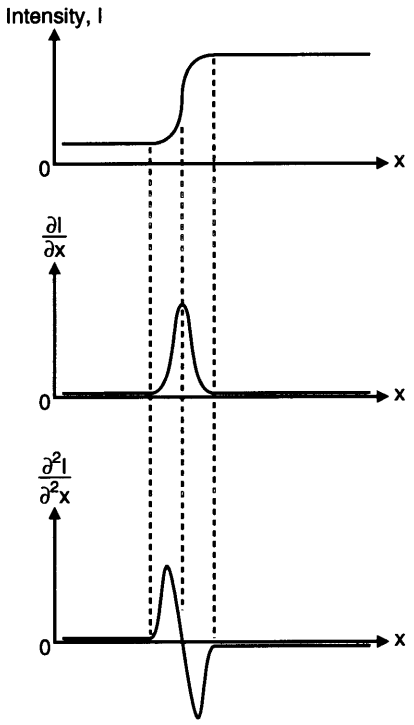


Figure 1.2: Machine vision technique for edge detection. x is a distance along a path perpendicular to the edge.

1.4.1 High Light Intensity Resolution

High light intensity resolution is needed for several reasons. It is obvious that the more detail an image has, the better, because then it would be possible to compare objects using information on their surface characteristics such as texture, color or surface orientation, which manifest themselves in subtle changes in light intensity distribution [15]. Also both spatial *and* light intensity resolution are key factors in several low–level image processing tasks such as edge detection, median filtering, segmentation and smoothing.

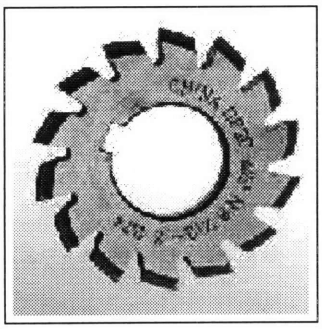
In the following edge detection will be taken as a case example. Figure 1.2 shows the standard technique used to detect edges in an image. The idea behind it is that edges are translated into abrupt changes in brightness; consequently they can be detected by taking the first two derivatives of the intensity function along a path perpendicular to the edge

(the variable x in Figure 1.2). If this is done, the edge is located where the first derivate of the intensity function experiences a maximum and where the second derivative is null [16]. There are several methods than can be used to implement this technique, as linear matched filtering, non–linear filtering, local thresholding and surface fitting; but the important point is that the light intensity resolution can dramatically alter the slope of the intensity function so that the location of the edge, as a machine understands it, can change significantly. Figure 1.3 confirms this fact; in this case two Sobel edge detections[1] were performed on an image, first on a version with 256 gray levels, and then on a version with 4 gray levels. The resulting images were combined (logic XOR operation) to show only the pixels in which they differ and as Figure 1.3 (e) shows, there is a noticeable disparity between the two. It can also be seen that the image with 4 gray levels seems to have new edges, a phenomenon that is always present when the number of intensity levels is reduced as signal–dependent quantization noise begins to appear in the form of false contours [17].

It is clear then that there is an intimate relationship between the precision of image processing algorithms and intensity resolution, this is why machine vision applications require high–resolution converters to digitize the signals coming from the sensing array. There are other "fringe" benefits of high light intensity resolutions; for example, aliasing issues are reduced when doing line detections, as E. R. Davies notes:

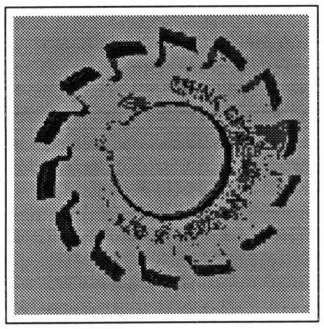
> The intrinsic error of the Sobel operator is about 1°: thus image noise will generally be the main cause of inaccuracy. In this respect, it should be noted that many mechanical components possess edges that are straight to a very high precision and that if each pixel of the image is quantized into at least 8 bits (256 gray levels), the aliasing problems are minimized and the ground is laid for accurate line transforms [18].

[1] The Sobel operator is a popular mathematical kernel that can be convolved with an image to detect edges.

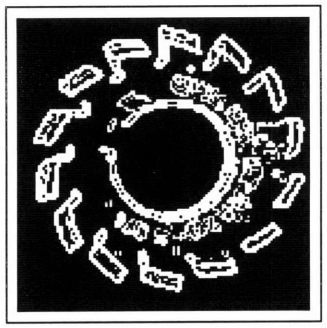


(a) Image "A": 256 gray levels.

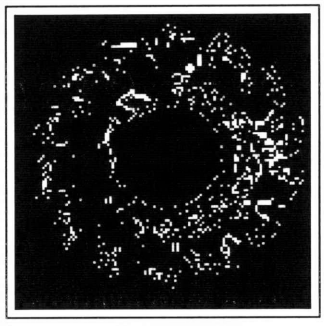
(b) Sobel edge detection of image "A".



(c) Image "B": 4 gray levels.



(d) Sobel edge detection of image "B".



(e) Difference between the two edge detections.

Figure 1.3: Light intensity resolution influence in edge detection algorithms.

1.4.2 High Frame Rate

Machines are usually deployed to control processes or situations that have an inherent high speed. One good example of this is industrial applications for inspection where containers (cans and bottles, for example) could be checked to measure certain parameters or to find irregularities, such as missing labels or damaged caps [16].

When these containers go in a conveyor belt at high speeds, a fast sampling system is needed to get all the information that is required and to avoid missing the inspection of one or several of the containers.

Other applications where imagers with a high frame rate are needed include the following [16]:

- Button inspection for the correct number of holes.
- Golf ball label inspection.
- Dust detection of LSI substrates.
- IC chip wire bonding.
- Adaptive cruise control for automobiles.

1.4.3 Brightness Adaptation

A very well–known problem in the imaging field is that the level of detail of an image –or a certain area within an image– is tightly related to the illumination it receives; that is to say, it is very difficult for either a human being or a machine to extract any significant amount of information (shapes, textures, etc.) when an image is very brightly or dimly illuminated. It should be noted that software solutions cannot be applied to mitigate this problem mainly because of the speed that is required; for example, no computer can perform brightness adaptation of a fairly large picture and still be able to display it in real time.

Consequently the problem has to be addressed in the imager, and one excellent solution is to compress or "compand" the transfer characteristic of the imager (the digital code vs. light intensity curve).

Figure 1.4 shows an image which is somewhat dark, the resulting edge detection and the transfer characteristic of an imager that could have been used to take the picture.[2] As it can be seen this characteristic is linear, thus imagers that have this response are called "linear imagers".

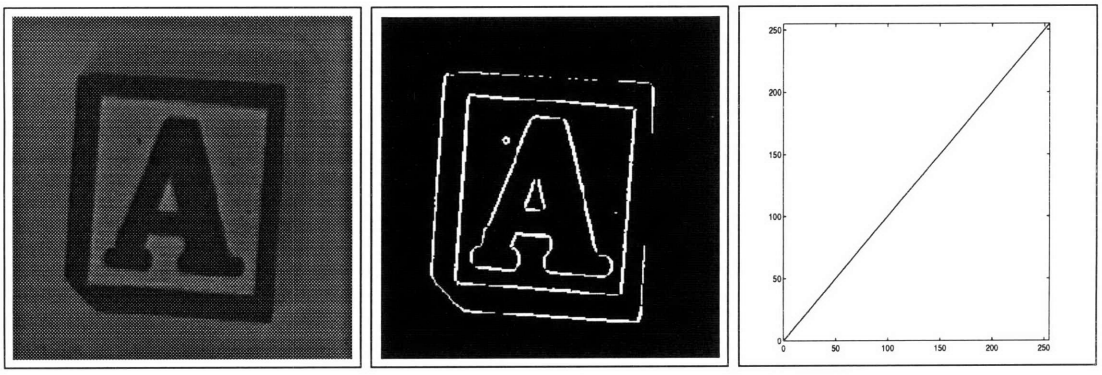
It is possible to improve the results of the edge detection by changing the shape of the imager transfer characteristic. Figure 1.5 shows the results that could be expected if the same original scene was captured using a hyperbolic transfer characteristic. Figure 1.5 (a) is noticeably brighter but it still maintains the level of detail and the general contrast of the image is better, as proved by the edge detection. It is important to note that in contrast to Figure 1.4 (b), the edges in Figure 1.5 (b) are wider and the shapes of the objects in the image are complete.

Using the same transfer characteristic for the entire scene is not always the right solution. There are circumstances, like those exemplified by Figure 1.6, where only an area of the image receives a very bright illumination. As it can be seen in the resulting edge detection, nearly all the information within the circle is lost.

In this situation the possibility of adapting the imager response locally is very desirable. For example, if an imager could use the transfer characteristic shown in Figure 1.7 (c) *only within the circle*, the intensity difference between the brightly illuminated spot and the rest of the picture would be softened, as shown by Figure 1.7 (b). The edge detection now reveals the information inside the bright spot because the localized transfer characteristic does not reach the full scale of the digital codes, in this way bright colors are imaged darker. Also, as the slope of the characteristic for bright colors is steeper than the linear option, there is an increased sensitivity for that intensity range which translates into a region with higher contrast and better color differentiation.

It should be clear now that the ideal situation would be to have an imager which can adapt its response (change its transfer characteristic) on a pixel–by–pixel basis according to the light intensity it receives. Such a system would capture images with excellent brightness

[2]The original images in this section were not taken with different imagers, they are computer–processed versions of the image shown in Figure 1.4 (a). However, they should closely resemble the results that could be obtained with imagers that have transfer characteristics similar to the ones displayed beside each figure.

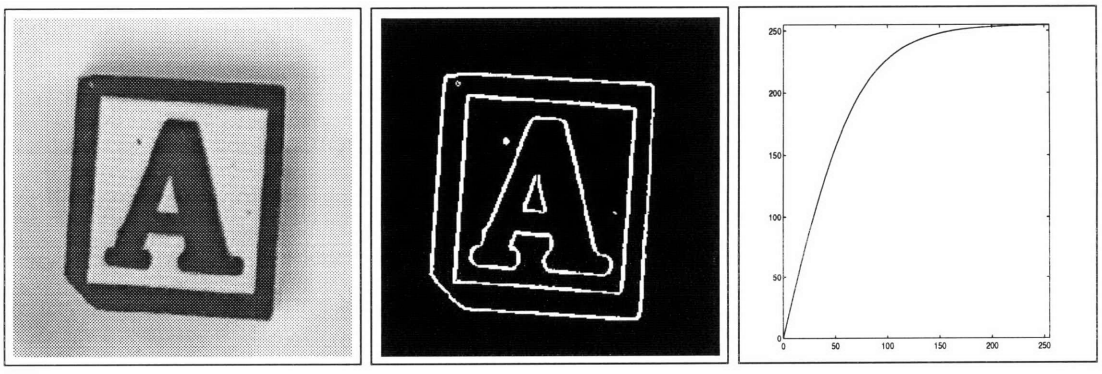


(a) Original image.

(b) Sobel edge detection.

(c) Digital code (y) vs. light intensity (x) curve of the imager.

Figure 1.4: Imaging with a linear transfer characteristic.

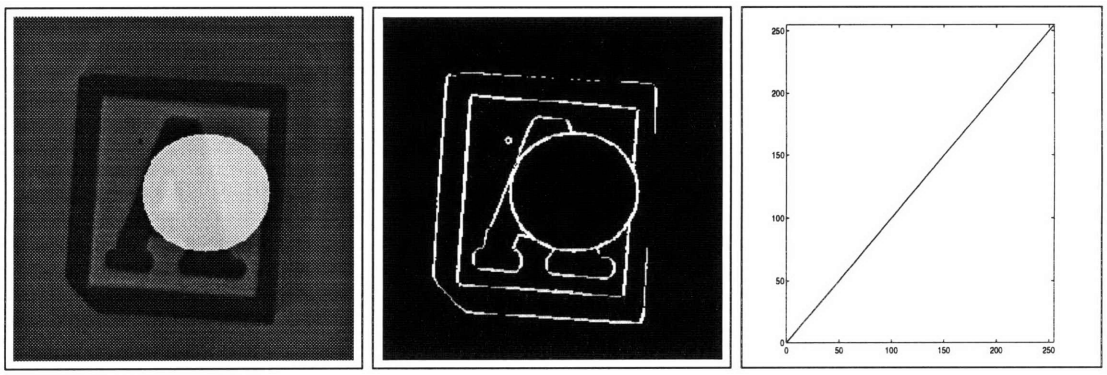


(a) Original image.

(b) Sobel edge detection.

(c) Digital code (y) vs. light intensity (x) curve of the imager.

Figure 1.5: Imaging with a hyperbolic tangent transfer characteristic.

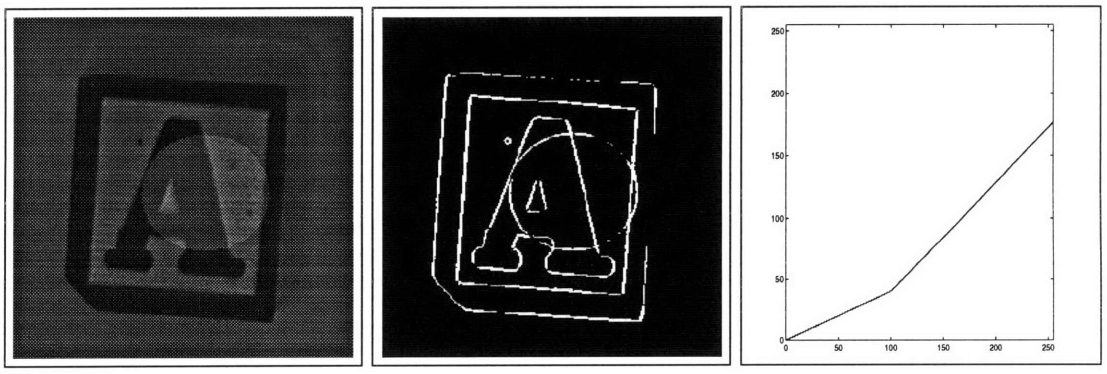


(a) Original image.

(b) Sobel edge detection.

(c) Digital code (y) vs. light intensity (x) curve of the imager.

Figure 1.6: Image with a brightly illuminated area.



(a) Original image.

(b) Sobel edge detection.

(c) Localized digital code (y) vs. light intensity (x) curve of the imager.

Figure 1.7: Image with a localized transfer characteristic adaptation.

balance and contrast regardless of the lighting conditions.

1.5 Imager Requirements for a Converter Array

Even though the immediate use of the imager to be designed is machine vision, it is important to consider the field of *human* vision for two reasons: one, because it gives the project more flexibility as in the long run new applications may appear; and two, because as it will be seen shortly, human vision poses particular requirements that can also improve the precision of machine vision algorithms.

Several studies report that the human eye is particularly deft in detecting edges from which shapes are determined [19]–[20]. Zusne describes the process of human vision as one divided in three hierarchies: at the bottom are the pixel and *edge* elements, the next level of complexity involves contours (shapes), and finally the last level of the hierarchy involves collecting the contours, region and edges to model objects [21]. McCafferty calls this *perceptual organization*:

> The term perceptual organization refers to the human visual system's capacity for detecting groupings and structures in images. It involves the partitioning of the image and findings of associations among the various parts based on some general set of criteria [...] such as similarity and proximity. It is generally hypothesized, by Biederman (1987) for example, that these groupings are used as individual and separate stimuli input to object recognition and image interpretation processes. In terms of the processing involved, one can envisage perceptual organization groupings being used to initiate object recognition procedures and to reduce the search space of all possible interpretations [20].

The imager then should not introduce distortions that could in any way alter the edges in the image, as these elements are placed at the very base of the human vision system. Furthermore, new theories support the idea that even small distortions could introduce great errors in the end result, the perceived image. The current perceptual organization research detected that the human eye also performs *shape completion.* An example of this

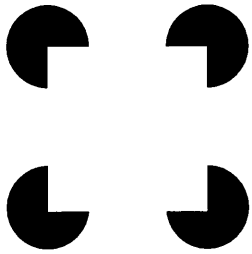


Figure 1.8: Example of the shape completion phenomenon.

can be seen in Figure 1.8 where the eye perceives a square lying with its corners in four circles rather than four independent, partial circles. The eye is said to create *virtual lines*, so distortions in the imager could either produce or modify these lines and consequently cause an error in the perception of an image.

It should be apparent by now that a good imager for human vision is also a good imager for machine vision and vice versa, because the same distortions that can lead a human being to misinterpret forms and shapes can also create false contours that could cause errors in crucial low level image processing tasks such as edge detection and segmentation.

1.6 Thesis Goal

This thesis is part of the project "Cost–Effective Hybrid Vision Systems for Intelligent Highway Applications" that is being carried by MIT with the funding of the National Science Foundation (NSF) [22]. The mission of the project is to "develop new cost–effective architectures for vision systems and to evaluate them for intelligent highway applications".

The goal of this thesis is to design an imager that could be used as the sensing element of the several systems the project calls for, like the smart camera for time–to–collision measurements (for collision avoidance), or the smart camera for three dimensional measurements (for adaptive cruise control); consequently the imager to be designed should have the characteristics enumerated in Table 1.1.

It is also very important to develop a scalable design; the key point of the Intelligent

Table 1.1
Required characteristics of the imager to be designed

Desired Characteristic	Design Specification
Medium/high light intensity resolution	8 bit converters
High frame rate (> 30 frames/sec)	80 frames/sec
Medium/high spatial resolution	1024 pixels
Local companding feature	Row–by–row companding

Highway project is to provide *cost–effective* solutions, so the imager has to be able to reduce its metrics (silicon area, frame rate, intensity resolution, etc.) if the application can tolerate a poorer imager performance.

1.7 Thesis Organization

This introductory chapter outlined the increasing importance of imaging solutions in real–world applications. It also gave a brief overview of the imager field, where there is a well–established CCD technology that produces fine solid–state image sensors and an emerging CMOS technology that is becoming a competitive choice in certain scenarios. After going over the main characteristics of the imagers, the unique requirements of machine vision applications were reviewed. Finally, the MIT Intelligent Highway project was established as the frame of reference for the imager specifications.

Chapter 2 describes the imager architecture chosen from a system perspective. Two novel concepts are introduced, the current–mode dual–slope converter and the distributed converter architecture. The different sources of ADC errors are explored with an emphasis on isolating which components cause these errors and how they can be bounded or minimized. Switched–current (SI) cells are also introduced as the way of solving the converter array matching problem. Finally, the whole set of specifications for the prototype ASIC is developed.

Chapter 3 deals with the transistor–level implementation of the different blocks in the system. The circuits used to build the current–mode dual–slope ADC are presented: a

switched–current cell, a current–output PMOS pixel and a low–power comparator.

Chapter 4 describes the test structures that were introduced in the prototype ASIC as well as other associated blocks that were needed to make the system functional. A brief commentary of the final layout can also be found here.

The summary of the project is in the final chapter of the thesis, Chapter 5. Several conclusions are also presented, including an analysis of how the presented architecture may fair with new fabrication processes.

Chapter 2

System Definition

Perhaps the most challenging application for an imaging system is machine vision, because it demands both high frame rate and high light intensity resolution. Meeting these two constraints seems difficult, because analog–to–digital converters suffer from a well–known trade–off between conversion time and number of bits. To circumvent this limitation several schemes and architectures have been proposed in an imager context [23]–[25]; nevertheless very exciting times still lay ahead because the ideal solution for this problem has yet to appear.

2.1 Column–Parallel Imager Architecture

An integrated imager should include at least a sensor array and data conversion circuits. In previous years, high–resolution designs featured a single ADC as traditionally the silicon area required by the converter did not allow for more than one per die, especially when a high spatial resolution was also part of the specifications. However, custom architectures and smaller transistor features have enabled designers to fit several converters in the same package and consequently use parallelism to work around the speed–resolution trade–off; for example, Mendis and others used several Sigma–Delta converters to improve the imager readout speed [24].

It is evident that this approach solves the problem by making yet another trade–off

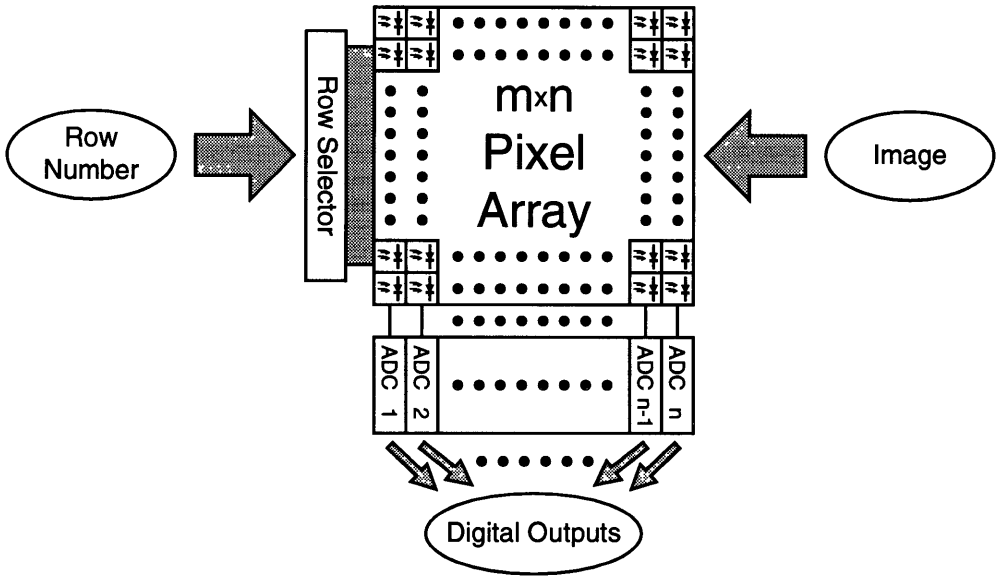


Figure 2.1: Schematic representation of a column–parallel imager with a sensing array of m rows and n columns.

between silicon real–state and speed, but this compromise is much more flexible as the design trade space is relatively flat, enabling the use of a variety of on–chip ADC architectures [25]. As E. R. Fossum says:

> It is possible to have a single ADC for the entire array operating at a high conversion rate, an ADC for each pixel operating at the frame rate, or an ADC for each column of the array. The latter architecture is referred to as column–parallel and represents a good trade of parallelism and chip area for low power [25].

The column–parallel architecture can be seen in Figure 2.1, where an imager has an analog–to–digital converter in each column so that all the pixels in a row can be read simultaneously. Consequently high resolution –albeit slow– converters can be used while still maintaining a fairly high frame rate. There is a price to pay for this good

performance: obviously there is a substantial increase in silicon area due to the added parallelism, but more importantly, the converters must have special characteristics because a large number of them is needed in imagers with practical spatial resolutions. These characteristics are:

- Small individual area, to minimize the overall area increase.
- Very small power dissipation.
- Small pitch, at least comparable to that of the pixels so that all converters can fit below the pixel array when the circuit is laid out.
- Tight matching, to avoid fixed pattern noise (FPN), a phenomenon that can occur in this system if the signals of two or more pixels that receive the same light intensity are digitized to different binary combinations.

In spite of these stringent requirements the column–parallel architecture will be used in this thesis because it provides a sound compromise between frame rate, intensity resolution and silicon area; moreover, the following sections will introduce a novel converter array that can be designed to closely match the preceding list of desirable characteristics.

2.2 A Novel Current–Mode Dual–Slope Converter

Full implementations of the column–parallel concept tend to use medium– and low–accuracy converters, mostly single–slope ADCs for their relatively small area requirement [26]. However, when higher accuracy is desired, other converter architectures come to the forefront. In this thesis, a dual–slope converter will be used because it offers good precision, robustness, and excellent component mismatch insensitivity. As it will be seen later, it also offers the promise of a very small implementation in terms of silicon area.

Figure 2.2 shows the classic circuit used to build this converter [27]. The conversion begins with the reset phase, when the capacitor C_1 is discharged by closing switch S_2. The next phase of operation is the fixed–time phase. Here the resistance R_1 performs a

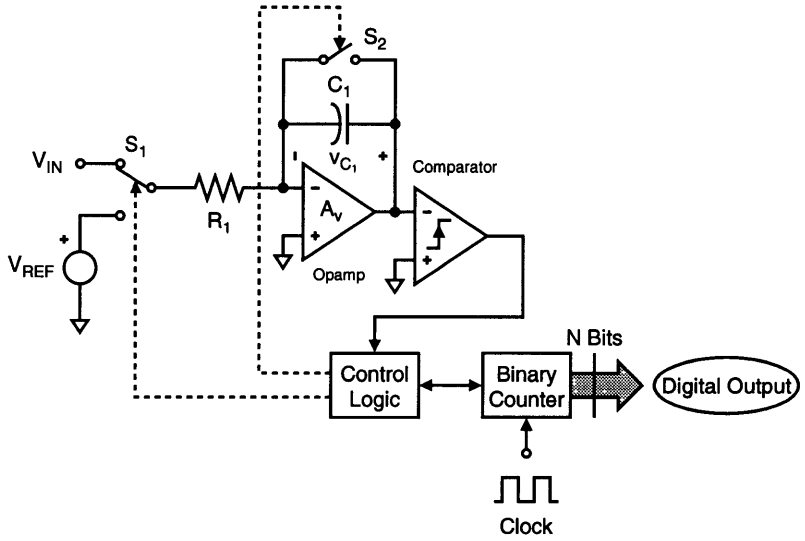


Figure 2.2: Classic implementation of a dual–slope ADC.

voltage–to–current conversion, that is to say, if the operational amplifier has a gain A_v high enough so that the inverting terminal can be considered a virtual ground, the current flowing through the resistor (and the capacitance) is:

$$i_{C_1}(t) \approx \frac{v_{IN}(t)}{R_1} \tag{2.1}$$

The current $i_{C_1}(t)$ will then charge capacitor C_1 following the relationship:

$$i_{C_1}(t) = C_1 \cdot \frac{\partial v_{C_1}(t)}{\partial t} \tag{2.2}$$

If the converter is in a sampled system, the input voltage will be constant throughout the conversion process and consequently the derivative of Equation 2.2 can be approximated by the division of differences. If $v_{C_1} = 0$ at $t_0 = 0$ the capacitor voltage will rise linearly, as dictated by Equation 2.3.

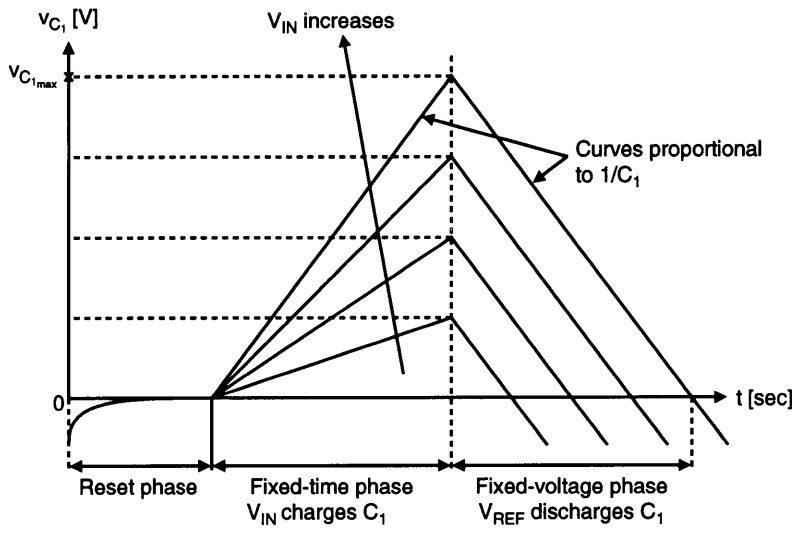


Figure 2.3: Voltage across the integrating capacitor of a voltage–mode dual–slope ADC.

$$I_{C_1} = C_1 \cdot \frac{\Delta v_{C_1}(t)}{\Delta t} = C_1 \cdot \frac{v_{C_1}(t) - v_{C_1}(t_0)}{t - t_0} \Longrightarrow v_{C_1}(t) = \left(\frac{I_{C_1}}{C_1}\right) \cdot t \tag{2.3}$$

Equation 2.3 shows that the resistor–capacitor–opamp system behaves like an integrator, and this is why the capacitor C_1 is often called the "integrating capacitor".

The phase lasts the full count of the binary counter. Once this block has reached its maximum value, the final phase of operation, the fixed–voltage phase, begins. Here capacitor C_1 is linearly discharged by the reference voltage V_{REF}, and the phase ends when the voltage across the capacitor reaches its reset value, in this example 0V. At that time the comparator indicates the end of the process by stopping the counter which then holds the result of the conversion. Figure 2.3 shows how the voltage across the capacitor C_1 evolves over time through the three phases of operation.

It should be apparent now that what this ADC really does is perform a variable voltage (v_{IN})–to–variable time (t_{var}) conversion, and then uses the counter as a discrete time base to quantize t_{var}.

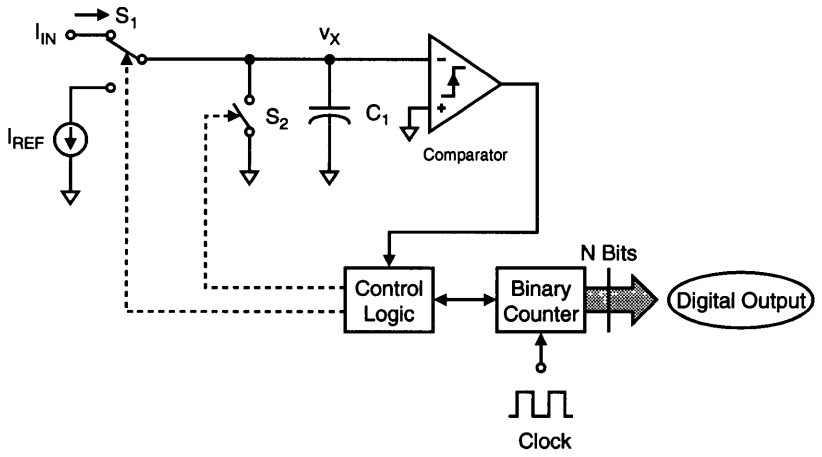


Figure 2.4: Current–mode dual–slope ADC.

The goal then is to design a smaller version of the converter depicted in Figure 2.2 so that it could fit in a full column–parallel scheme. The two components that make the voltage–mode dual–slope ADC big and power hungry are the resistor R_1 and the operational amplifier. The only reason why this integrator needs an opamp is because the signals to integrate are *voltages*... but there is no real need for this. It would be much simpler if the signals were *currents* because then, *for DC signals*, the integrator would be reduced to a single capacitor. Obviously the reference signal is always constant, but in an imager (and in fact in any sampled system), the signals coming from the pixels are also constant, so an imager–specific dual–slope ADC could be easily implemented as it is shown in Figure 2.4. Another advantage that comes with the elimination of the operational amplifier is a considerable reduction in the power dissipated by the system, this is particularly important in a column–parallel scheme because of the number of converters used and the layout density.

The implementations of Figure 2.2 and Figure 2.4 are equivalent; this can be proved by pointing out that for the proposed DC current–mode integrator

$$v_X(t) = \left(\frac{I}{C_1}\right) \cdot t \tag{2.4}$$

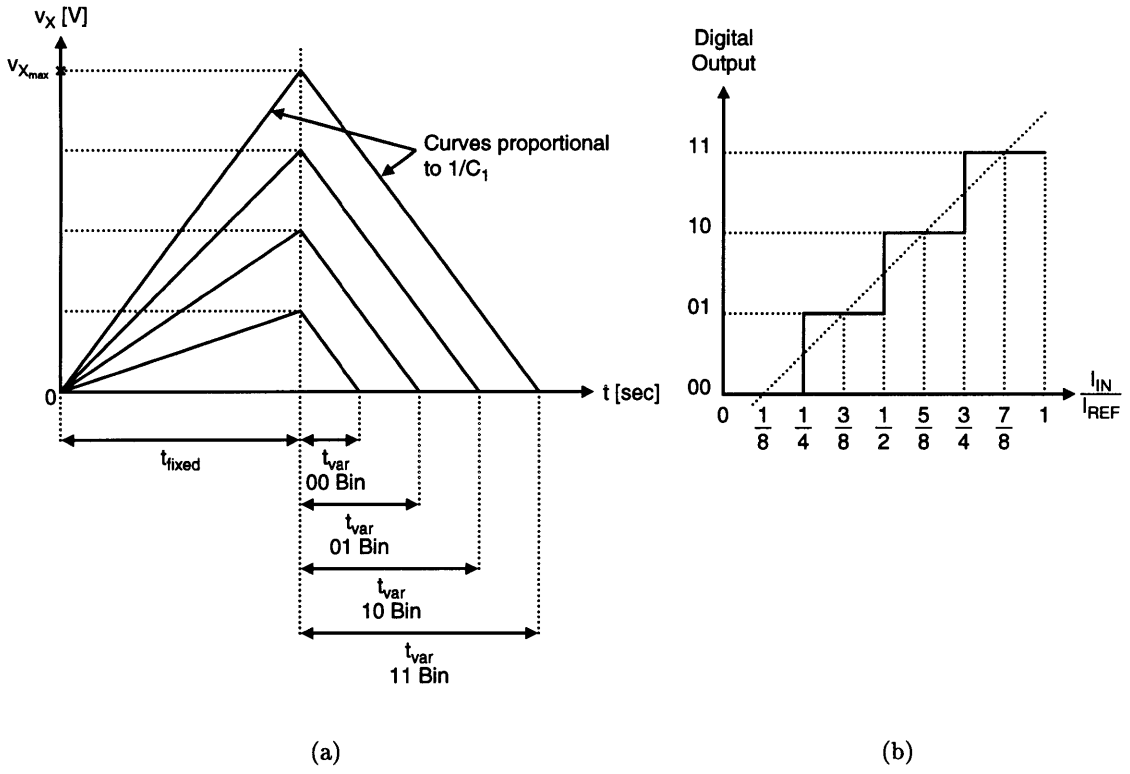


Figure 2.5: Graphic view of the conversion process in the novel dual–slope converter. (a) Voltage across the integrating capacitor C_1 and (b) converter transfer characteristic.

where v_X is the integrated signal and I, the signal to integrate, can be the current coming from the pixel or the reference current. The current–mode version of the dual–slope ADC performs a fixed–time integration with the pixel current as the integrand, and then a fixed–current integration with the reference current as the integrand just like the voltage–mode version does for v_{IN} and V_{REF}, so that the voltage waveform across the integrating capacitor remains unchanged (Figure 2.5)[1] and thus the two converters are

[1] In the following figures a two bit ADC is assumed.

Table 2.1
Notation used to describe the transfer characteristic of the ADC

Variable	Description
C_1	Integrating capacitor
V_X	Voltage across capacitor C_1
I_{PIXEL}	DC current coming from the pixel(s)
$t_{clk} = \frac{1}{f_{clk}}$	Counter clock period/frequency
t_{fixed}	Fixed–time phase duration
n	Counter bit length
t_{var}	Fixed–current phase duration
I_{REF}	Converter reference current
d	Output digital code
$IP(\cdot)$	Integer part function

equivalent from a behavioral point of view. It is useful to have a mathematical expression to describe Figure 2.5 (b). With the aid of Table 2.1, the variable integration time t_{var} and the capacitor terminal voltage V_X are given by

$$V_X = \frac{I_{PIXEL}}{C_1} \cdot t_{fixed} \Longrightarrow V_{X_{max}} = \frac{I_{REF}}{C_1} \cdot t_{fixed} \tag{2.5}$$

$$t_{var} = \frac{V_X \cdot C_1}{I_{REF}} \Longrightarrow t_{var} = \frac{I_{PIXEL}}{I_{REF}} \cdot t_{fixed} \tag{2.6}$$

Finally, after some rearranging,

$$\boxed{d = IP\left(2^n \cdot \frac{I_{PIXEL}}{I_{REF}}\right)} \tag{2.7}$$

It can be argued that in a column–parallel scheme the reference voltage source could have been shared by all the converters while the same could be more difficult to do –if not outright

impossible– with a reference current source. This would offset the area and power gains that came with the removal of the operational amplifier but only if the individual reference current sources are of comparable area. Consequently, it is necessary to explore what is the influence of the reference current source and the other blocks in the performance of the converter in order to determine which circuits could be used to implement the proposed architecture.

2.2.1 Components Variations and the Converter Performance

2.2.1.1 Integrating Capacitor

The conversion process is independent of the actual integrating capacitor value, a fact that can be proved

a) Mathematically, with Equation (2.7) where no capacitance dependencies are detected, or

b) Graphically, with Figure 2.5 where it is clear that the capacitor magnitude alters the slope of the v_X vs. t relationship for *both* integration periods, thus the net conversion time remains unchanged.

In fact, with a similar argument it can be proved that the capacitor can even be non–linear as long as its charge vs. voltage curve does not have hysteresis. It is also important to note that the capacitor terminal is a floating node. On the one hand this has a positive effect because no voltage clipping –and consequently no irrecoverable error– can occur, an additional advantage of the current–mode implementation over the classic implementation, where the opamp power supplies determine the range of v_X. On the other hand, the capacitor terminal is now influenced by phenomena typical of high impedance nodes, such as ground bounce.

The actual capacitor value *does* determine the maximum value of v_X, as Equation (2.5) shows, so some attention should be paid to the capacitor tolerance in order to avoid unwanted substrate inversions or dielectric breakdowns.

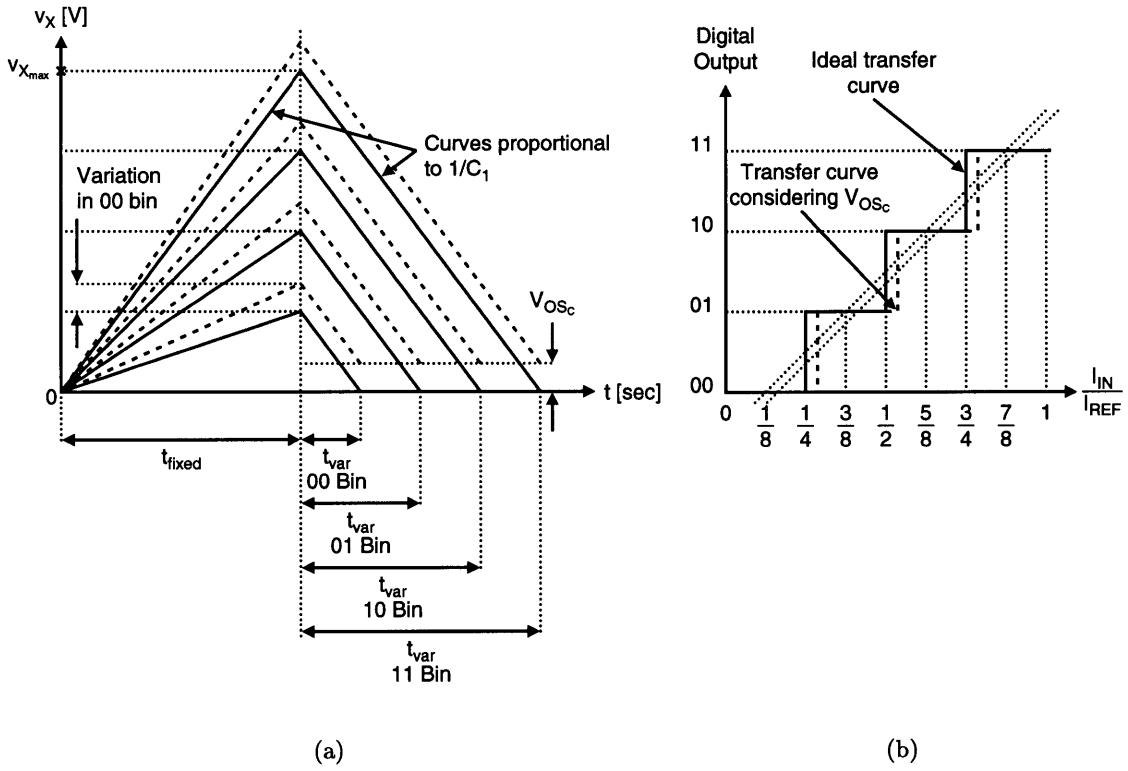


Figure 2.6: Effect of the comparator offset V_{OSc} in the conversion process. Only the 00 combination bin is altered.

2.2.1.2 Comparator Offset

Referring once again to Figure 2.5, the end of the conversion time is the point where the integrated voltage is equal to the comparator reference voltage (ground in Figure 2.4). However, if the comparison has some error due to an offset voltage in the comparator the conversion time will be shorter or longer than expected, and consequently this deviation from the ideal behavior will produce an offset error in the transfer characteristic of the ADC. An example of this can be seen in Figure 2.6 where a positive offset voltage V_{OSc} has been assumed.

The worst-case scenario would be a comparator offset big enough so that one or more

digital combinations are lost, but the typical values of V_{OS_C} make this a very unlikely situation for low resolution converters, even if dynamic comparators are used. For high resolution converters the loss of a digital code is much more likely so the offset problem should be properly addressed, but fortunately there are several offset reduction techniques that can be used to minimize V_{OS_C} [28]–[31].

It should be pointed out that there is no real need to completely eliminate the offset, as long as it is constant and does not cause the loss of a digital combination, it can be removed from the digital output once the conversion has finished. Then, the only problem that remains are possible offset drifts within the conversion cycle.

2.2.1.3 Reference Current

Fluctuations in the reference current will alter the slope of the integrating capacitor voltage curves during the second integration period, as seen in Figure 2.7. This is evident when Equation (2.6) is analyzed, because there it is shown that the variable time of integration t_{var} is inversely proportional to the reference current I_{REF}. Figure 2.7 also shows that the net effect of the changes in I_{REF} is the introduction of a gain error. This error does not seem to affect some of the most important characteristics of the converter (INL, DNL, monotonicity) *but* it alters the input range of the ADC, this is a concern even for low resolution converters so the reference current variations should be treated with care.

Considering that the focus of this thesis is an imager with an array of converters, the gain error in the transfer characteristic should be properly bound to minimize FPN; that is, the difference between the digital codes of any two converters should be less than one bit at all times if both have the same input current. For the gain error this bound will be translated into a very small mismatch between the reference current sources, a very unfortunate conclusion because precision current sources can take considerable silicon area.

2.2.1.4 Counter Clock Frequency

The counter clock frequency is another parameter whose variations should be studied as this counter is the time base used to quantize the variable time of integration t_{var}.

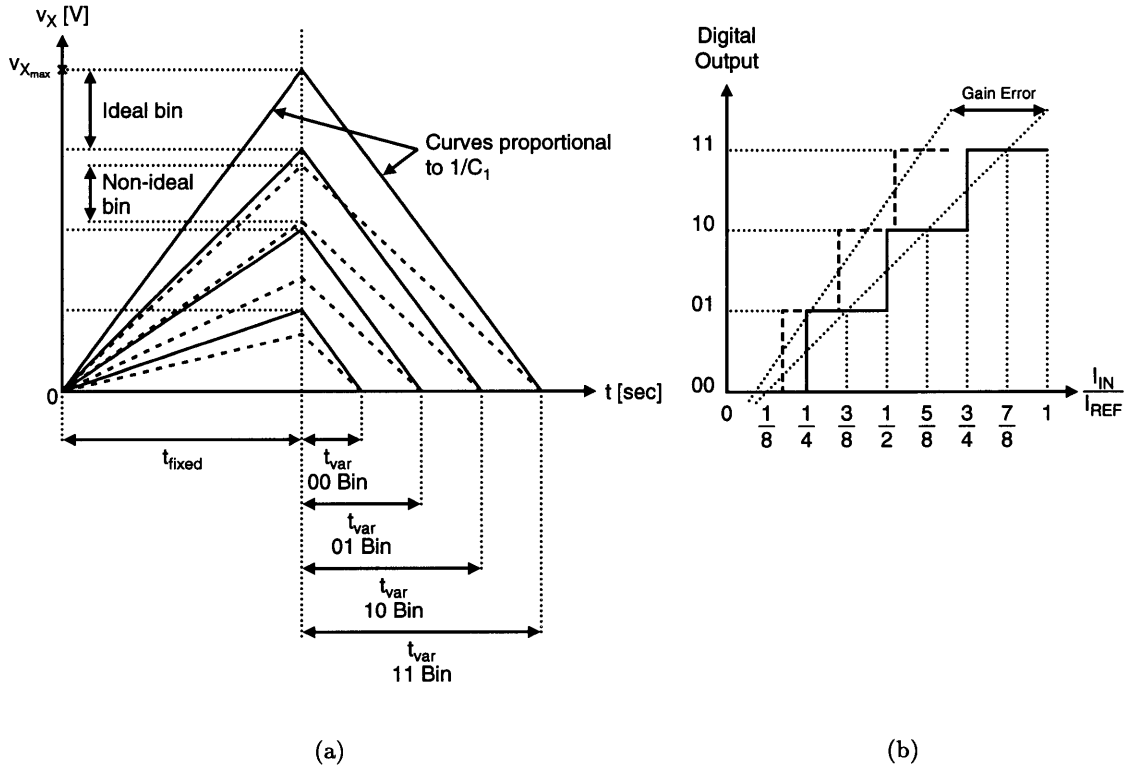


Figure 2.7: Reference current effect in the conversion process. All the bins are reduced or enlarged by the same amount.

Fortunately these variations are non–critical because it is possible to use crystal oscillators that have extremely low frequency deviation, and what is more, the dual–slope ADC has a "natural" insensitivity towards this parameter. As Grebene says:

> The conversion accuracy is independent of [...] the clock frequency, since this parameter affects the ramp–up and ramp–down times equally, as long as [its] value remains stable during the integration cycle. In this manner, long–term drifts due to time or temperature effects are largely avoided [32].

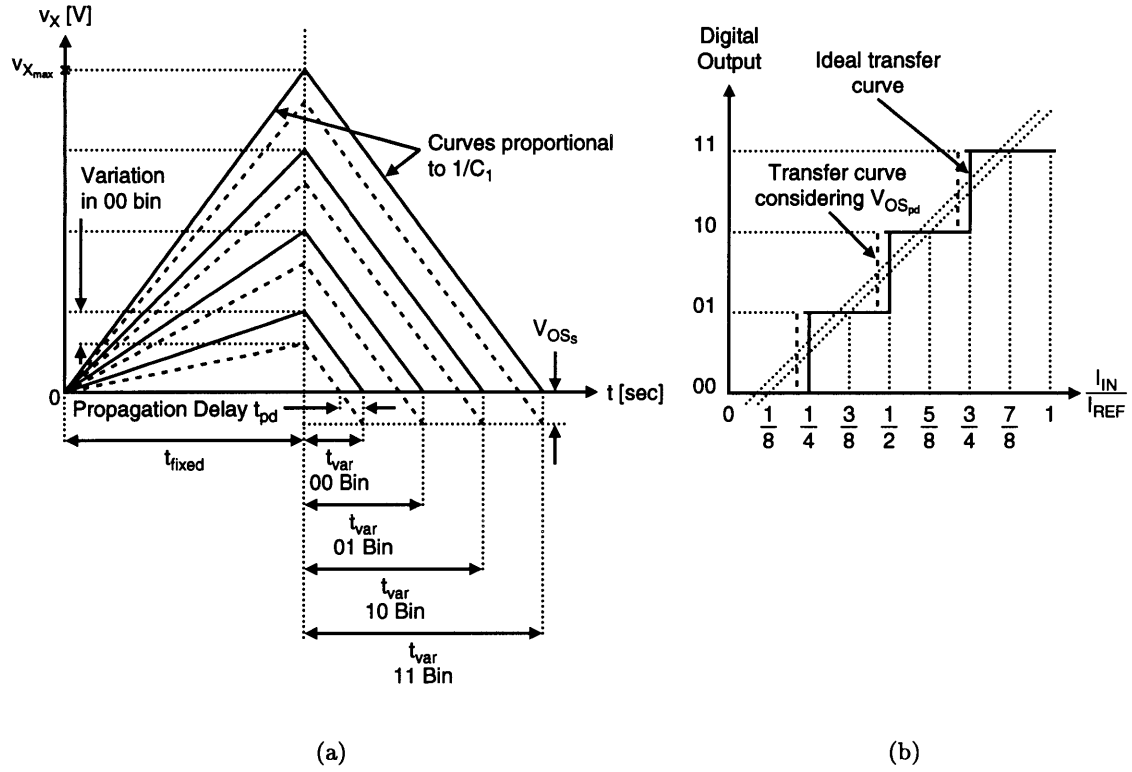


Figure 2.8: Effect of the comparator propagation delay in the conversion process and the way it is modeled as a comparator offset voltage.

2.2.1.5 Comparator Propagation Delay

Up to this point it has been assumed that the counter stops instantly whenever the integrator voltage matches the comparator reference voltage. Unfortunately the comparator output takes some time to reflect this event thus introducing a finite delay to the conversion process. This delay can modeled as a *negative* comparator offset voltage as both have the same net effect in the transfer characteristic of the ADC (Figure 2.8), so the same conclusions of Subsection 2.2.1.2 apply in this case.

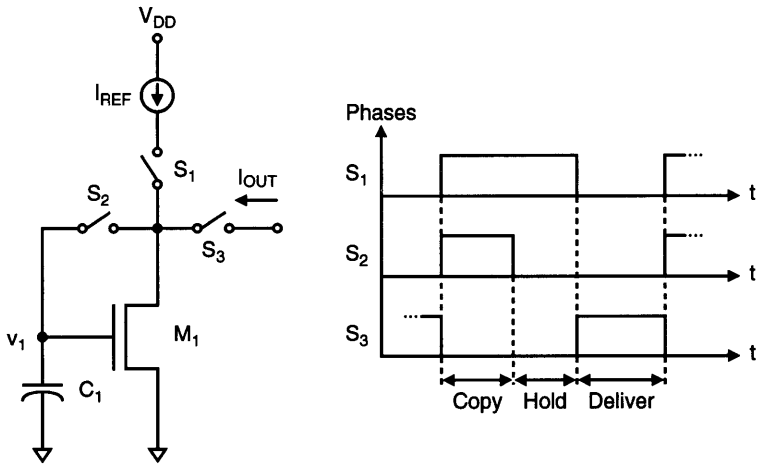


Figure 2.9: Simple switched–current cell.

2.2.1.6 Conclusions of the Component Tolerance Analysis

The preceding analysis confirmed that the dual–slope converter is indeed a very robust ADC, the only real nonlinearities of the system are a small differential nonlinearity produced by the clock jitter during the fixed current phase and a possible hysteresis in the charge vs. voltage curve of the integrating capacitor. The architecture could be implemented in a relatively small area and with a reduced power dissipation using the current–mode approach provided that there is a simple way to build the precision reference current sources needed by the converter array.

2.3 Converter Matching Solution: Switched–Current Cells

It is extremely hard to design several current sources that would be matched with the precision required, the fabrication process variations make this task nearly impossible. Fortunately it seems that the circuit shown in Figure 2.9 can be used to solve the problem [33]. This system is often called a switched–current (SI) cell or current copier and it is routinely

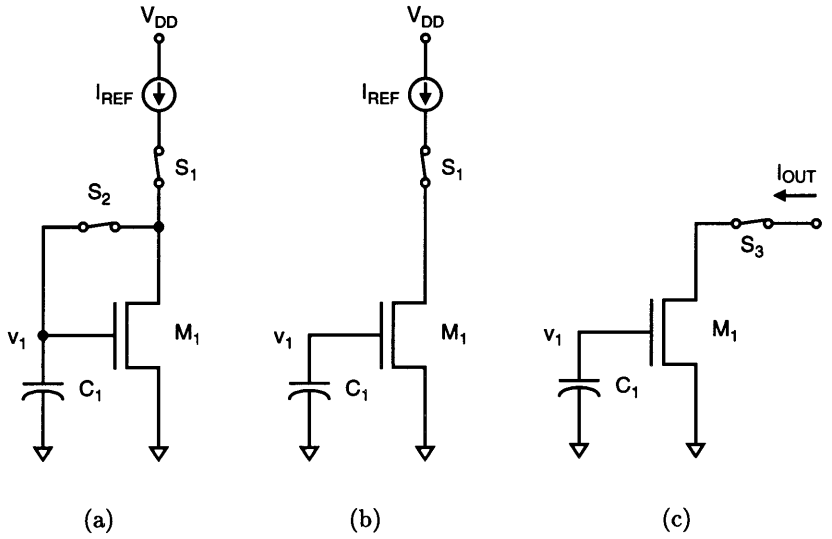


Figure 2.10: Phases of operation of a switched–current cell. (a) Sample/copy, (b) hold and (c) deliver.

used in discrete filter design, but it is also ideally suited for the task of producing several tightly matched current references.

The current copier can be thought of as analog memory cell with two main phases of operation and an intermediate one. The first phase of operation is the copy or sample phase, when switches S_1 and S_2 are closed in order to copy the current I_{REF}, as shown in Figure 2.10 (a). Assuming that the voltage across the capacitor C_1 was initially zero, I_{REF} will linearly charge this capacitance until the threshold voltage of transistor M_1 is reached. From this point on, some of I_{REF} will be diverted to the transistor, while the rest continues to charge the gate capacitance until the voltage in this node is such that all of the current to be copied flows through the transistor. When this happens, S_1 and S_2 can be opened and S_3 can be closed so that the gate of the transistor is isolated and thus M_1 is capable of sinking I_{REF} ($I_{OUT} \approx I_{REF}$), as depicted in Figure 2.10 (c). Generally there is an intermediate step between the copy and the delivery of the current to minimize the charge injected to node v_1 [34]. Switch S_1 is opened a few nanoseconds after S_2 so that the

channel charge of this switch will not disturb the voltage stored in C_1, this is the hold phase that can be seen in Figure 2.10 (b). The channel charge from switch S_2 does reach node v_1, so here it might be necessary to use techniques that minimize charge injection depending on the precision that is required from the copy process.

It is important to note that these cells have a superb process parameter insensitivity: given enough settling time, the gate voltage will reach its final value regardless of the actual capacitor value, the actual magnitude of the threshold voltage or the particular dimensions of the transistor. Practical current copier cells suffer from several problems that create an error between the reference current and the stored current. The main factors that are involved in this difference are junction leakage from the MOS switches, channel length modulation, charge feedthrough from the switches and parasitic capacitive coupling from drain to gate of the transistor. All these sources of errors are covered in [35]–[36], while [37]–[40] provide better explanations and models of switch charge feedthrough. In spite of these errors, Daubert points out that

> The relative error is the most important in applications such as D/A conversion [...] This error is the difference in the memorized currents of two copiers, derived from the same current [assuming a 1% mismatch between the devices indicated]. The current copier technique, non dependent on device matching, has very small relative errors, measured in parts per million. In contrast, use of the conventional current mirror technique would result in errors of close to 1% [33].

The system shown in Figure 2.11 will be used to generate all the reference current sources needed by the pseudo–converters of the array. A "master" reference current is sequentially copied to *all* the SI cells, so that while the error between any of the individual currents copied and this master current may be in the 1% or 2% range, the difference between any two copied currents is only the relative error, which as was stated above is only in the part per million range.

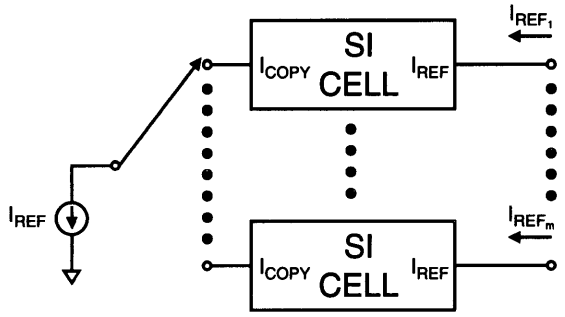


Figure 2.11: Generation of the reference current sources for the converter array.

2.4 A Novel Distributed Converter Architecture

To take full advantage of the proposed parallelism a suitable architecture should remove the blocks that dissipate the most power from the individual converters and make these blocks common to the array. The structure that accomplishes this task can be seen in Figure 2.12. Under this scheme an $m \times n$ RAM is needed, where m is the number of rows of the pixel array and n is the bit length of the counter; furthermore, this memory also needs to have independent input and output ports. Figure 2.12 shows that an array of pseudo–converters (switches S_1 and S_2, capacitor C_1 and the comparator) share the control logic while the counter is fed to the input port of the RAM. The comparators outputs go not to the control logic as before but to the Write Enable pins of the rows of the memory, so that the write feature is normally on until the end of the conversion. In this way the count is repeatedly stored in the different rows of the RAM until the comparator associated with a particular row signals the end of the conversion.

This novel architecture enables the system to read one row of the pixel array at a time, which constitutes a big improvement in terms of speed. Moreover, unless the image captured has extremely high light intensities in a row, the *average* scan time of a row could be significantly reduced, because it would be fairly easy to implement a logic block that could detect the moment when all the converters have finished their respective conversions

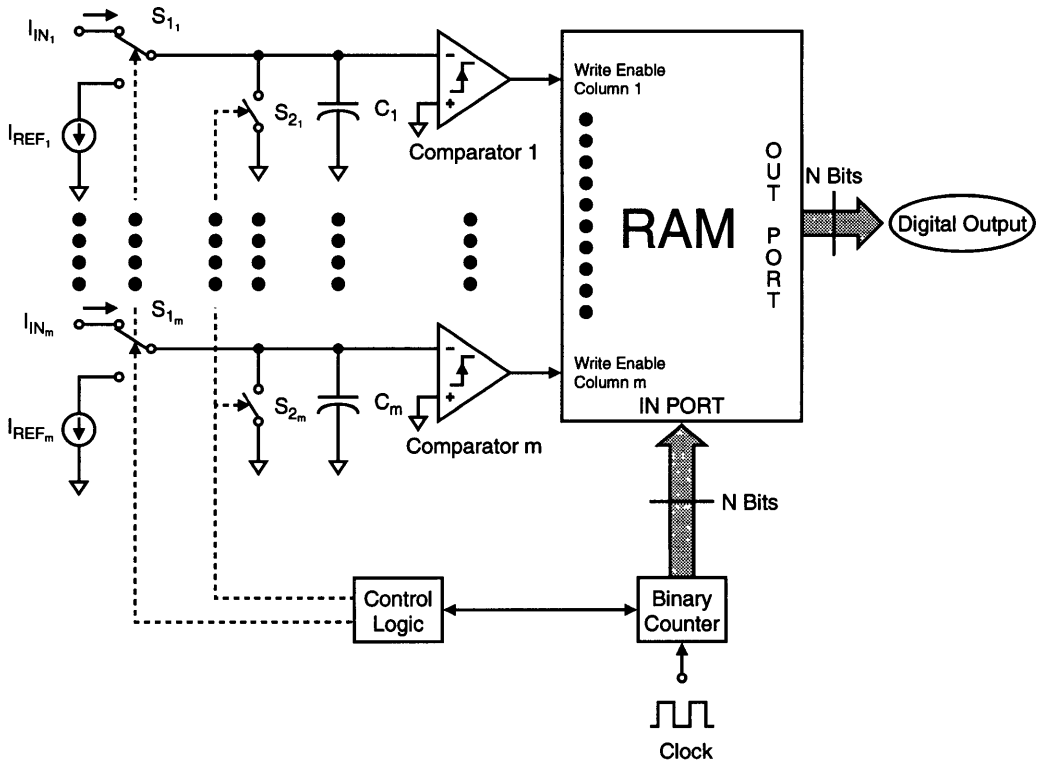


Figure 2.12: Proposed distributed converter architecture.

and then immediately start scanning the following pixel row. With this approach, further improvements in frame rate could be achieved.

2.5 Local Companding

One of the main reasons why the dual–slope converter was selected for this thesis is that the size of the bins in the ADC transfer characteristic is controlled by the counter; that is, one of the most critical parameters of the system is determined by a time base, a feature that can be easily and precisely controlled. Typical dual–slope converters use a local oscillator to generate the clock signal of the binary counter, as it can be seen in Figure 2.13 (a); however, just by modulating the frequency of this clock signal it would possible to change the shape of

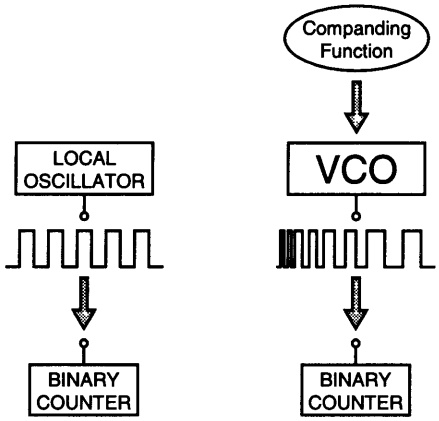


Figure 2.13: Two systems that can generate the time base for the dual–slope converter. (a) Usual system and (b) companding–capable system.

the converter transfer characteristic at will. This effect could be easily achieved by inserting a voltage–controlled oscillator (VCO) in the system, as shown in Figure 2.13 (b). The key objective then is to find the voltage waveform that can drive the VCO in such a way that the desired imager response is obtained.

It is possible to generate the hyperbolic transfer function that was introduced in Chapter 1 with the VCO, as Figure 2.14 (b) shows. This transfer function was obtained using a maximum of 6 bits (only 64 digital codes) which proves that decent results can be achieved even with low intensity resolutions. The approximation was done in a piecewise fashion using the following frequencies: 6.4MHz, 5MHz, 3MHz, 2MHz, 1.2MHz and 400KHz. In this particular example it would be feasible to generate the input function of the VCO with a very low resolution DAC and some timing logic, a very simple and cost–effective solution.

All the converters in the array have the same transfer characteristic because the counter is common to all of them, so it is *not* possible to have different companding options along one row. However, the controlling function of the VCO can change *from row to row*, so that the response of the imager can be adapted locally on a row–by–row basis depending on the

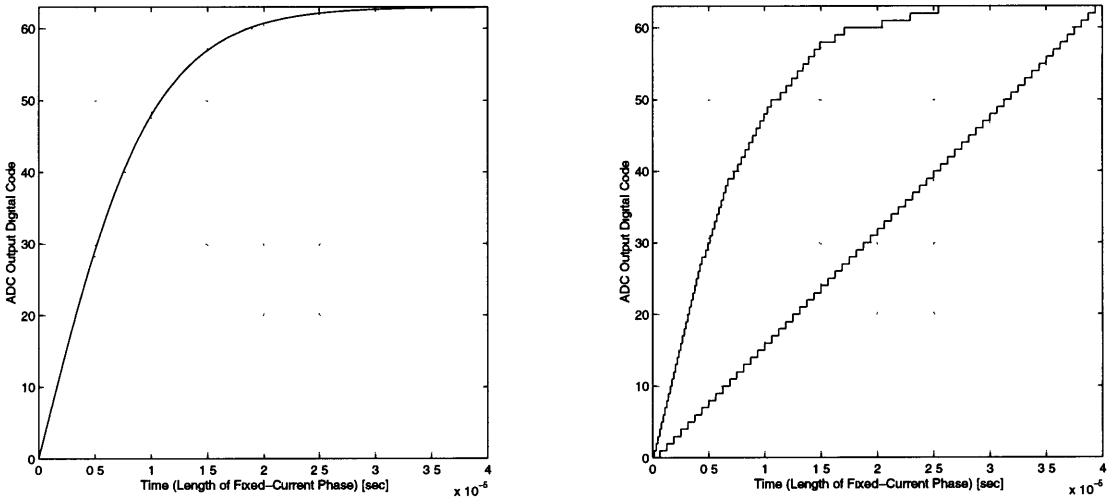


Figure 2.14: Companding example: hyperbolic transfer function. (a) Continuous case, (b) a 5 part piecewise approximation and a linear transfer function offered as a measuring tool.

light intensity distribution, which, as it was stated in Chapter 1, is one of the most valued features in an imager.

2.6 Specifications of the Novel Current–Mode Dual–Slope Converter

The purpose of the prototype ASIC is to test the performance of a system that implements the novel concepts previously introduced in this chapter. Table 2.2 summarizes the imager specifications that were established with this idea in mind, and also considering that the system is going to be used in machine vision applications. The imager operation is divided in three phases. During the first phase the following activities take place:

- The pixels collect photogenerated charge.

Table 2.2
Imager specifications

Specification	Variable	Magnitude	Units
Spatial Resolution	Row	128	–
	Col	8	–
Maximum Light Integration Time	t_{int}	2.5	msec
Light Intensity Resolution	n	8	bits
Maximum Frame Rate	F	80	frames/sec
Maximum Fixed Pattern Noise	FPN	≤ 0.4	% FS

- The SI cells are refreshed, the master reference current is copied to all the cells.
- The comparator is offset–canceled.
- The contents of the RAM are read. The bit rate of this process is

$$\text{Bit Rate} = \frac{Col \times n}{t_{int}} = 25.6 \text{ Kbits/sec} \tag{2.8}$$

  The Enhanced Parallel Port (EPP) of a PC can achieve transfer rates between 500Kbits/second and 2Mbits/second [41] so it is possible to use a personal computer to control the system, to receive the data and to display the resulting image.

The next two phases of operation of the imager are the fixed–time and the fixed–current phases of the dual–slope converter which were covered in detail previously. Due to the nature of the dual–slope converter, these two phases last $2^n \cdot T_{clk} = 2^n / f_{clk}$. Then, considering that with the proposed architecture it is possible to read one row at a time

$$F = \frac{1}{t_{int} + Row \cdot 2 \cdot \frac{2^n}{f_{clk}}} \Rightarrow f_{clk} = \frac{2^{n+1} \cdot Row}{\frac{1}{F} - t_{int}} \Rightarrow \boxed{f_{clk} \approx 6.55\text{MHz}} \tag{2.9}$$

The prototype ASIC will be fabricated through MOSIS [42] in the Hewlett–Packard CMOS14TB 0.5μm process. This is an n–well, triple metal process which has been designed

for a $V_{DD} = 3.3$V power supply. It is expected that the actual value of the integrating capacitance will be in the picofarad range, so the only way of implementing it in a reduced area is to use the gate capacitance of an MOS transistor, all the other options (metal 1–to–metal 3, poly–to–metal 3, etc.) would occupy an enormous space. Consequently the voltage across the capacitor should never be below the threshold voltage of the MOS transistor to maintain a strong inversion layer. For the CMOS14TB process this threshold is on the order of $V_T \approx 0.9$V, and considering that the pixel should need some voltage drop to operate, it was *chosen* $V_{X_{max}} = 2.2$V.

The reference current source magnitude was also chosen. In this case the objective was to minimize the integrating capacitor value, a result that could have been achieved with a very low reference current. However, the "master" reference current source was going to be implemented off–chip, so the smaller the magnitude of this source, the tougher it would have been to actually build it with discrete components. Taken all these considerations into account, $I_{REF} = 1\mu$A. Once this magnitude is *chosen*, from Equation (2.5) and Equation (2.9)

$$C_1 = \frac{I_{REF}}{2 \cdot V_{X_{max}} \cdot F \cdot Row} \Rightarrow \boxed{C_1 \approx 22\text{pF}} \tag{2.10}$$

Now from Appendix B and Equation (2.10), for a maximum offset error of $E = 1/4$ LSB

$$V_{OS} = \frac{I_{REF}}{C_1 \cdot f_{clk}} \cdot E \Rightarrow V_{OS} = \frac{V_{X_{max}}}{2^n} \cdot E \Rightarrow V_{OS} \approx 2.15mV \tag{2.11}$$

If the comparator offset voltage is *arbitrarily chosen* to be $V_{OS_C} = 550\mu$V, then also from Appendix B and Equation (2.10)

$$V_{OS} = V_{OS_C} + V_{OS_{pd}} \Rightarrow V_{OS_{pd}} = V_{OS} - V_{OS_C} \Rightarrow \boxed{V_{OS_{pd}} \approx 1.6\text{mV}} \tag{2.12}$$

$$t_{pd} = \frac{V_{OS_{pd}} \cdot C_1}{I_{REF}} \Rightarrow t_{pd} = \frac{V_{OS_{pd}}}{2 \cdot V_{X_{max}} \cdot F \cdot Rows} \Rightarrow \boxed{t_{pd} \approx 36\text{nsec}} \tag{2.13}$$

It is worthwhile noting that the comparator will be offset canceled, so the value $V_{OS_C} = 550\mu$V is a performance that can be achieved with relative ease. It is also important to note that the delay time t_{pd} includes not only the comparator propagation delay but also any other source of delay between the moment the integrating capacitor reaches the reference voltage to the moment the counter value is finally stored in the RAM.

Taking the results from Appendix C, for a maximum mismatch of 1 bit ($m = 1$)

$$P_{I_{REF}} = \frac{\Delta I_{REF}}{I_{REF}} \Rightarrow \frac{\Delta I_{REF}}{I_{REF}} = \frac{1 - 2 \cdot E}{2^{n+1} - 2 \cdot m - 1} \Rightarrow \boxed{\frac{\Delta I_{REF}}{I_{REF}} \approx 0.2\%} \tag{2.14}$$

$$FPN \leq 100 \cdot \frac{m}{n} \Rightarrow \boxed{FPN \leq 0.4\%\text{FS}} \tag{2.15}$$

Equation (2.14) gives only one half of the allowed mismatch because in Appendix C the variation of I_{REF} was defined as $I_{REF} \pm \Delta I_{REF}$, so the total current mismatch is approximately 0.4%, which is on the order of magnitude of the *absolute* error of the SI cells. Table 2.3 summarizes the specifications for the current–mode dual–slope converter.

2.7 Summary

This chapter described a column–parallel imager from a system perspective. This architecture has a converter array that digitizes one row of the sensing array at a time.

Table 2.3
Specifications of the current–mode dual–slope distributed ADC

Specification/Component	Magnitude	Units
Resolution	8	bits
Offset error	$< 1/4$	LSB
Gain error	< 1	LSB
Clock frequency	6.55	MHz
Comparator offset voltage	550	μV
Comparator propagation delay	36	nsec
Integrating capacitor	22	pF
Reference current	1	μA
Reference current mismatch	< 0.4	%
Power supply	3.3	V

A novel current–mode dual–slope converter was introduced as the building block of this converter array. The sources of errors in the transfer characteristic of the dual–slope ADC were studied, and the matching of the reference currents in the array emerged as the critical error. The switched–current cells were presented as the most adequate way of solving this problem as they can achieve current matching in the parts per million range. A novel distributed converter architecture was designed to minimize the complexity, area and power dissipation of the system; this array of ADCs is made of shared blocks that dissipate the most power and ultra–low power pseudo–converters that are present in all the columns of the imager. It was also described how the introduction of a voltage–controlled oscillator can enable a local companding option. When this block drives the counter of the dual–slope converter, it is possible to change the transfer characteristic of the converter array on a row–by–row basis. The specifications of an experimental integrated circuit were derived; the imager has a spatial resolution of 128 rows and 8 columns, the sensing array can be read 80 times per second and the pixel currents are digitized to 8 bits.

Chapter 3

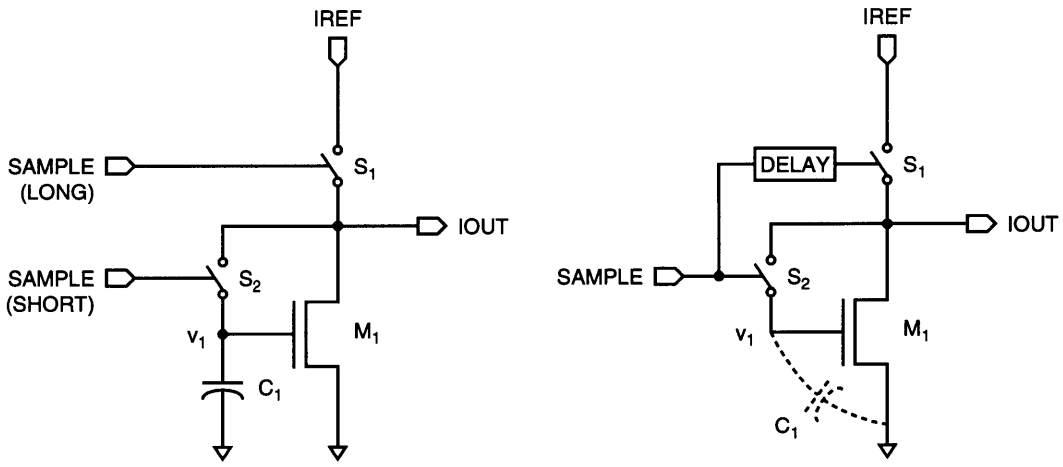
Transistor–Level Design

3.1 Switched–Current Cell

The basic circuit that was designed is shown in Figure 3.1 (a). A drawback of this particular incarnation of the current copier is that it needs two phase signals for the sample switches, as it is desirable to open S_2 a few nanoseconds before S_1 (Section 2.3). The circuit that was actually used is shown in Figure 3.1 (b), where a local delay block has been added so that only one control signal is required per cell.

Aside from the delay block, two other simple ideas were introduced to minimize the reference–to–copy error in the SI cell. The first idea was to use the common "dummy" switch technique, which as a rule of thumb cancels about 80% of the charge injected in the gate of transistor M_1. The second idea was to increase the capacitor C_1 in order to reduce the voltage swing produced by the channel charge of switch S_2. In this particular instance the gate–to–source capacitance of transistor M_1 was used to implement C_1 (Figure 3.1).

One of the main concerns in the design of the SI cell was its output resistance. The reference current normally increases with the voltage across the integrating capacitor C_{INT} due to the channel–length modulation effect so the fixed–current phase of the ADC is sped up in a non–linear fashion. To minimize the reference current change transistor M_1 was



(a) Original circuit.

(b) Circuit with only one sample signal.

Figure 3.1: Basic switched–current cell used in the prototype ASIC.

made extremely long, a decision which had two positive side effects:

- It increased the gate capacitance of the device which reduced the effect of the charge injection even more.
- It placed the transistor in the proper operating region. The high process transconductance parameter[1] of the CMOS14TB technology enabled a unity size transistor to support the 1μA reference current with a very small gate–to–source voltage. In fact this voltage was so small that the transistor would normally be in the subthreshold region; consequently a W/L ratio much less than unity assured that the transistor would always operate where the output resistance is maximized, that is to say in the strong saturation region.

Finally, a simple cascode was used to boost the output resistance even more. The fact that the integrating capacitor was going to be implemented with an NMOS transistor

[1]The product $\mu \cdot C'_{ox}$ is usually called the process transconductance parameter [43].

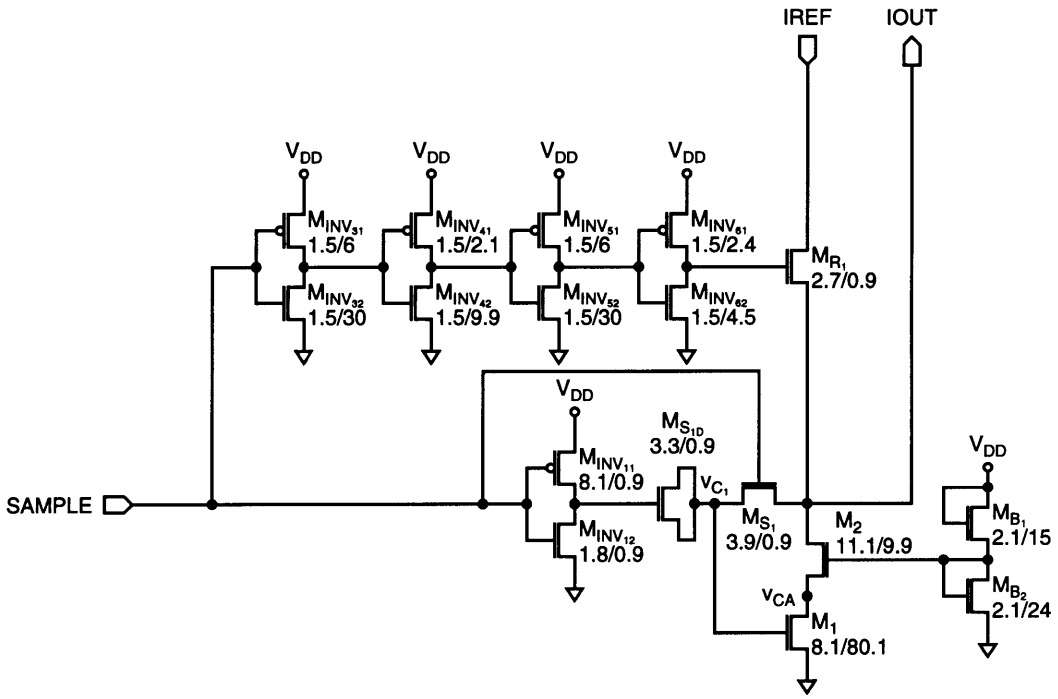


Figure 3.2: Final design of the switched–current cell.

(Section 2.6) meant that the output voltage of the SI cell would never be below 0.7V, the approximate value of the NMOS transistor threshold voltage for the CMOS14TB technology. This provided enough room for the biasing of the cascode structure and guaranteed that the reference current source would operate in the saturation region throughout the fixed–current phase.

3.1.1 Final Design

Figure 3.2[2] shows the final design of the SI cell. M_1 is the transconductance and also the implementation of capacitor C_1, M_{S_1} is switch S_1 with the associated "dummy" switch made by transistor $M_{S_{1D}}$ and its inverter, transistors $M_{INV_{11}}$ and $M_{INV_{12}}$; transistor M_2 is the cascode with its biasing, transistors M_{B_1} and M_{B_2}; and transistor M_{R_1} is the

[2]All the transistor dimensions in this chapter are expressed in micrometers.

Table 3.1
Dimensions of the switched–current cell transistors

Main Cell	
Device	Width/Length
M_1	8.1/80.1
M_2	11.1/9.9
M_{B_1}	2.1/15
M_{B_2}	2.1/24
M_{S_1}	3.9/0.9
$M_{S_{1_D}}$	3.3/0.9
$M_{INV_{11}}$	8.1/0.9
$M_{INV_{12}}$	1.8/0.9
M_{R_1}	2.7/0.9

Delay Block	
Device	Width/Length
$M_{INV_{31}}$	1.5/6
$M_{INV_{32}}$	1.5/30
$M_{INV_{41}}$	1.5/2.1
$M_{INV_{42}}$	1.5/9.9
$M_{INV_{51}}$	1.5/6
$M_{INV_{52}}$	1.5/30
$M_{INV_{61}}$	1.5/2.4
$M_{INV_{62}}$	1.5/4.5

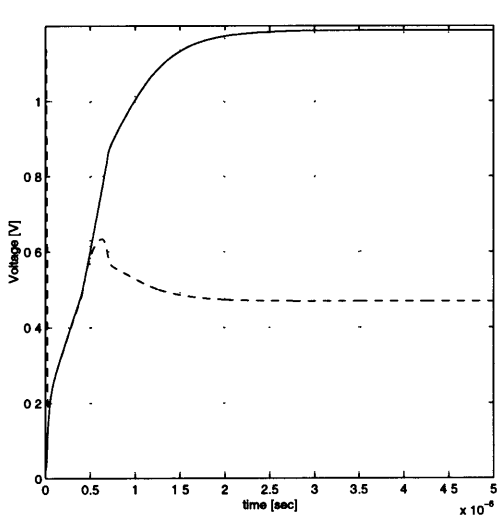
implementation of switch S_2. Transistors $M_{INV_{3x}}$–$M_{INV_{6x}}$ implement the local delay block.

All the switches were made with NMOS transistors as no rail–to–rail operation was needed, and its length was not the minimum allowed by the process (0.6μm) in an effort to minimize the leakage currents that could eventually alter the voltage stored at the gate of M_1. Table 3.1 summarizes the dimensions of all the transistors involved in the circuit.

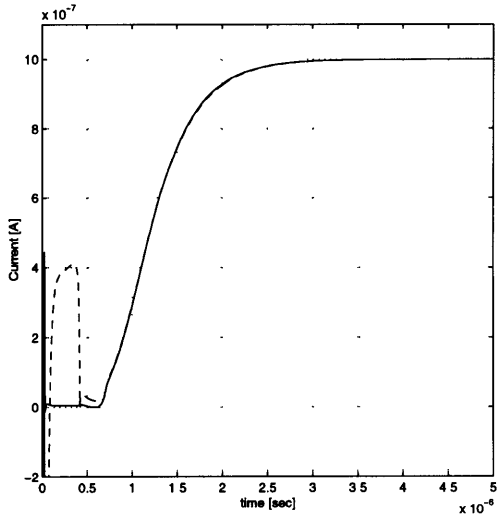
3.1.2 Settling Behavior

Figure 3.3 (a) and (b) show the typical settling behavior of the gate voltage and drain current of transistor M_1. This behavior differs somewhat from the results derived in Section A.1 for two main reasons: the way the capacitor C_1 is implemented and the presence of the cascode structure.

Up to about 125nsec the gate voltage waveform has a much higher slope than originally predicted due to a couple of factors: First, if the gate voltage of M_1 is assumed to be initially near ground, the transistor is in the cut–off region and the gate capacitance that is being charged is only the gate–to–source overlap capacitance, which is much smaller than the gate capacitance when the transistor is "on". Second, the bias voltage of transistor M_2 is near the midpoint of the power supply range, therefore if the intermediate node of the



(a) Gate voltage of transistor M_1 (solid curve) and intermediate node of the cascode structure (dashed curve).



(b) Drain current of transistor M_1 (solid curve) and drain current of the cascode transistor M_2 (dashed curve).

Figure 3.3: Switched–current cell settling behavior.

cascode structure (v_{CA}) was initially above ground the function of the terminals of M_2 is inverted and the charge at the mentioned node is quickly eliminated thus increasing the total current at the gate of M_1.

When this discharge process has ended, the function of the terminals of M_2 is inverted again and the parasitic capacitance of v_{CA} is charged up, as it can be seen in the dashed curve of Figure 3.3 (a). This event introduces a breakpoint in the gate voltage curve by essentially decreasing the total current that goes to the gate of transistor M_1; therefore the voltage waveform during this period has a smaller slope than the previous section, as shown by the solid curve of Figure 3.3 (a) between approximately 125nsec and 400nsec.

When the voltage at v_{CA} is a threshold voltage below the bias of M_2, the transistor enters the cut–off region and all the current I_{REF} flows again through the gate capacitance of M_1. The voltage curve at this node consequently regains the same slope it had at the

beginning of the settling process until the threshold voltage of transistor M_1 is reached (400nsec to 600nsec section).

After transistor M_1 is "on", the drain current evolves slower than predicted mainly due to mobility degradation effects. As it can be seen the settling process is a little bit more involved than previously thought, so the results obtained from Equation A.15 were taken only as a good estimate, and the actual settling time was determined with empirical data collected from simulations for all the fabrication runs available. After leaving enough time to account for process parameter variations (mainly threshold voltage and process transconductance) it was determined that $t_{settle} \approx 5\mu$sec.

Figure 3.2 shows that the delay element was implemented with a chain of digital inverters. Though no more than 2nsec to 5nsec are needed to turn off switch S_2, the targeted delay of the block was 50nsec (about 1% of the settling time) so as to have room to tolerate significant process parameters variations. The high process transconductance parameter of the CMOS14TB technology and the small gate capacitance of switch S_1 created a slight complication in that it was difficult to achieve the desired performance with small inverters; therefore transistors with a W/L ratio well below unity were needed to introduce any sizable delay in each stage. Due to the fact that the converter layout needed to have a very small pitch to match the width of the pixel, long transistors fitted naturally in the overall layout and thus the problem was not as serious as it appeared at first. Figure 3.4 shows that the delay block helped reduce the charge injection at the gate of transistor M_1 by 2mV. If a small–signal transconductance $g_{m_1} \approx 5\mu$S and a reference current $I_{REF} = 1\mu$A are assumed, this voltage difference represents 3 LSBs, a very important figure because the precision of the reference current directly affects the gain error of the converter (Subsection 2.2.1.3).

Table 3.2 shows the relevant parameters of the final design. It should be noted that the output resistance is not the result of a small–signal simulation, rather it is the result of measuring the actual value of the reference current when the output voltage of the SI cell is at 1V and 2.75V, the two extremes of the integrating capacitor voltage range. The noise current was estimated using Equation A.67.

Table 3.2
Switched–current cell characteristics

Parameter	Variable	Magnitude
Nominal current	I_{REF}	1μA
Output resistance	$R_{OUT_{SI}}$	$2G\Omega$
Output capacitance	$C_{OUT_{SI}}$	32fF
Storage capacitor	C_1	1.4pF
Small–signal transconductance @ $I_{OUT} \approx I_{REF}$	g_m	5μS
Noise current	$3 \cdot \sqrt{\overline{i^2_{REF}}}$	1.2pA
Settling time	t_{settle}	5μsec
Area	A_{SI}	$7500\mu m^2$

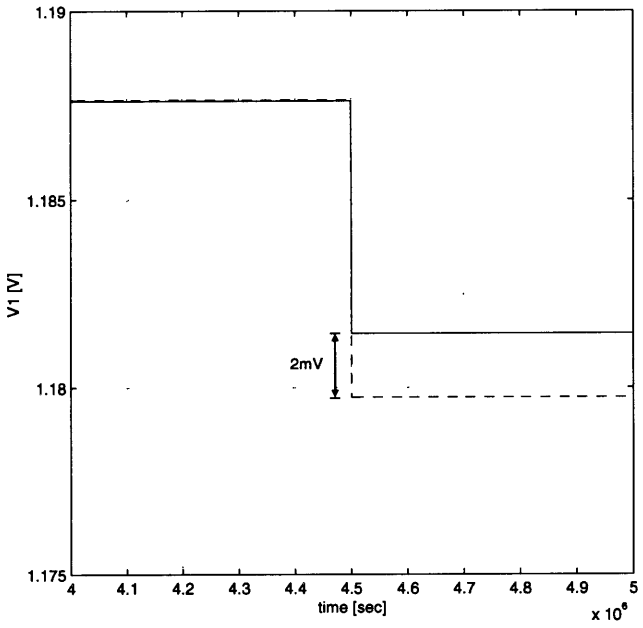


Figure 3.4: Effect of the delay block: the dashed curve represents the case where switches S_1 and S_2 turn off simultaneously while the solid curve represents the case where there is a 50nsec delay between the operation of the switches.

Table 3.3
Integrating capacitor characteristics

Parameter	Variable	Magnitude
Nominal capacitance	C_{INT}	22pF
Width	$W_{C_{INT}}$	17.7μm
Length	$L_{C_{INT}}$	9.9μm
Number of gates	–	37
Actual area	$A_{C_{INT}}$	6484μm^2

3.2 Integrating Capacitor

As it was stated in Section 2.6 the integrating capacitor of the pseudo–converter is implemented with an NMOS transistor, using its gate–to–source and gate–to–drain capacitance. The total area of this transistor is calculated from

$$t_{ox} \approx 100\text{Å} \rightarrow C'_{ox} = \frac{\varepsilon_{si}}{t_{ox}} \Rightarrow C'_{ox} \approx 3.45 \frac{\text{fF}}{\mu\text{m}^2} \tag{3.1}$$

where ε_{si} is the permitivity of silicon and t_{ox} is the width of the gate oxide. With the integrating capacitor value shown in Table 2.3,

$$A_{C_{INT}} = \frac{C_{INT}}{C'_{ox}} \Longrightarrow A_{C_{INT}} \approx 6370\mu\text{m}^2 \tag{3.2}$$

In addition, the gate capacitance of an NMOS transistor remains fairly linear as long as the device is in the strong inversion region, although as it was seen in Subsection 2.2.1.1 this is not an obligatory requirement. The capacitor was implemented with 37 transistors placed in parallel, each of them with an aspect ratio $W/L = 17.7\mu\text{m}/9.9\mu\text{m}$. Table 3.3 summarizes the most important characteristics of the integrating capacitor.

3.3 Toggle Switch

The next step of the design was to build the toggle switch S_1 of Figure 2.4, repeated for convenience in Figure 3.5. The typical circuit used to build this switch is shown in Figure 3.6 (a), however this implementation is not well suited for the current–mode converter because the most important node of the ADC, the integrating capacitor, is very sensitive to any charge injection as it is a high impedance point. Unfortunately, transistors M_{T_1} and M_{T_2} either dump or remove charge from the capacitor C_{INT} when they turn "on" or "off" thus causing nonlinear voltage swings at the start of the fixed–current phase. The main problem is that the pixel current has a 1μA range, so it is impossible to predict the charge that will be dumped to the integrating capacitor when transistor M_{T_1} turns "off" as the process is signal dependent.

It was evident that the solution would had to involve a redesign of the original circuit. After several failed attempts, the circuit of Figure 3.6 (b) emerged as the best way of minimizing the charge injection problem in the integrating capacitor. The idea behind this implementation is to provide a discharge path for the channel charge of the switches. The reference current source generated by the SI cell is "on" during the fixed–time phase *and* the fixed–current phase of the converter, thus creating a circuit with a *finite* time constant for the charges to go through. Even though this time constant is very high (as Table 3.2 and Table 3.3 show, both the integrating capacitor and the SI cell output resistance are huge), the reduced size of the switching transistors and the mere presence of a discharge path was enough to minimize the problem. To maintain the functionality of the ADC the pixel current range was changed from $[0\mu\text{A}, 1\mu\text{A}]$ to $[1\mu\text{A}, 2\mu\text{A}]$ to compensate for the added presence of I_{REF} during the fixed–time phase. This new scheme also eliminated both switching transistors M_{T_1} and M_{T_2} and replaced them with a single CMOS pass gate. The operation of the new system can be divided in four parts:

Temporary Load Phase

A new phase is introduced because the integration time of the pixels is much higher than the refresh time of a single SI cell. It is not a good idea to just turn the cell "off"

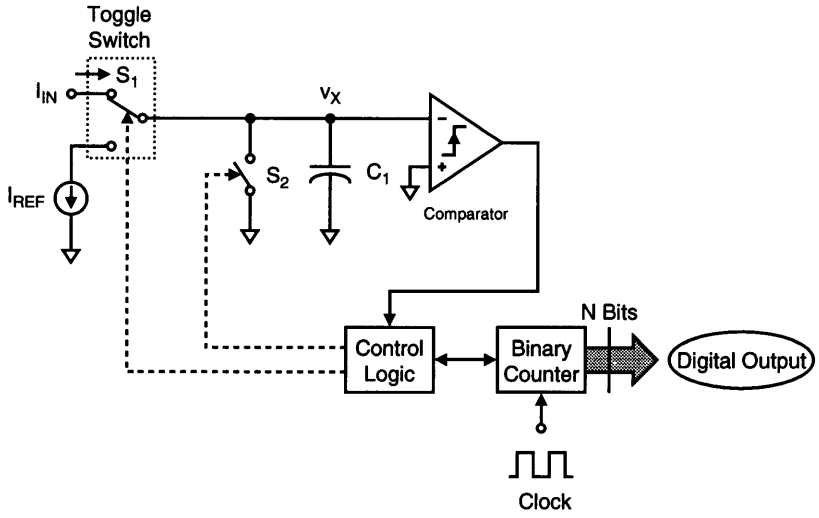
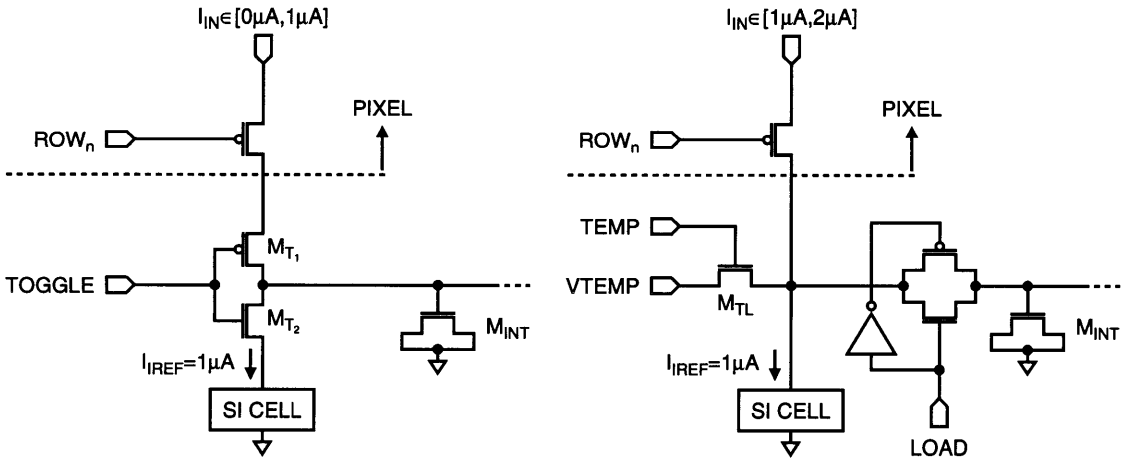


Figure 3.5: Current–mode dual–slope ADC.



(a) Traditional circuit.

(b) Circuit used in the design.

Figure 3.6: Toggle switch implementation.

with a pass transistor after it has been refreshed because the current would then take some time to re-established itself at the beginning of the fixed–current phase, and also there would be a huge charge demand from transistors M_1 and M_2 when they turn "on". Consequently, the cells need individual temporary loads so that the copied currents can continue to flow through some circuitry until they are needed, this is why transistor M_{TL} was introduced in the basic SI cell design (Figure 3.6 (b)). The function of this transistor is to connect each cell that has finished its refresh process to a temporary voltage source that is common to the array. M_{TL} then stays "on" from this point in time until the end of the pixel integration period.

Pixel Current Settling Phase

When the photon integration period has ended a row switch that should be present in the pixel turns "on" and the signal current flows out of the pixel to the temporary load. Note that this switching event causes no charge injection problem as the integrating capacitor is isolated from this part of the circuit by the CMOS pass gate.

Fixed–Time Phase

When the pixel current is properly established, the pass gate turns "on" and transistor M_{TL} turns "off" so that the difference between the pixel current and the reference current flows through the integrating capacitor.

Fixed–Current Phase

When the fixed–time phase ends the row switch in the pixel turns "off" while the reference current continues to operate. The charge from the switch goes mainly through the SI cell to ground so any nonlinear effect in the integrating capacitor is minimized.

Figure 3.7 shows the difference between the original circuit (solid curve) and the new circuit (dashed curve). It is obvious that there is a substantial difference in performance, and although the new circuit produces a somewhat round peak, the "effective" switching point (where the asymptotes of the two curve sections meet) is quite close to the actual switching point.

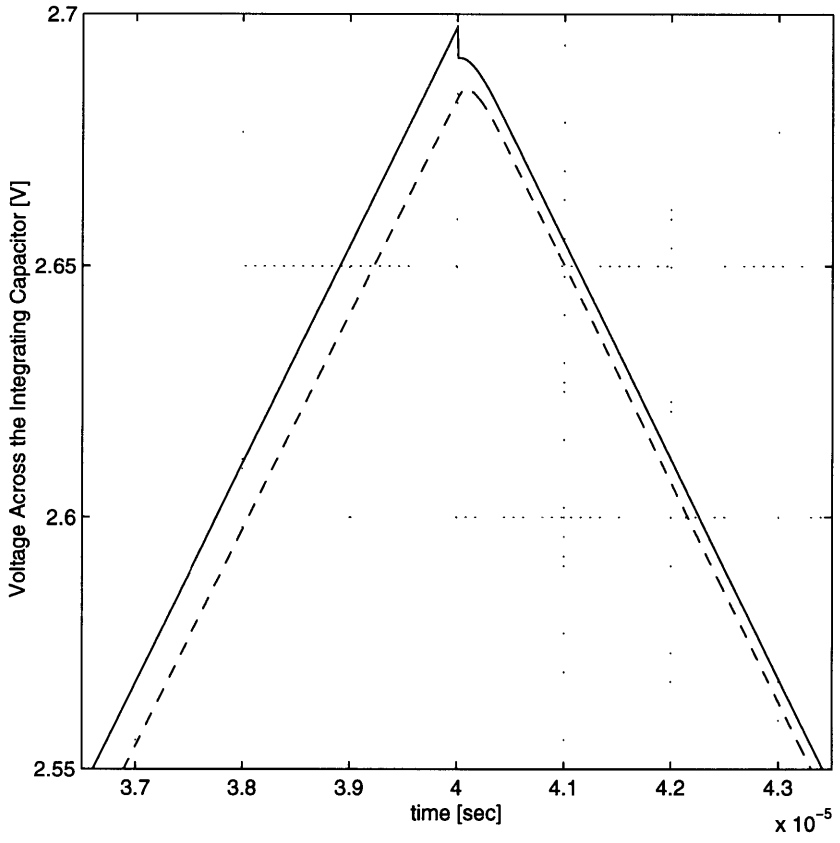


Figure 3.7: Effect of the new toggle switch in the integrating capacitor voltage.

3.4 Pixel

The current–mode design calls for an input current flowing *from* the positive power supply *to* the integrating capacitor, which suggests that at least one PMOS transistor is needed in the pixel. The other requirements demanded from the pixel were:

1. **High fill factor**

   It is desirable to devote most of the available area to the collection of photogenerated charge in order to improve the pixel sensitivity, but the presence of NMOS and PMOS transistors in the same pixel severely hurts the fill factor because the layout rules

demand a substantial separation between a well and the active areas outside the well; consequently it seems that the pixel implementation should only include PMOS devices.

2. **Small Area**

   It is important to minimize the area of the pixels to pack more of them in the sensing array and increase the spatial resolution.

3. **High Sensitivity**

   There is a direct relationship between the sensitivity of the pixel and the length of the photon integration time. If a given light intensity can produce the same variations in the pixel output in a shorter period of time, then it would be possible to decrease the photon integration time and consequently increase the frame rate of the imager.

4. **Electronic Shutter**

   As it was described in Chapter 2, the system digitizes one row of the sensing array at a time, so barring some extra changes in the system, the image would be made of lines that do not correspond to the same exact moment in time; this could lead to smeared images if elements in the scene that it is being captured move too fast. A shutter solves this problem by sampling and memorizing the scene at fixed intervals, so its behavior is similar to a sample and hold block in that both create intermediate storage for slower systems. Due to physical reasons a mechanical shutter is not well suited for imagers with high frame rates, consequently the option that is left is to implement an electronic shutter in the pixel.

5. **High Output Resistance**

   The switched–current cell needed a high output resistance to avoid nonlinearities during the fixed–current phase. The same reasoning applies to the pixel where a high output resistance is needed to avoid nonlinearities, in this case, during the fixed–time phase.

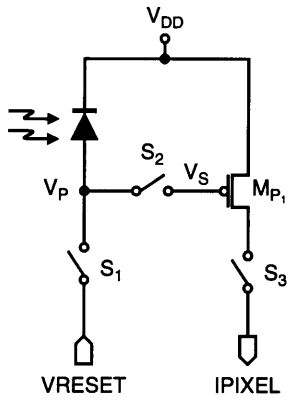


Figure 3.8: Pixel implementation.

3.4.1 Pixel Implementation

The pixel architecture chosen for the design is shown in Figure 3.8 [44]. This circuit has the following phases of operation:

Reset Phase

Here switches S_1 and S_2 are closed while the switch S_3 is opened. The anode of the photodiode and the gate of transistor M_{P_1} settle to a certain reset voltage V_{RESET} that should be below the power supply so as to reverse bias the photodiode.

Photon Integration Phase

Here switch S_1 is opened, and consequently the voltage across the photodiode is free to change over time. The photogenerated holes accumulate in the gate capacitance of transistor M_{P_1} and therefore the voltage at this node (V_S) increases. If the illumination that the pixel receives is constant, then the process can be modeled as a DC photocurrent charging a capacitor; this is the particular scenario depicted in Figure 3.9.

Output Phase

The photon integration phase ends the moment switch S_2 is opened. As a result of

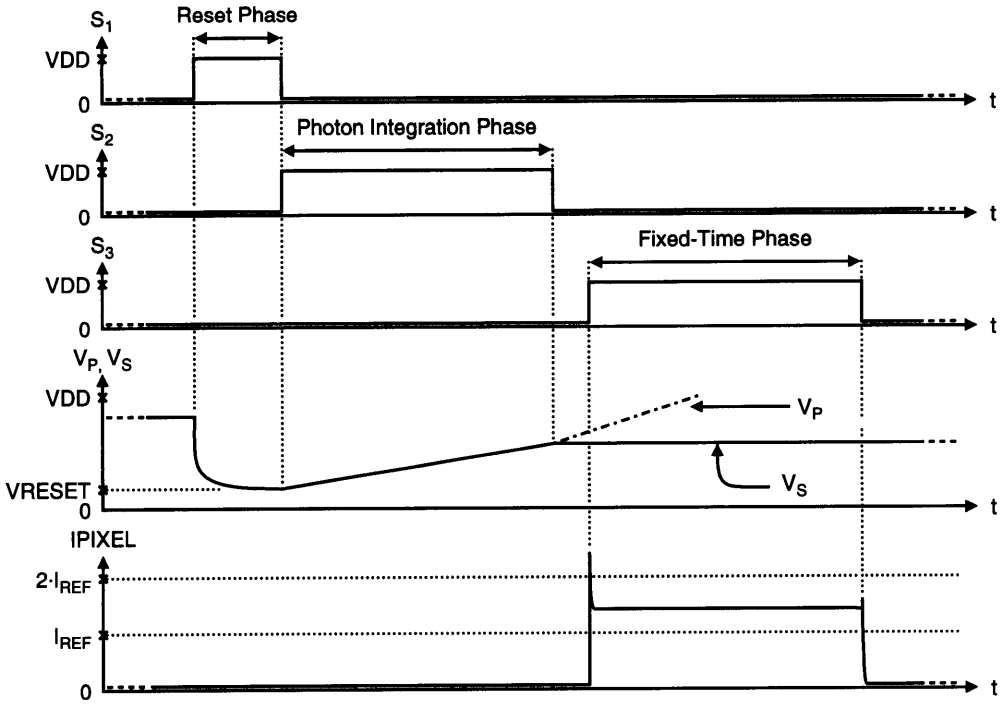
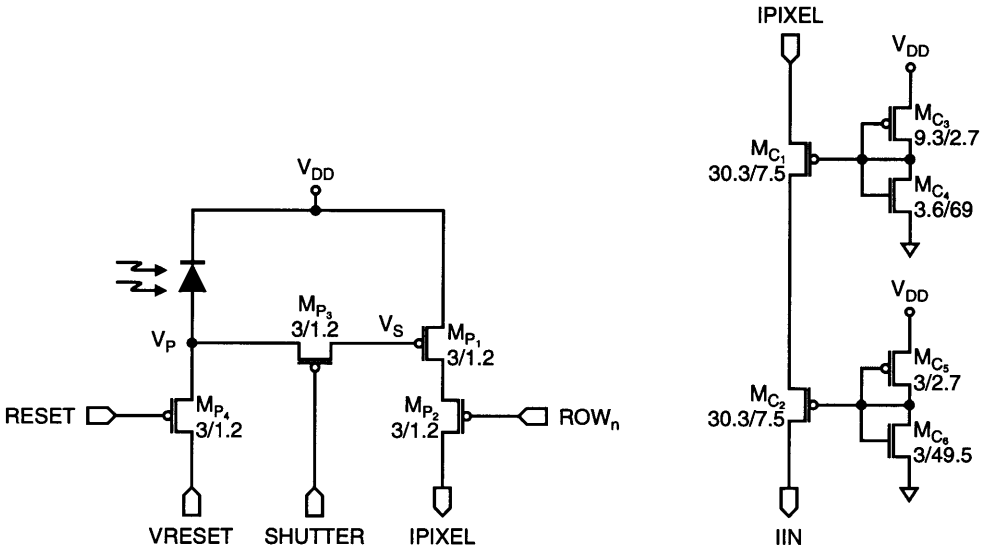


Figure 3.9: Pixel phases of operation.

this, the gate of transistor M_2 is isolated so this node can be used as the memory element needed to implement the electronic shutter. When the converter is ready to read the pixel, switch S_3 is closed, and a current which is ideally proportional to the square of $V_{DD} - V_S$ flows out of the pixel. As the controlling signal of switch S_2 is common to all the pixels, the entire image is stored in the array *at the same time*, so smearing problems are reduced to a minimum.

Figure 3.10 (a) shows the final design used in the prototype ASIC. As in the case of the switched–current cell, the switch transistors of the pixel are not the shortest allowed by the CMOS14TB technology; in this case the motivation was to minimize the leakage currents in order to have a better SNR at nodes V_P and V_S. It should be noted that the photogenerated currents are in the picoampere range, so the reverse saturation currents of the switches junctions are a real concern.



(a) Pixel.

(b) Column double cascode.

Figure 3.10: Final pixel design.

The pixel architecture chosen also has the advantage of providing some antiblooming suppression. If the p^+–diffusion area that acts as the photodiode receives a very strong illumination, all the excess charges generated are likely to be swept by the transistor action of a lateral PNP bipolar device formed by the photodiode/p^+–diffusion (P), n–well (N) and p–substrate (P) layers (Figure 3.11). This parasitic transistor also prevents photogenerated carriers from reaching the node V_S during the output phase or from wandering to other pixels, so crosstalk between adjacent pixels is minimized [44]. Figure 3.11 also shows that in the layout the topmost metal layer (Metal 3) was used both as a power bus and as a light shield.

The pixel had a very low output resistance due to the naturally higher channel–length modulation parameter (λ_p) of the PMOS transistors and the short length of M_{P_1}. This situation could not be solved by stretching the transistor because the fill factor would have been extremely small in that circumstance, and even then the resistance

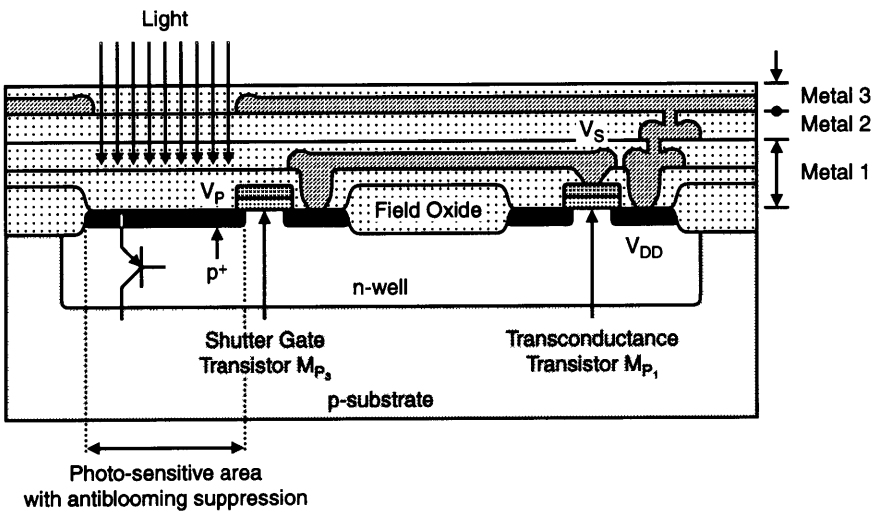


Figure 3.11: Pixel cross-section.

would not have been as high as needed. For this reason a double cascode structure was introduced, and its final design can be seen in Figure 3.10 (b). The fill factor and the size of the pixel made it impossible to accommodate these two transistors plus their associated biasing networks in the pixel, so they were placed at the bottom of the sensing array, one per column.

An unexpected benefit of the new switching scheme described in Section 3.3 was that the pixel operated in a region where a greater sensitivity could be achieved. In the mentioned section it was established that the pixel range would have to go from I_{REF} to $2 \cdot I_{REF}$ instead of from 0 to I_{REF} as before. Figure 3.12 shows the drain current of transistor M_{P_1} (the output current of the pixel) versus the voltage at the gate of this transistor, V_S, which is directly proportional to the illumination received.

It can be seen that for the original toggle switch design, the input range of the pixel was $[2.25\text{V}, 2.5\text{V}]$; in contrast, the new switching scheme creates a pixel with an input range of $[2.12\text{V}, 2.25\text{V}]$, so the input range has been cut in half, from 250mV to 130mV. This is a very important result because small photocurrents can then produce bigger changes in the pixel output current. Additionally, the mobility degradation effects in this case are helpful

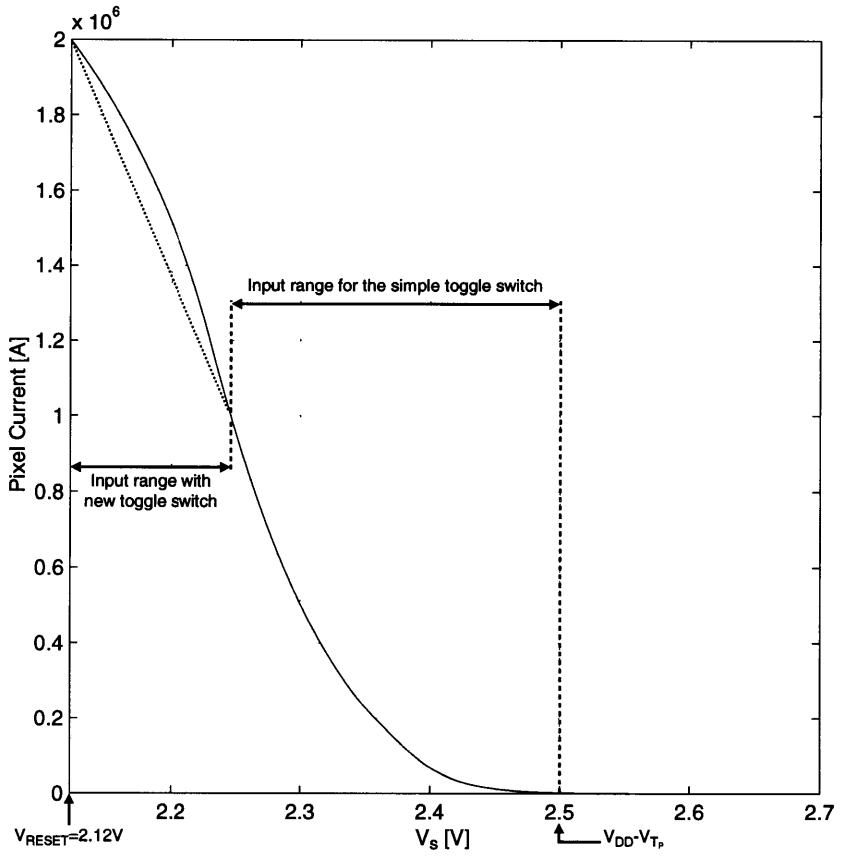


Figure 3.12: Pixel output current vs. photogenerated voltage.

because they linearize the response of the pixel, as it can be seen in the upper portion of Figure 3.12. Table 3.4 summarizes the main characteristics of the pixel while Table 3.5 and Table 3.6 summarize the dimensions of the transistors used in the pixel and in the column double cascode.

3.5 Comparator

The last block to be designed was the comparator. This subsystem posed a particular challenge because it needed to be precise, fast, dissipate very little power, work in a continuous-time fashion and also have some type of offset cancelation. Several alternatives

Table 3.4
Pixel characteristics

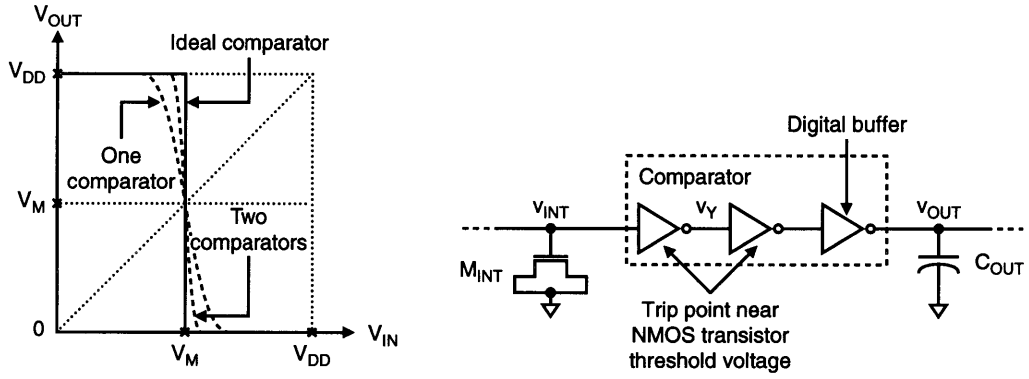
Parameter	Variable	Magnitude
Transistor count	–	4
Output current range	–	1μA
Input voltage range	–	130mV
Fill factor	–	18%
Output resistance	$R_{OUT_{PIXEL}}$	3.8GΩ
Output capacitance	$C_{OUT_{PIXEL}}$	56fF
Output noise current	$3 \cdot \sqrt{i^2_{PIXEL}}$	1.5nA
Nominal reset voltage	V_{RESET}	2.12V
Actual area	A_{PIXEL}	900μm^2

Table 3.5
Dimensions of the pixel transistors

Device	Width/Length
M_{P_1}	3/1.2
M_{P_2}	3/1.2
M_{P_3}	3/1.2
M_{P_4}	3/1.2

Table 3.6
Dimensions of the column double cascode

Device	Width/Length
M_{C_1}	30.3/7.5
M_{C_2}	30.3/7.5
M_{C_3}	9.3/2.7
M_{C_4}	3.6/69
M_{C_5}	3/2.7
M_{C_6}	3/49.5



(a) Ideal comparator and inverter chain transfer characteristics.

(b) Circuit implementation.

Figure 3.13: Chain of digital inverters used as a voltage comparator.

were explored, including a high gain operational amplifier running in an open loop configuration and various positive feedback/DRAM latches. The opamp was not as fast as needed and the latches were extremely fast but could not be offset canceled or could not operate at all times.

Finally, a new approach was taken. As seen in Figure 3.13 (a), from a behavioral standpoint a properly designed chain of digital inverters like the one of Figure 3.13 (b) has a transfer characteristic very similar to that of an ideal comparator. This idea was first used by Boonstra [45] and it is a very clever way of implementing a small, low power, fast, continuous–time comparator. The caveat is that the design is not very flexible: the reference voltage, the voltage against which the input voltage is compared, cannot be set externally because it depends on the dimensions of the transistors in the inverters (especially the ones in the first stage); also, the range of reference voltages is limited to the interval $[V_{DD} - V_{T_P}, V_{SS} + V_{T_N}]$, which for the CMOS14TB technology is about 1.68V, barely over 50% of the power supply range.

The offset cancelation of the comparator is done using the so–called chopper stabilization. This scheme puts the first inverter in unity gain mode, as shown in Figure 3.14. Here

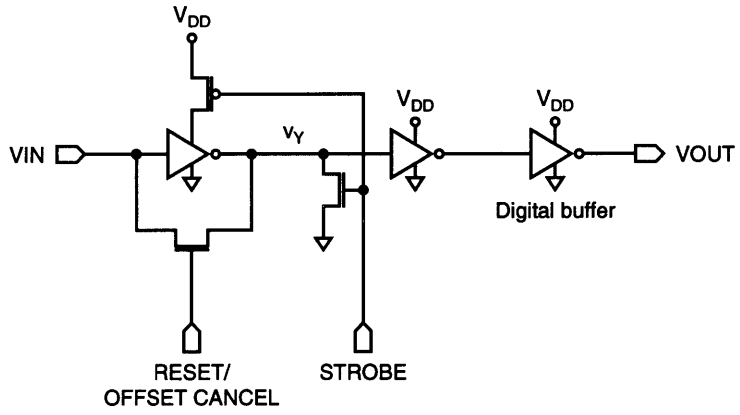


Figure 3.14: Scheme to reduce the currents caused by the overlap capacitors.

the trip point of the inverter (V_M) is stored in the input capacitor, which in this case is also the integrating capacitor. One of the nicest features of the dual–slope ADC is that the conversion results are independent of the actual reset voltage, a fact that enabled the use of the offset cancelation switch as the reset mechanism of the integrating capacitor. Therefore the reset voltage is approximately equal to the trip point of the converter and there is no risk of placing the capacitor in the weak inversion or cut–off regions because V_M is always greater than the NMOS transistor threshold voltage.

There was an additional issue to resolve in this comparator considering that it was going to be used in a current–mode converter. The gate–to–drain overlap capacitors of both the NMOS transistor ($C_{ov_{GS}}|_{NMOS}$) and the PMOS transistor ($C_{ov_{GD}}|_{PMOS}$) in the first inverter injected a current i_{INV} to the integrating capacitor following the relationship

$$i_{INV} = (C_{ov_{GD}}|_{PMOS} + C_{ov_{GS}}|_{NMOS}) \cdot \frac{\partial (v_Y - v_{INT})}{\partial t} \tag{3.3}$$

where v_Y is the output voltage of the first inverter. According to this expression there is an unwanted current added to the input current during the fixed–time phase and to the reference current during the fixed–current phase. In the latter case the problem is not all

that significant because the reference current is much bigger than the current caused by the overlap capacitors; on the contrary, the pixel current can be comparable to i_{INV} depending on the illumination received by the pixel, so clearly this current should be eliminated during the fixed–time phase. The solution implemented was to first reduce the width of the transistors in the inverter to minimize the magnitude of the overlap capacitors and second, to ground the output node of the first digital inverter as it can be seen in Figure 3.14. The function of the transistors gated by the STROBE signal is to pull v_Y close to the lower rail after the reset phase and during the entire fixed–time phase.

The modifications introduced in the circuit took care of the changes in v_Y, but v_{INT} does change over time, so i_{INV} was still present in the system. Fortunately the current caused by the overlap capacitors is signal dependent as it is a function of the rate of change in the integrating capacitor voltage: small input currents –which are the main concern– generate a small $\Delta v_{INT}/\Delta t$ and thus i_{INV} is very small, so it seems that though the current caused by the overlap capacitors could not be completely eliminated, at least it was reduced to a point were it did not affect the conversion process.

Figure 3.15 shows the actual implementation of the comparator. The first two stages were designed to have a trip point close to $1V$ (the targeted reference voltage) while the last stage was used as a buffer with a centered trip point.

Transistor M_{CO_8} was introduced to solve a glitch in the output discovered in the simulations: when the input current is small, the maximum voltage across the integrating capacitor is fairly close to the reset voltage, so during the fixed–current phase v_{INT} rapidly goes below the reference voltage and eventually settles to a value close to ground. When the conversion process is finished, the reset phase starts. Immediately after transistor M_{CO_4} turns "on", a charge redistribution process takes place between the integrating capacitor and the output capacitor of the first inverter. As the integrating capacitor is huge, the starting point of the reset phase for both nodes is very close to the voltage that C_{INT} had just before the reset phase, approximately 0V. After this redistribution both nodes start to climb up to the trip point of the inverter; however, this happens slowly enough that the drop in v_Y to a logic zero value propagates all the way to the output causing a glitch that

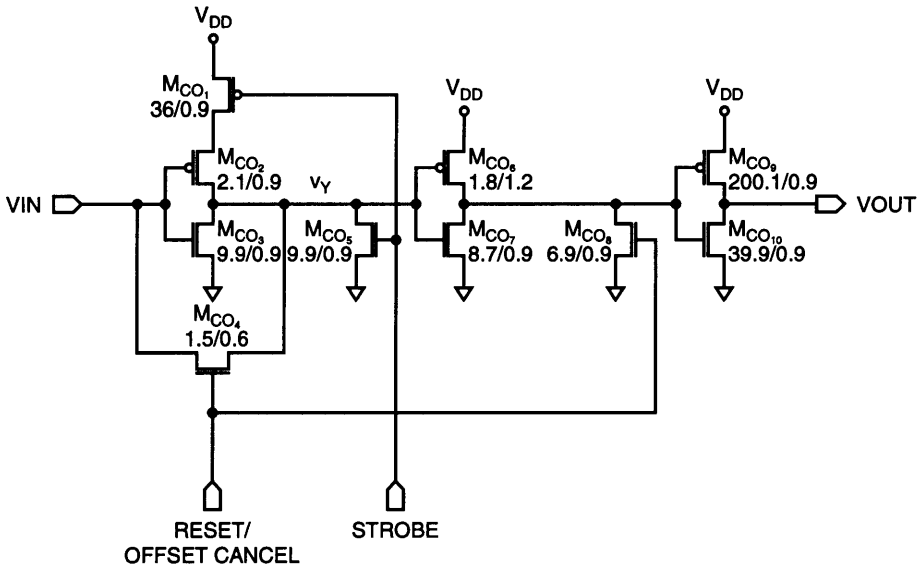


Figure 3.15: Final comparator design.

might latch a new count and consequently erase the result of the conversion. Transistor M_{CO_8} ensures that the output of the comparator will remain a logic one throughout the reset phase.

Figure 3.16 shows the behavior of the comparator with and without the i_{INV} reduction circuitry, in this case for an input current $I_{PIXEL} = 1.5\mu$A. As can be seen, without transistors M_{CO_1} and M_{CO_5} the output of the first inverter decreases in a linear fashion towards ground when the reset phase ends, and consequently the current caused by the overlap capacitors is nearly constant. Though it seems that the magnitude of these currents is insignificant, it should be noted that an LSB of the converter is about $1\mu\text{A}/2^8$, or approximately 4nA.

Another interesting fact from the curves of Figure 3.16 is that the end of the conversion finds the voltage across the integrating capacitor near ground, a situation that occurs every time the input current is not very close to I_{REF}. There are two points that can be drawn

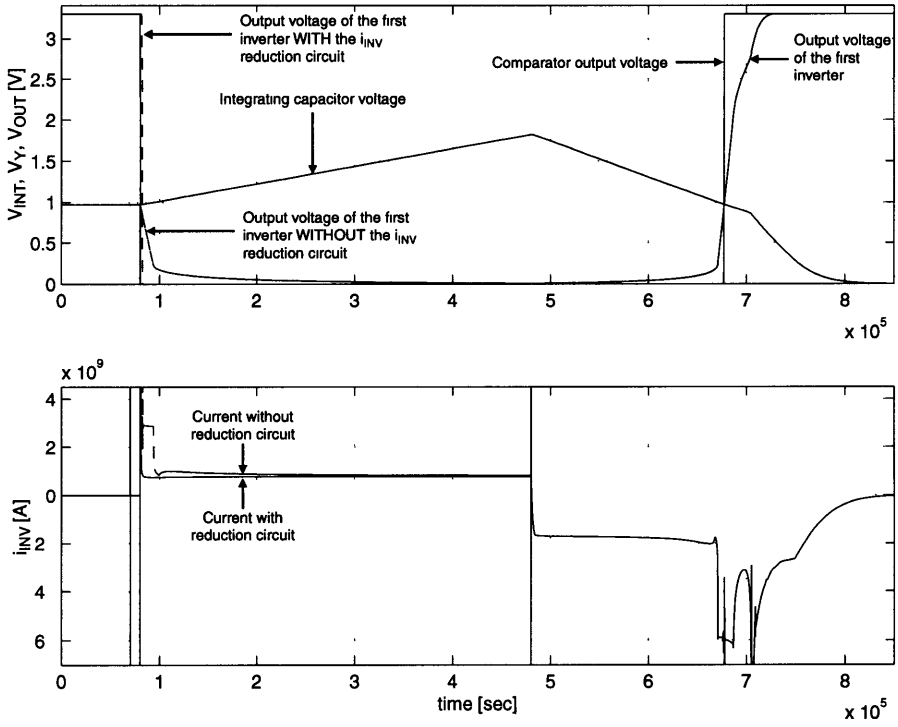


Figure 3.16: Transient comparator behavior.

from this observation:

- The SI cell ends up in the linear region, but this is not a problem because the conversion process ends well before the cell enters this low resistance region.
- The SI cell refresh process will frequently start from ground. When the sample switch in the cell closes, there is yet another charge redistribution process between the output capacitance of the cell and the gate capacitance of transistor M_1, which will significantly lower the initial gate voltage of this transistor. Consequently the refresh process is clearly a large–signal one. Section A.1 studies this issue in detail.

Table 3.7 summarizes the main characteristics of the comparator while Table 3.8 summarizes the dimensions of the transistors used in this system.

Table 3.7
Comparator characteristics

Parameter	Variable	Magnitude
Transistor count	–	10
Nominal reference voltage	V_{REF}	1V
Nominal propagation delay @ C_{OUT} = 30pF	t_{pd}	20nsec
Nominal rise/fall time @ C_{OUT} = 30pF	t_{rf}	4.2nsec
Sensitivity	S_{COMP}	300μV
Area	A_{COMP}	3600μm^2

Table 3.8
Dimensions of the comparator transistors

Device	Width/Length	Device	Width/Length
M_{CO_1}	36/0.9	M_{CO_6}	1.8/1.2
M_{CO_2}	2.1/0.9	M_{CO_7}	8.7/0.9
M_{CO_3}	9.9/0.9	M_{CO_8}	6.9/0.9
M_{CO_4}	1.5/0.6	M_{CO_9}	200/0.9
M_{CO_5}	9.9/0.9	$M_{CO_{10}}$	39.9/0.9

3.6 Full Pseudo–Converter

To minimize the design cycle and the total area of the prototype ASIC some blocks originally proposed to be integrated were taken out of the chip, as shown by Figure 3.17. Basically the subsystems that were removed were the counter and the RAM memory, and this is the reason why the the comparator needed a buffer stage. The load capacitance of this buffer was estimated at 30pF, which includes the internal junction capacitance of the final inverter, the distributed capacitance of the metal line stretching from the converter to the pad, the package capacitance and the test board line capacitance up to the external latch.

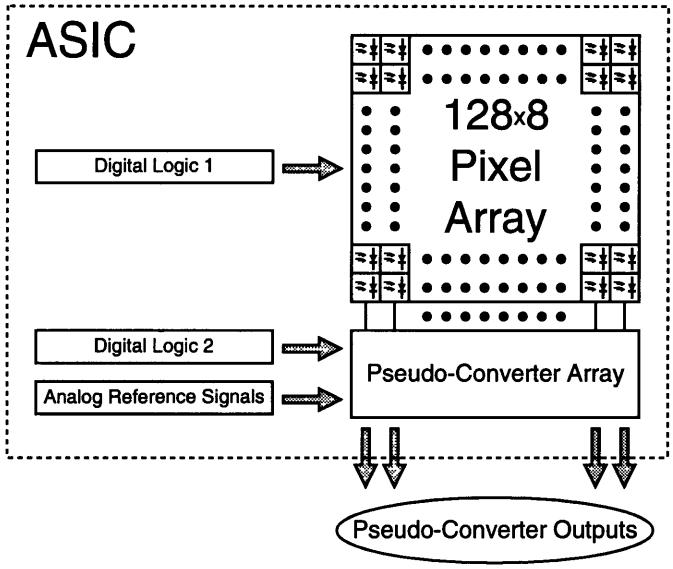


Figure 3.17: Blocks that were integrated in the prototype ASIC.

Figure 3.18 shows the complete pseudo–converter at a transistor level. The only addition that was not previously described is a NOR gate that controls the access of the SI cell to the temporary load. Figure 3.6 (b) showed a signal called $TEMPLOAD$ controlling the transistor switch M_{TL}, but the final implementation used a simple logic block in order to reduce the signals that were to be generated outside the pseudo–converter. In this scenario the NOR gate ensures that the SI cell is *always* connected to the temporary load anytime SAMPLE is low. When the LOAD signal experiences a low to high transition all the SI cells are disconnected from the common temporary load and subsequently connected to the different integrating capacitors. With this simple addition there is no extra control signal needed thus both the circuit layout and the test board are greatly simplified.

Table 3.9 summarizes the most important characteristics of the pseudo–converter. It may seem that the power dissipation should be close to $V_{DD} \cdot I_{REF}$, but it is a little bit higher than that because the power dissipation of the different blocks in the pseudo–converter is so small that the current transients contribution to the total power dissipation is no longer insignificant.

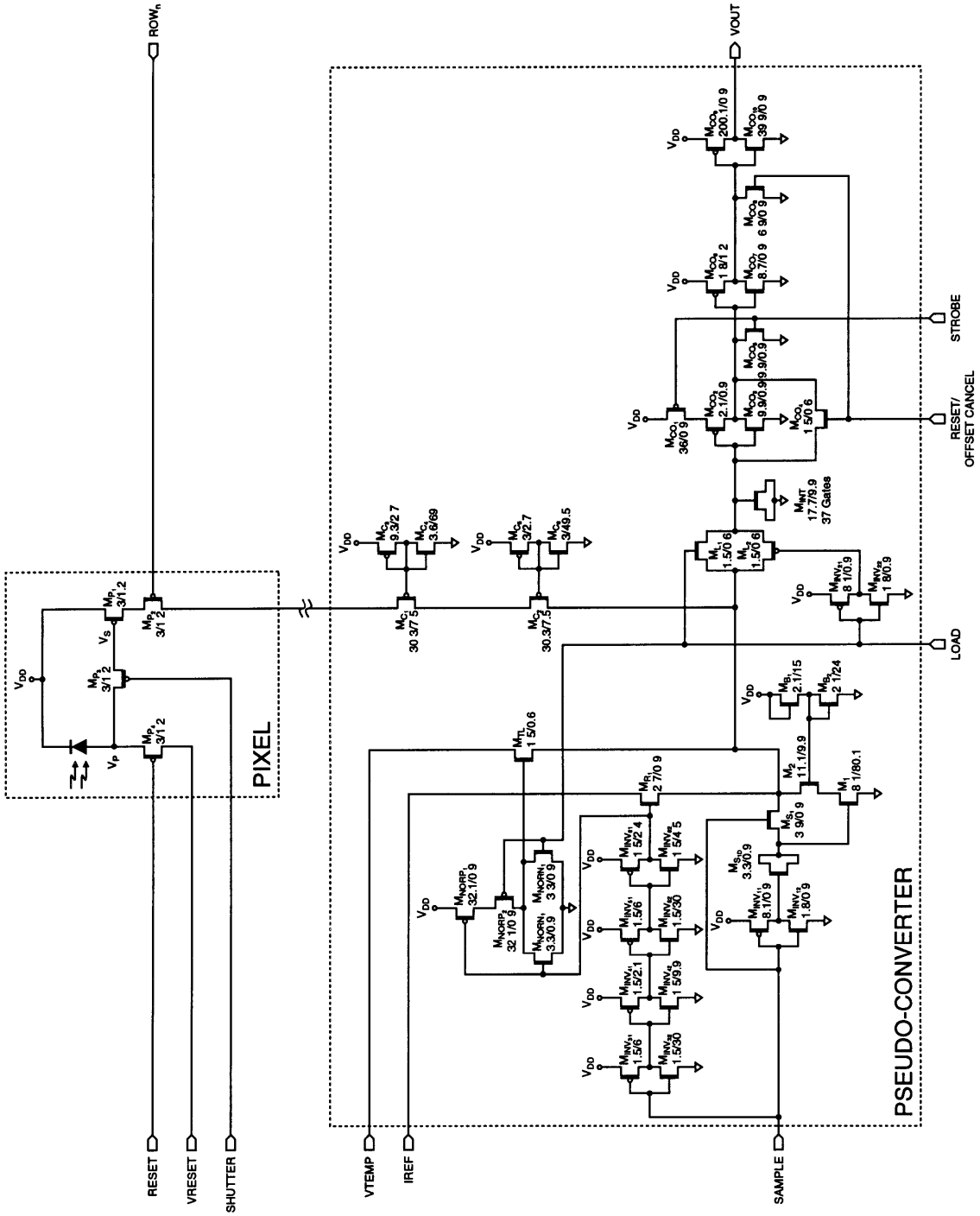


Figure 3.18: Pseudo–converter final design.

Table 3.9
Pseudo–converter characteristics

Parameter	Variable	Magnitude
Transistor count	–	43
Nominal power dissipation	P_{CONV}	60μW
Precision	–	8 bits
Power supply	V_{DD}	3.3V
Area	A_{CONV}	0.03mm^2

Figure 3.19 shows the response of the pseudo–converter for different pixel currents. As a result of the careful design there are no glaring nonlinearities at the switching points (the end of the reset phase and the end of the fixed–time phase) so it is expected that the converter array will achieve the desired specifications.

3.7 Summary

This chapter described the pseudo–converter and the pixel used in the experimental integrated circuit at a transistor level. A local delay block was added to the architecture of the original switched–current cell to reduce the copy–to–reference error. A cascode structure was also added to the cell in order to improve the linearity of the conversion process during the fixed–current phase. A switching scheme was devised to minimize the charge injection in the integrating capacitor of the pseudo–converter, with this new scheme the channel charge of the switches always have a path to ground other than the integrating capacitor. A comparator made of two digital inverters was presented, and the offset cancelation mechanism of this system is also used as the reset switch for the the integrating capacitor. Spurious currents caused by the first inverter of the comparator were identified as an additional source of error in the conversion process, and modifications to the original design were introduced to eliminate these currents during the relevant phases of operation. An active pixel with five PMOS transistors was described, and a column double cascode was designed to improve the linearity of the conversion process during the fixed–time phase.

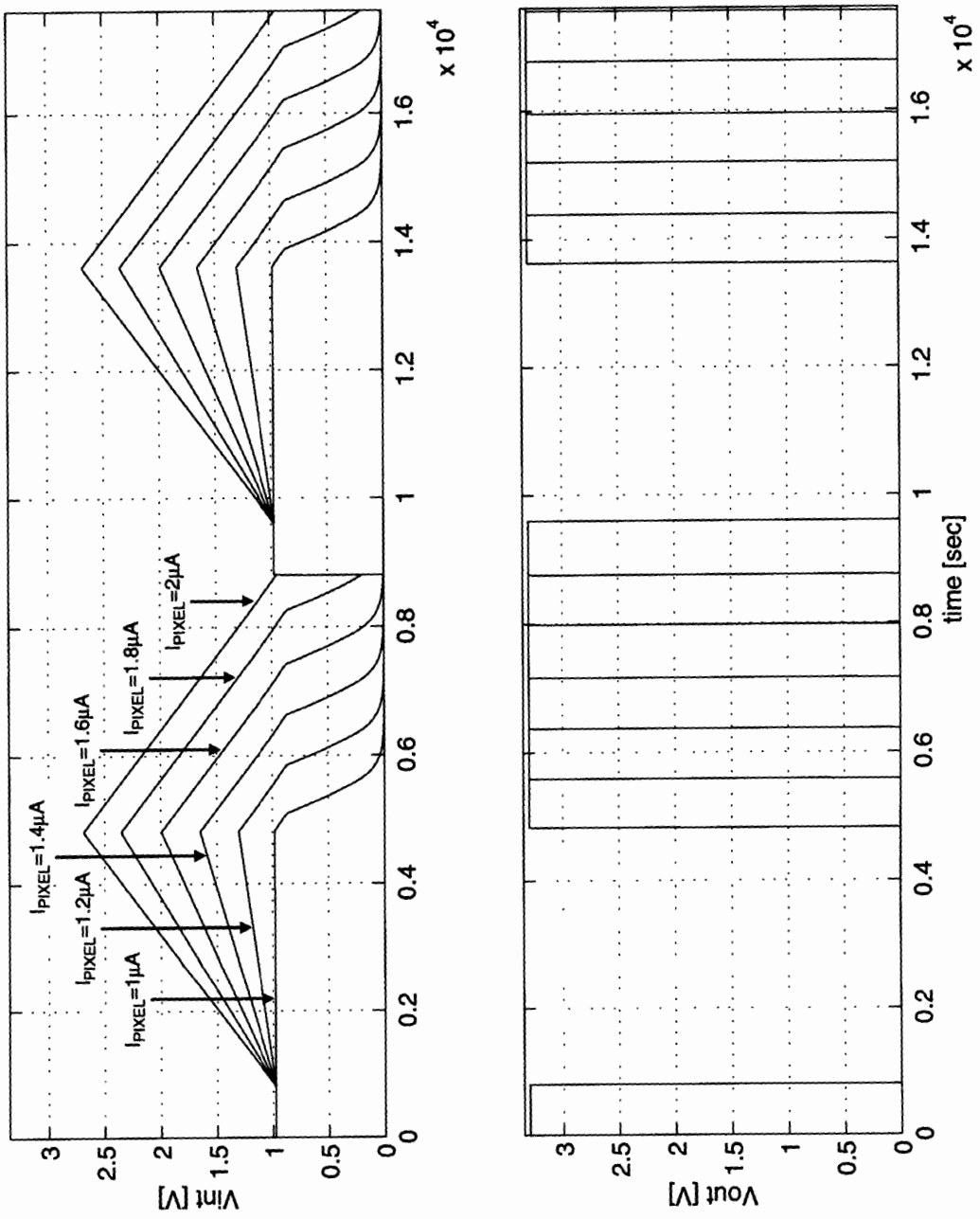


Figure 3.19: Pseudo–converter response for different pixel currents.

Chapter 4

Control Logic, Test Structures and Layout

4.1 Control Logic

In the first generation of the imager the majority of the control logic is implemented in the test board, but still several digital subsystems needed to be integrated in the ASIC to make a complex system like the imager work and to ease the design of the mentioned test board.

4.1.1 Sample Signals Generation

With the introduction of the local delay block in the current copier only one sample signal was needed per cell (Subsection 3.1). Still 8 control signals were left so a decoder was integrated in order to generate these control signals and help reduce the pin count of the package. This system was designed using a "pseudo–CMOS" NOR array as Figure 4.1 shows. The decoder gives a great flexibility to the system because the input bits can be created with a simple 3 bit counter, and thus the settling time of the SI cells can be controlled by adjusting the frequency of the counter clock. An ALL signal had to be introduced to logically disable the decoder to avoid glitches in the output. The concern is

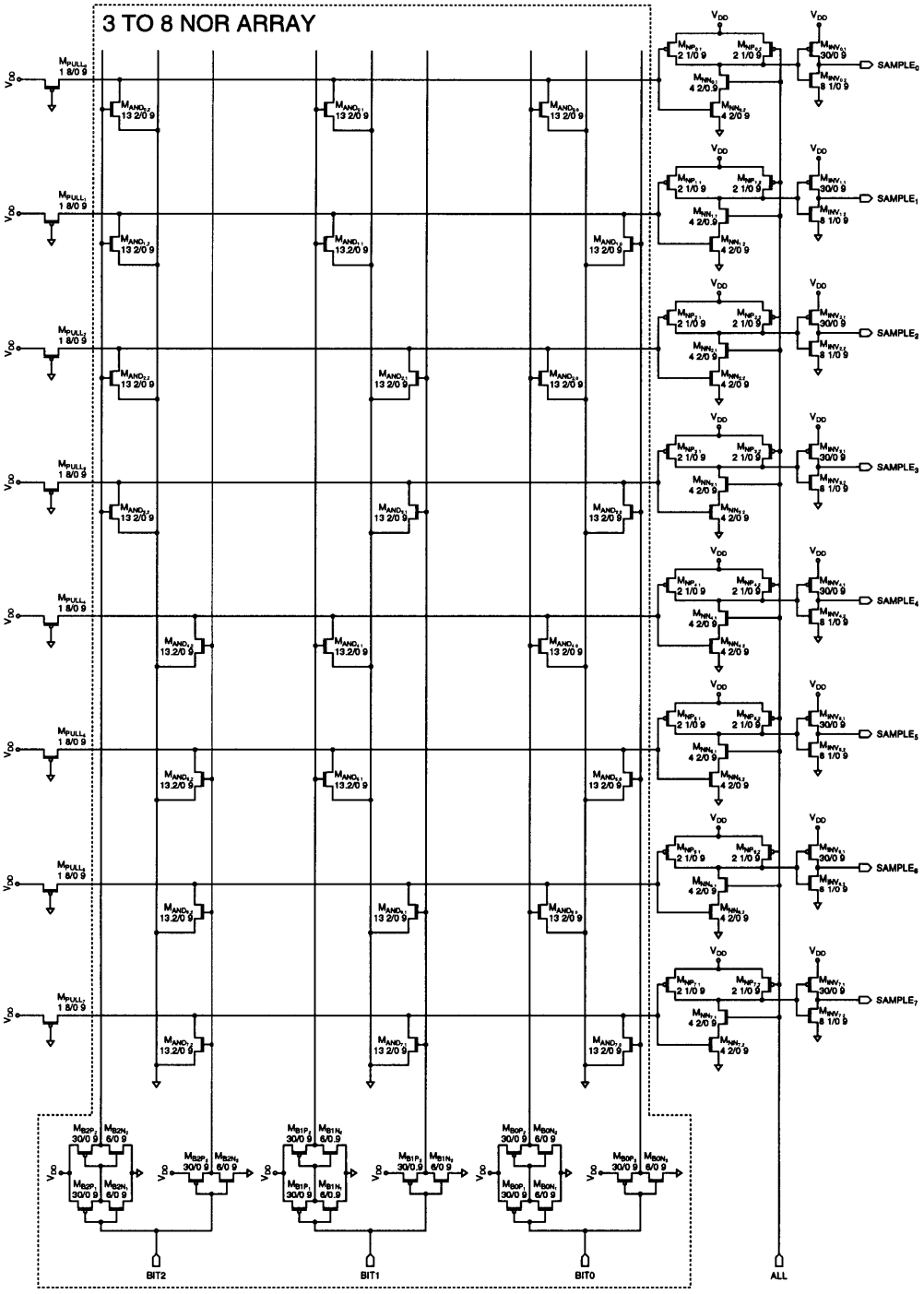


Figure 4.1: Generation of the sample signals for the switched–current cells.

that the counter bits may not change states simultaneously, for example, the least significant bit may be altered very quickly while the most significant bit may only be altered when the changes have rippled through the digital system. Consequently there might be a short transition period where the count has an erroneous value that can cause "spikes" in some SAMPLE lines. These spikes are extremely harmful because they change the voltage at the storage capacitor of the SI cell (the gate of transistor M_1 in Figure 3.2) in an irreversible way until the next refresh cycle. Therefore the ALL signal is used as a gating function so that the count can freely change whenever ALL is low, the spikes then may appear at the input of the NAND gates but they do not reach the output of the decoder.

4.1.2 Pixel Array Row Selector

Yet another decoder was integrated to generate the ROWn signals for the sensing array. This 7–to–128 decoder was implemented with the same NOR array used to generate the SAMPLE signals, as shown in Figure 4.2. In the case of the previous decoder no action was taken to cut the static power dissipation of the "pseudo–CMOS" logic because the array was very small, but 128 lines can dissipate a huge amount of power; therefore a DOFF signal was introduced so that the array could be turned "off" all the time except during the fixed–time phase. A PNONE signal was also implemented to place all the row signals in a high state and consequently disable the pixel array.

4.1.3 Bias Selector

The cascode structures used in the design, especially the column double cascode had very tight specifications in terms of the voltage drop they needed to operate. To counteract any possible process variations that could significantly change the bias voltages of these structures, a bias selector was introduced in the prototype, as shown by Figure 4.3.

When the BIE signal is high the bias voltages for the cascodes come from three external voltage sources, ECBSI for the SI cell cascode, ECBCT for the upper transistor in the column double cascode, and ECBCB for the lower transistor in the column double cascode. When BIE is low the internal bias networks are used to provide the appropriate voltages.

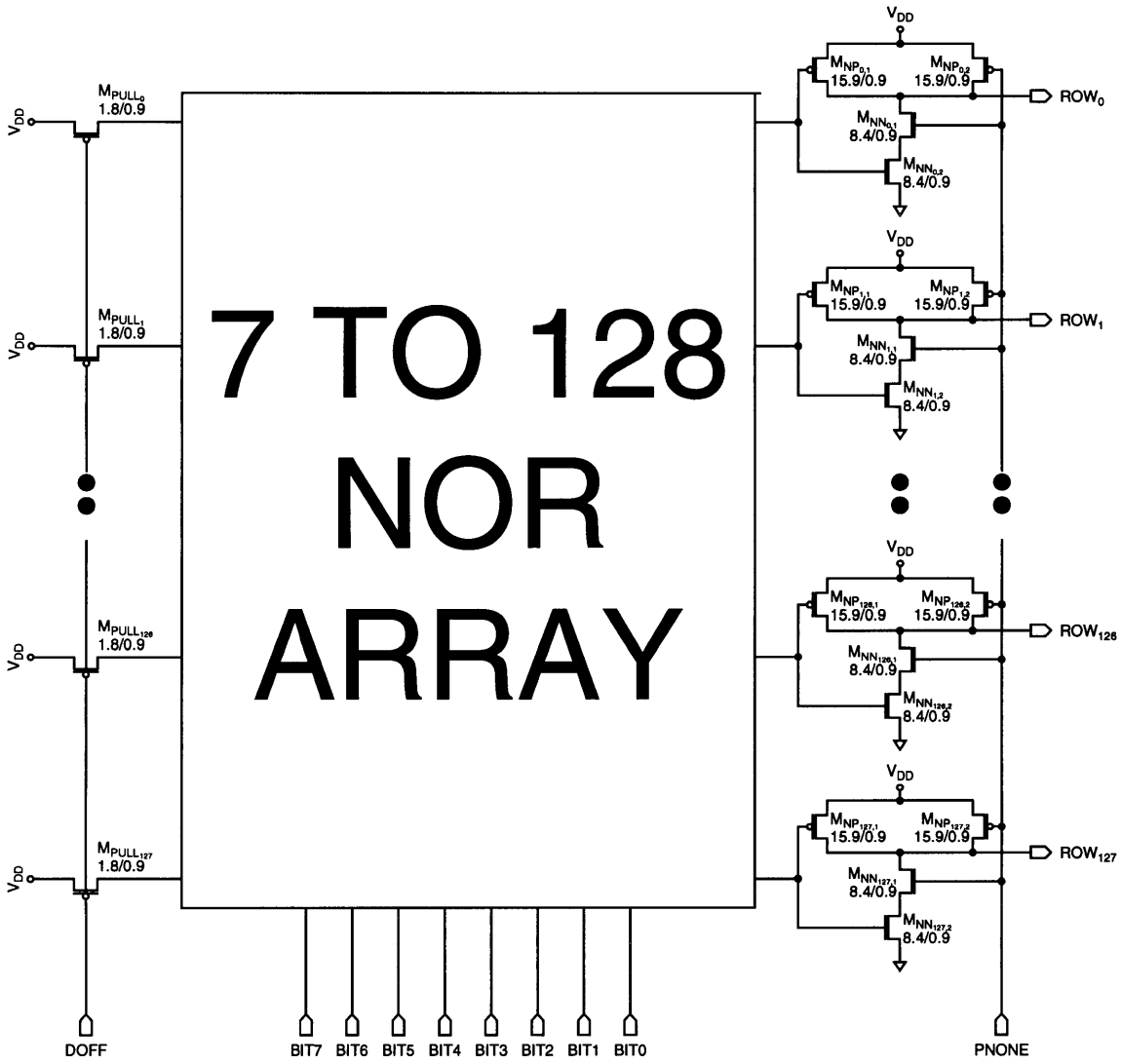


Figure 4.2: Row decoder for the pixel array.

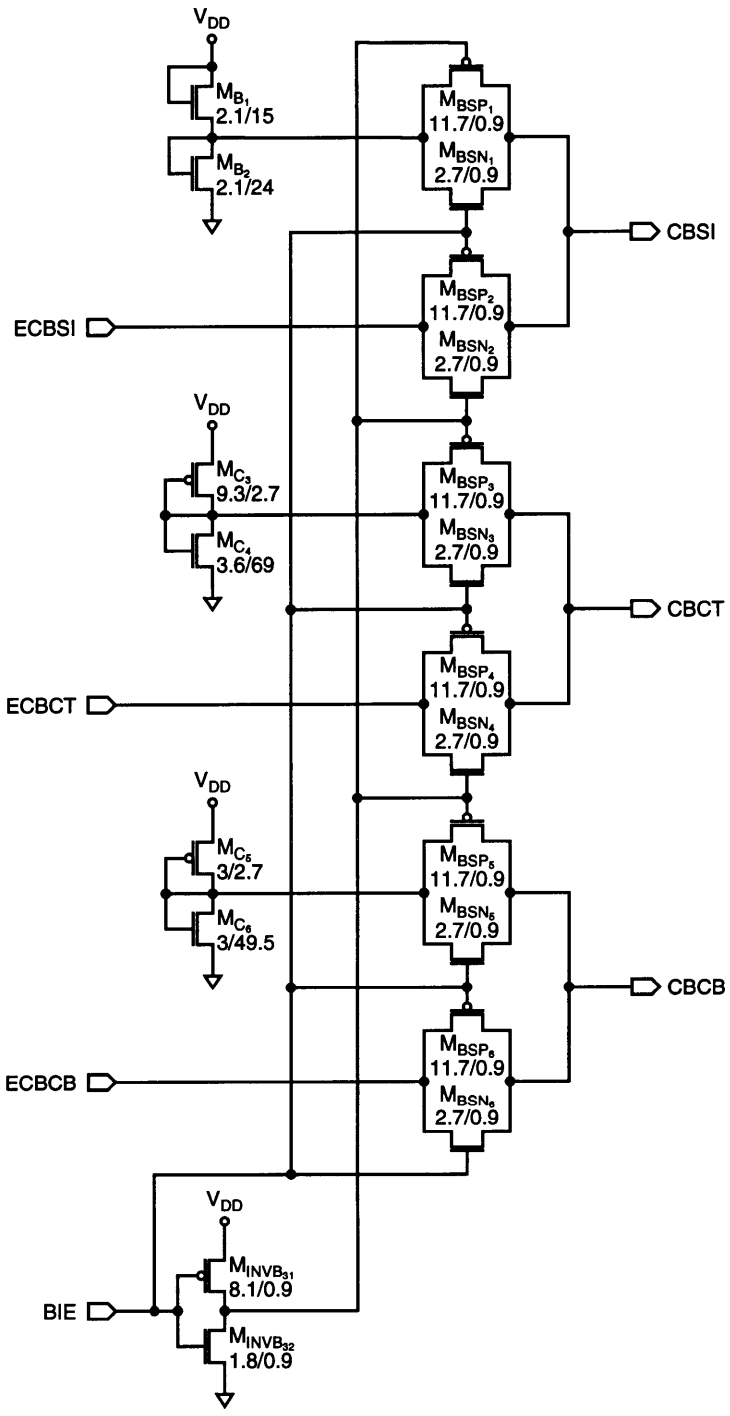


Figure 4.3: Cascodes bias selector.

4.2 Test Structures

Several structures were added to the prototype ASIC to achieve the following objectives:

- Allow the independent testing of all the major blocks in the system.
- Get hard data that could be used in the debugging process of the circuit.
- Increase the testability of the system.

4.2.1 Circuits for ADC Characterization

The first of these structures was placed in the pseudo–converter, as it can be seen in Figure 4.4. The IIE signal selects the source of the converter input current; when IIE is low the converter array digitizes the pixel currents, but when IIE is high a single converter digitizes an external current source IEXT. The specific converter to be used is chosen via the CONVERTER SELECT BUS, a trio of signals that go to the system of Figure 4.5. This decoder is common to the converter array and its transistor–level implementation is the same that was used in the system of Section 4.1.1. The function of this block is to generate the signals $\mathrm{SEL}_0 \ldots \mathrm{SEL}_7$ or turn all of them to a high state when IIE is low. With these two additions it is possible to characterize each ADC in the array separately by selecting it and sweeping IEXT from 1μA to 2μA. This process then gives the necessary data to plot the transfer characteristic of all the converters so that individual metrics like DNL, INL and gain error can be extracted. The same data can also be used to determine the actual matching of the converters in the array by simply comparing their individual transfer characteristics.

The NPIXEL signal is a control signal that follows the relationship

$$NPIXEL = (ROW_0 \bullet ROW_1 \bullet \cdots \bullet ROW_{126} \bullet ROW_{128}) \tag{4.1}$$

In other words NPIXEL is a gating function that emulates the row select signals of the pixel array.

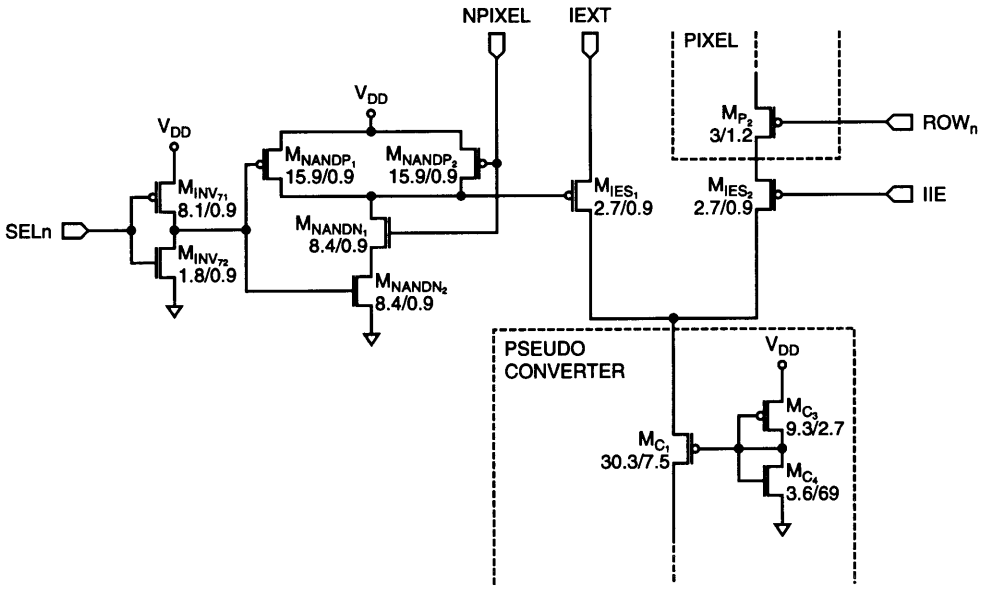


Figure 4.4: Converter input current selector.

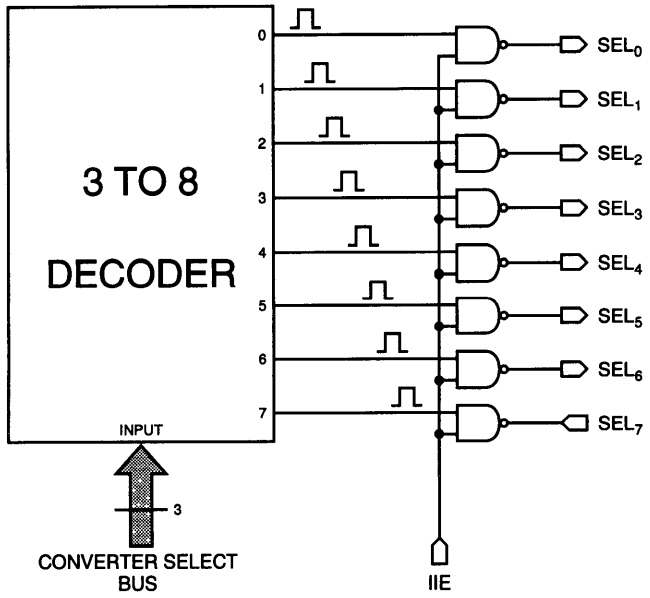


Figure 4.5: Generation of the select signals for individual converters.

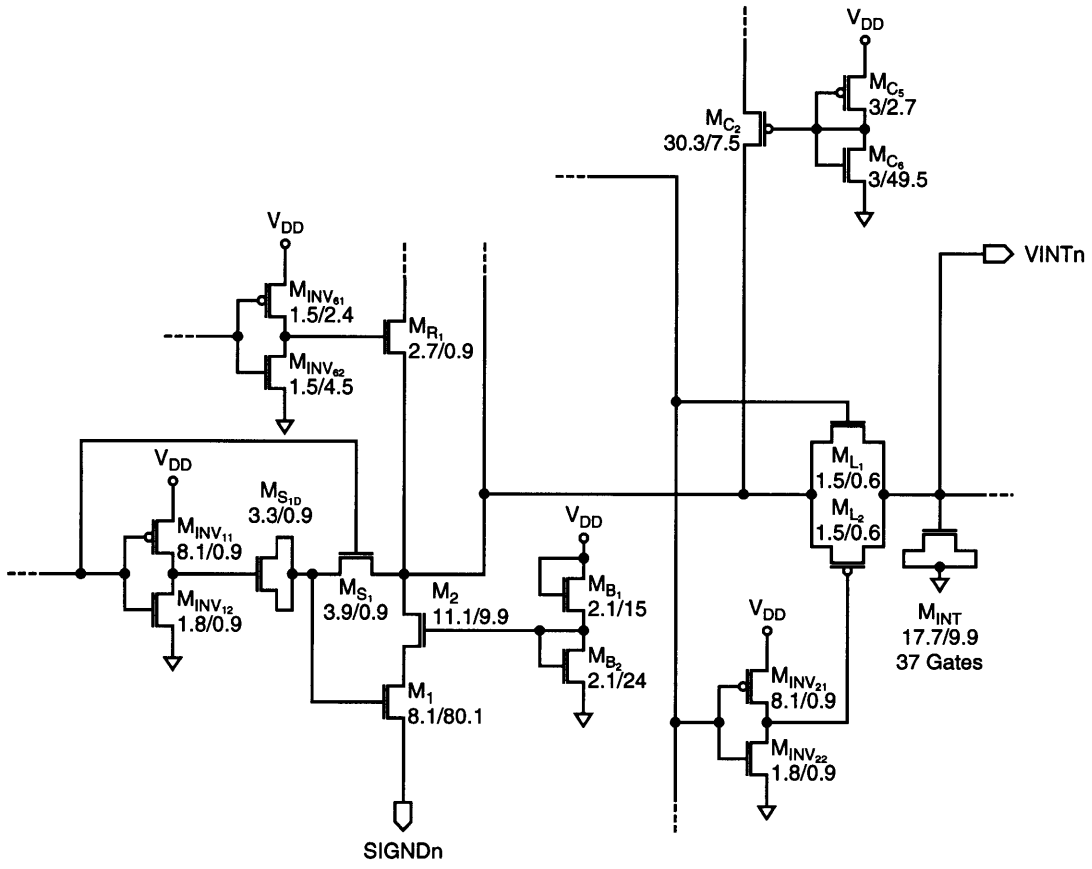


Figure 4.6: Nodes that were taken to external pins for debugging purposes.

4.2.2 Circuits for Testing Individual Blocks

The second alteration of the circuit for testing purposes can be seen in Figure 4.6. This section of the pseudo–converter shows that two nodes of the circuit are taken to the exterior: the integrating capacitor terminal and the source of transistor M_1, the transconductance of the SI cell. These two nodes plus the reference current terminal IREF (Figure 3.18) enable the testing of the different blocks of the converter:

- When the SI cell is its the sample phase, the voltage at IREF is equal to the gate voltage of transistor M_1, so this terminal can be used to measure the actual voltage settling behavior of the cell.

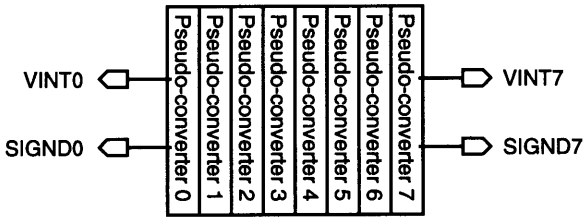


Figure 4.7: Converters that were chosen for debugging purposes.

- SIGNDn can be used to monitor the evolution of the copied current of the SI cell. The results obtained here can be used to calculate the current matching between the different SI cells.

- VINTn is a major diagnostic tool. Being the most important node of the converter, it can be used to measure the actual value of the integrating capacitance (with the aid of an external current source IEXT of known magnitude), it can be used to identify the phase where eventual nonlinearities occur, it can be used to measure the reset voltage (the trip point of the first digital inverter of the comparator), etc.

- It is also possible to completely characterize the behavior of the comparator using VINTn (the input node of the comparator) and OUTn.

As it can be seen in Figure 4.7 only the first and last pseudo–converters are used for debugging purposes. The main reason for this is that taking SIGNDn and VINTn to external pins breaks the symmetry of the array layout, and consequently there might be some extra variations in the process parameters that could lead to a higher mismatch between the ADCs. Also, the terminal VINTn adds the package capacitance to C_{INT} so the maximum voltage at this node will be smaller that the targeted 2.75V of the other converters.

4.3 Layout

4.3.1 Pixel

The CMOS14TB process silicides all the exposed active areas to minimize their resistance, including the p^+–diffusion that acts as the cathode of the photodiode. Unfortunately this layer is opaque to visible light, so the optical efficiency of the pixel is degraded. To partially counteract this deleterious effect, the area of the pixel was increased and ended up being a square with 30μm sides, as shown in Figure 4.8. The control signals were laid out in Metal 1, and they run horizontally, RESET and VRESET at the top, SHUTTER and ROWn at the bottom. The column line IPIXEL is laid out in Metal 2, and runs vertically along the rightmost edge of the pixel. The transistors were placed at the corners of the square so as to leave most of the central area for the photodiode. The reset switch is at the upper left corner while the shutter and row switches together with the transconductance transistor M_{P_1} are at the lower right corner.

The entire sensing array sits in a single n–well, so body plugs in each pixel were needed to maintain the required bias locally. These plugs were laid out in an "L"–shaped fashion to also provide electrostatic repulsion so that no photogenerated carriers can drift out of the active area. The pixel architecture with its lateral PNP transistor and these plugs greatly enhance the antiblooming properties of the sensing array and also contribute towards a low crosstalk between adjacent pixels.

4.3.2 Pads

The pads for the input and output analog signals did not have any diode protection because this type of circuits limit the range of the input voltages to the power supply range. This was deemed unsuitable for a prototype chip because it cuts the flexibility of the testing process and limits the number of experiments that can be performed with the ASIC.

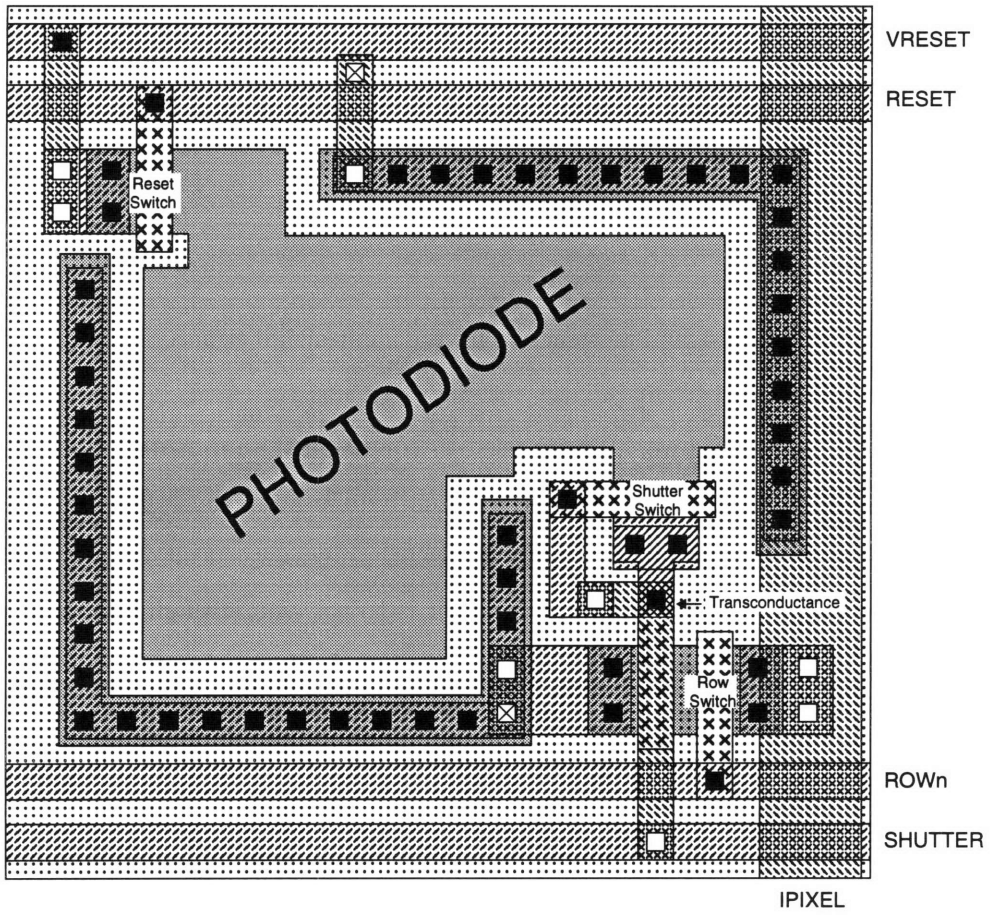


Figure 4.8: Pixel layout.

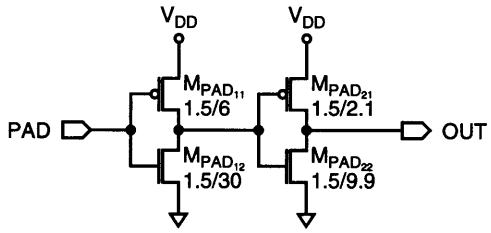


Figure 4.9: Pad structure for the input digital signals.

Buffers like the one in Figure 4.9 were used to condition the input digital signals. The majority of the commercial parts that could eventually be used in the test board operate in TTL levels of 0V to 5V; unfortunately the CMOS14TB process was designed for a maximum power supply of 3.3V so the function of the buffer is to act as a level shifter. In the event that the test board can also operate at 3.3V levels, these buffers only add a minor delay to the control signals.

4.3.3 Pseudo–Converter

As it was stated in Section 3.6 the converters should have a narrow pitch of 30μm to match the width of the pixel. Consequently the pseudo–converter layout is a thin long strip, as shown in Figure 4.10. This illustration also shows that nearly half the length of the system is occupied by the integrating capacitor, an inevitable consequence stemming from its large magnitude. The comparator also occupies a more significant portion of the layout than originally anticipated, but this is mainly because a buffer stage is required to drive the external capacitance. This will not be a concern in future generations of the design if the RAM is integrated, as the load capacitance of a memory cell is significantly smaller than the 30pF the comparator is now designed to drive.

Figure 4.10: Pseudo–converter layout.

4.3.4 Imager

Figure 4.11 shows the complete imager layout, including the pad frame. The row selector seems to occupy a significant portion of the total area, but it should be pointed out that this happens because the sensing array is only 8 columns wide. Vertically the die is constrained by the pixel and pseudo–converter arrays, but horizontally the die is constrained by the pad size and their minimum allowed separation. The die shown in Figure 4.11 has a width of 2.5mm and a length of 6.3mm for a total area of approximately $16mm^2$.

Figure 4.12 shows a schematic representation of the pad frame and the signals that are assigned to each pad. The package used was a PGA 65, Kyocera part number KD–P86542–A, which has a 0.4" cavity. The correspondence between the pads and the pins in the package can be seen in Figure 4.13, and Table 4.1 briefly describes the functionality of each pin.

4.4 Summary

This chapter described a pixel array row selector and a decoder that generates the sample signals of the switched–current cells, two circuits that were needed to improve the functionality of the ASIC. A bias selector was also introduced in the chip to have a backup system in the event that process variations significantly alter the built–in bias voltages. Several structures that enhance the testability of the system were also presented; they include a selector that enables the characterization of every converter in the array, four nodes that were taken to external pins for circuit debugging purposes, a subsystem to measure the current of the pixel array and digital level shifters. The layout of the pixel and the rest of the blocks in the chip was described, as well as the pad frame and package used.

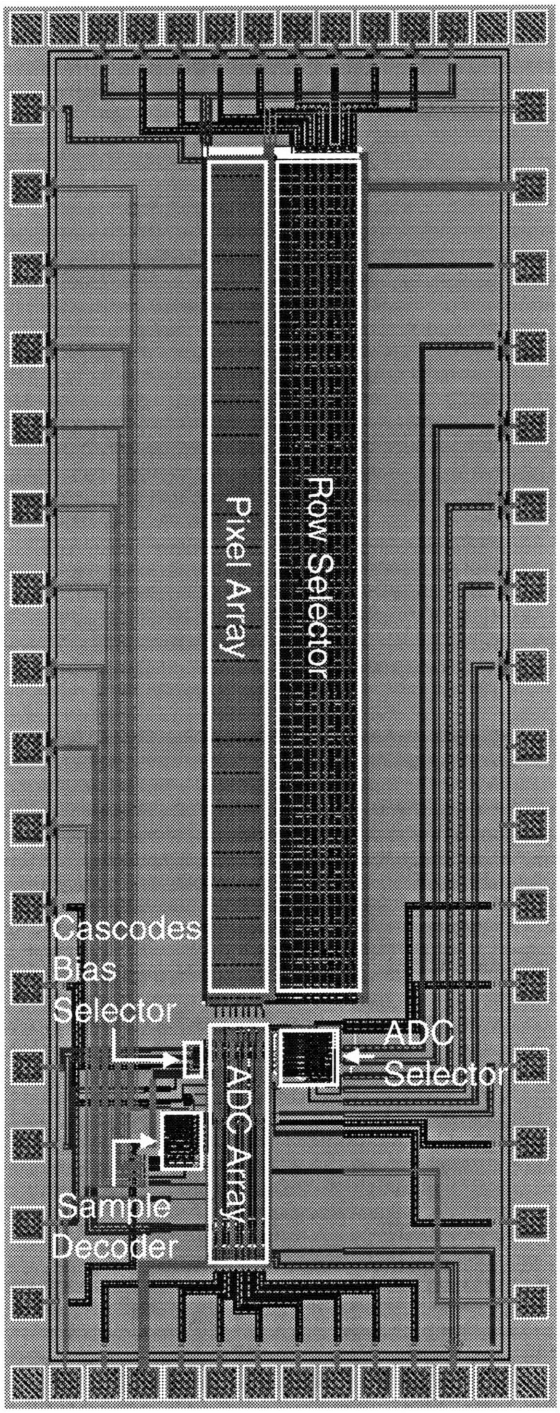


Figure 4.11: Complete imager layout.

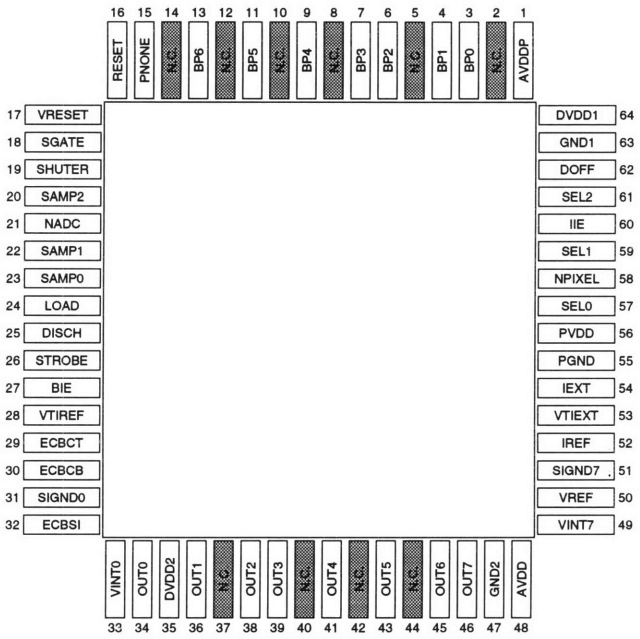


Figure 4.12: Prototype ASIC pad frame.

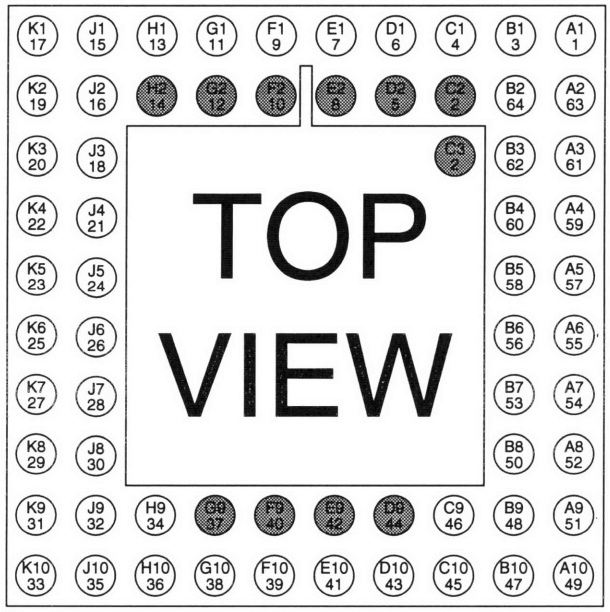


Figure 4.13: Prototype ASIC package.

Table 4.1
Prototype ASIC pins description

Pin	Mnemonic	Description
1	AVDDP	Pixel array positive power supply
2	N.C.	No connection
3	BP0	Pixel array row selector bit 0 (LSB)
4	BP1	Pixel array row selector bit 1
5	N.C.	No connection
6	BP2	Pixel array row selector bit 2
7	BP3	Pixel array row selector bit 3
8	N.C.	No connection
9	BP4	Pixel array row selector bit 4
10	N.C.	No connection
11	BP5	Pixel array row selector bit 5
12	N.C.	No connection
13	BP6	Pixel array row selector bit 6 (MSB)
14	N.C.	No connection
15	PNONE	Pixel array row selector disable signal
16	RESET	Pixel array reset signal
17	VRESET	Pixel array reset voltage
18	SGATE	SI cell sample signal decoder disable signal
19	SHUTER	Pixel array shutter signal
20	SAMP2	SI cell sample signal decoder bit 2 (MSB)
21	NADC	Pseudo–converter selection decoder disable signal
22	SAMP1	SI cell sample signal decoder bit 1
23	SAMP0	SI cell sample signal decoder bit 0 (LSB)
24	LOAD	Pseudo–converter load switch control signal
25	DISCH	Comparator offset cancelation control signal/ Pseudo–converter reset control signal
26	STROBE	Comparator disable signal
27	BIE	Cascodes bias source selector
28	VTIREF	Temporary load for the master reference current source
29	ECBCT	External bias for the column cascode upper transistor
30	ECBCB	External bias for the column cascode lower transistor
31	SIGND0	Source terminal of pseudo–converter 0 SI cell transconductance transistor
32	ECBSI	External bias voltage for the SI cell cascode transistor

continued on next page

continued from previous page

Pin	Mnemonic	Description
33	VINT0	Pseudo-converter 0 integrating capacitor terminal
34	OUT0	Pseudo-converter 0 output
35	DVDD2	Digital systems positive power supply 2 (of 2)
36	OUT1	Pseudo-converter 1 output
37	N.C.	No connection
38	OUT2	Pseudo-converter 2 output
39	OUT3	Pseudo-converter 3 output
40	N.C.	No connection
41	OUT4	Pseudo-converter 4 output
42	N.C.	No connection
43	OUT5	Pseudo-converter 5 output
44	N.C.	No connection
45	OUT6	Pseudo-converter 6 output
46	OUT7	Pseudo-converter 7 output
47	GND2	Ground 2 (of 2)
48	AVDD	Analog systems positive power supply
49	VINT7	Pseudo-converter 7 integrating capacitor terminal
50	VREF	Temporary load for the master reference current source
51	SIGND7	Source terminal of pseudo–converter 7 SI cell transconductance transistor
52	IREF	Master reference current source input terminal
53	VTIEXT	Temporary load for the external converter input current source
54	IEXT	External input current source
55	PGND	Pad buffers ground
56	PVDD	Pad buffers positive power supply
57	SEL0	Pseudo–converter selection decoder bit 0 (LSB)
58	NPIXEL	Gating control signal for the input current selector circuit
59	SEL1	Pseudo–converter selection decoder bit 1
60	IIE	Converter input current source selector
61	SEL2	Pseudo–converter selection decoder bit 3 (MSB)
62	DOFF	Pixel array row selector "on"/"off" control signal
63	GND1	Ground 1 (of 2)
64	DVDD1	Digital systems positive power supply 1 (of 2)

Chapter 5

Conclusions

Certainly parallelism is one of the first tools that is used when the speed of a system needs to be increased. However, the introduction of parallelism to an analog circuit is not a simple task as there are new constraints that have to be met. In this thesis, the system that was parallelized was an an analog–to–digital converter, a challenging system to design in its own right. For a stand–alone converter errors of the ideal transfer characteristic should be bounded within a certain interval to achieve a functional, monotonic system; but once the converter is placed in an array, the error interval is reduced even more to achieve a good matching between all the units. Section 1.4 showed that for machine vision applications the matching between the converters in the array needed to be the highest possible, a maximum difference of one bit between all the units in the array. The particular requirements of a column–parallel imager were addressed with two novel concepts described in Chapter 2, the current–mode dual–slope converter and the distributed converter architecture.

Though the current mode approach was chosen primarily to drastically reduce the power dissipation of the converter array, it also ended up being the most appropriate for a seamless integration of the pixel and converter arrays. In contrast to a charge–output pixel where a preamplifier is required to provide some drive capability, a current–output pixel has the ability to input its signal directly to the ADC, with the obvious silicon area and power dissipation savings that this imply. Section 3.4.1 also showed that whenever a transistor is relatively free of mobility degradation, the sensitivity of the current–output pixel is greatly

influenced by the reset voltage of the pixel array. This happens because the result of the light illumination (charge) is *not* the output of the pixel. The transconductance transistor then not only changes the domain of the signal (charge to current) but also provides amplification at the same time. This feature is unique to the current–output pixel because in the case of the charge–output pixel the result of the light illumination *is* the output, and in the case of the voltage–output pixel, an amplifier would require at least an additional transistor which would reduce the fill factor.

5.1 Possible Design Modifications

In terms of the relative magnitude of the different components of the novel converter, the most positive effects can be achieved by reducing the reference current:

⊕ **Lower power dissipation**

Though part of the power dissipation resides in the current transients, an important part is also created by the reference current flowing through the transconductance transistor of the switched–current cell.

⊕ **Smaller switched–current cell transconductance transistor**

A high output resistance is needed from the SI cell to maintain a good degree of linearity in the conversion process. As to the first order the output resistance of an MOS transistor is inversely proportional to the drain current, a smaller reference current would be able to reduce the size of the transconductance transistor in the SI cell while maintaining the same output resistance.

⊕ **Higher pixel sensitivity**

The average transconductance decreases with the reference current following a square root relationship while the total output current range of the pixel decreases linearly with the reference current, so the overall pixel sensitivity increases with a lower reference current.

⊕ **Smaller Integrating Capacitance**

The magnitude of the integrating capacitor is directly proportional to the reference current, so there is a huge area reduction to be gained with every reduction in the reference current source magnitude.

⊖ **Lower switched–current cell SNR**

Through some simple derivations based on the results of Section A.2 it can be proved that the noise of the SI cell is proportional to $I_{REF}^{\frac{3}{4}}$, thus the signal–to–noise ratio of the cell *decreases* proportionally to $I_{REF}^{\frac{1}{4}}$, so a significant reduction of the reference current may limit the precision of the system.

⊖ **Higher incidence of spurious currents**

A smaller reference current would also mean that all the spurious currents, like the currents due to the presence of the comparator overlap capacitances, would increase their importance and consequently there might be a point where new additions to the architecture (analog buffers, for example) are necessary.

It can be seen then that the system would enormously benefit from a reduction in the reference current. This action coupled with a migration to a fabrication process designed for lower power supplies can make the novel current–mode dual–slope converter presented in this thesis a high–resolution, ultra–low–power converter. The two factors that limit the precision that can be achieved with lower reference currents and power supplies are the switched–current cell SNR and the switching nonlinearities in the integrating capacitor.

Unfortunately there is not too much that can be done to increase the conversion speed. The main bottleneck is the propagation delay of the continuous–time comparator, which depends largely on the fabrication process that is being used. Even with newer fabrication processes it is difficult to imagine that the propagation delay would be significantly lower than its present average value of 20nsec, so the conversion time of this particular incarnation of the dual–slope converter is not likely to be much higher than 10Ksamples/sec. The frame rate of the imager can be doubled if a second array of converters is used so that two rows can be read simultaneously, but it is obvious that this should be done when a very high frame

rate is an absolute necessity as the added area would increase the cost of the integrated circuit.

5.2 Novel Converter and Future Fabrication Processes

It is interesting to analyze what would happen to the converter design as it evolves to newer fabrication processes. The switched–current cell is highly insensitive to process parameter variations, actual process parameters magnitudes and power supplies, so this subsystem should be able to be ported to newer processes without any problem. The process transconductance parameters are likely to increase as the gate oxide thickness is being reduced from one generation to the next, so the transconductance transistor of the SI cell may have to be stretched to achieve constant operation in the strong saturation region, especially if the reference current is also reduced.

The comparator is made of digital inverters so it is inherently process independent. It should only be redesigned to set the trip point of the first inverter close to the NMOS transistor threshold voltage, which is being reduced about 20% per generation, but aside from this there should not be any future problem with this block.

The pixel architecture should also be able to remain unaltered with newer fabrication process. It is obvious that the 5 transistors in the pixel which mainly act as switches will be reduced with each generation as the the minimum transistor length is systematically shortened, but the total pixel area should also be reduced to increase the spatial resolution of the imager; consequently the fill factor is expected to remain somewhere in the 15%–25% range.

The integrating capacitor is the element which occupies the majority of the converter area. The magnitude of this capacitor will obviously change with newer fabrication processes, but it is harder to predict its future evolution as it depends on several parameters that are a function of the technology: the power supply, the NMOS transistor threshold voltage and the gate oxide thickness. In order to make a good prediction the following

assumptions were made:

- The transconductance transistor of the pixel and the column double cascode will use about 17% to 20% of the power supply range to operate.
- The trip point of the inverter is going to be in around $1.4 \cdot V_{T_N}$, where V_{T_N} is the NMOS transistor threshold voltage.
- The NMOS transistor threshold voltage is going to decrease approximately 20% per generation.

Table 5.1 and Figure 5.1 were constructed with the help of these assumptions and the National Technology Roadmap for Semiconductors [46]. It can be seen that the area of the integrating capacitor decreases continually but it stays relatively flat for future fabrication processes. This is mainly due to an also flatter oxide thickness reduction, and the roadmap only forecasts that the gate oxide should be lower than 4nm by the year 2007, so no accurate prediction can be done past this point. In any case it is evident that the total area of the integrating capacitor diminishes for future generations, more significantly in the near term and more slowly in the long term. This is an important fact because it indicates that the total area of the novel converter presented in this thesis will decrease from one generation to the other. In the description of the converter layout (Subsection 4.3.3) it was pointed out that the width of the converter should match the width of the pixel, and it was stated previously that the pixel area would more than likely be reduced to increase the spatial resolution, so the combined effect of a pixel width reduction and an integrating capacitor area reduction should combine to either keep the length of the converter constant or slightly diminish it.

Table 5.1
Evolution of the integrating capacitor area with future technologies

Gate Length [μm]	Power Supply [V]	Threshold Voltage [V]	Gate Oxide [nm]	Capacitor Area Area [μm^2]
2.0	5	0.9	40	16028
1.2	5	0.8	20	8523
0.8	5	0.75	15	6500
0.5	3.3	0.65	10	6331
0.35	3.3	0.6	8	4878
0.25	2.5	0.45	6	4808
0.18	1.8	0.35	6	4613

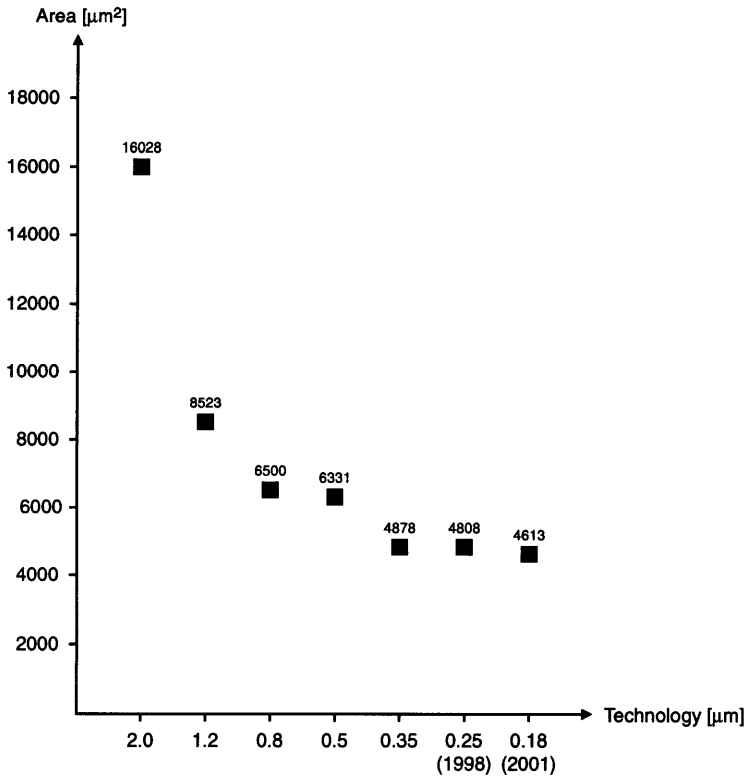


Figure 5.1: Evolution of the integrating capacitor area with future technologies.

Appendix A

Switched–Current Cell Topics

The following sections thoroughly cover some important aspects of the SI cells that are either inadequately described or outright absent in the literature. The results and derivations obtained here are used throughout the thesis.

A.1 Large–Signal Settling Behavior

Most of the material devoted to the analysis of SI cells assume a small–signal settling behavior [47]. Perhaps this is a safe assumption in the digital circuits where these cells are normally used, but as Section 3.5 shows, depending on the magnitude of the pixel current it is possible to always have a large–signal settling process in the current copier cells. Consequently it is necessary to develop a mathematical description of the sample phase in order to estimate the time that has to be alloted for the refresh process. Figure A.1 and Table A.1 will be used as an aid to this analysis.

A.1.1 Gate Voltage Settling Behavior

It will be assumed that at $t_0 = 0$ the gate capacitance is initially discharged and consequently the transistor M_1 is in the cut–off region.

Table A.1
Notation used to describe the settling behavior of an SI cell

Variable	Description
C_G	Capacitance at the gate of the NMOS transistor
v_G	Voltage across the gate capacitor C_G
i_G	Current flowing through capacitor C_G
i_D	Current flowing through the NMOS transistor
I_{REF}	Current to be copied
v_{DS}	Drain–to–source voltage of the NMOS transistor
v_{GS}	Gate–to–source voltage of the NMOS transistor
V_T	Threshold voltage of the NMOS transistor
W, L	Width and length of the NMOS transistor
μ_n	Mobility of the electrons in the NMOS transistor
C'_{ox}	Gate capacitance per unit area of the NMOS transistor
t_{sat}	Time when the NMOS transistor saturates
t_{settle}	Settling time of the SI cell

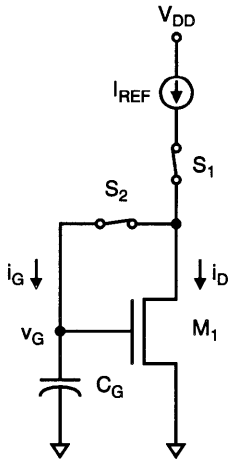


Figure A.1: Current copier in its sample or copy phase.

For $0 < v_G < V_T$

$$i_G = C_G \cdot \frac{\partial v_G(t)}{\partial t} \tag{A.1}$$

No drain current flows through the transistor so $i_G = I_{REF}$. Plugging this in Equation A.1

$$\frac{I_{REF}}{C_G} = \frac{\partial v_G(t)}{\partial t} \tag{A.2}$$

As both I_{REF} and C_G are constant

$$\frac{I_{REF}}{C_G} = \frac{\Delta v_G(t)}{\Delta t} = \frac{v_G(t) - v_G(t_0)}{t - t_0} \tag{A.3}$$

Remembering that the gate capacitance was initially discharged at the beginning of the copy process

$$v_G(t) = v_{GS}(t) = \frac{I_{REF}}{C_G} \cdot t \tag{A.4}$$

for $t \leq t_{sat}$. After this point the transistor is "on", and assuming that the resistance of switch S_2 is negligible, $v_{GS} \approx v_G$ so $v_{DS} = v_G > v_{GS} - V_T$ and transistor M_1 is always in the saturation region. Consequently,

$$I_{REF} = i_D + i_G \Rightarrow I_{REF} = \frac{\mu_n \cdot C'_{ox}}{2} \cdot \frac{W}{L} \cdot (v_G - V_T)^2 + C_G \cdot \frac{\partial v_G(t)}{\partial t} \tag{A.5}$$

Though Equation A.5 neglects the channel–length modulation, it still is a first order non–linear differential equation, a very difficult expression to solve analytically. Using

Maple V Release 3 [48] it was obtained

$$v_G(t) = V_T - \frac{\sqrt{\frac{\mu_n \cdot C'_{ox}}{2} \cdot \frac{W}{L} \cdot I_{REF}}}{\frac{\mu_n \cdot C'_{ox}}{2} \cdot \frac{W}{L}} \cdot tanh\left(-\frac{\sqrt{\frac{\mu_n \cdot C'_{ox}}{2} \cdot \frac{W}{L} \cdot I_{REF}}}{C_G} \cdot (t - t_{sat})\right) \tag{A.6}$$

for $t > t_{sat}$. Then

$$v_G(t) = V_T - \sqrt{\frac{2 \cdot I_{REF}}{\mu_n \cdot C'_{ox} \cdot \frac{W}{L}}} \cdot tanh\left(-\frac{1}{C_G} \cdot \sqrt{\frac{\mu_n \cdot C'_{ox}}{2} \cdot \frac{W}{L} \cdot I_{REF}} \cdot (t - t_{sat})\right) \tag{A.7}$$

Now

$$V_T = \frac{I_{REF}}{C_G} \cdot t_{sat} \Rightarrow t_{sat} = \frac{V_T \cdot C_G}{I_{REF}} \tag{A.8}$$

Consequently

$$v_G(t) = \begin{cases} \frac{I_{REF}}{C_G} \cdot t & t \leq \frac{V_T \cdot C_G}{I_{REF}} \\ V_T + \sqrt{\frac{2 \cdot I_{REF}}{\mu_n \cdot C'_{ox} \cdot \frac{W}{L}}} \cdot & \\ \cdot tanh\left(\frac{\sqrt{\frac{\mu_n \cdot C'_{ox}}{2} \cdot \frac{W}{L} \cdot I_{REF}}}{C_G} \cdot \left(t - \frac{V_T \cdot C_G}{I_{REF}}\right)\right) & t > \frac{V_T \cdot C_G}{I_{REF}} \end{cases} \tag{A.9}$$

An HSPICE simulation was performed to test the validity of Equation A.9. To have a greater degree of realism, an NMOS LEVEL 3 model from the CMOS14TB process was used. Table A.2 summarizes the relevant parameters of this run as well as the component values used in the simulation. Figure A.2 shows that the theoretical results closely match the simulated results.

Table A.2
Parameters used in the HSPICE settling time simulation

Parameter	Value	Units
V_T	0.7	V
$\mu_n \cdot C'_{ox}$	196.47	μA/V^2
C_G	1	nF
I_{REF}	1	μA
W/L	8.1/80.1	μm/μm

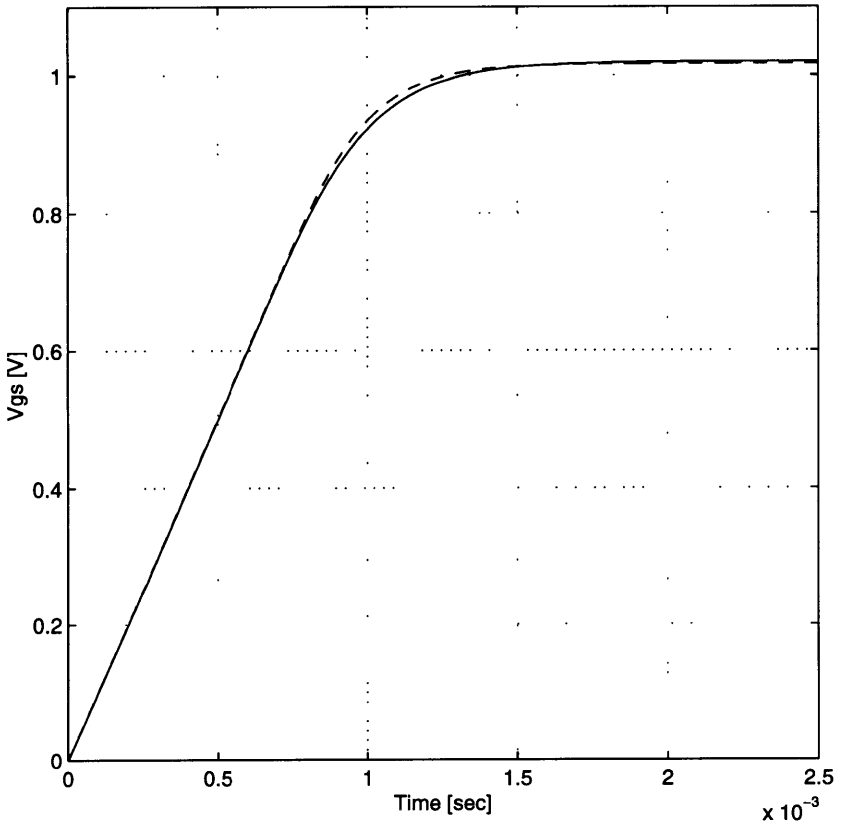


Figure A.2: Settling behavior of the gate voltage of the SI cell NMOS transistor. The solid curve is the result of the HSPICE simulation and the dashed curve is the plot of Equation A.9 with the values of Table A.2.

A.1.2 Drain Current Settling Behavior

For $0 < v_G < V_T$ the NMOS transistor is "off", and consequently $i_D = 0$; but for $v_G > V_T$ neglecting channel–length modulation

$$i_D = \frac{\mu_n \cdot C'_{ox}}{2} \cdot \frac{W}{L} \cdot (v_G - V_T)^2 \tag{A.10}$$

And plugging in the results from Equation A.7,

$$\begin{aligned} i_D = \; & \tfrac{\mu_n \cdot C'_{ox}}{2} \cdot \tfrac{W}{L} \cdot \left(V_T + \sqrt{\tfrac{2 \cdot I_{REF}}{\mu_n \cdot C'_{ox} \cdot \frac{W}{L}}} \cdot \right. \\ & \left. \cdot tanh \left(\frac{\sqrt{\frac{\mu_n \cdot C'_{ox}}{2} \cdot \frac{W}{L} \cdot I_{REF}}}{C_G} \cdot \left(t - \tfrac{V_T \cdot C_G}{I_{REF}} \right) \right) - V_T \right)^2 \end{aligned} \tag{A.11}$$

So

$$i_D = \frac{\mu_n \cdot C'_{ox}}{2} \cdot \frac{W}{L} \cdot \frac{2 \cdot I_{REF}}{\mu_n \cdot C'_{ox} \cdot \frac{W}{L}} \cdot tanh^2 \left(\frac{\sqrt{\frac{\mu_n \cdot C'_{ox}}{2} \cdot \frac{W}{L} \cdot I_{REF}}}{C_G} \cdot \left(t - \frac{V_T \cdot C_G}{I_{REF}} \right) \right) \tag{A.12}$$

Finally,

$$\boxed{i_D(t) = \begin{cases} 0 & t \leq \frac{V_T \cdot C_G}{I_{REF}} \\ I_{REF} \cdot tanh^2 \left(\frac{\sqrt{\frac{\mu_n \cdot C'_{ox}}{2} \cdot \frac{W}{L} \cdot I_{REF}}}{C_G} \cdot \left(t - \frac{V_T \cdot C_G}{I_{REF}} \right) \right) & t > \frac{V_T \cdot C_G}{I_{REF}} \end{cases}} \tag{A.13}$$

Figure A.3 shows that again the simulated results closely match the theoretical results of Equation A.13.

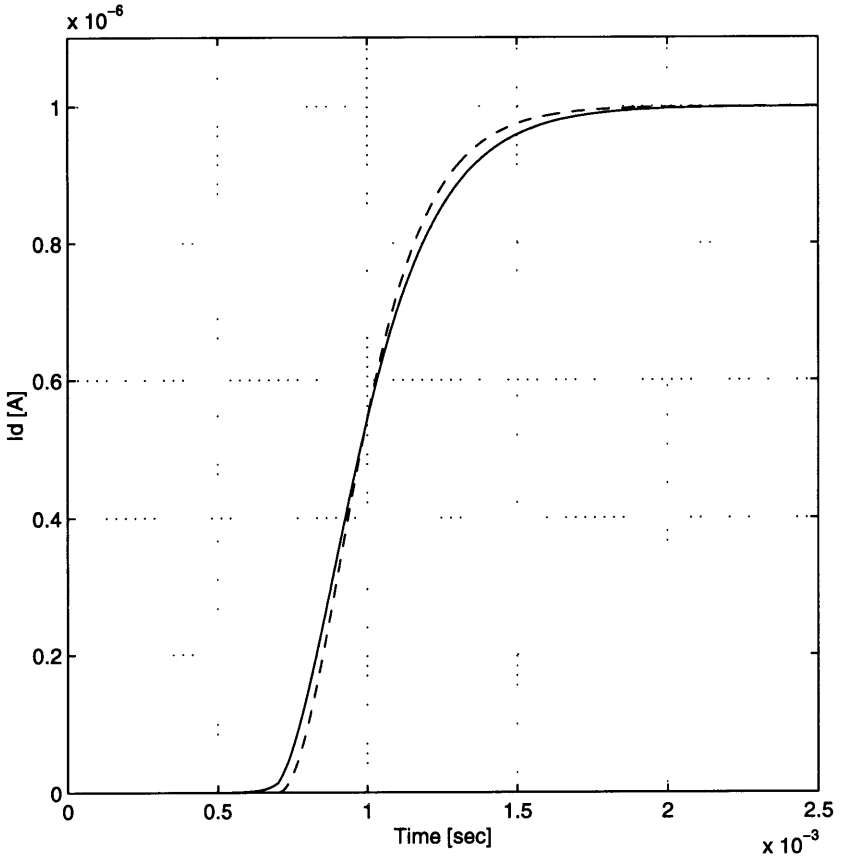


Figure A.3: Settling behavior of the drain current of the SI cell NMOS transistor. The solid curve is the result of the HSPICE simulation and the dashed curve is the plot of Equation A.13 with the values of Table A.2.

A.1.3 Settling Time Derivation

The drain current settles to a k percent of its final value in $t = t_{settle}$ seconds, where t_{settle} is obtained from

$$\frac{k}{100} \cdot I_{REF} = I_{REF} \cdot tanh^2 \left(\frac{\sqrt{\frac{\mu_n \cdot C'_{ox}}{2} \cdot \frac{W}{L} \cdot I_{REF}}}{C_G} \cdot \left(t_{settle} - \frac{V_T \cdot C_G}{I_{REF}} \right) \right) \tag{A.14}$$

And solving for t_{settle},

$$t_{settle} = \frac{V_T \cdot C_G}{I_{REF}} + \frac{atanh\left(\sqrt{\frac{k}{100}}\right)}{\sqrt{\frac{\mu_n \cdot C'_{ox}}{2} \cdot \frac{W}{L} \cdot \frac{I_{REF}}{C_G}}} \tag{A.15}$$

With the values of Table A.2, for a 99% settling time, Equation A.15 gives

$$t_{settle} \approx 1.65 \cdot 10^{-3}\text{sec} \tag{A.16}$$

and the drain current for this point in the HSPICE simulation is

$$i_D = 0.9810837422\mu\text{A} \tag{A.17}$$

so it can be seen that Equation A.13 accurately predicts the large–signal current settling behavior of an SI cell. As it was stated earlier, this last derivation is extremely important because now it is possible to calculate the total time that should be allocated for the refresh of the SI cell array.

A.1.4 HSPICE Simulation Deck

```
.MODEL NMOS NMOS LEVEL=3 PHI=0.700000 TOX=9.6000E-09 XJ=0.200000U TPG=1
+ VTO=0.6566 DELTA=6.9100E-01 LD=4.7290E-08 KP=1.9647E-04
+ UO=546.2 THETA=2.6840E-01 RSH=3.5120E+01 GAMMA=0.5976
+ NSUB=1.3920E+17 NFS=5.9090E+11 VMAX=2.0080E+05 ETA=3.7180E-02
+ KAPPA=2.8980E-02 CGDO=3.0515E-10 CGSO=3.0515E-10
+ CGBO=4.0239E-10 CJ=5.62E-04 MJ=0.559 CJSW=5.00E-11
+ MJSW=0.521 PB=0.99
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 4.1080E-07
.PARAM VDD = 3.3   VSS = 0
.PARAM W1  = 8.1U  L1  = 80.1U
.PARAM WS1 = 3.5U  LS1 = 1U
VDD     1   0       DC 'VDD'
VSS    11   0       DC 'VSS'
IREF    1   2       PULSE 0 1U
VID     2   3       DC 0
M1      3   5 11 11 NMOS W=W1  L=L1  PS=0 PD=0 AS=0 AD=0
VC      4   5       DC 0
MS1     2   6  4 11 NMOS W=WS1 L=LS1 PS=0 PD=0 AS=0 AD=0
C1      5   0       1N
VPHI1   6   0       DC 'VDD'
.IC V(7)='VSS'
.TRAN 1U 2.5M
.PRINT TRAN I(VID)
.OPTIONS POST NUMDGT=10 ACCURATE INGOLD=1
.OPTIONS ABSV=1E-25 ABSI=1E-25
.OPTIONS GMIN=1E-20 CHGTOL=1E-20
.OPTIONS METHOD=GEAR MAXORD=2 IMAX=100
.END
```

A.2 Noise Analysis

It is important to arrive to a general expression for the noise current of a switched–current cell because this is another source of mismatch between the reference current sources of the pseudo–converter array. The noise current can be thought of as a current with two parts, one which will be called the "direct" noise component and the other which will be called the "sampled" noise component. Both are described in the following sections using the notation summarized in Table A.3.

A.2.1 Direct Noise

The direct noise is the component that is present when the SI cell is delivering the copied current to a load, and it is entirely due to the input–referred noise generator of the NMOS transistor. Figure A.4 shows the situation that is going to be analyzed.

A.2.1.1 Direct Noise Power Spectral Density

The pulse $q(t)$ defined in Table A.3 can be represented in the frequency domain as [49],

$$Q(f) = \tau_D \cdot sinc\left(\pi \cdot f \cdot \tau_D\right) \tag{A.18}$$

And the gating function $\phi_3(t)$ then can be expressed in terms of this pulse as

$$\phi_3(t) = q(t) * \sum_{j=-\infty}^{\infty} \delta\left(t - n \cdot T_c\right) \stackrel{\mathcal{F}\{\}}{\Longrightarrow} \Phi_3(f) = Q(f) \cdot \frac{1}{T_c} \cdot \sum_{n=-\infty}^{\infty} \delta\left(f - \frac{n}{T_c}\right) \tag{A.19}$$

After some manipulations,

$$\Phi_3(f) = \frac{\tau_D}{T_c} \cdot \sum_{n=-\infty}^{\infty} sinc\left(n \cdot \pi \cdot f_c \cdot \tau_D\right) \tag{A.20}$$

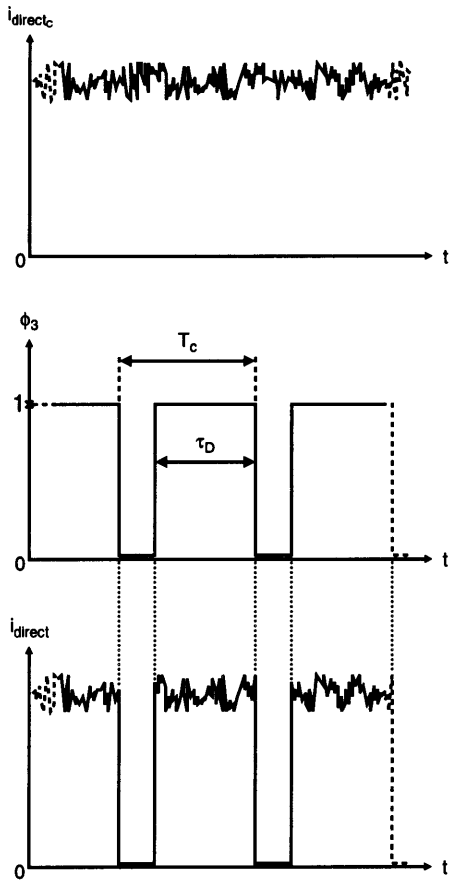


Figure A.4: Direct noise component of the switched–current cell.

With the frequency description of the gating function it is now possible to describe the load current $i_{direct}(t)$ as

$$i_{direct}(t) = i_{direct_C}(t) \cdot \phi_3(t) \overset{\mathcal{F}\{\}}{\Longrightarrow} I_{direct}(f) = I_{direct_C}(f) * \Phi_3(f) \tag{A.21}$$

$$I_{direct}(f) = \frac{\tau_D}{T_c} \cdot \sum_{n=-\infty}^{\infty} sinc\,(n \cdot \pi \cdot f_c \cdot \tau_D) \cdot I_{direct_C}\,(f - n \cdot f_c) \tag{A.22}$$

Table A.3
Notation used in the noise analysis of an SI cell

Variable	Description
$i_{direct_C}(t)$	Continuous–time load current
$i_{direct}(t)$	Actual load current
$i_{sample}(t)$	Noise current due to the cell sampling process
$v_{G_C}(t)$	Continuous–time voltage across capacitor C_G
$v_G(t)$	Actual voltage across capacitor C_G
$\phi_2(t)$	Switch S_2 gating function (Figure 2.9)
$\phi_3(t)$	Switch S_3 gating function (Figure 2.9)
$V_{IS}(s)$	Laplace representation of the ideal sampling function
$H_{SH}(s)$	Laplace representation of a sample and hold circuit
$S_G(f)$	Power spectral density (PSD) of the noise across capacitor C_g
$S_{in}(f)$	PSD of the unified noise generator (Subsection A.2.2.1)
$S_M(f) = \overline{v_M^2}/\Delta f$	PSD of the input–referred noise of the NMOS transistor
$A_{OUT}(f)$	Frequency domain expression of the SI cell output filter
τ_D	Duration of the delivery phase
τ_S	Duration of the sample phase
$T_c = \frac{1}{f_c}$	Period of switches S_2 and S_3 gating functions
$\delta(t)$	Continuous–time impulse or Diriac function
$u(t)$	Unity step or Heaviside function
k	Boltzmann's constant
T	Temperature
r_o	Small–signal output resistance of the NMOS transistor
C_G	Capacitance at the gate of the NMOS transistor
$q(t)$	Pulse defined as $q(t) = \begin{cases} 1 & \text{if } t \in [-\frac{\tau_D}{2}; \frac{\tau_D}{2}] \\ 0 & \text{otherwise} \end{cases}$

The noise is usually expressed in terms of power spectral density (PSD) so,

$$I^2_{direct}(f) = \left(\frac{\tau_D}{T_c}\right)^2 \cdot \left(\sum_{n=-\infty}^{\infty} sinc\left(n \cdot \pi \cdot f_c \cdot \tau_D\right) \cdot I_{direct_C}\left(f - n \cdot f_c\right)\right)^2 \tag{A.23}$$

If the values of $I_{direct_C}(f)$ are assumed uncorrelated at different frequencies,

$$I^2_{direct}(f) = \left(\frac{\tau_D}{T_c}\right)^2 \cdot \sum_{n=-\infty}^{\infty} sinc^2\left(n \cdot \pi \cdot f_c \cdot \tau_D\right) \cdot I^2_{direct_C}\left(f - n \cdot f_c\right) \tag{A.24}$$

As $I^2_{direct}(f) = g_m^2 \cdot S_M(f)$,

$$I^2_{direct}(f) = \left(\frac{\tau_D}{T_c}\right)^2 \cdot g_m^2 \cdot \sum_{n=-\infty}^{\infty} sinc^2\left(n \cdot \pi \cdot f_c \cdot \tau_D\right) \cdot S_M\left(f - n \cdot f_c\right) \tag{A.25}$$

Up to this point an exact analysis has been carried out, but it is very difficult to gain any insight using Equation A.25 which can only be solved using a mathematical software package. Consequently it is necessary to make a sensible approximation to simplify the preceding expression. The $sinc^2(\cdot)$ function decays very rapidly; however, a very simple yet pessimistic approximation is to assume that the function *remains* constant with a magnitude equal to its DC value (Figure A.5). If this is done and assuming that the transistor noise source is white with a magnitude η_{in} and a bandwidth Δf, the preceding expression reduces to

$$\overline{i^2_{direct}} \approx \left(\frac{\tau_D}{T_c}\right)^2 \cdot g_m^2 \cdot \eta_{in} \cdot \left[1 + 2 \cdot \sum_{n=1}^{\frac{\Delta f}{f_c}} sinc^2\left(n \cdot \pi \cdot f_c \cdot \tau_D\right)\right] \cdot \Delta f \tag{A.26}$$

An interesting conclusion can be found if $\overline{i^2_{direct}}/(g_m^2 \cdot \eta_{in})$ is tabulated as a function of $\Delta f/f_c$ and τ_D/T_c [50]. Table A.4 shows that if $\Delta f < f_c$ there is no overlap between the spectrums and consequently

$$\overline{i^2_{direct}} \approx \left(\frac{\tau_D}{T_c}\right)^2 \cdot g_m^2 \cdot \eta_{in} \cdot \Delta f \tag{A.27}$$

Table A.4
Direct noise as a function of duty cycle and bandwidth

$\frac{\tau_D}{T_c}$	$\overline{i^2_{direct}}/(g_m^2 \cdot \eta_{in})$ as a function of $\Delta f/f_c$				
	100	10	6	1	1/2
1.000	1.000	1.000	1.000	1.000	1.000
0.950	0.950	0.940	0.930	0.910	0.900
0.800	0.800	0.790	0.780	0.710	0.640
0.600	0.600	0.590	0.590	0.540	0.370
0.500	0.500	0.490	0.480	0.450	0.250
0.350	0.350	0.340	0.330	0.280	0.120
0.200	0.200	0.190	0.180	0.110	0.004
0.100	0.100	0.090	0.086	0.029	0.010
0.005	0.049	0.040	0.029	0.007	0.003
0.000	0.000	0.000	0.000	0.000	0.000

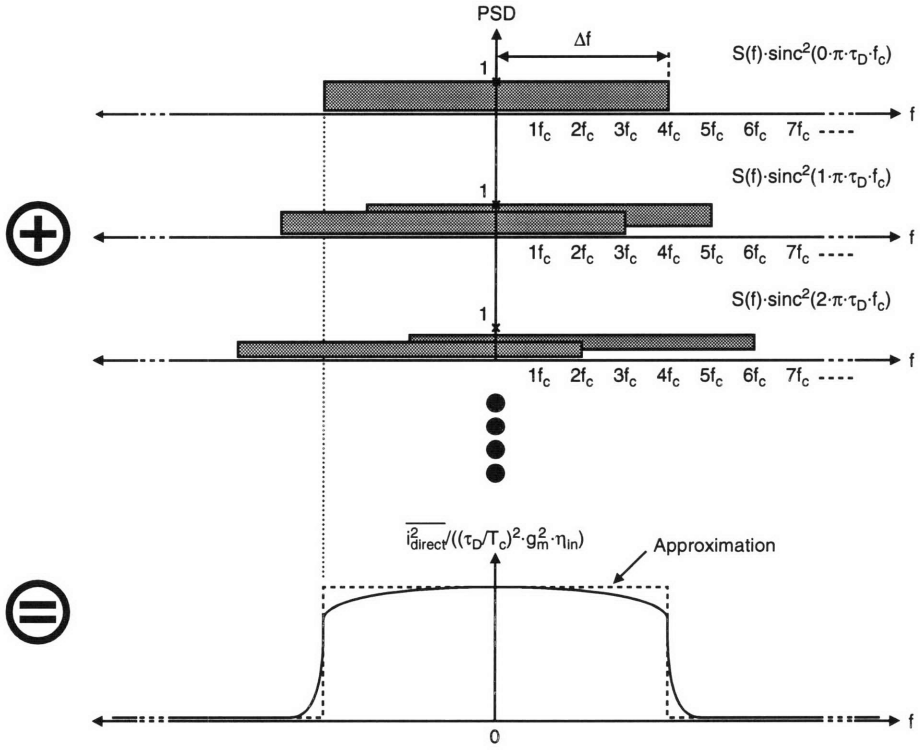


Figure A.5: Simplification of the direct noise analysis.

As Δf increases, it can be seen in Table A.4 that after $\Delta f/f_c > 10$,

$$\overline{i^2_{direct}} \approx \frac{\tau_D}{T_c} \cdot g_m^2 \cdot \eta_{in} \cdot \Delta f \tag{A.28}$$

If in a particular application $\Delta f/f_c \in [1;10]$ then it is always safe to take the worst–case scenario which in the case of the direct noise is Equation A.28 ($\tau_D/T_c < 1$, so $\tau_D/T_c > (\tau_D/T_c)^2$). If a parameter p is defined as

$$p = \begin{cases} 1 & \text{if } \frac{\Delta f}{f_c} < 10 \\ 2 & \text{otherwise} \end{cases} \tag{A.29}$$

Then the general expression for the direct noise component is

$$\boxed{\overline{i^2_{direct}} \approx \left(\frac{\tau_D}{T_c}\right)^p \cdot g_m^2 \cdot \eta_{in} \cdot \Delta f} \tag{A.30}$$

A.2.2 Sampled Noise

The second noise component in a switched–current cell is the noise that is "frozen" in the capacitor C_G when the sampling phase ends. The situation is graphically described in Figure A.6, where it has been assumed that the drain voltage of the NMOS transistor is close to ground at the start of the sample process. There are two main noise generators in this situation: the input–referred noise of the NMOS transistor and the channel noise of switch S_2, which is implemented with another NMOS transistor. The first step of the analysis is to unify these two generators to simplify the subsequent derivations.

A.2.2.1 Unified Noise Generator

The objective here is to go from the circuit of Figure A.7 (a) which has the two noise generators to the circuit of Figure A.7 (b) whose single noise generator alters only the

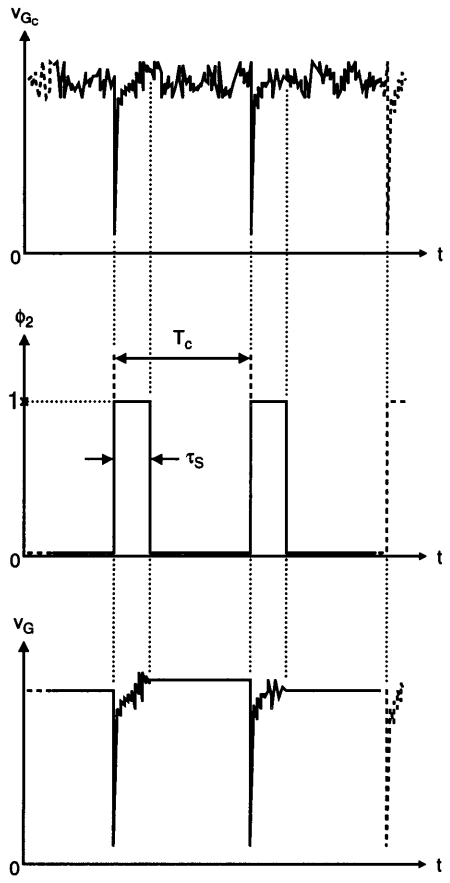


Figure A.6: Sampled noise component of the switched–current cell.

gate–to–source voltage of the NMOS transistor. This is a very convenient configuration because the noise current of the transistor can be readily calculated as $i_D = g_m \cdot v_{GS}$. Here it is assumed that the voltage across the capacitor C_G is close to its settling value; in other words, the analysis is done at a point close to the end of the sampling phase so that small–signal parameters can be used. Applying Kirchhoff's voltage law (KVL) in the circuit of Figure A.8 (a),

$$v_o = v_G + v_R + \frac{v_o - v_R}{R_{on} + \frac{1}{s \cdot C_G}} \cdot R_{on} \tag{A.31}$$

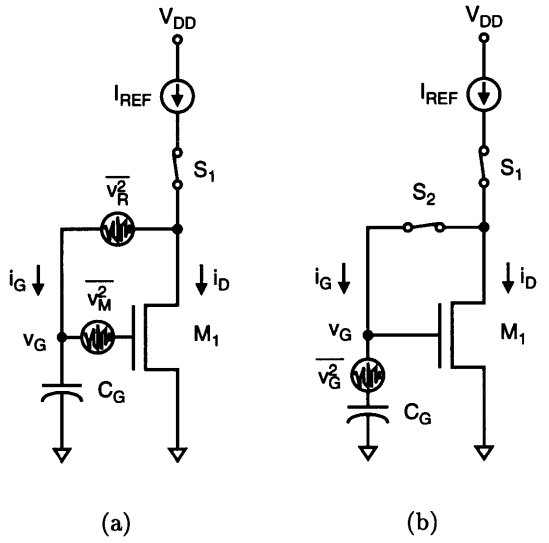


Figure A.7: Schematics used in the unified noise generator analysis, (a) original circuit and (b) the desired circuit.

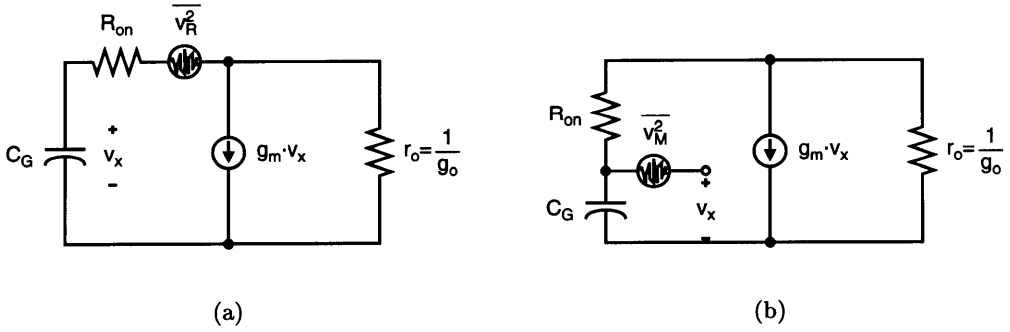


Figure A.8: Small–signal circuits used in the unified noise generator analysis, (a) for switch S_2 generator and (b) for the the NMOS transistor input–referred generator.

After some rearranging Equation A.31 leads to

$$v_o = (1 + s \cdot C_G \cdot R_{on}) \cdot v_G + v_R \tag{A.32}$$

Now applying Kirchhoff's current law (KCL) in the circuit of Figure A.8 (a),

$$g_o \cdot v_o + g_m \cdot v_G + \frac{v_o - v_R}{R_{on} + \frac{1}{s \cdot C_G}} = 0 \tag{A.33}$$

Plugging the results of Equation A.32 into Equation A.33 and rearranging terms,

$$\frac{v_G}{v_R}(s) = \frac{\frac{g_o}{g_m + g_o}}{1 + s \cdot C_G \cdot \frac{1 + g_m \cdot R_{on}}{g_m + g_o}} \tag{A.34}$$

As usually $g_m \gg g_o$ and $R_{on}/r_o \to 0$, the preceding expression can be drastically simplified. Defining $\omega_0 = g_m/C_G$, Equation A.34 reduces to

$$\boxed{\frac{v_G}{v_R}(s) \approx \frac{\frac{g_o}{g_m}}{1 + \frac{s}{\omega_0}}} \tag{A.35}$$

It can be seen that v_R goes through a low–pass filter of cut–off frequency $\omega_{-3\text{dB}} = \omega_0$ and as $g_o/g_m \ll 0$, it is also greatly attenuated. This result should have been expected because the switch noise only alters the drain–to–gate voltage of the transistor, which has no effect in the performance of the system as long as the transistor remains in the saturation region.

Turning the attention to the input–referred noise generator of the transistor, and ap-

plying KVL to the circuit of Figure A.8 (b),

$$v_o = v_G + \frac{R_{on}}{R_{on} + \frac{1}{s \cdot C_G}} = (1 + s \cdot C_G \cdot R_{on}) \cdot v_G \tag{A.36}$$

Applying KCL to the same circuit,

$$g_o \cdot v_o + g_m \cdot (v_G + v_M) + \frac{v_G}{\frac{1}{s \cdot C_G}} \tag{A.37}$$

Combining Equation A.36 and Equation A.37 and after some intermediate steps,

$$\frac{v_G}{v_M}(s) \approx \frac{\frac{g_m}{g_m + g_o}}{1 + \frac{s}{\omega_0}} \tag{A.38}$$

With the same approximations and definitions as in the switch noise case, Equation A.38 reduces to

$$\boxed{\frac{v_G}{v_R}(s) \approx \frac{1}{1 + \frac{s}{\omega_0}}} \tag{A.39}$$

In can be concluded that the noise of the switch and the noise of the transistor go through the same filter but the latter one is *not* attenuated. Combining Equation A.35 and Equation A.39 it is possible to arrive to the single noise generator circuit of Figure A.7 (b),

$$v_G(s) = \frac{v_G}{v_R}(s) \cdot v_R(s) + \frac{v_G}{v_M}(s) \cdot v_M(s) \tag{A.40}$$

But as it pointed out earlier $g_o/g_m \ll 1$ so

$$v_G(s) \approx \frac{v_G}{v_M}(s) \cdot v_M(s) \tag{A.41}$$

Finally,

$$\boxed{\overline{v_G^2} \approx \left|\frac{1}{1+\frac{s}{\omega_0}}\right|^2 \cdot \overline{v_M^2}} \tag{A.42}$$

A.2.2.2 Sampled Noise Power Spectral Density

From Figure A.7 the voltage at the gate of the transistor is

$$v_G(t) = \sum_{n=0}^{\infty} v\left(n \cdot T_c\right) \cdot \left[u\left(t - n \cdot T_c\right) - u\left(t - n \cdot T_c - \tau_S\right)\right] \tag{A.43}$$

Performing a Laplace transformation and after some rearranging,

$$V_G(s) = \frac{1 - e^{-s \cdot \tau_S}}{s} \sum_{n=0}^{\infty} V(n \cdot T_c) \cdot e^{-s \cdot n \cdot T_c} \tag{A.44}$$

If $\tau_S \to 0$ the noise sampling would be ideal, so if the following functions are defined

$$V_{IS}(s) = \sum_{n=0}^{\infty} V_{GC}(n \cdot T_c) \cdot e^{-s \cdot n \cdot T_c} \tag{A.45}$$

$$H_{SH}(s) = \frac{1 - e^{-s \cdot \tau_S}}{s} \tag{A.46}$$

Equation A.43 can be expressed as,

$$V_G(s) = H_{SH}(s) \cdot V_{IS}(s) \tag{A.47}$$

As in noise calculations the phase is not important,

$$V_G(s) = |H_{SH}(s)| \cdot V_{IS}(s) \tag{A.48}$$

After some mathematical manipulations, it can be shown that

$$|H_{SH}(j\omega)| = \frac{\tau_S}{2} \cdot \left| sinc\left(\omega \cdot \frac{\tau_S}{2}\right)\right| \tag{A.49}$$

so that

$$V_G(j\omega) = \frac{\tau_S}{2} \cdot \left| sinc\left(\omega \cdot \frac{\tau_S}{2}\right)\right| \cdot V_{IS}(j\omega) \tag{A.50}$$

where V_{IS} is the ideal sampling function as defined by Equation A.45. Taking the Fourier transform of the preceding expression,

$$V_G(f) = \frac{\tau_S}{T_c} \cdot |sinc(\pi \cdot \tau_S \cdot f)| \cdot \sum_{n=-\infty}^{\infty} V_{G_C}(f - n \cdot f_c) \tag{A.51}$$

It is important to note that $V_{G_C}(f)$ is the Fourier transform of the *continuous-time* function of the voltage across the capacitor C_G. Defining,

$$S_G(f) = \frac{\overline{v_G^2(f)}}{\Delta f} \tag{A.52}$$

$$S_{in}(f) = \frac{\overline{v_{G_C}^2(f)}}{\Delta f} \tag{A.53}$$

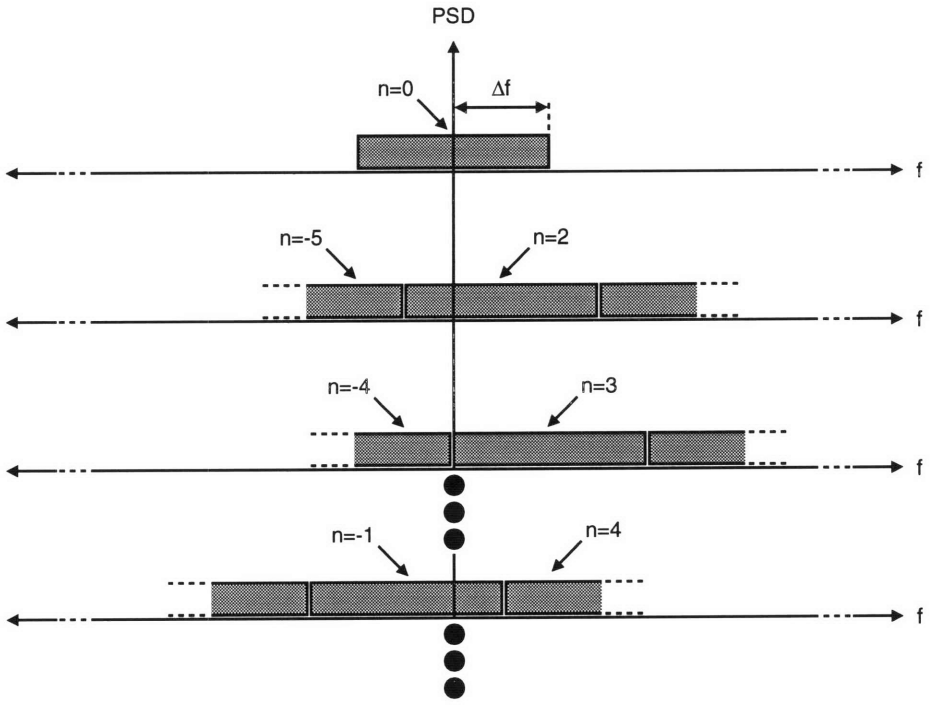


Figure A.9: Simplification of the sampled noise analysis.

then from Equation A.53

$$S_G(f) = \left(\frac{\tau_S}{T_c}\right)^2 \cdot sinc^2\left(\pi \cdot \tau_S \cdot f\right) \cdot \sum_{n=-\infty}^{\infty} S_{in}\left(f - n \cdot f_c\right) \tag{A.54}$$

where it has been taken advantage of the fact that $|sinc(\cdot)|^2 = sinc^2(\cdot)$. If $S_{in}(f)$ describes a white noise source of magnitude η_{in} and bandwidth Δf, then with the aid of Figure A.9 [51],

$$\sum_{n=-\infty}^{\infty} S_{in}\left(f - n \cdot f_c\right) \approx 2 \cdot \frac{\Delta f}{f_c} \cdot \eta_{in} \tag{A.55}$$

so that finally

$$S_G(f) \approx 2 \cdot \frac{\Delta f}{f_c} \cdot \left(\frac{\tau_S}{T_c}\right)^2 \cdot sinc^2\left(\pi \cdot \tau_S \cdot f\right) \cdot \eta_{in} \tag{A.56}$$

And the noise current is

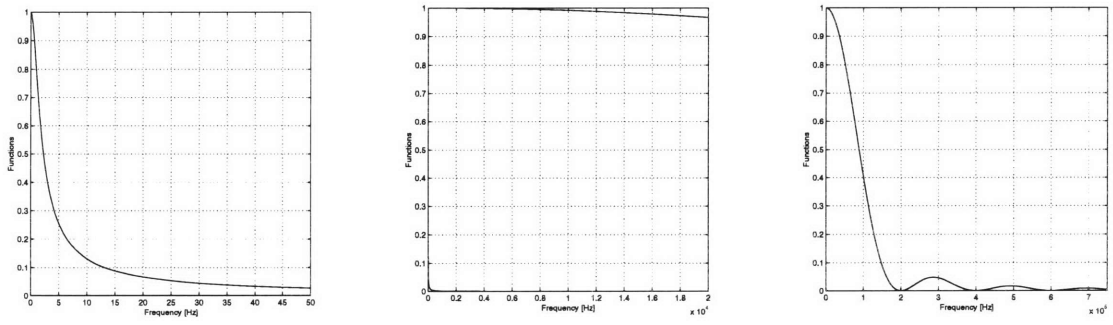
$$\overline{i^2_{sample}} = 2 \cdot g_m^2 \cdot \int_0^\infty S_G(f) \cdot |A_{OUT}(f)|^2 \cdot df \tag{A.57}$$

$$\overline{i^2_{sample}} = 4 \cdot g_m^2 \cdot \frac{\Delta f}{f_c} \cdot \left(\frac{\tau_S}{T_c}\right)^2 \cdot \eta_{in} \cdot \int_0^\infty sinc^2\left(\pi \cdot \tau_S \cdot f\right) \cdot |A_{OUT}(f)|^2 \cdot df \tag{A.58}$$

where $A_{OUT}(f)$ is the expression that describes the circuit at the output of the NMOS transistor, which in the case of the current–mode dual–slope converter is a low–pass filter made of the transistor output resistance r_o and the integrating capacitor C_{INT}.

Now is the moment to make yet another approximation to easily solve the integral of Equation A.58. As it was seen in the unified noise generator analysis, the input–referred noise voltage goes through a low–pass filter with a cut–off frequency of $\omega_{-3\text{dB }A} = g_m/C_G$; and the noise current, which is directly proportional to the noise voltage, goes through the previously mentioned output low–pass filter which has a cut–off frequency of $\omega_{-3\text{dB }B} = g_o/C_{INT}$. As the integrating capacitor is much larger than the gate capacitance and $g_o \ll g_m$ (refer to Chapter 3 for the actual values of the design), the real filtering is done by the SI cell output circuitry. With this in mind, it is fairly easy to see that the function $A_{OUT}(f)$ decays much faster than the $sinc^2(\cdot)$ function, as shown in Figure A.10. This fact has a simple explanation: as the refresh period of the SI cell is much smaller than the delivery phase, then

$$\tau_D \approx T_c \Longrightarrow \tau_S \to 0 \quad \text{and} \quad f_{-3\text{dB}} = \frac{1}{2 \cdot \pi} \cdot \frac{g_o}{C_{INT}} \ll \frac{1}{T_C} \tag{A.59}$$



(a) (b) (c)

Figure A.10: Simplification of the sample noise integral. (a) For low frequencies the output filter decays quickly and the $sinc^2(\cdot)$ function remains at unity, (b) for medium frequencies the $sinc^2(\cdot)$ function starts to decrease while the output filter is close to zero, and (c) for high frequencies the $sinc^2(\cdot)$ function decays completely. In all the figures $\tau_D \approx 5\mu$sec, $r_o \approx 3.8$GΩ and $C_{INT} \approx 22$pF.

This inequity is such because g_o should be extremely small to minimize the channel–length modulation effects in the SI cell (an important source of converter nonlinearities), and the integrating capacitor C_{INT} should be fairly large to reduce both charge injection problems and the maximum voltage across it. Figure A.10 plots both $A_{OUT}(f)$ and $sinc^2(\pi \cdot \tau_S \cdot f)$ with the actual values used in the system (refer again to Chapter 3). It is obvious then that the $sinc^2(\cdot)$ function has nearly no effect and can be approximated to the unity for the frequencies of interest so that

$$\int_0^\infty sinc^2(\pi \cdot \tau_S \cdot f) \cdot |A_{OUT}(f)|^2 \cdot df \approx \int_0^\infty |A_{OUT}(f)|^2 \cdot df \approx \Delta f \tag{A.60}$$

Finally, the simplified expression for the noise current is

$$\boxed{\overline{i^2_{sample}} \approx 2 \cdot g_m^2 \cdot \frac{\Delta f}{f_c} \cdot \left(\frac{\tau_S}{T_c}\right)^2 \cdot \eta_{in} \cdot \Delta f} \tag{A.61}$$

In this case η_{in} is the magnitude of the unified noise generator, which is approximately equal to the input–referred noise of the NMOS transistor, as it was seen in Section A.2.2.1.

A.2.3 Final Result

Now that all the relationships have been established the final expression for the total noise in an SI cell can be obtained. As it was discussed previously, the noise bandwidth for both noise currents is the same, so taking advantage of the expression $\Delta f = \frac{\omega_{-3\text{dB}}}{4}$ [52] the bandwidth of the system is:

$$\omega_{-3\text{dB}} = \frac{g_o}{C_{int}} \Longrightarrow \Delta f = \frac{g_o}{4 \cdot C_{int}} \tag{A.62}$$

Then, combining Equation A.30 and Equation A.56,

$$\overline{i^2_D} = \overline{i^2_{direct}} + \overline{i^2_{sample}} \tag{A.63}$$

After some simplifications,

$$\overline{i^2_D} \approx \frac{g_m^2 \cdot \eta_{in} \cdot \Delta f}{T_c^2} \cdot \left[2 \cdot \tau_S^2 \cdot \frac{\Delta f}{f_c} + \tau_D^2\right] \tag{A.64}$$

As it was stated previously the duty cycle of switch S_2 is near the unity because the refresh period is much smaller than the period of time when the cell is delivering current to a load; consequently $\tau_D \approx T_c$ and $\tau_S \ll \tau_D$. Also, in the previous section it is was explained

that $\Delta f \ll f_c$ so after all these approximations Equation A.64 reduces to

$$\overline{i_D^2} \approx g_m^2 \cdot \eta_{in} \cdot \Delta f \tag{A.65}$$

This expression may come as a surprise because after all the derivations, the end result is the input–referred noise current of the transistor, as if no sampling process was taking place. The explanation of this conclusion is very simple: the output filter of the SI cell *for this very special application* has an extremely low cut–off frequency, so most of the sampling noise is filtered out and never gets to the load.

Assuming that the sampling process in the SI cell is fast enough so that the flicker noise can be neglected, the noise of the NMOS transistor is

$$\eta_{in} \approx \frac{4}{3} \cdot \frac{k \cdot T}{g_m} \tag{A.66}$$

Also noting that $\overline{i_D^2}$ is the standard deviation of the drain noise current and that statistically 99.7% of all possible values of this noise current fall under the interval $\pm 3 \cdot \left|\overline{i_D^2}\right|$, then the worst case scenario would be to have a noise current in the order of

$$\boxed{i_D = \sqrt{3 \cdot g_m \cdot k \cdot T \cdot \frac{g_o}{C_{INT}}}} \tag{A.67}$$

Appendix B

Converter Offset Determination

Referring to Figure 2.6, Figure 2.8 and Table 2.1 it is fairly easy to determine the maximum offset voltage and comparator propagation delay for a desired converter offset error. For a given pixel current I_{PIXEL}, the second phase of integration is described by

$$v_X(t) = \frac{I_{PIXEL}}{C_1} \cdot t_{fixed} - \frac{I_{REF}}{C_1} \cdot t \tag{B.1}$$

where Equation (2.5) has been used to determine the maximum voltage across the capacitor C_1. If there is a certain offset V_{OS} in the system the first bin does not end at $I = I_{REF}/2^n$ but rather at a different current that will be called I'_{PIXEL}. When $t = t_{00}$ then $v_X(t) = V_{OS}$ and $I_{PIXEL} = I'_{PIXEL}$ in Equation (B.1) so that

$$V_{OS} = \frac{I'_{PIXEL}}{C_1} \cdot t_{fixed} - \frac{I_{REF}}{C_1} \cdot t_{00} \tag{B.2}$$

Considering that $t_{fixed} = 2^n/f_{clk}$ and that $t_{00} = 1/f_{clk}$, then

$$V_{OS} = \frac{I'_{PIXEL}}{C_1} \cdot \frac{2^n}{f_{clk}} - \frac{I_{REF}}{C_1} \cdot \frac{1}{f_{clk}} = \frac{1}{C_1 \cdot f_{clk}} \cdot \left(2^n \cdot I'_{PIXEL} - I_{REF}\right) \tag{B.3}$$

Now I'_{PIXEL} will be expressed as

$$I'_{PIXEL} = \frac{I_{REF}}{2^n} + \frac{I_{REF}}{2^n} \cdot E \tag{B.4}$$

where E is the desired offset error *in LSBs*; for example, if an offset error of 1/2 LSB is desired, then $E = 0.5$. Introducing Equation (B.4) in Equation (B.3) gives

$$V_{OS} = \frac{1}{C_1 \cdot f_{clk}} \cdot \left[2^n \cdot \left(\frac{I_{REF}}{2^n} + \frac{I_{REF}}{2^n} \cdot E\right) - I_{REF}\right] \tag{B.5}$$

Finally

$$\boxed{V_{OS} = \frac{I_{REF}}{C_1 \cdot f_{clk}} \cdot E} \tag{B.6}$$

Equation (B.6) gives the expression of the *total* offset voltage, which will be part comparator offset voltage, part comparator propagation delay.

B.1 Propagation Delay Equivalent Offset

To find out the equivalent expression in volts for the propagation delay t_{pd}, the time t will be replaced by $t = t_{00} - t_{pd}$ in Equation (B.1), which will give the ending time of the first bin, so that

$$V\left(t_{00} - t_{pd}\right) = \frac{I''_{PIXEL}}{C_1} \cdot t_{fixed} - \frac{I_{REF}}{C_1} \cdot \left(t_{00} - t_{pd}\right) = 0 \tag{B.7}$$

Then,

$$I''_{PIXEL} = \frac{I_{REF}}{t_{fixed}} \cdot \left(t_{00} - t_{pd}\right) \tag{B.8}$$

Replacing I'_{PIXEL} for I''_{PIXEL} in Equation (B.2) will give the expression for the "equivalent" offset voltage due the comparator propagation delay

$$V_{OS_{pd}} = \frac{1}{C_1} \cdot \left[\left(\frac{I_{REF}}{t_{fixed}} \cdot \left(t_{00} - t_{pd}\right)\right) \cdot t_{fixed} - I_{REF} \cdot t_{00}\right] \tag{B.9}$$

which reduces to

$$V_{OS_{pd}} = -\frac{I_{REF} \cdot t_{pd}}{C_1} \tag{B.10}$$

B.2 Total Offset

The total offset is given by

$$V_{OS} = \underbrace{\frac{I_{REF}}{C_1 \cdot f_{clk}} \cdot E}_{\text{Total Offset}} = \underbrace{V_{OS_C}}_{\text{Comparator Offset}} - \underbrace{\frac{I_{REF} \cdot t_{pd}}{C_1}}_{\text{Propagation Delay}} \tag{B.11}$$

From the preceding expression it is obvious that once an ADC offset error is determined, then the offset voltage can be readily computed using Equation (B.6). From there, either the comparator offset voltage or the comparator propagation delay must be picked, after which the other quantity (the propagation delay or the offset) is easily calculated using Equation (B.10) or Eq (B.11).

Appendix C

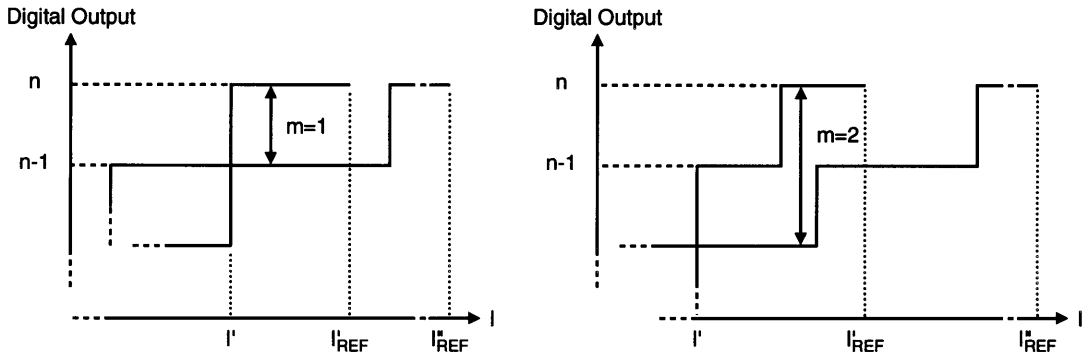
Current Matching Determination

C.1 Simplified Analysis

It is possible to develop an analytic expression to determine the matching needed between two reference current sources to bound the gain error to a desired precision. Referring to Figure C.1, I'_{REF} and I''_{REF} are the full–scale currents for two converters with different gains, and the parameter m is the number of bits that represent the precision required (measured from the maximum number of bits n); that is, the different converters will be matched at least up to $n - m$ bits.

With the notation described in Table 2.1, Figure C.1 can be used to define

$$\left.\begin{aligned} I' &= I'_{REF} - m \cdot \tfrac{I'_{REF}}{2^n} = I'_{REF} \cdot (1 - \tfrac{m}{2^n}) \\ I' &= I''_{REF} - (m+1) \cdot \tfrac{I''_{REF}}{2^n} = I''_{REF} \cdot \left(1 - \tfrac{m+1}{2^n}\right) \end{aligned}\right\} K = \frac{I'_{REF}}{I''_{REF}} = \frac{1 - \frac{m}{2^n}}{1 - \frac{m+1}{2^n}} \qquad \text{(C.1)}$$



(a) $m = 1$ (b) $m = 2$

Figure C.1: Blowout of two ADC transfer characteristics with different gains.

Defining ΔI_{REF} as half the maximum current mismatch,

$$\left.\begin{aligned} I'_{REF} &= I_{REF} - \Delta I_{REF} \\ I''_{REF} &= I_{REF} + \Delta I_{REF} \end{aligned}\right\} K = \frac{I'_{REF}}{I''_{REF}} = \frac{I_{REF} - \Delta I_{REF}}{I_{REF} + \Delta I_{REF}} \Rightarrow \Delta I_{REF} = I_{REF} \cdot \frac{1-K}{1+K} \tag{C.2}$$

After introducing Equation (C.1) into Equation (C.2) and massaging the resulting expression ΔI_{REF} is determined by

$$\Delta I_{REF} = I_{REF} \cdot \frac{1}{2^{n+1} - 2 \cdot m - 1} \tag{C.3}$$

It is interesting to note that the parameter m really does not make any significant difference when the total number of bits n is high, as $2^{n+1} \gg m$ and $n \gg m$ because it is not desirable to loose too much resolution in current mismatches. It seems that m would

never be greater than 1, but this might be possible in some applications due to the fact that the human eye cannot differentiate very bright images. As the gain error starts to affect the higher bins before the lower bins, a value of m such that $1 < m \ll n$ would cause at least a one bit error between two converters starting at bin $n - m$, which for a high resolution ADC corresponds to bright light intensities.

C.2 Analysis with the Comparator Offset

The preceding analysis assumed that the only source of error present was the gain error, but if the offset error is also considered, then the worst-case scenario would be described by the following relationships

$$\left.\begin{aligned} I' &= I'_{REF} - m \cdot \tfrac{I'_{REF}}{2^n} - E' = I'_{REF} \cdot (1 - \tfrac{m}{2^n}) - E' \\ I' &= I''_{REF} - (m+1) \cdot \tfrac{I''_{REF}}{2^n} + E' = I''_{REF} \cdot \left(1 - \tfrac{m+1}{2^n}\right) + E' \end{aligned}\right\} \tag{C.4}$$

where E' is the *total* maximum offset error expressed in Amperes. Defining

$$K_1 = 1 - \frac{m}{2^n} \tag{C.5}$$

$$K_2 = 1 - \frac{m+1}{2^n} \tag{C.6}$$

then the two relationships in Equation (C.4) can be combined to get

$$\Delta I_{REF} = \frac{I_{REF} \cdot (K_1 - K_2) - 2 \cdot E'}{K_1 + K_2} \tag{C.7}$$

Expressing E' in LSBs, that is to say

$$E' = \frac{I_{REF}}{2^n} \cdot E \tag{C.8}$$

where E is the maximum offset error in LSBs, then the maximum deviation ΔI_{REF} is

$$\boxed{\Delta I_{REF} = I_{REF} \cdot \frac{1-2 \cdot E}{2^{n+1}-2 \cdot m-1}} \tag{C.9}$$

It is easy to see that Equation (C.9) has the same form of Equation (C.3), and when $E = 0$ (no offset error), Equation (C.9) indeed reduces to Equation (C.3). The other extreme would be to make $E = 1/2$; in this case $\Delta I_{REF} = 0$, which means that the transfer characteristics of the two converters are at the limit thus no deviations in the reference current are allowed lest a mismatch greater than 1 bit is acceptable.

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