Correlation of Silicon Microroughness With Electrical Parameters of SOI-AS (Silicon-On-Insulator With Active Substrate)

by

Hasan M. Nayfeh

Submitted to the Department of Electrical Engineering
and Computer Science in partial fulfillment of the
requirements for the degree of M.S.

at the

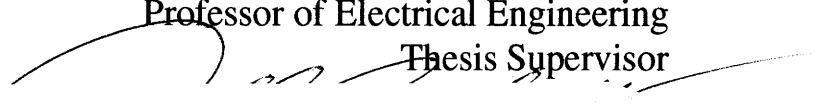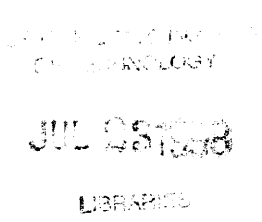MASSACHUSETTS INSTITUTE OF TECHNOLOGY

May 22, 1998

© Hasan M. Nayfeh, MCMXCVIII. All rights reserved.

Author ....
Department of Electrical Engineering and Computer Science
May 22, 1998

Certified by ....
Dimitri A. Antoniadis
Professor of Electrical Engineering
Thesis Supervisor

Accepted by ....
Artur C. Smith
Professor of Electrical Engineering
Graduate Officer

Correlation of Silicon Microroughness on Electrical Parameters of SOIAS (Silicon-On-Insulator With Active Substrate)

by

Hasan M. Nayfeh

Submitted to the Department of Electrical Engineering and Computer Science on May 22, 1998, in partial fulfillment of the requirements for the degree of
Master of Science in Electrical Engineering and Computer Science

Abstract

The technology of the formation of SOIAS (Silicon-on-Insulator With Active Substrate) requires us to utilize the lower quality back side surface of the silicon film of the original Separation by Implantation of Oxygen (SIMOX) wafer. Transistor action occurs within a distance of approximately ten nanometers from the top silicon surface. This calls for an investigation and optimization of the surface properties of SOIAS. Novel chemical mechanical polishing (CMP) techniques were used to achieve surface roughness values as good as bulk silicon (2-3 Angstroms). Electrical parameters were determined by measuring the interface state density (D_{it}) using charge pumping, and the dielectric breakdown using time-zero breakdown (TZBD). The effective mobility (μ_{eff}) has been measured as a function of vertical electric field. Surface characterization was performed using atomic force microscopy (AFM). The relationship between surface roughness and these parameters has been determined by measuring the above electrical parameters on fabricated gated P-i-N diodes and NMOS transistors with different surface roughness.

This work has discovered that the electrical performance of SOIAS is slightly improved by polishing. The mobility has been shown to be capable of matching or exceeding bulk-Si devices. A SOIAS wafer with a 8% smaller roughness than its bulk counterpart has a 9% larger surface mobility at an effective electric field of 0.8 MV/cm. The trend of improving mobility is also found amongst SOIAS wafers themselves as it is found that a 97% reduction in surface roughness leads to a 16% increase in mobility. Moreover, comparing two SOIAS wafers, the roughest and the smoothest, we discover that reducing the roughness by a factor of 92% reduces the interface trap density by 22%. However, the interface trap density could not be reduced to values measured on bulk-Si for SOIAS wafers polished to comparable roughness. However, it was found that polished samples have less on-wafer variation of D_{it}. This is a requirement for the microelectronics industry since that then translates into threshold voltage control on chip. It has also been found that oxide reliability does not depend upon the surface roughness.

Acknowledgments

This page left intentionally blank

Table of Contents

List of Figures

List of Tables

Chapter 1

Introduction

The SOIAS (Silicon on Insulator with Active Substrate) process previously developed at MIT allows the transfer of a thin single-crystalline layer of device-quality silicon from a SOI wafer to a bulk carry-wafer allowing 3D integration.

This project investigates the relationship between the surface morphology of the silicon film of this novel SOI-based technology and its electrical parameters. The SOIAS involves integration in the third dimension, allowing the formation of a buried gate and possibly other interconnect layers. This gate can be used as a back-gate control of the threshold voltage of devices. This leads to large savings in power consumption, and consequently can be used for ultra-low-power application. A proper study of the silicon film quality of SOIAS must be conducted in order for this technology to emerge as a force in the semiconductor industry.

1.1 Motivation

The theory of why surface roughness affects electrical properties is that atomic roughness is the physical origin of surface states [1]. This gives impurities sites to reside in at the surface and hence results in higher values for interface state density D_{it}. These sites can then be occupied by carriers causing lower values of mobility. Furthermore, if the trapped carrier has an electric charge, the mobility will also be degraded due to coulombic scattering. In addition, as the scaling down of transistor dimensions becomes a viable thrust for the industry to achieve larger density of integrated circuits, reduction of the oxide thickness becomes mandatory. This poses a serious challenge to avoid dielectric breakdown. The quality of the Si-SiO_2 will be crucial in achieving this goal. Hahn et al. [4] reports that roughness reduces the intrinsic breakdown field strength by field enhancement at pointed

bumps at the irregular Si-SiO$_2$ interface. Therefore, a surface with atomic smoothness must be produced using chemical mechanical polishing (CMP) in order to achieve high breakdown fields. Lin et al. report that there is a better coupling between gate voltage and surface potential due to smoother surfaces[15]; hence, a smoother surface is expected to have higher mobilities. These above reasons, demonstrate that effects of Si/SiO$_2$ interface roughness are no longer negligible in device behavior for ULSI technology[23].

1.2 Previous Work in Correlating Surface Roughness with Electrical Parameters

Determination of the relationship between the surface morphology of the silicon interface of transistors with electrical performance has been conducted for bulk silicon technology. Hahn et al. reports a strong correlation between Hall mobility and interface state density with atomic roughness at the Si-SiO$_2$ interface at high inversion [1]. They show that a larger surface roughness translates into a larger density of surface states and a lower value for mobility [1]. It has also been demonstrated that there is an increased interface state density D$_{it}$ with an increase in surface roughness [20]. It is also shown that an increase in surface roughness reduces the field needed to breakdown the gate oxide.

Lin et al. performed a detailed study of the effects of surface roughness on the electrical properties of bulk Si devices. He found that interface roughness will:

1. Modulate the local surface electric field

2. Reduce the channel mobility

3. Enhance the Fowler-Nordheim Tunneling Current

4. Modify the quantum oscillation pattern

5. Diminish the hot carrier population

6. Slightly degrade the oxide strength

Chan et al. performed an experiment on thin film poly transistors to determine the con-tribution of surface morphology on the performance of devices. He did this by comparing devices that had polishing done on them to ones that had not. His experiments constantly showed that devices that were polished had the best performance. For example, there was a two-fold improvement of the drain current in saturation. In fact, wafers that were pol-ished gave higher field-effect mobility, higher saturation current, higher dielectric break-down strength, improved turn-on characteristics, and improved short channel behavior[15].

1.3 Goal of Thesis

This thesis attempts to determine the relationship between the surface morphology and electrical parameters of this novel SOI based structure. Several steps were taken in order to accomplish this goal. First, the wafers were prepared. This involved fabrication steps utilizing new and advanced technologies such as bonding. Secondly, a means of creating splits of different morphology was accomplished. This was done by touch-polishing wafers using CMP technology. Wafers then had their morphology improved dramatically using this and at the same time, the film thickness was a controlled parameter. Next, the wafer morphology was characterized by using state-of-the-art Atomic Force Microscopy to obtain and analyze pictures of the surface on an atomic scale. After that, a full process was done whereby special structures were fabricated that were used to study the electrical properties of the material. The structures were measured and the data was then correlated with the morphology data.

Chapter 2

Background on Semiconductor Surface Science

2.1 Importance of Surface in Device Performance

The surface of silicon plays a very important role in the performance of electron devices. The surface unlike the bulk of the material is an abrupt end so that the periodicity of the crystal is lost. This results in atoms at the surface having dangling bonds, hence, making it susceptible to contamination and giving rise to interface states which could be charged. In addition to this charge, there are charge centers located in the oxide which is grown on the silicon surface. The major cause of these centers are defects that are related to the chemical structure of the interface [25]. There are three types of charges in a Si/SiO_2 structure [25]:

1. **Fixed Oxide Charge:** The source of this charge is from structural defects in the oxide layer such as ionized silicon located in the oxide layer (~25 Angstroms from the Si/SiO_2 interface). Oxide fixed charge is defined as localized charge centers that cannot change their charge state by exchange of mobile carriers with the silicon.

2. **Mobile Oxide Charge:** This is charge due to ionic impurities such as Na^+, Li^+, K^+ and possibly H^+.

3. **Oxide trapped charge:** This is from holes or electrons trapped in the bulk of the oxide. Possible source of this charge are ionizing radiation and avalanche injection.

4. **Si/SiO_2 Interface Trapped Charge:** These are positive or negative charges. There are three causes for it: (1) Structural, oxidation-induced defects, (2) metal impurities, or (3) defects caused by bond breaking processes such as radiation. Interface trap charges are charges localized on centers that can exchange charge state with the silicon. These charges

will change the electrostatics of the device and hence, they must be understood and minimized in order to optimize device performance. One of the goals of this work is to minimize the fourth kind of charge- interface trapped charge by improving the morphology of the Si/SiO_2 interface using CMP.

2.2 The Si/SiO_2 Interface

This quality of this interface is a prime indicator of the performance of a transistor device. There are five features of the $Si-SiO_2$ interface [25]:

1. The $Si-SiO_2$ interface has charge centers called oxide fixed charge. The charges have a positive polarity. They are immobile under an applied electric field. They do not exchange charge with the silicon when the gate bias is varied.

2. The interface has traps. The traps change occupancy with gate bias. They have energy levels distributed throughout the bandgap. They do not communicate with each other, so they do not form an energy band.

3. The interface potential varies at the interface from point to point due to random distribution of localized charged interface traps and of the oxide fixed charge.

4. Individual interface trap capture cross sections may be distributed over a range of values due to bent or stretched bonds.

5. Interface trap characteristics of thermal oxidation are donor type in the upper half of the bandgap.

As stated before, it has been demonstrated that a better quality interface in terms of morphology results in a smaller interface trap density D_{it}. Interface traps are within 10 angstroms of the $Si-SiO_2$ interface, so it is not surprising that the morphology of the interface is related to the trap density. In this project, I make this interface as smooth as possi-

ble and then determine the relationship between the morphology and the quality of the interface.

Interface traps can be produced in several different ways [25]:

1. Thermal oxidation in dry oxygen or steam

2. Plasma Oxidation

3. Avalanche injection of electrons or holes into the SiO_2

4. Diffusion of metals such as chromium to the Si-SiO_2 interface

5. Exposure of the MOS system to ionizing radiation

There exist different models that explain the origin of interface traps [25]:

1. **Coulombic Model:** Claims that charges in the oxide induce potential wells in the silicon. The energy eigenvalues of these wells are the interface trap levels. The levels are located near the silicon band edges.

2. **Bond Model:** Claims that interface trap level distribution is produced by a distribution of bond angles or by stretched bonds at the silicon surface. These could be due to local strain or local nonstoichiometry at the Si-SiO_2 interface.

3. **Defect Model:** Says that defects within or near the interfacial region cause interface trap levels. The defects could be stacking faults, micropores, or even various atomic or molecular fragments left as a residue of imperfect oxidation. Four types of defects: 1) excess silicon (trivalent silicon), 2) excess oxygen (nonbridging oxygen), 3) impurities, 4) states in the oxygen charge induced-potential wells. There are three sources of excess oxygen: 1) Due to the oxidation reaction, 2) the strain in the region might be relieved by formation of the excess oxygen defect, 3) there are water-related electron traps near the Si-SiO_2 interface that might be related to nonbridging oxygen defects.

Some of these defects can be removed by passivating the surface by hydrogen and as a result satisfying the valence bonds. However, interface traps due to surface morphology can not be annealed out. The morphology itself has to be improved in order to improve this factor. Another method of quantifying the quality of the interface is to determine the field for oxide breakdown. It has been shown that a bumpy surface will have enhanced fields, causing breakdown at a smaller voltage than a smoother surface. This field can be determined by performing a time zero dielectric breakdown measurement [10].

Chapter 3

Background on SOIAS

3.1 Introduction to SOIAS

The SOIAS (Silicon on Insulator on Active Substrate) is an improvement upon regular SOI technology [10]. The improvement is that a back-gate is implemented. This offers many advantages. The advantages are due to the fact that the back gate can control the threshold voltage of the device. This allows one to control the threshold voltage dynamically. For instance, when a system is in a standby mode, it dissipates power. To counter this, we can use the back-gate to increase the threshold voltage, so that this power is reduced; hence, SOIAS is a step towards achieving ultra-low power devices. Not only can we achieve low-power, but also we can achieve high performance by lowering the threshold voltage when we require high transconductance giving a higher current drive. In addition, this back-gate scheme allows one to control the threshold voltage of a discrete device independently giving full control over every device on the chip.

3.2 Previous Work Done in SOIAS

Yang [10] has implemented a CMOS process on SOIAS substrates. Device and simple circuit fabrication was successful. Yang achieved about three decades of switch in off current and a 1.5 times increase in drive current for both NMOS and PMOS at V_{DS} of 1 Volt. Independent control of the back gates was also verified. It was shown that a 36% change in speed can be attained with 250 mV switch in threshold voltage at 1 V supply voltage. Also, large dynamic threshold voltage control was demonstrated. It was also shown that threshold voltage control is not deteriorated for effective channel length scaling down to ~0.2 microns [10].

However, the D_{it} value for the bonded SIMOX SOIAS wafer (BSIMOX) was worse than its bulk and SOI counterparts. Here is a table giving the D_{it} values for 4 different substrates:

Substrate Type	Average Interface States $(cm^{-2}eV^{-1})$
Bulk	$3.1x10^{10}$
SOIAS (BESOI)	$3.9x10^{10}$
SIMOX	$4.8x10^{10}$
SOIAS (BSIMOX)	$1.2x10^{11}$

Table 3.1: Average Interface Trap Density For Different Substrate Materials [10]

In this project, I will fabricate the BSIMOX SOIAS structure. As will be explained in Chapter 4, there are two methods of creating SOIAS wafers. Both start by using a SOI wafer, but SOI wafers can be created in several ways. Two popular methods are SIMOX (Separation by Implantation of Oxide) and BESOI (Bonded etch-backed SOI). It is known that the silicon quality is worse for SIMOX because of implantation damage to the crystal. The table acknowledges this. In this project, I created SOIAS wafers using SIMOX wafers. As can be seen from the table, the interface trap density is one order of magnitude large than bulk wafers, so there is plenty of room for optimization. A time zero dielectric breakdown measurement was also done for all four wafers. It demonstrated that the cumulative failure rate was almost the same for all types of wafers. The effective mobility of the four types of wafers was also calculated. That measurement showed that there is a slight improvement of mobility for smoother surfaces.

Chapter 4

Building SOIAS Wafers

4.1 Why SOIAS?

The goal of the SOIAS wafer is to create a means of controlling the threshold voltage other than using a well bias. This is done by creating a back gate inside the wafer. Figure 4.1 shows how the resulting structure should appear. We have a polysilicon film inside acting as the back gate. In addition to this, we also want to reap the benefits of SOI, so we want the wafer to be sitting on an insulating layer, and not to be in contact with the substrate.

The advantages of SOI are well known and understood. Present day technology utilizes bulk silicon wafers for fabrication of ULSI circuitry. Well formation in SOI is much simplified compared to bulk since there are no substrate effects. Also, in bulk-Si, there exists a parasitic effect called latch-up. It involves turning on a parasitic BJT which is composed of the source, drain and substrate regions. In SOI since we are dielectrically isolated from the substrate, we do not have latch-up problems. Latch-up forces one to separate wells of adjacent devices by a relatively large distance. In SOI, since there is no latch-up, we can pack more transistors per unit area. Another advantage is that SOI is not as sensitive to small perturbations. It offers better immunity to single-event upsets compared to bulk silicon because there is a smaller active silicon volume for charge to be collected. This causes SOI to be a good candidate for use in high radiation environments lending itself for many military and aerospace applications. Not only that, but sensitive charge memory devices like 1 G-bit DRAM built on SOI substrates are more reliable than their bulk counterparts [24].

SOI devices achieve higher circuit speeds and dissipate less power compared to bulk silicon devices[24]. Higher speeds can be achieved since SOI devices have smaller parasitic capacitance. Namely, the source/drain to substrate capacitance is reduced dramatically because of the buried oxide separating the two. This lowering of the capacitance then gives a higher speed of operation.

Bulk silicon MOSFET devices have another parasitic effect. The source to body potential difference makes the threshold voltage larger causing reduction of the drive current. SOI devices on the other hand have a much smaller body effect since the body is floating because of the oxide isolation. The larger drive current in SOI lends itself to higher speed applications compared to bulk devices.

4.2 Different Methods of Creating SOIAS Wafers

There exist several different methods of creating a SOIAS wafer using standard SOI material. Each method has its own advantages and disadvantages. These issues could be related to the complexity of the process, or the end products quality or a combination of the two. The difference in the methods is the type of SOI wafer one starts with. Presently, there are three major types of SOI wafers that have been fabricated and been proven to work. They are: SIMOX, BESOI, and Smart Cut.

1. **SIMOX** [8]: Separation by IMplantation of OXide, is considered to be the most advanced and promising for high density CMOS circuits [8]. It involves performing an implantation of oxygen ions into a bulk silicon wafer, and then performing a high temperature anneal to recover the crystal quality of the silicon. The formation of the oxide occurs by the ions chemically reacting with the silicon to form oxide precipitates. Since the molar volume of oxide is 1/0.44 times larger than silicon, extra space needs to be created to accommodate the oxide. This is done by an emission of Si interstitial atoms. This requires

breaking Si-Si chemical bonds which have an energy of ~5 eV. This energy can be provided by the bombarding ions themselves. After being emitted, the Si interstitials then migrate and reconstruct the surface and at the same time, they impede any further oxygen ion bombardment, so a steady state is reached. SIMOX wafers have a silicon thickness variation on the order of angstroms since it depends upon chemical reactions inside the bulk. Moreover, a desired thin film thickness is easily attained by altering the dose and energy of the ion bombardment.

2. **BESOI** [8]: Bonded Etch-back Silicon On Insulator utilizes bonding technology. The steps involved are: mating two silicon wafers together at room temperature, annealing the bonded wafers above 800° C in order to increase the bonding strength, and then one of the wafers is thinned down by polishing [8]. The major disadvantage of BESOI is that it is difficult to attain very thin silicon films and at the same time have them be uniform on a macroscopic scale. This is the case, since polishing is used as the technique to achieve the required silicon thickness. An advantage of BESOI over SIMOX is that since no implantation is involved, the material quality of the silicon film in BESOI is potentially better than SIMOX.

3. **SMART CUT** [8]: This method involves bonding two wafers together and then mechanically separating the bonded SOI layer from the original starting silicon substrate. This is done by implanting hydrogen. The wafer deleminates at the point where the hydrogen ions exist. This technique has been shown to have a better thickness uniformity than SIMOX. Also, it allows one to reuse the silicon after the break, so it saves on supplies. However, much more research needs to be performed before this technology is used in mass production. At present, this technology needs more work to make it a more reliable

one. In this thesis, the wafers used to make SOIAS wafers will be SIMOX wafers. The SIMOX wafers obtained where from IBIS Corporation.

4.3 SOIAS Wafer Preparation

The formation of the SOIAS structure begins by creating a handle wafer. It is simply a bulk silicon wafer with a thermal oxide grown on top. This thermal oxide will serve as the dielectric isolation from the substrate like the buried oxide in SIMOX. On a separate stack, a thermal oxide is grown on top of a SIMOX wafer. This oxide will serve as the back-gate of the transistor to be. An amorphous silicon film is then grown on top of this oxide. This will serve as the back-gate material to be. This stack is then flipped and bonded to the handle wafer. Therefore, the bonding interface is between the thermal oxide and the amorphous silicon.

Now, the silicon film from the SIMOX wafer is removed via wet etch using tetramethyl aluminum hydroxide (TMAH) solution. The buried SIMOX oxide serves as an etch stop so that the film thickness variation of the resulting silicon film is comparable to the original SIMOX silicon film. The final step is to etch the buried oxide using a diluted (7:1) H_2O: HF buffered oxide etch (BOE) solution. One concern, however, is the occurrence of silicon islands called inclusions. They occur a distance of about 25 nm from the bottom interface. They have the same crystal orientation as the substrate and they are about 30 nm thick and 30 to 200 nm long [8]. So, after removing the Si with the TMAH, we first perform a BOE etch to expose these islands in TMAH which are now near the top since we have flipped the SIMOX wafer. After that, we etch away the islands using these numbers as an indicator for the time required.

Figure 4.1below shows the resulting five film structure.
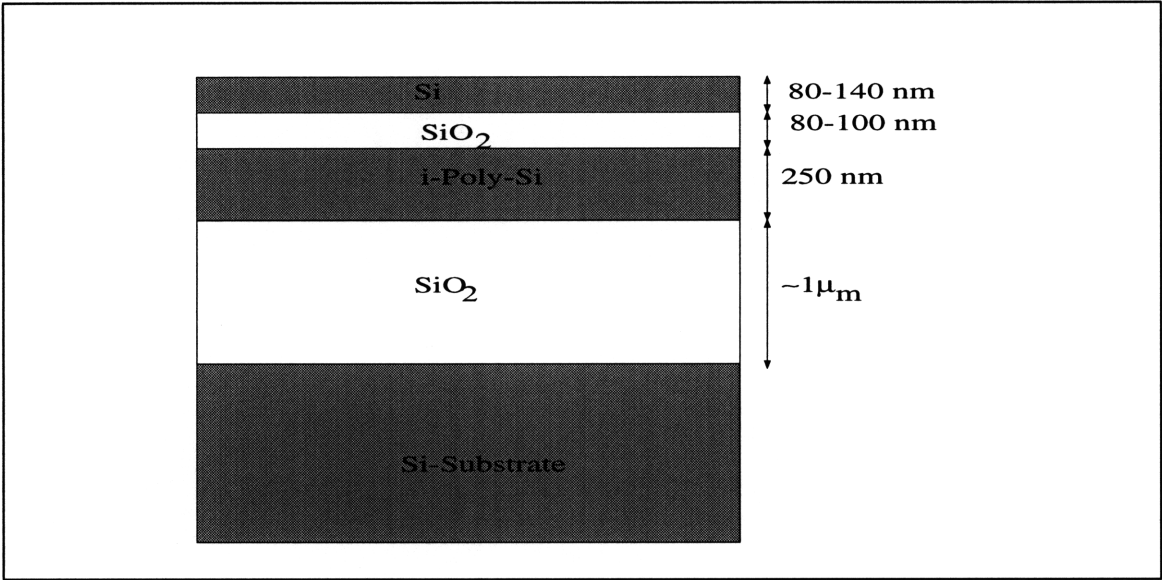
Figure 4.1: SOIAS Wafer

Figure 4.2 below summarizes the steps taken to achieve the SOIAS structure.
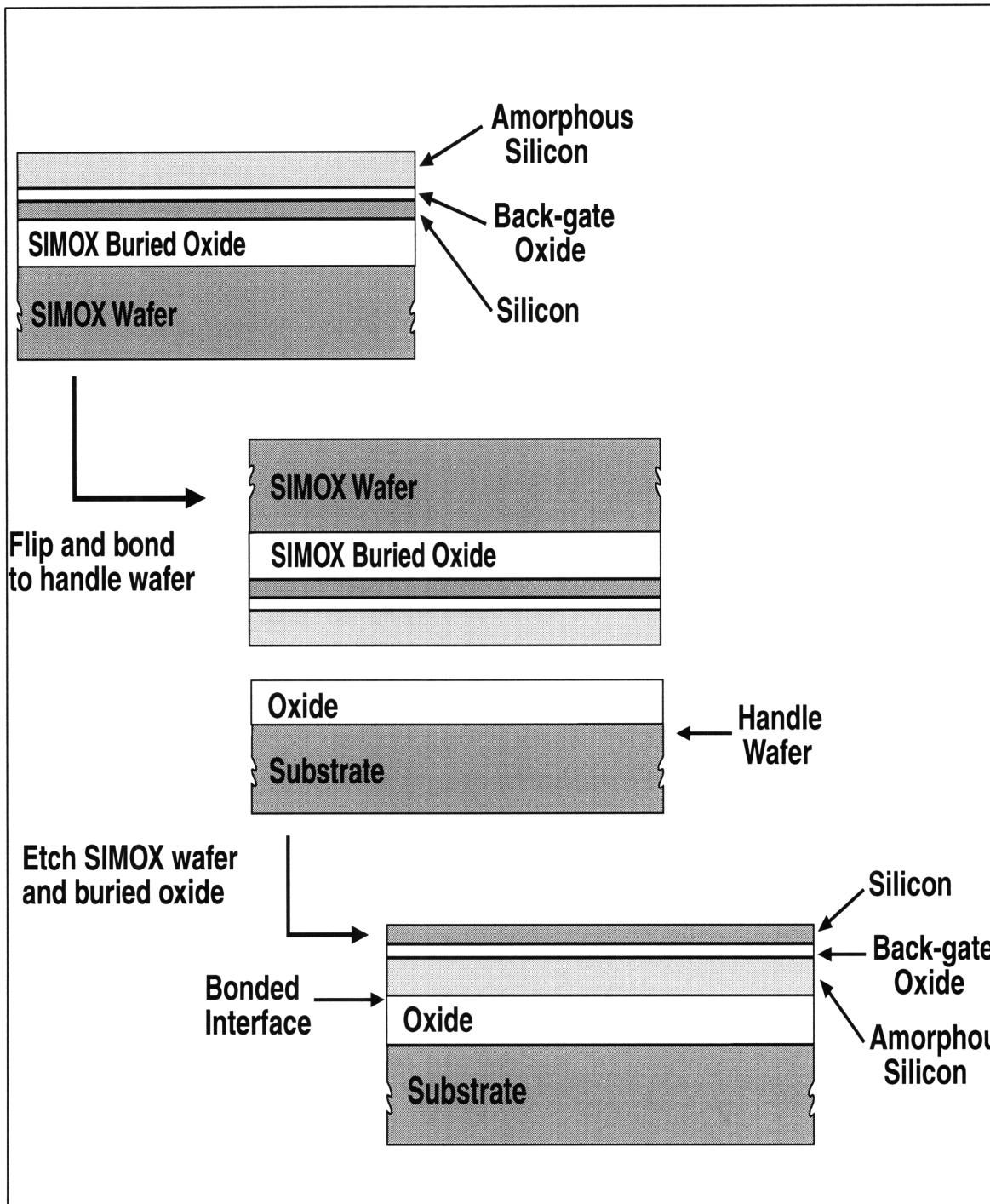
Figure 4.2: *Steps for creation of SOIAS wafer*

Chapter 5

Wafer Characterization

After creating the wafers, a full analysis of the wafer was performed that includes determination of the silicon film thickness and morphology of the surface.

5.1 Determination of Silicon film thickness using Ellipsometry Techniques

There are two different techniques to determine the film thickness, one is spectroscopic ellipsometry and the other is standard ellipsometry. Spectroscopic ellipsometry is used to measure structures with more than two underlying films. This is the case for the SOIAS wafers, which have 4 films to take into account. This is possible since it uses a wide spread of different frequencies. Standard ellipsometry on the other hand is used for two films at most and uses one wavelength, namely the He-Ne laser (633 nm).

5.1.1 Spectroscopic Ellipsometry

Spectrosopic ellipsometry is a non-destructive method of determining the film thicknesses of a multi-film structure [26]. It works by shining a laser beam of variable wavelengths from a range of 230 nm to 930 nm and recording the change of amplitude of the beam and the change of phase and polarization [26]. The real and imaginary parts of the index of refraction are determined as a function of the wavelength of the incident light. They are both determined simultaneously, so one does not have to use the Kramer-Kronig dispersion integrals [26]. From these data, the thickness can be deduced within an accuracy of 1 nm [26]. This method not only can determine thickness but also it can give information about crystallinity, void fraction, interface roughness and the composition of mixed layers[26].

There are issues to watch for when performing a spectrosopic ellipsometry measurement. Light is reflected at the planar interface between a film and an ambient phase. One

obvious criterion is that this ambient phase must transmit light [26]. For our case, the ambient phase is the native oxide which grows on silicon. So this film must be taken into consideration for accurate results. In addition, the optical properties at the surface differ from deeper in the bulk. So surface states are an important consideration. The following effects should be accounted for: a contaminant or oxide film and a stressed beilby layer- (a layer with a high density of dislocations due to mechanical forces involved in the preparation of the sample) [26]. This layer is most probably present on the wafers for this project due to the CMP. Finally, surface roughness is also an important consideration. All of these effects should be considered as a potential source of error.

5.1.2 Ellipsometry

Ellipsometry, on the other hand, works by shining a single frequency of light with elliptical polarization from a He-Ne laser. From the fresnel equations, we can determine the reflectivity for the directions perpendicular and parallel to the plane of incidence respectively. These two reflectvities are different. In ellipsometry, we adjust the polarization of the incident beam such that the reflected beam is linearly polarized. From this, we can obtain two equations with the two unknowns being the complex index of refraction of the material, and the thickness of the material.

The ellipsometer can then, therefore, measure the following parameters [27]:

• The complex index of refraction $N = n + j\delta$

• The thickness of the film

From examination of the reflected linearly polarized beam, we can determine the relectivity of the parallel and perpendicular. We then can take the ratio of these two:

$$R_p / R_s = (|R_p| / |R_s|)e^{j(\Delta_p - \Delta_s)} = \tan(\Psi)e^{j\Delta} \qquad (5.1)$$

From knowledge of Ψ and Δ, one can obtain the index n, and the thickness t. This is

28

done by a computer program that can find the values.

Standard ellipsometry is a valuable technique for determining the optical properties of materials at wavelength regions where the materials are strong absorbing. It is also very useful for small samples because it requires reflection from a small area ($1mm^2$ or less) [27]. One disadvantage of standard ellipsometry is that the measurement is dependent upon intensity fluctuations of the light source, since only the phase shifts are measured [8].

Spectroscopic ellipsometry was used to determine the film thicknesses of the SOIAS wafers and standard ellipsometry was used on the SOI wafers in conjunction with a special two-film program.

5.2 Determination of Silicon Morphology Using AFM

5.2.1 Introduction to AFM

Because interfaces have important implications for processing and device performances, AFM has been used to investigate both the (100) Si surface morphology and topography[16]. Before the invention of the AFM, light scattering or interferometric methods were used to determine roughness with an accuracy of sub-nanometer, but only in the vertical direction. Lateral resolution was on the scale of microns. The AFM has a resolution on the order of angstroms both in the lateral and vertical directions. AFM always one to laterally map a surface with a precision on the nanometer scale. Atomic resolution has been reported. It has been an instrumental tool in examining surfaces in modern technology.

Figure 5.1 below is a schematic of an AFM.
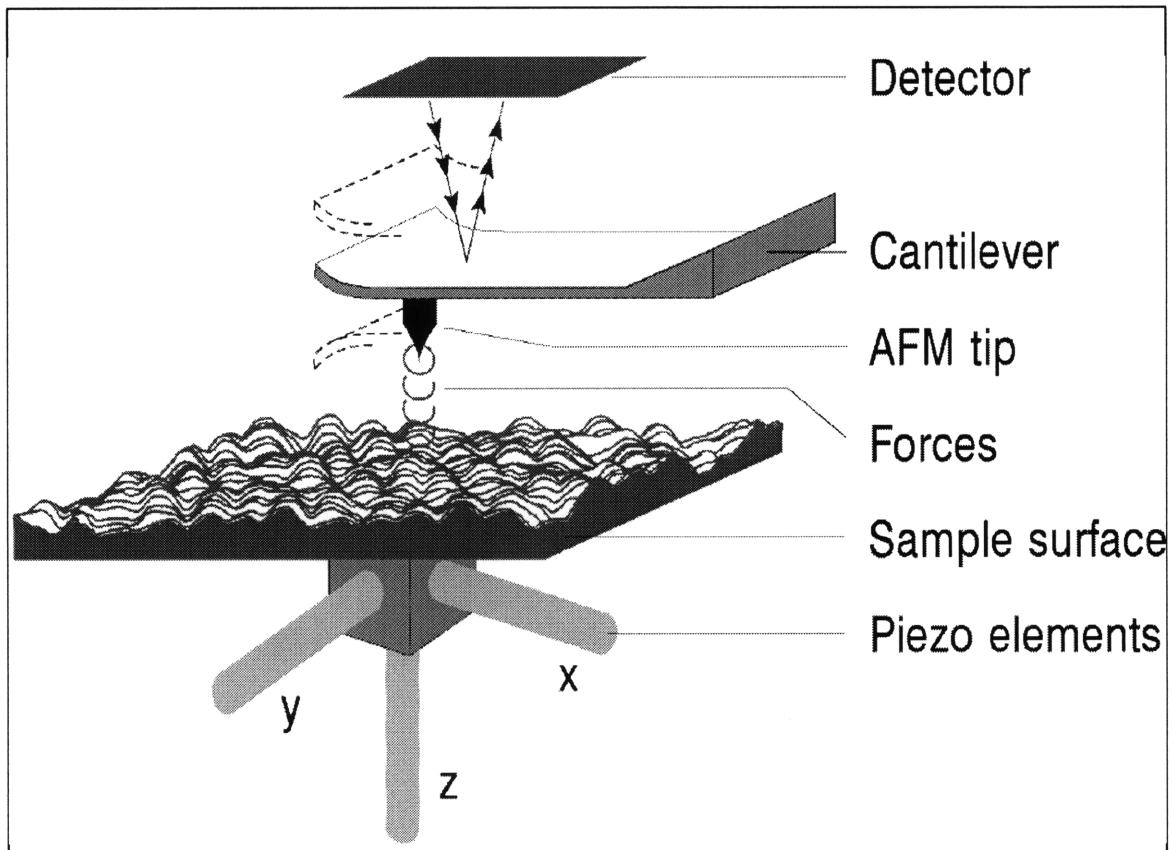
Figure 5.1: Schematic of AFM [31]

As can be seen in Figure 5.1, the AFM consists of a sharp tip at the end of a soft canti-

lever. As the tip is scanned across the sample, the cantilever bends under the effect of the

particular tip-sample interaction being used by the probe. The AFM we use has a mono-

lithic silicon tip and cantilever, with the tip having a radius of curvature of approximately

50nm. The small size of the cantilever (approximately 100µm x 50µm x 1µm) permits it to

have a low force constant, giving greater sensitivity and a high resonant frequency reduc-

ing the effects of vibrations. Typically, the force constant of the cantilever is 1-50 N/m,

while its resonant frequency is 100-400 kHz[31].

The cantilever deflection can be measured by two methods, optically and electrically.

The electrical method monitors the resistance change in a piezoresistor built into the canti-

lever. This method is useful when imaging light-sensitive samples. The AFM I used at

MIT uses an optical deflection-measurement system. Figure 5.2 shows a schematic of a deflection system based on the piezoresistor method.
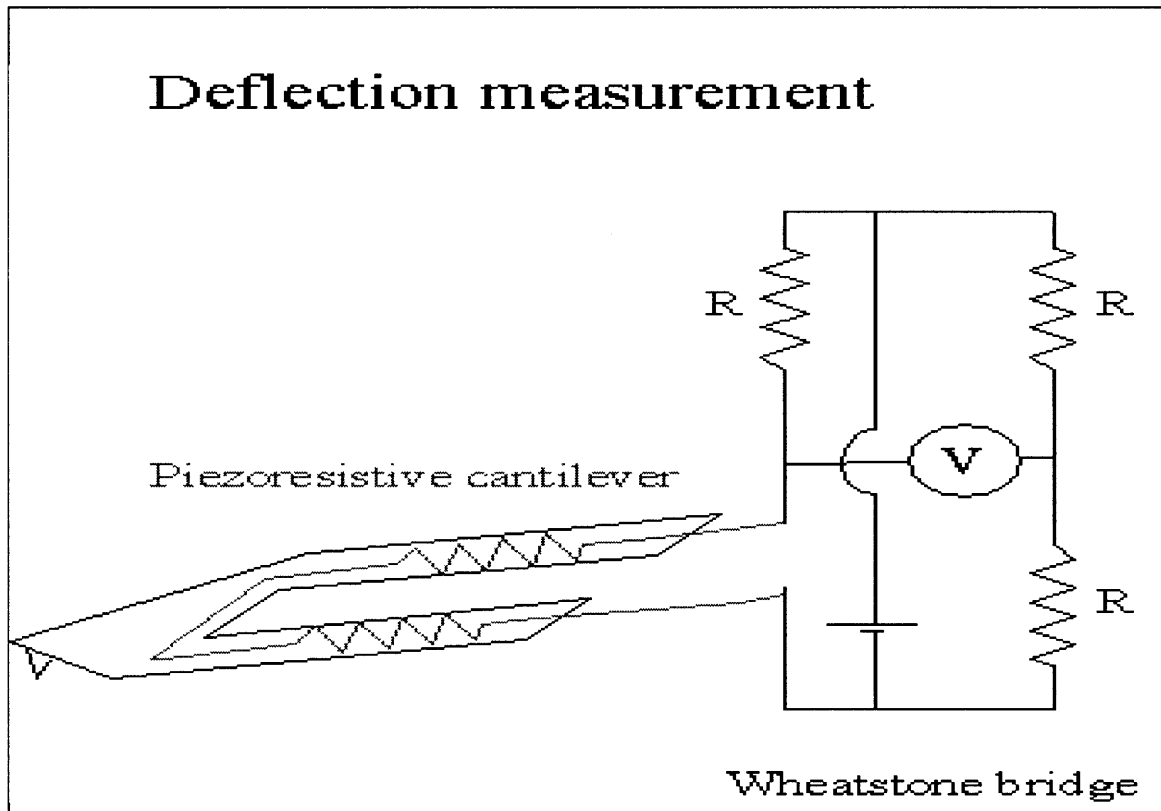
Figure 5.2: Piezoresistive Cantilever Detection Set-Up

The scanning element of the AFM consists of two parts. The sample rests on a stage with a helical underbody, supported by three piezoelectric tubes. This permits both the coarse approach of the sample to the tip, by rotating the stage with the piezotubes, and lateral motion of up to several millimeters in both directions. Fine positional control comes from the piezoelectric scan tube mounted vertically above the sample, to which the cantilever is attached[31]. The AFM I used at MIT uses a motor for the coarse movements. Figure 5.3 shows the piezo tube used in our AFM here at MIT. It allows three dimensional movement of the tip:
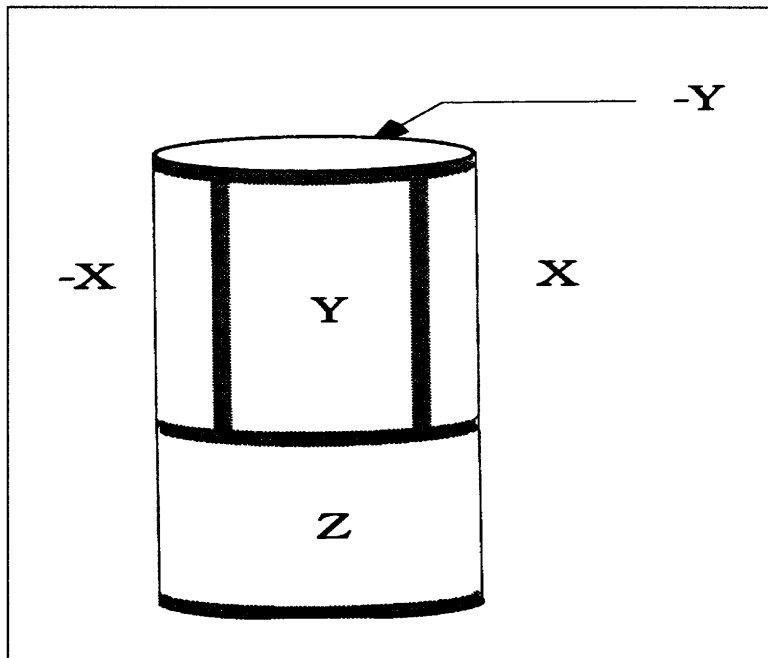
Figure 5.3: Piezo Tube Scanner Used in AFM

5.2.2 How the AFM Works

The principle of operation is based on a scientific phenomena called Van der Waals (VDW) forces. Two electrically neutral and non-magnetic bodies held at a distance of one to several tens of nanometers experience Van der Waals (VDW) forces [28]. VDW forces can be classified into 3 different categories- orientation, induction and dispersion [28]:

1. **Orientation:** this results from interaction between two polar molecules having permanent multipole moments.

2. **Induction:** This is due to the interaction of a polar and a neutral molecule where the polar molecule induces polarity in the neutral molecule.

3. **Dispersion:** This is due to non-polar molecules having a small finite dipole which fluctuates causing an attractive force between the two molecules.

Dispersion is the most dominant of the three except for the special case when the two molecules are strong polar molecules. The VDW forces increase rapidly as the distance between the two molecules approach each other with a power law:

$$F = s^{-7}$$
(5.2)

where s is the distance. If s is larger than several nanometers, the VDW forces become less effective as the:

$$F = s^{-8}$$
(5.3)

As the AFM probe tip is brought closer to the sample, it is attracted by the long range VDW forces. Once the probe is very close to the surface, the electron orbitals of the atoms on the surface of the probe and sample start to repel each other. As the gap decreases, the repulsive forces dominate over the attractive forces. The forces depend on the distance from probe to sample, the probe geometry, and contamination on the sample surface. A force as small as 10 nN can be sensed. A map of the surface is obtained by maintaining a constant force and recording the deflection of the cantilever.

5.2.3 AFM Criteria

The criteria for an AFM is [28]:

1. vibration isolation

2. positioning devices

3. scanning units

4. electronic feedback system

5. computer automation

The force sensor has several criteria [28]:

1. The force constant has to small enough to allow detection of small forces. The force constant is determined by the material used to construct the cantilever as well as the geom-

etry.

2. The resonance frequency should be large in order to be insensitive to mechanical vibration since the mechanical vibration coupling is reduced by its frequency divided by the resonant frequency of the spring squared. Also, a high resonance frequency allows one to scan at a higher speed [28]. Typical resonance frequencies vary from 15kHz-500kHz. The resonant frequency is given by:

$$\omega = \sqrt{\frac{k}{m}} \tag{5.4}$$

where k is the elastic constant, and m is the mass. Since k is small, we then want the mass to be very small. The other constraint is the tip. The radius of the tip should be made as small as possible so that one can probe a small area of the sample.

3. To achieve atomic resolution, sharp tips with small effective radius of curvature are mandatory.

4. The angle the tip opens up should be as small as possible so one can probe into pits and troughs.

The mass of the tip should be made to be as small as possible. Tips are made by micro-machining materials such as silicon oxide, silicon nitride, and even bulk silicon. Before micromachining, each tip would have to be fabricated individually, for example, from dia-mond. Now, mass production of tips that are almost identical is possible due to microma-chining.

As an example, a typical microfabricated tip has a size of about 100 microns and a thickness of 1 micron. This gives a spring constant ranging from 0.1-1 N/m corresponding to a resonance frequency range of 10-100 kHz.

Tips with radius as small as 300 angstroms have been fabricated using micromachining techniques. This is considerably larger than the size of an atom, but it can be used to image atoms since there exists protuding nanotips from this large radius.

An important issue is the detection of cantilever movement. The requirements for this are [28]:

1. High sensitivity at the sub-angstrom level

2. Independence of detection mechanism with cantilever movement.

There are several options of detection. One of these utilizes the phenomena of tunneling. This is done by placing an STM tip opposite to the tip. The tunneling current from AFM tip to STM tip is then exponentially dependent upon the distance between them. This allows one to measure a deflection as small as 0.01 angstroms. The disadvantage of this method is that tunneling is dependent upon the surface quality of the cantilever. Also, the tunneling actually changes the spring constant of the cantilever. In addition, this method is not safe against thermal drift. Thermal drifts will also cause a change in the force constant. Another disadvantage of STM compared to AFM is that one needs a conducting substrate in order to perform this tunnelling, while AFM relies on VDW forces which are sensed by all kinds of materials including insulators [28].

Another method is using a capacitance setup. A capacitor plate is deflected by the tip and the change of capacitance is determined and hence the deflection of the tip. The method used in the operation of the AFM for this project was the laser beam deflection method. The cantilever deflection is measured by detecting the deflection of the laser beam which is reflected off the rear side of the cantilever. The reflected beam is sensed by a photodetector which then converts the signal to an electric signal which is then sent to a computer to be processed.

This has an advantage over the tunneling method since a negligible force is put on the tip. The major requirements of this method is a large mirror like reflection surface at the rear of the cantilever and that the cantilever be larger than the wavelength of the laser beam so that it is not diffracted.

5.2.4 Operating Methods in AFM:

There are several different methods of operating the AFM with each one giving us insight on a special measurement. Each mode of operation needs to be selected according to the experiment performed.

In non-contact modes, the probe is pulled by the surface primarily by the capillary forces on contaminated surfaces and Van der Walls forces on clean samples. The tip plays a significant role in this mode of operation. A dull large radius tip will have a large area that interacts with the contamination layer via capillary action. This results in a large attractive force. On the other hand, a sharp, small radius tip will have a much smaller area of interaction so they have a smaller capillary action force attracting them, thus, they can be moved in and out of this layer more readily than the dull tip. In contact modes, the probe is in the repulsive force region, and the cantilever is pushed away from the sample. The method used in this project to image the silicon film surfaces was non-contact force microscopy. In this type of microscopy, the tip does not touch the sample. The tip-surface separation is increased to a value between 10-100 nm. At that distance only long-range forces such as VDW, electrostatic, and magnetic dipoles come into play. Unlike contact microscopy where we keep the force constant by moving the tip up and down, in non-contact since we are dependent upon these long range forces, it is difficult to measure such a small force. Instead, what is done is that the cantilever is excited at its resonance frequency by means of a piezoelectric device. As the tip scans an arbitrary surface, the resonance frequency changes. The frequency is then monitored to map the surface.

The theory of why the resonance frequency shifts is that a force gradient changes the spring constant by:

$$k_{new} = k_{old} - \frac{dF}{dx}$$

(5.5)

Where F denotes the force. An attractive force will give a smaller constant and a repulsive force will increase the constant. This change of the spring constant then changes the resonance frequency:

$$\omega_{new} = \omega_{old}\left(1 - \frac{\frac{dF}{dx}}{k_{old}}\right)$$

(5.6)

There are two methods to measure the shift in resonance frequency:

1. **Slope detection method-** The cantilever is driven by a piezoelectric. The amplitude at the tip is on the order of 1-10 nm. It is driven slightly below the resonance frequency. The amplitude change or phase shift of the vibration as a result of the tip-surface force interaction is measured by the laser beam deflection system as discussed before. A feedback loop adjusts the tip-surface separation by maintaining a constant force gradient.

2. **Frequency Modulation Method-** Changes in the oscillation frequency caused by variations of the force gradient of the tip-sample interaction are directly measured by a frequency counter.

Abstract A.5 gives information about the operation of the AFM used in this project, the Digital Instruments Nanoscope III Scanned Probe Microscope.

5.2.5 Previous Work Done in AFM imaging of Silicon Surfaces
Previous work has been done in imaging silicon surfaces using AFM [16]. The front silicon film in SIMOX wafers has been characterized [16]. For this project, the silicon inter-

face is the bottom of the silicon film in the original SIMOX wafer. Previous work has been done in imaging the bottom interface by exposing the surface by etching away the buried oxide. It has been reported that the backside is quite a rough interface[16]. Guilhalmene et al. have discovered that the morphology of the back interface is a mosaic one due to recrystallization of the damaged silicon layer during the buried oxide formation[16]. They have also found that the roughness values of the upper buried oxide interface in SIMOX material is higher than for wafer bonded material due to the dependence between the BOX growth and the rearrangement of the implantation damaged silicon [16].

Methods have been proposed to improve the morphology of the back surface with annealing being the most common one. Annealing gives enough energy for the atoms at the interface to rearrange so as to reduce the surface roughness. It has been demonstrated that additional annealing of SIMOX wafers for 6 hours reduced the surface roughness by a factor of two [16]. The physical explanation behind that is that annealing gives the atoms enough energy to reconstruct the silicon surface. Guilhalmene et al. have found that additional anneals removed the square-rugged morphology due to solid-phase epitaxial growth, and that the new morphology becomes a square structure replaced by a spiral "step and terrace" morphology [16].

As was explained in the background, there are several methods of operating the AFM. Gilicinshki et al. [19] gives an overview of studying silicon surface roughness by using AFM. He has found that tapping mode AFM provides the best quality data for surface roughness determinations. Special care needs to be taken in imaging silicon surfaces since it has been found to be especially susceptible to damage by tip-sample interactions, hence causing artifacts in the image. That is why tapping mode is the best option to use. The other main option, contact mode, was found to be sensitive to the force applied in the experiment. On the other hand, tapping mode AFM features a decrease in lateral tip-sur-

face interaction because the tip is not in continuous contact with the surface resulting in less artifacts in the image.

An important concern in AFM is the quality of the tip. The resolution of the image is limited by the diameter of the stylus tip. It is important to image the tip to determine size and shape, since damage is possible during operation. Broken tips will give artifact-free data, with lower roughness than actually present, resulting in unreliable images of the surface. Tapping mode tips are single crystal etched silicon probes with diameters under 20 nm. Contact mode tips have diameters from 25-50 nm-giving lower values for roughness than tapping mode tips.

There are three numerical techniques to quantify the morphology:

1. **Average roughness** (RA): Average of the absolute values of surface height variations.

$$R_a = \frac{1}{n}\left(\sum_{n=1}^{N} |Z_n - Z_{av}| \right)$$ (5.7)

where:

$$z_{av} = \frac{1}{N} \sum_{n=1}^{N} Z_n$$ (5.8)

Z_{av} is the average height of the surface. N is the number of data points.

2. **RMS roughness:** Square root of the mean of squares of distances from the mean surface level.

$$RMS = \frac{1}{L_x L_y} \int_0^{L_y} \int_0^{L_x} f(x, y)dxdy$$ (5.9)

where $f(x, y)$ is the surface relative to center plane, and L_x and L_y are the length scales over which the surface calculation is being conducted in the x and y directions respectively.

5.2.6 Measurement of SOIAS Wafers Using AFM

Tapping mode AFM was done in air with a Digital Instruments multi-mode AFM using etched silicon crystal silicon tips. Figure 5.4 below shows a picture of the AFM used for this project:
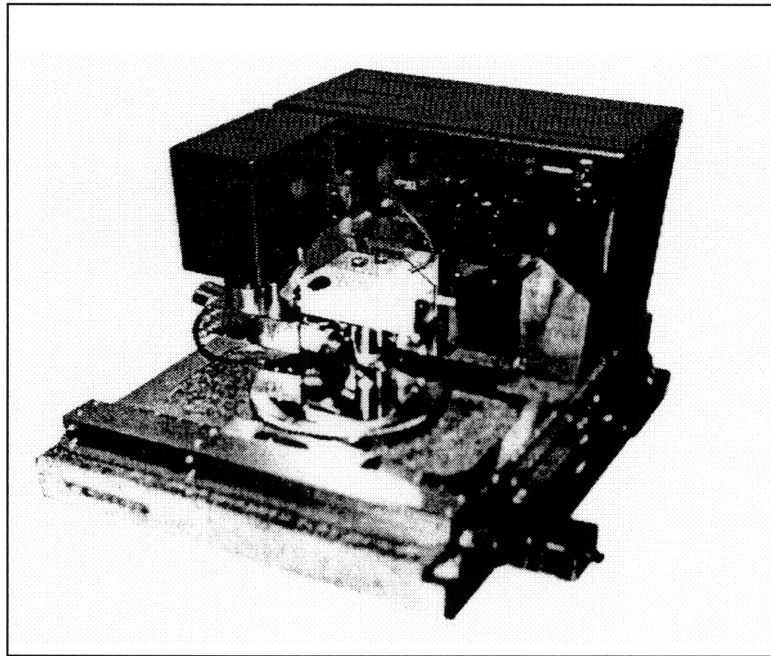
Figure 5.4: Dimension 3000 SPM With Motorized X-Y Stage

Before performing the touch polish on the wafers to be used for the project, I first performed tests on dummy SIMOX wafers so as to optimize the process to the point where the surface roughness is reduced to a value comparable to bulk prime wafers, and at the same time, the silicon removal rate being controlled.

Below are the AFM images before and after touch polish for the wafers used in this project.
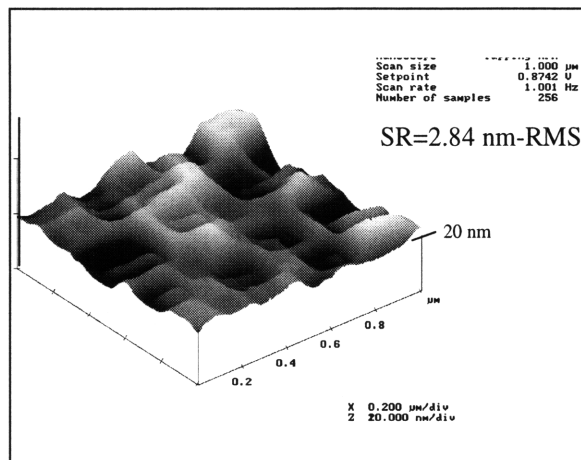
Figure 5.5: AFM Image SOIAS2
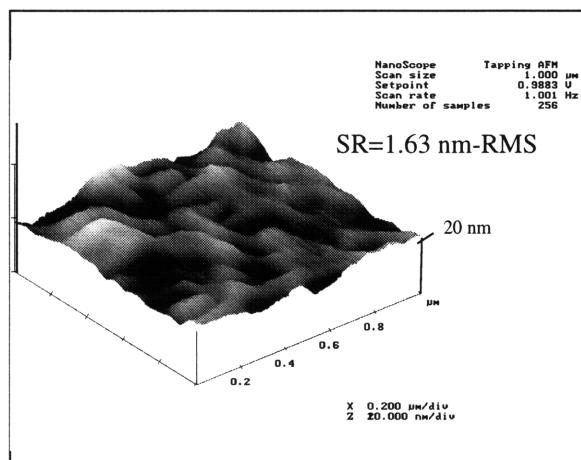
Figure 5.6: AFM Image SOIAS3
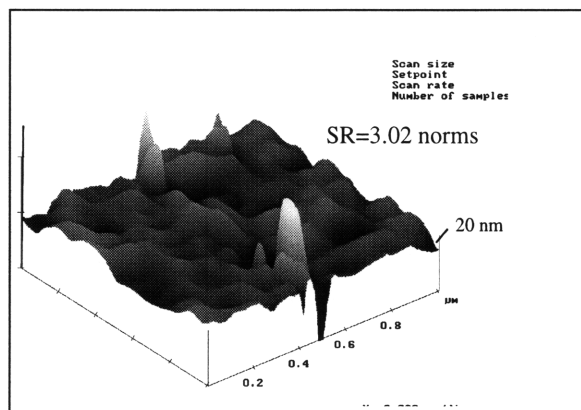
Figure 5.7: AFM Image SOIAS4
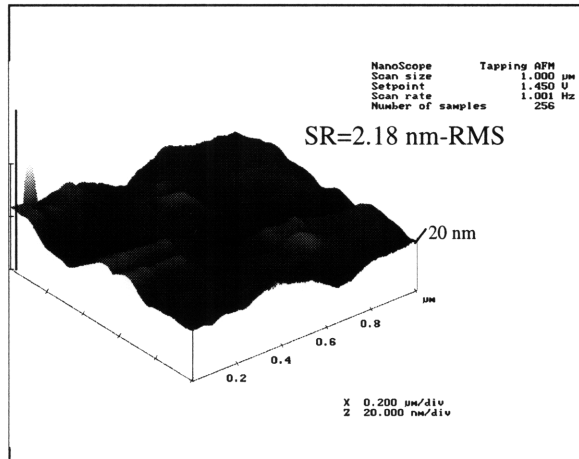
Figure 5.8: AFM Image SOIAS5
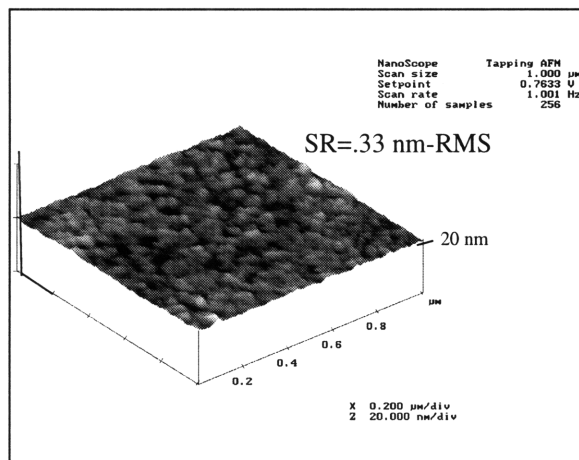
Figure 5.9: AFM Image SOIAS6
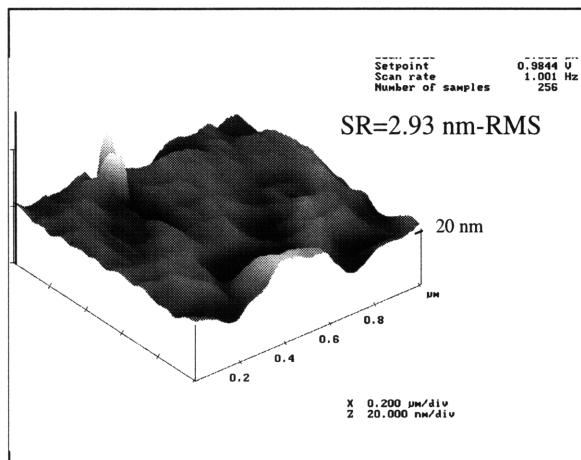
Figure 5.10: AFM Image SOIAS7
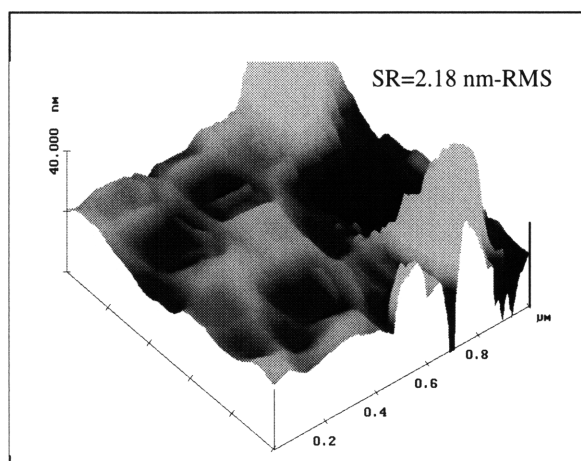
Figure 5.11: AFM Image SOIAS8
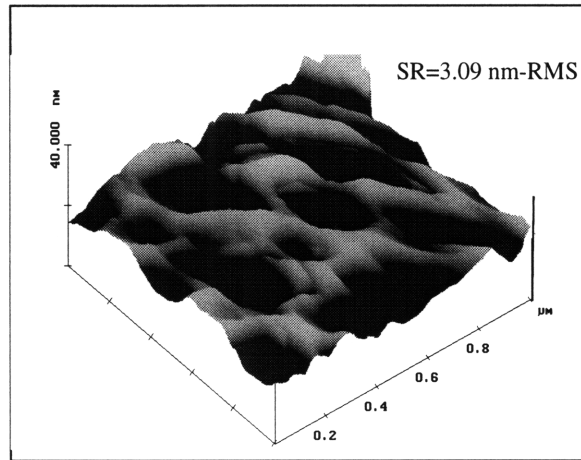
Figure 5.12: AFM Image SOIAS9
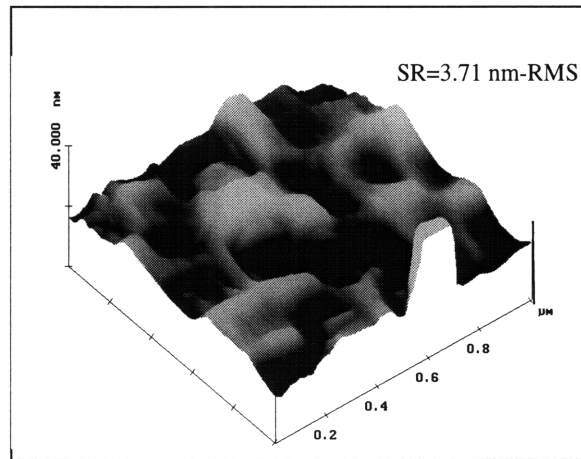
Figure 5.13: AFM Image SOIAS10
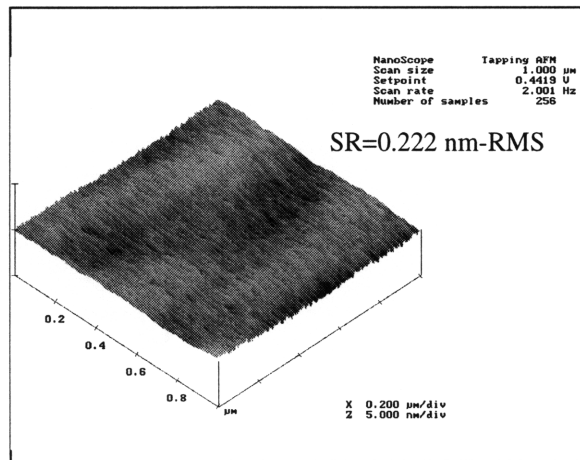
Figure 5.14: AFM Image SIMOX Wafer SOI6S

The touch polish was then performed on the SOIAS wafers. The resulting surface images are given below.

5.2.7 AFM Images of SOIAS Wafers after Touch Polish
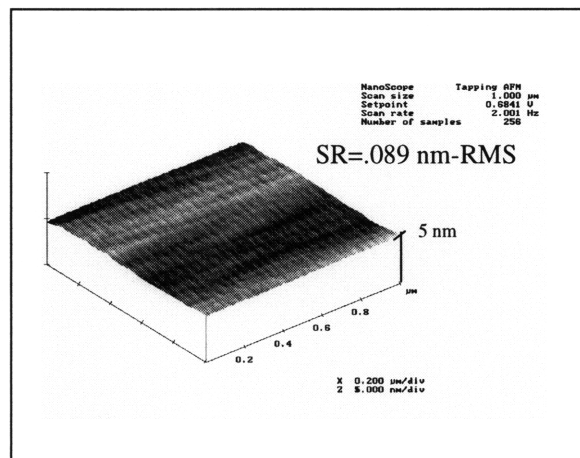
Figure 5.15: AFM Image SOIAS 2- touch polished
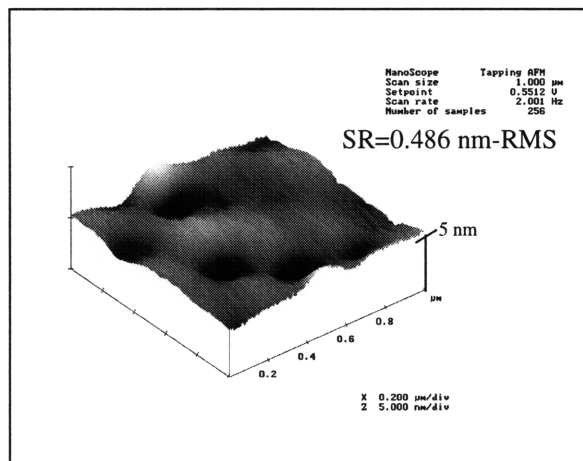
Figure 5.16: AFM Image SOIAS 3 - touch polished
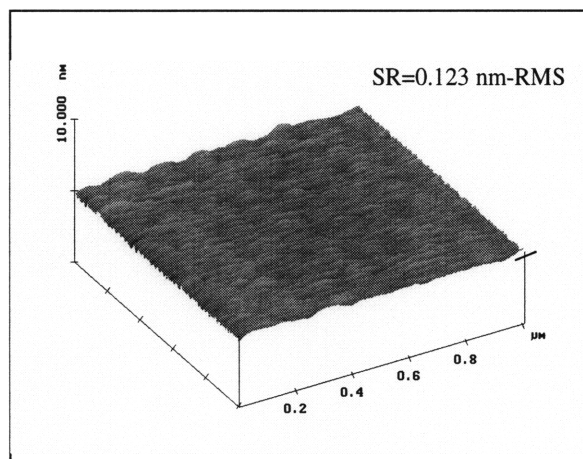
Figure 5.17: AFM Image SOIAS 4- touch polished
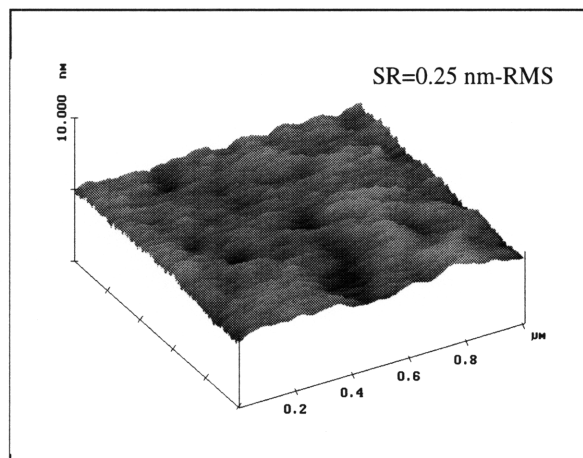
Figure 5.18: AFM Image SOIAS 6- touch polished
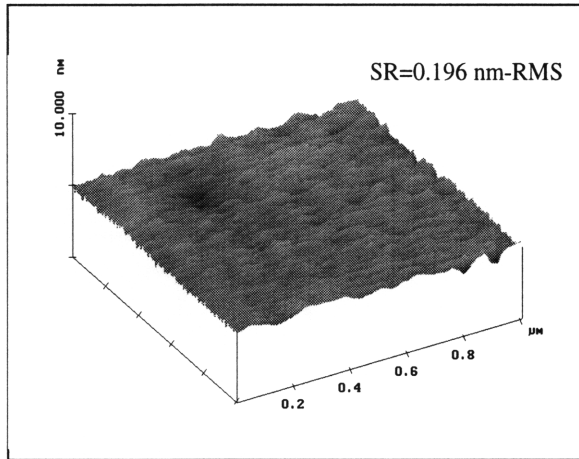
Figure 5.19: AFM Image SOIAS 7- touch polished
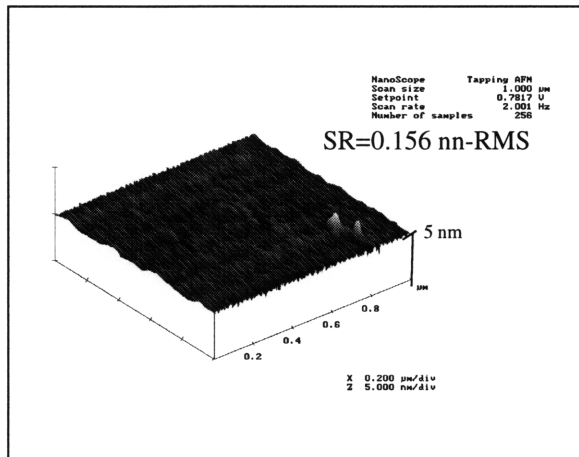
Figure 5.20: AFM Image SOIAS 10- touch polished
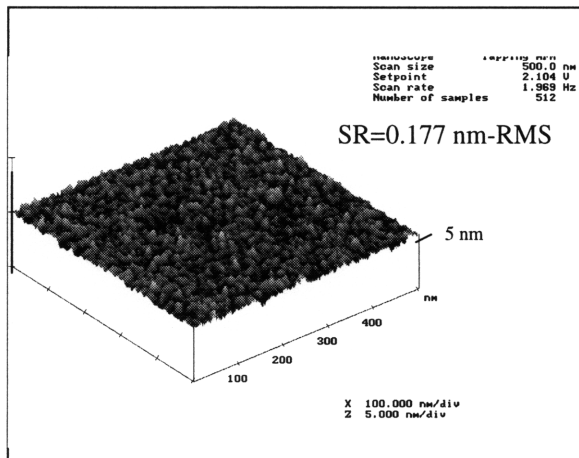
Figure 5.21: AFM Image of Bulk Wafer
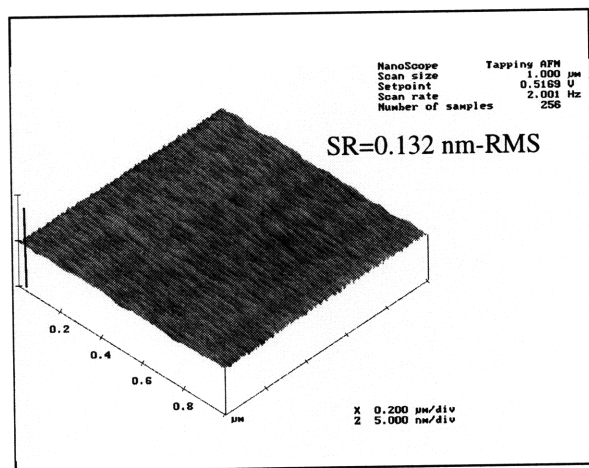
Figure 5.22: AFM Image Touch Polished SIMOX Wafer (SOI3S)

5.2.8 Analysis of AFM Results

A complete summary of the AFM results is given below in Tables 5.1-5.4:

Table 5.1: SOIAS WAFERS BEFORE TOUCH POLISH

Wafer	RMS (nm-rms)	Ra (nm)	Lateral Wavelength (microns)
2 (*SOIAS*)	2.84	2.19	0.334
3 (*SOIAS*)	1.63	1.29	0.505
4 (*SOIAS*)	3.02	1.91	0.334
5 (*SOIAS*)	2.18	1.72	0.25
6 (*SOIAS*)	2.64	2.22	0.334
7 (*SOIAS*)	2.66	1.92	1.0
8 (*SOIAS*)	2.18	2.18	0.334
9 (*SOIAS*)	3.09	2.40	1.0
10 (*SOIAS*)	3.71	2.39	0.334

Table 5.2: SOIAS WAFERS and SOI WAFERS AFTER TOUCH POLISH

WAFER	RMS (nm-rms)	RA (nm)	Lateral Wavelength (microns)	Time of Polish (minutes)
2 *(SOIAS)*	0.089	0.074	1.0	2
3 *(SOIAS)*	0.486	0.359	0.334	1
4 *(SOIAS)*	0.123	0.096	1.0	4
5 *(SOIAS)*	2.18	1.72	0.334	NONE
6 *(SOIAS)*	0.25	0.193	0.505	1
7 *(SOIAS)*	0.196	0.147	0.333	2
8 *(SOIAS)*	2.18	2.18	0.334	NONE
9 *(SOIAS)*	3.087	2.401	1.0	NONE
10 *(SOIAS)*	0.156	0.137	0.334	4
3s *(SOI)*	0.132	0.108	1.0	4
4s *(SOI)*	0.134	0.109	1.0	4
5s *(SOI)*	0.224	0.177	0.33	NONE
6s *(SOI)*	0.222	0.180	0.33	NONE

Table 5.3: Percent Change of Morphology Parameters (+/- Increase/ Reduction)

WAFER	RMS (%)	RA (%)	Lateral Wavelength (%)	Time Touch Polish
2 *(SOIAS)*	-75	-96.63	98	2
3 *(SOIAS)*	-70.18	-72.17	0	1
4 *(SOIAS)*	-80.4	-94.97	300	4
6 *(SOIAS)*	-75	-88.74	-49.5	1
7 *(SOIAS)*	-96.86	-89.78	-66.7	2
10 *(SOIAS)*	-50.8	-93.24	51.2	4
3s *(SOI)*	-41.07	-41.07	203	4
4s *(SOI)*	-38.42	-67.16	203	4
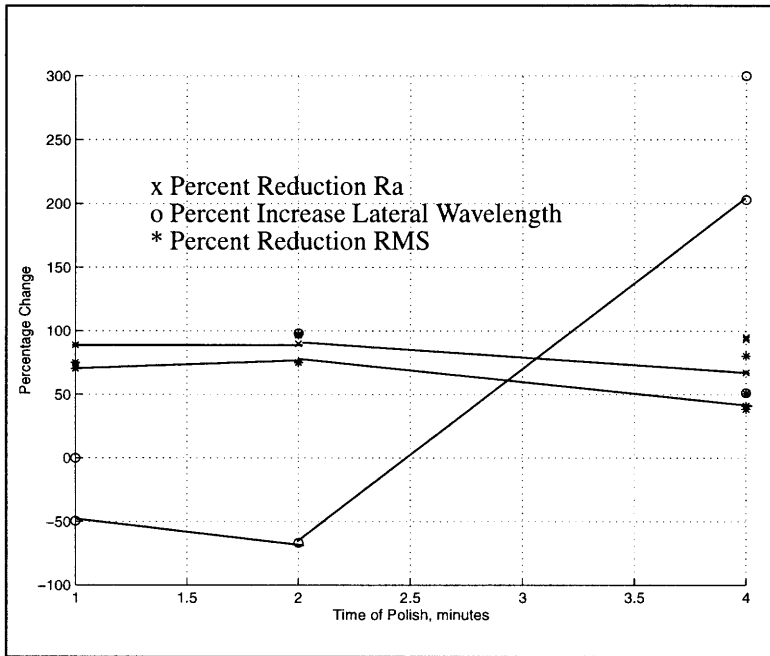
Figure 5.23: Percentage Change of Morphology Parameters With Polish Time

Table 5.4 shows the effect of pirahna and HF clean on the morphology is negligible,

and can only improve the morphology:

get better than before the clean.

Table 5.4: Piranha, Pirahna+HF Effect on Morphology

Condition	RMS (nm)	RA (nm)	Lateral Wavelength (microns)
Original	0.394	0.270	0.334
Pirahna (3:1H$_2$SO$_4$: H$_2$O$_2$)	0.222	0.178	0.505
Pirahna (3:1H$_2$SO$_4$: H$_2$O2)	0.222	0.178	0.505
Pirahna (3:1H$_2$SO$_4$: H$_2$O$_2$)	0.219	0.173	0.505

Table 5.4: Piranha, Pirahna+HF Effect on Morphology

Condition	RMS (nm)	RA (nm)	Lateral Wavelength (microns)
Pirahna+HF	0.183	0.146	0.505

5.3 Discussion of AFM Results

The tables show the unifying feature that the morphology after the CMP is strongly dependent on the initial morphology of the wafer. This is demonstrated since we attain different values for morphology parameters at the same CMP conditions, where the only variable that is changing is the time of the touch polish. This statement assumes that the CMP experimental conditions remain approximately constant.

5.3.1 RMS Value

From Figure 5.23, we observe that the RMS value remains about the same for all times. There is a very slight reduction in RMS as we go from the 1 minute polish to the 2 minute polish. However, when we move to the 4 minute polish, the surface roughness became slightly less. As we move from SOIAS2 to SOIAS10, where SOIAS2 received 2 minutes of touch polish, and SOIAS10 received 4 minutes, we see that the change in RMS is reduced. The main difference between the morphology of the two wafers is that SOIAS2 has a smaller RMS roughness than SOIAS10 to start (2.84 nm compared to 3.71 nm). Also, the morphology of SOIAS2 has a larger wavelength so it is less "bumpy" on a lateral scale. The data shows that increasing the touch polish by 2 minutes slightly deteriorates the change in rms, indicating that every wafer needs to be treated individually in order to get required results. It shows that a rougher surface and a surface that is laterally more varying needs a longer touch polish time to reduce the RMS value.

5.3.2 RA:

The average height measurement is similar in trend to the RMS measurement, but it has some subtle differences. Figure 5.23 demonstrates that the data for same polish times are closer to each other, demonstrating that measuring RA is less sensitive to the initial morphology of the wafer. The RA measurement also seems to be more consistent. We expect that wafers starting off with the same morphology end up with also a similar morphology after the touch polish. This is shown for wafers SOI3S and SOI4S whose morphology remained very similar after the touch polish.

The measurement also shows that a wafer that is more bumpy laterally and vertically requires a longer polish time (more than double) than a wafer that is initially smoother as can be seen by observing the difference between the 2 minute and 4 minute touch polish. As in the RMS measurement, the data shows that polishing for a longer time for wafers with similar morphology give a larger change for the better.

5.3.3 Lateral Wavelength

From Figure 5.23, one observes the trend that a larger touch polish time gives a larger lateral wavelength, meaning the morphology has smaller frequency components, making it smoother in the lateral direction. However, wafers SOIAS7 and SOIAS6 experienced a larger PSD afterwards. They both had a morphology with the same lateral wavelength before starting (1 μm wavelength). That shows that if the wafer morphology is smooth initially then the CMP will make it a bit worse than before and introduce higher frequency components. On the other hand, a wafer that has high frequency components to start, will have much lower frequency components after the CMP.

5.3.4 Processing steps effect on roughness/ Spatial dependence

A SIMOX reject wafer was exposed to chemicals that are often seen during the processing, namely pirahna and HF. It was discovered that the pirahna clean reduces the surface

roughness slightly and smoothens laterally. It was also found that HF smoothens and does not effect the lateral wavelength. As a test, we determined the effect of oxidizing and then stripping the oxide on the morphology of a dummy SIMOX wafer. It must be noted that the wafer underwent a pirahna clean before the oxidation. The result of the oxidation was to slightly roughen the surface. A wafer with an initial surface roughness of 0.08 nm-rms had its roughness increased to 0.161 nm-rms (see Figures 5.20 and 5.21).
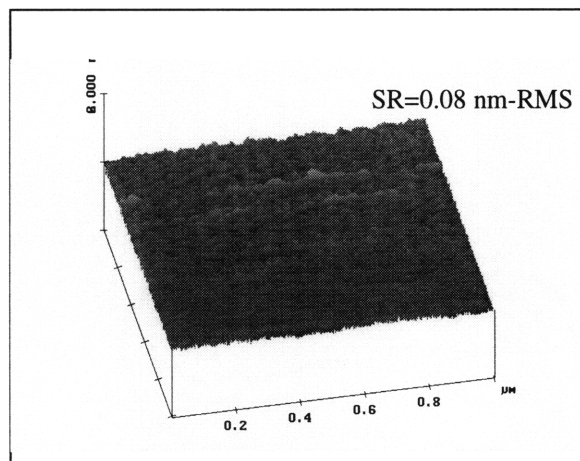
Figure 5.24: Wafer 8C after polishing
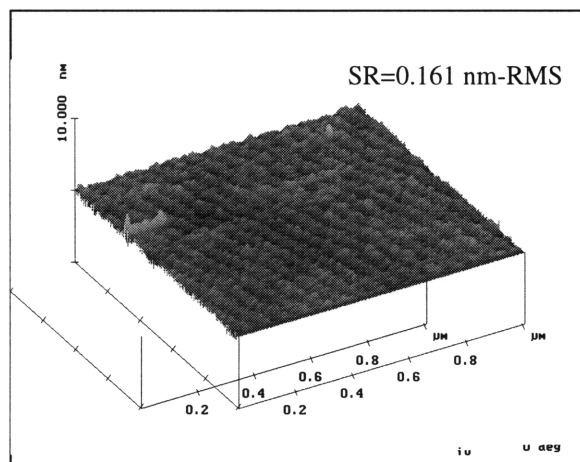
Figure 5.25: Wafer 8C after oxidation thinning

As a test, the roughness was determined at different locations of the wafers to determine the spatial variation of the roughness. Touch polished wafers using the RODEL recipe had a 0.23 A-RMS/cm variation. I then determined the film uniformity after the touch polish to be 7 angstroms/inch. That translates to a 28 angstrom variation on a 4 inch wafer. The dummy SIMOX wafers from IBIS had 8 angstrom/inch variation to start with. That gives a 32 angstrom variation of silicon thickness. This allows us to conclude that the variation in silicon film thickness improved by ~4 angstroms after the touch polish.

Chapter 6

Improving Morphology

6.1 Chemical Mechanical Polishing (CMP)

Chemical-mechanical polishing (CMP) of silicon with a colloidal suspension of silica is a standard technology for the preparation of smooth, defect-free silicon surfaces [17]. The surface of the silicon film on the top of the stack is touch-polished using CMP in order to achieve an atomically smooth surface (~1-2 angstroms RMS). The RMS roughness was defined earlier in Eq. 5.9.

CMP combines the mechanical action of a rotating polymeric polishing pad with the chemical activity of an alkaline polishing slurry containing silica particles[3]. CMP works by selectively removing bumpy features over depressions so as to achieve as flat a surface as possible. For this project, CMP will be used to decrease the surface roughness by removing these bumps.

6.2 How CMP Works

The chemical component of CMP works by etching silicon. Silica particles in the slurry create chemically activated ions that can terminate on silicon atoms. These silicon bonds have a larger electronegativity compared to the Si-Si bonds, so a positive polarization is left on them. OH$^-$ ions from the slurry solution, which has a basic pH value of around ten, attack the Si-Si bonds and break them forming Si- OH$^-$ bonds and the leftover Si reacts with a proton supplied by the surrounding water creating Si-H. This also produces another OH$^-$ ion that can contribute to the removal process, so a chain reaction occurs with the end result being a removal of silicon.

The mechanical component of CMP does not only involve the actual shear forces introduced at the pad wafer interface, but it also accelerates the chemical reaction rate of

silicon removal. Fustetter et al. [3] report that the mechanical component in CMP results in a lowering of the activation energy of the above mentioned chemical reaction and hence an increased silicon removal during CMP as compared to pure chemical etching.

It is found that after CMP, the surface is passivated by hydrogen, so that the surface is hydrophobic. This makes the surface chemically stable[17]. The polishing removal rate is dependent upon the pH of the slurry. The rate peaks at a pH of 11.0. After CMP, Si <100> exhibits termination by SiH_x where x could be monohydride, dihydride, or trihydride. For pH other than 11, Si atoms are terminated also by OH groups. There is a small increase in the removal rate for slightly acid pH. OH⁻ is consumed during CMP. MIR-FTIR spectra show peaks corresponding to monohydride structures, tri-hydrides, and di-hydrides. Absorption in the spectrum is found that corresponds to oxidation of the silicon surface atoms that are terminated with hydrogen [17]. This shows that there is backbond oxidation of terminating (mono)hydrides. The spectra also shows that there is a preference to create suboxides like SiO_2, instead of the stoichiometric SiO_4. Some examples of terminating structures are- $HSi(SiO_2)$ and $H_2Si(O_2)$. These groups are observed for pH levels other than 11. This means that at these pH levels, there is a different removal mechanism. It is removal of silicon by oxidation of terminating H by OH⁻ group which comes from the slurry[17].

Pietsch et al. [17] gives the four characteristics of CMP:

1. Increase in removal rate, with increase in pH.

2. OH⁻ important for removal mechanism, and they are consumed during polishing.

3. Colloidal silicon (Siton) acts as a transmitter of OH⁻.

4. There is a different mechanism at pH=11 than all the other possible pHs.

6.3 CMP Experiments at MIT

The major challenge of the CMP portion of the project is not only to achieve a surface roughness of a couple of angstroms, but also at the same time remove less than 200 angstroms of the Si film. Reducing the surface roughness is an accomplished and well understood practice for manufacturers of silicon wafers, but fine control over the etch rate has is not a well-known practice in industry given the large boule they have to work with. I received a recipe from RODEL Inc. The recipe and the equipment needed is given in Appendix A.5.

6.3.1 Results of test experiment: Touch Polish of SIMOX dummy wafers

Wafer	tsi initial (angstroms)	tsi final (angstroms)	Surface Roughness initially (nm RMS)	Surface Roughness final (nm RMS)
4C	2150	1907	0.548	0.473
5C	2150	2709	0.628	0.140
7C	2150	2543	0.733	0.179
8C	2139	1991	0.595	0.090

Table 6.1: Touch Polish of SIMOX Dummies

From Table 6.1, we deduce that the approximate rate of removal for this recipe is 50 angstroms/minute.

6.3.2 Results of Touch Polish Experiment:
Below are two tables showing the surface roughness before and after the touch polish with the time of polish using the RODEL recipe:

57

Wafer	SRinitial (nm RMS)	SR final (nm RMS)	Time of Polish (minutes)
SOIAS1	2.58	2.578	No Polish
SOIAS2	2.52	0.165	2
SOIAS3	2.02	0.490	1
SOIAS4	3.96	0.120	4
SOIAS5	2.37	2.37	No Polish
SOIAS6	0.33	0.250	1
SOIAS7	2.93	0.120	2
SOIAS8	2.18	2.18	No Polish
SOIAS9	2.56	2.56	No Polish
SOIAS10	3.41	0.156	4 minutes

Table 6.2: Touch-Polish Experiment Results on SOIAS Wafers

Wafer	SRinitial (nm RMS)	SRfinal (nm RMS)	tsi initial (Anstroms)	tsi final (Anstroms)
SOI3S	0.22	0.132	2413	2238
SOI4S	0.22	0.134	2410	2269
SOI5S	0.224	0.224	2431	2431
SOI6S	0.222	0.222	2419	2419

Table 6.3: Touch Polish SOI Wafers

Wafers SOI3S and SOI6S underwent 4 minutes of the touch polish. From table 6.3, we calculate that SOI3S had 175 angstroms removed giving an approximate rate of removal of 43.8 angstroms/minute.

After the touch-polish, the devices were fabricated. Appendix A.2 gives the processing and fabrication steps.

Chapter 7

Measurements

7.1 Fabricated Devices

NMOS and P-i-N gated diodes were fabricated into the silicon film of the SOIAS structure. This was done as explained before following a standard CMOS process but excluding all steps related to PMOS and converting processing steps dealing with production of NMOS transistors, to ones that produce gated P-i-N diodes. The P-i-N gated diodes were used to determine the interface state charge density. The motivation for building gated P-i-N diodes is that it has been demonstrated that charge pumping measurements on SOI silicon films give accurate value for the D_{it} [7]. The NMOS transistors were used to conduct mobility measurements as a function of vertical electric field. This also is a prime indicator of the surface quality [12].

One consideration is that small dimension gated P-i-N diode is preferred so as to minimize any currents due to geometrical factors. This would overestimate the charge-pumping current and hence the D_{it}.

7.2 Device Characterization

The first step done is a full characterization of devices so that parameters may be determined. This includes threshold voltage (V_t) and subthreshold slope (SS). These two parameters are determined by performing IV measurements on MOSFET devices. The IV curves can be found in Appendix B.1. Table 8.1 below gives a summary of the electrical parameters:

WAFER	DIE	Vt (volts)	S (mV/ decade)	ΔL (μm)	Rext (ohms)	Roughness (nm-rms)
SOIAS2	(3,6,L)	.734	84.8	.109	13.2	.165

	(4,6,L)	.695	85.8	.30	38.3	
	(5,6,L)	.731	83.7	.189	34.7	
SOIAS3	(4,4,L)	.760	84.4	-.077	109	.486
	(1,3,L)	.750	82.1	-.281	27.6	
	(8,2,L)	.766	82.7	-.435	49.9	
	(2,3,L)	.804	89.3	-.157	18.9	
SOIAS7	(8,1,L)	.854	73.6	-.09	8.49	.196
	(8,3,L)	.716	73.2	-.121	76	
SOIAS8	(7,1,L)	.768	82.9	-.128	180	2.18
	(8,1,L)	.709	96.8	-.618	80	
	(5,2,L)	.817	90.0	-.296	24.3	
	(4,2,L)	.843	92.0	-.317	105.9	
SOIAS 10	(2,3,L)	.609	82.6	-.051	20.3	.156
SOI6S	(8,1,L)	.764	76.8	-.53	61	
	(8,3,L)	.777	88.6	-.075	298	
BULK2	(8,1,L)	.716	83	-.370		.169
	(6,2,L)	.812	82			

7.3 Interface State Density (D_{it})

There exist several methods of determining D_{it}. One can use MOS capacitance and conductance measurements, but the issues of series resistances, parasitic capacitors, and interface coupling make it very difficult to interpret these measurements [9]. As explained above, charge pumping has been demonstrated as the superior technique.

7.3.1 Charge Pumping on P-i-N Gated Diodes

Charge pumping works by repeatedly switching the film from inversion to accumulation and vice-versa [6]. In inversion, some of the minority carriers are trapped at interface states. When the gate is switched to accumulation, most of the minority carriers leave via the drain contact, however, those that were on the interface state sites recombine with

majority carriers [6]. These majority carriers are supplied by the substrate, therefore, producing a substrate current, called the charge pumping current. However, for SOI material, the substrate is insulated from the Si film via the buried oxide. So, a means of fabricating a source of majority carriers must be created. This is accomplished by using P-i-N gated diodes. The P region acts as the source of majority carriers so it is the analog of the substrate, and the N region acts to control the potential of the channel just like a source or drain in a MOSFET. The charge pumping current is given by [6]:

$$I_{cp} = q^2 fWLD_{it}\Delta\psi_s \qquad (7.1)$$

where D_{it} is the average concentration of interface traps, f is the frequency of the pulse applied to the gate, and $\Delta\psi_s$ is the surface potential range swept during the pulse. For my experiment, I used a trapezoidal pulse and the surface potential range swept for that is [6]:

$$\Delta\psi_s = \frac{2kT}{q}\ln\left(v_{th}n_i\sqrt{\sigma_n\sigma_p}\sqrt{\tau_r\tau_f}\frac{|V_{fb} - V_T|}{|\Delta V_g|}\right) \qquad (7.2)$$

where v_{th} is the thermal velocity of the carriers, σ_n and σ_p are the capture cross sections for electrons and holes respectively, τ_r and τ_f are the rise and fall times of the ΔV_g pulse.

Plugging in Eq. 7.2 into Eq. 7.3 gives:

$$Icp = 2qfwlD_{it}kT\ln\left(v_{th}n_i\sqrt{\sigma_n\sigma_p}\sqrt{\tau_r\tau_f}\frac{|V_{fb} - V_T|}{|\Delta V_g|}\sqrt{\tau_r\tau_f}\right) \qquad (7.3)$$

During the sweep of the gate, the film goes into three different regions:

1. No inversion (no carriers are trapped) so $I_{cp} \approx 0$

2. $V_g > V_T$ Inversion regime, I_{cp} plateaus.

3. $V_{GL} > V_{FB}$ Surface does not return to accumulation, so $I_{cp} \approx 0$.

7.4 Charge Pumping Experimental Setup/Measurement

The input signal to the gate is a square wave pulse from a HP81223 Pulse Generator at 10 kHz with a peak to peak voltage of 2 Volts centered at V=0 Volts. The HP4140B is used to measure the charge pumping current through the drain. It is also used to apply a ground potential to the source and a potential to the substrate. An oscilloscope is used to monitor the signal to the gate.

For each device, two measurements were performed. I first applied a square wave pulse at 10 kHz and plotted the low gate voltage level as a function of the charge pumping current. As explained above, I observed a plateau. I then choose a point on the plateau, and use that low gate voltage level for the next step. I then apply a triangular voltage wave to the gate with the low gate voltage level determined from the step before, and plot the charge pumping current as a function of frequency of the pulse. The plots for these two figures for each device are shown in Appendix B.2. I have included one example in the main body of this work:
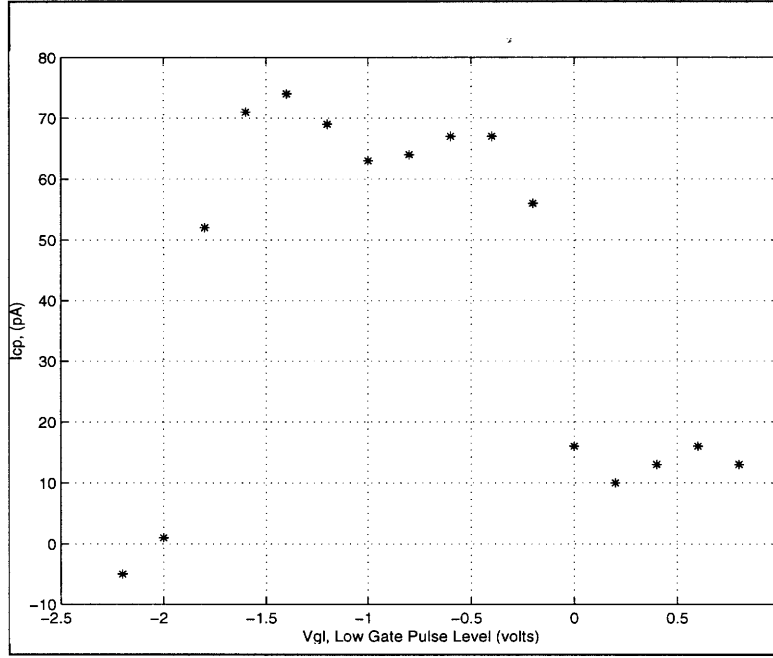
Figure 7.1: Bulk2 Signature

The capture cross-section values are obtained by plotting the recombination charge per cycle versus the frequency of the gate pulse [6]. The limit of the charge becoming zero gives a frequency f_o. From that, we can determine the cross-section constants using the following equation [6]:

$$\sqrt{\sigma_n \sigma_p} = \frac{1}{v_{th} n_i} \frac{\Delta V_g}{\left| V_{FB} - V_T \right|} \frac{f_o}{\sqrt{\alpha(1-\alpha)}} \qquad (7.4)$$

Where α is the fraction of the period when Vg is rising. In order to obtain an accurate value for D_{it}, I made sure that I am only studying the front interface by designing the devices so that they are not fully depleted. If they were, there would be a sharp peak in the charge pumping current curve that is explained by pumping of some of the back interface traps. Secondly, the back gate was maintained either in strong inversion or in accumulation.

7.5 Actual Determination of D_{it}

D_{it} was determined by calculating the average recombination charge as a function of frequency. This was done by applying a sawtooth waveform to the gate of the transistor and recording the current as the frequency is adjusted. The recombination charge is given by:

$$Q_{it} \equiv \frac{I_{cp}}{fWL} \tag{7.5}$$

A sawtooth waveform has $\alpha=1/2$. The plot of Q_{it} versus the logarithm of the frequency is a straight line and the slope gives the D_{it}. Manipulation of Eq. 7.3 gives:

$$D_{it} \equiv \frac{slope}{4.6qkT} \tag{7.6}$$

where q is the electronic charge, k is boltzman's constant, and T is the temperature.

The experiment was performed on each wafer. The plots can be seen in Appendix B.2. I have included a plot for one of the wafers below:
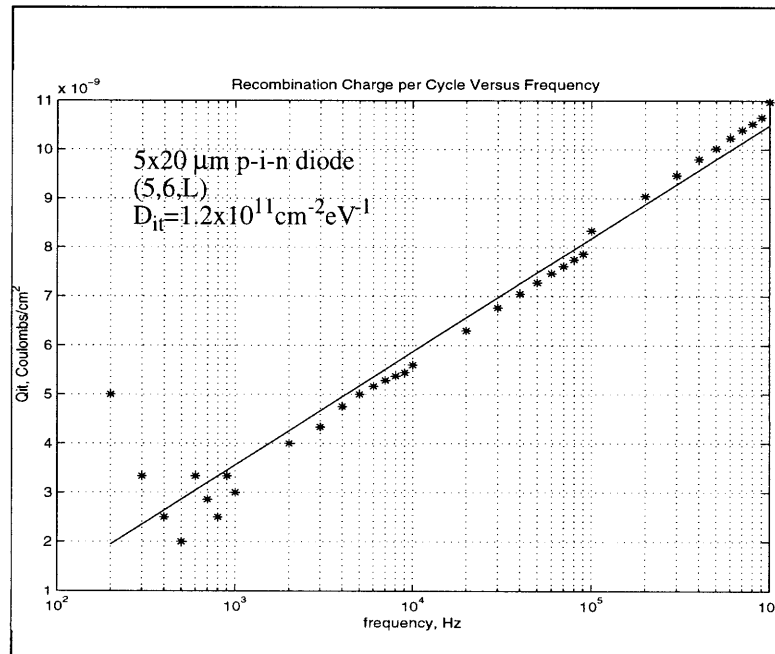
Figure 7.2: Bulk2 Dit Determination

The table below shows D_{it} values for several devices on the same wafer:

Wafer	Rough-ness (nm RMS)	D_{it} (cm^{-2}eV)	D_{it} (cm^{-2}eV)	D_{it} (cm^{-2}eV)	D_{it} (cm^{-2}eV)	D_{it} (cm^{-2}eV)
SOIAS2	.165	7.42×10^{11}	6.45×10^{11}	6.22×10^{11}	6.26×10^{11}	6.99×10^{11}
SOIAS3	.486	6.25×10^{11}	7.35×10^{11}	7.48×10^{11}	8.76×10^{11}	9.66×10^{11}
SOIAS7	.196	2.78×10^{11}	2.11×10^{11}	3.48×10^{11}	4.58×10^{11}	3.59×10^{11}
SOIAS8	2.18	8.11×10^{11}	5.96×10^{11}	5.34×10^{11}	1.12×10^{12}	1.23×10^{12}
SOIAS10	.156	1.45×10^{12}	1.13×10^{12}	1.08×10^{12}	1.06×10^{12}	7.22×10^{11}
SOI3S	.132	2.19×10^{11}	1.53×10^{11}	1.04×10^{11}	1.06×10^{11}	
SOI6S	.122	9.04×10^{11}	5.22×10^{11}			
BULK2	.169	1.20×10^{11}	1.33×10^{11}	5.97×10^{11}		

Table 7.1: D_{it} Numbers

Figure 7.4 plots the data in the table:
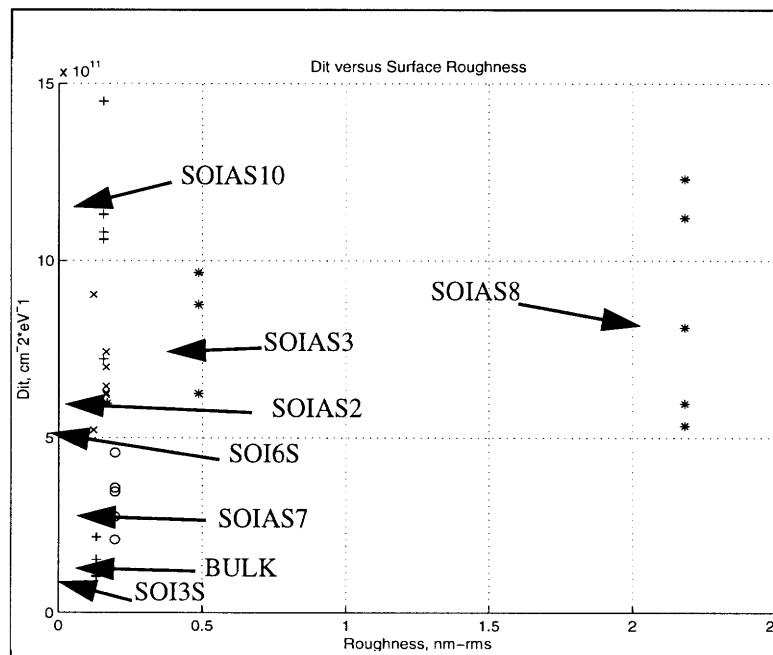
Figure 7.3: D_{it} Versus Interface Roughness- Several Samples

Ignoring some of the samples, we observe that there is a trend for D_{it} to increase with surface roughness. Moreover, the plot demonstrates that a smoother surface has less on-wafer variation of D_{it}, an important factor in V_t control. This can be seen more clearly by plotting a few of the wafers, namely, SOIAS2, SOIAS3, and SOIAS8:
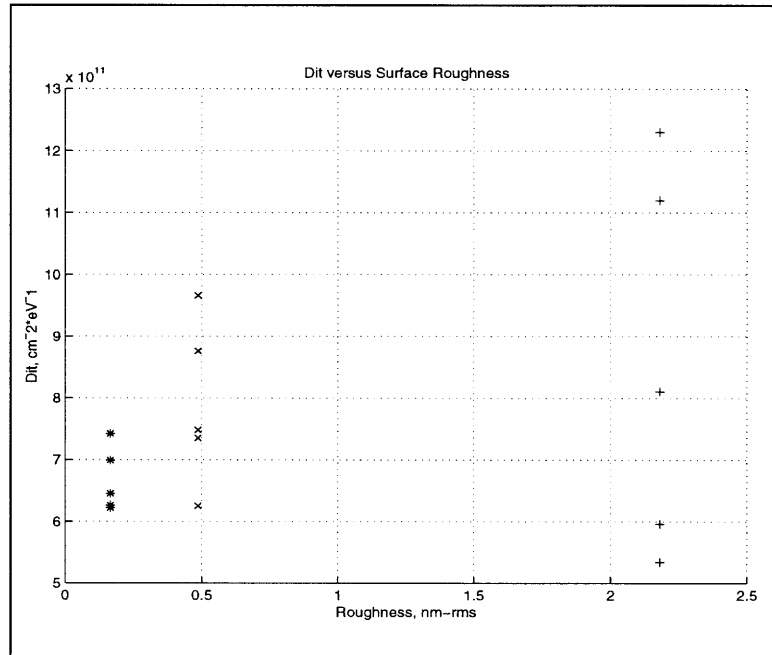
Figure 7.4: Dit Versus Roughness

From the plot, we notice that there is a slight increase in D_{it} for rougher samples. I have fitted the average value of several samples on the same wafer.

7.6 Time-Zero Dielectric Breakdown (TZDB)

The quality of the Si-SiO$_2$ interface has major consequences on electric devices. A rough Si surface that has been oxidized will result in a poor quality interface. This in turn makes the devices susceptible to early breakdown, hence degrading yield and reliability of MOS VLSI circuits. As device dimensions get smaller in the semiconductor industry, thin-

ner oxides and shallower junctions will be used making surface microroughness even more important for device performance and reliability.

The integrity of the Si-SiO$_2$ interface is determined by performing the TZBD test. It involves providing a step voltage input to the gate of the transistor, and determining the electric field required to cause the device to fail. It is expected that polished samples give a higher success rate since surface asperity results in enhanced localized electric fields causing breakdown to occur at lower applied electric fields as compared to a smooth surface [10]. Low breakdown fields are due to field enhancement from bumps at the injecting electrode. They also cause polarity-dependent field enhancement[14]. Positive gate bias (electron injection from the substrate) causes a much lower breakdown voltage than negative bias (electron injection from gate)[14]. The sharpness of the bumps, and hence the field enhancement, is greatest at the Si-SiO$_2$ interface. It has been found that there is greater field enhancement for electron injection at the Si-SiO$_2$ interface compared to the gate-SiO$_2$ interface. Field enhancement depends on the dimensions of the bump. For a fixed bump height, the field enhancement increases as the radius of curvature at the tip of the bump decreases.

There are several mechanisms that can bring about breakdown other than due to asperities in the morphology of the silicon surface. The key issues in reliability is that the surface be free of particles, organic impurities, metallic impurities, native oxide, adsorbed impurity molecules. It is reported that oxide defects are the major cause of oxide breakdown. The oxide defects are caused by precipitates in the oxide. The precipitate included in the oxide film reduces the effective thickness of intrinsic oxide and hence decreases the breakdown strength at the oxide defect area [22]. There are three steps in the breakdown mechanism:

1. Voltage applied to gate is not dropped across the defect but across the intrinsic oxide

part. [22]

2. This intrinsic oxide short circuits when the voltage exceeds its intrinsic breakdown strength. [22]

3. The defect part begins to conduct when the leakage current through it exceeds a certain level [22].

These other reasons for breakdown should be taken into account when correlating the breakdown field with the surface roughness.

7.7 TZDB Results

Here is the plot showing the cumulative percentage of devices broken down at a particular electric field for a field of 30 devices. Each wafer is plotted on this graph. The graph shows that there is no correlation between breakdown field of the oxide and surface roughness.
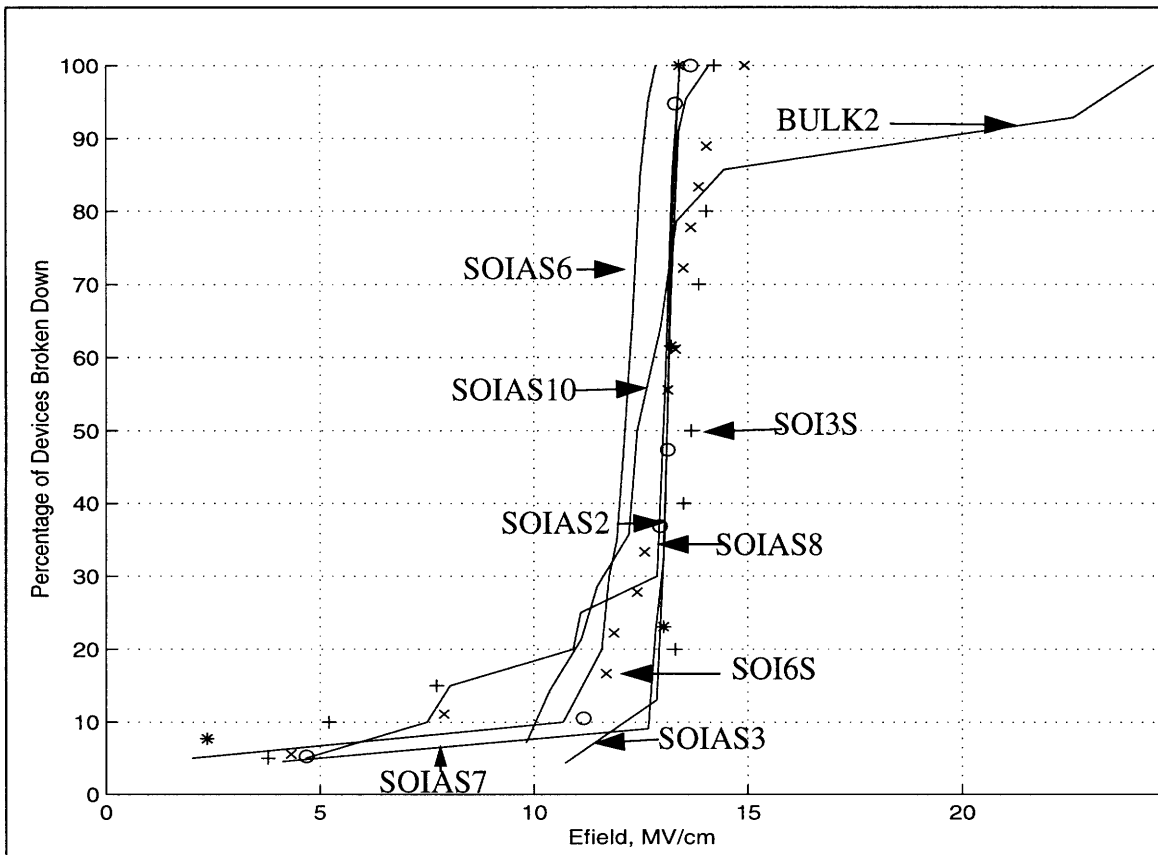
Figure 7.5: TZDB CURVES

In addition to the TZDB measurement, I investigated the oxide quality by examining the onset of the Fowler Nordheim current as a rougher sample would be expected to begin tunneling at a smaller electric field. This was done by calculating the electric field across the oxide needed to give a gate current Ig=1pA. Below are the figures showing the gate current:
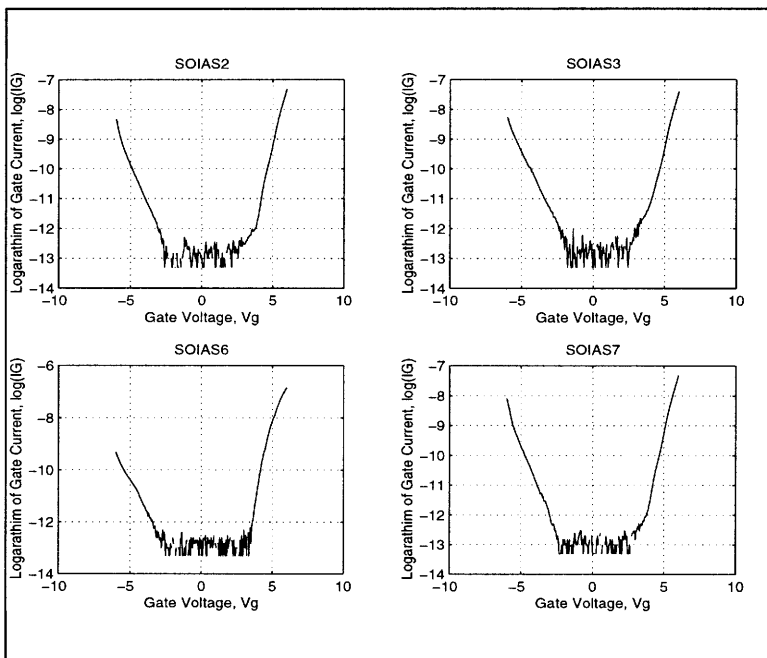
Figure 7.6: Fowler Nordheim SOIAS2, 3, 6, 7
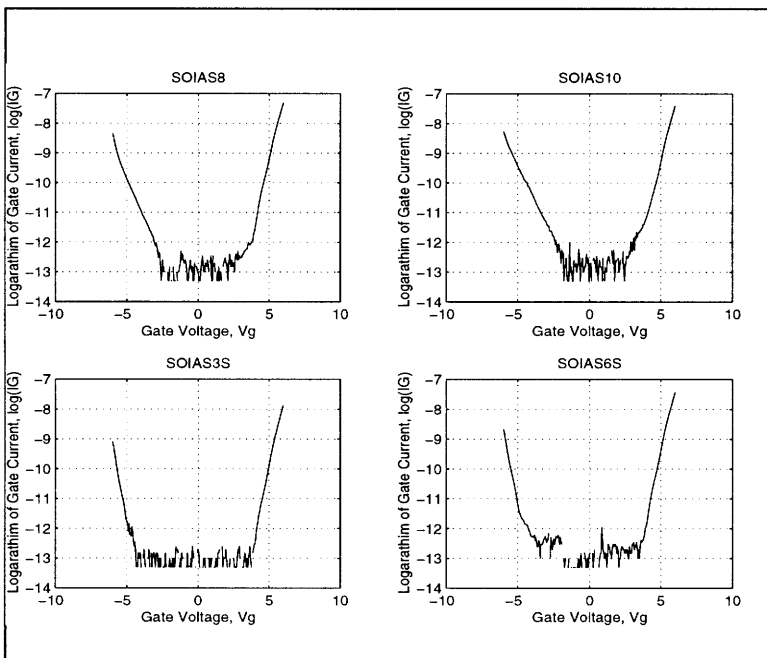
Figure 7.7: Fowler Nordheim SOIAS8,10, SOI3S,6S
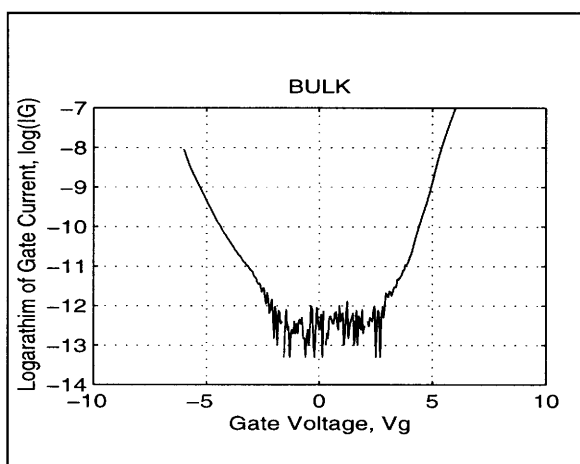
Figure 7.8: Fowler Nordheim Bulk2

The plots were compared by determining the electric field required that gives a 1pA gate current. Table 7.4 gives the data, and Figure 7.12 plots it:

WAFER	Roughness (nm-rms)	Electric Field (MV/cm)
SOI3S	0.132	7.47
SOIAS10	0.156	5.69
SOIAS2	0.165	6.79
BULK2	0.169	5.36
SOIAS7	0.196	6.75
SOI6S	0.222	7.06
SOIAS6	0.250	7.17
SOIAS3	0.486	5.68
SOIAS8	2.181	6.73
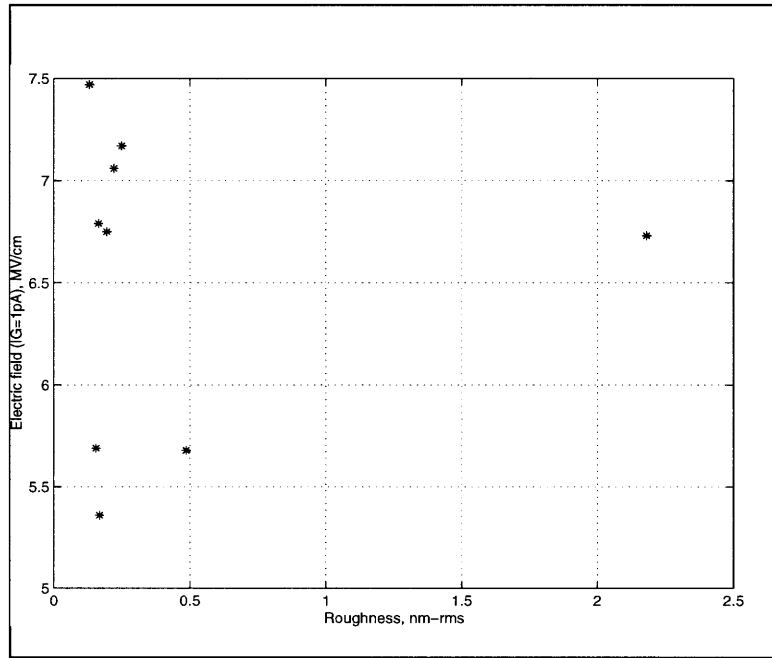
Figure 7.9: Roughness Versus Efield @ IG=1pA

Figure 7.9 shows that there is not correlation between surface roughness and the Fowler Nordheim current, enforcing the conclusion obtained from the TZDB measurement.

7.8 Effective Mobility (μ_{eff})

Measurement of the effective mobility of carriers will give an indication of the quality of the film since a large number of impurities will result in more scattering of carriers and hence, a smaller value of mobility [12]. The effective channel mobility may be determined from the following two equations:

$$\mu_{eff} = \frac{I_D}{\left(\frac{W}{L}\right)Q_i V_{ds}} \qquad (7.7)$$

$$Q_i'(V_{gs}) = \int\limits_{-\infty}^{V_{gs}} C_g'(V_{gs})dV_{gs}$$

(7.8)

where the prime denotes per unit area.

The effective mobility is plotted as a function of the effective electric field. The effective electric field is defined as:

$$E_{eff} = \frac{Q_b + Q_n/2}{\varepsilon_{Si}}$$

(7.9)

Where Q_b is the bulk charge and Q_n is the inversion layer charge.

It has been shown that channel mobility increases as the surface microroughness decreases[12]. This is because Si-SiO$_2$ interface roughness is a cause of carrier scattering thus degrading the mobility of devices. This phenomena is accentuated when a large gate voltage is applied, meaning more carriers, since the carriers are closer confined to the interface. Also, the density of the coulomb centers at the interface increases with increased roughness[13]. The roughness scattering is especially important at high carrier concentrations, whereas at low carrier concentrations the mobility is determined predominantly by coulomb and phonon scattering[13].

Channel mobility degradation due to interface roughness is solved theoretically by treating the surface roughness as a perturbation in the potential well. If a large electric field is applied, electrons will be strongly confined to the interface. If the surface roughness size is comparable to the average distance of the electron gas from the interface, then the perturbation theory is not valid anymore. As the electric field becomes smaller, then the mobility degradation predicted by perturbation theory is more consistent with the experimental results. The reason behind the discrepancy is that electrons can not feel the

full RMS roughness if the interface is very rough, but will travel conformably along the interface [23].

The mobility measurement is shown below in Figure 7.11. The curve shows that the polished SOIAS sample (SOIAS10) has a larger mobility than the un-polished sample (SOIAS8).
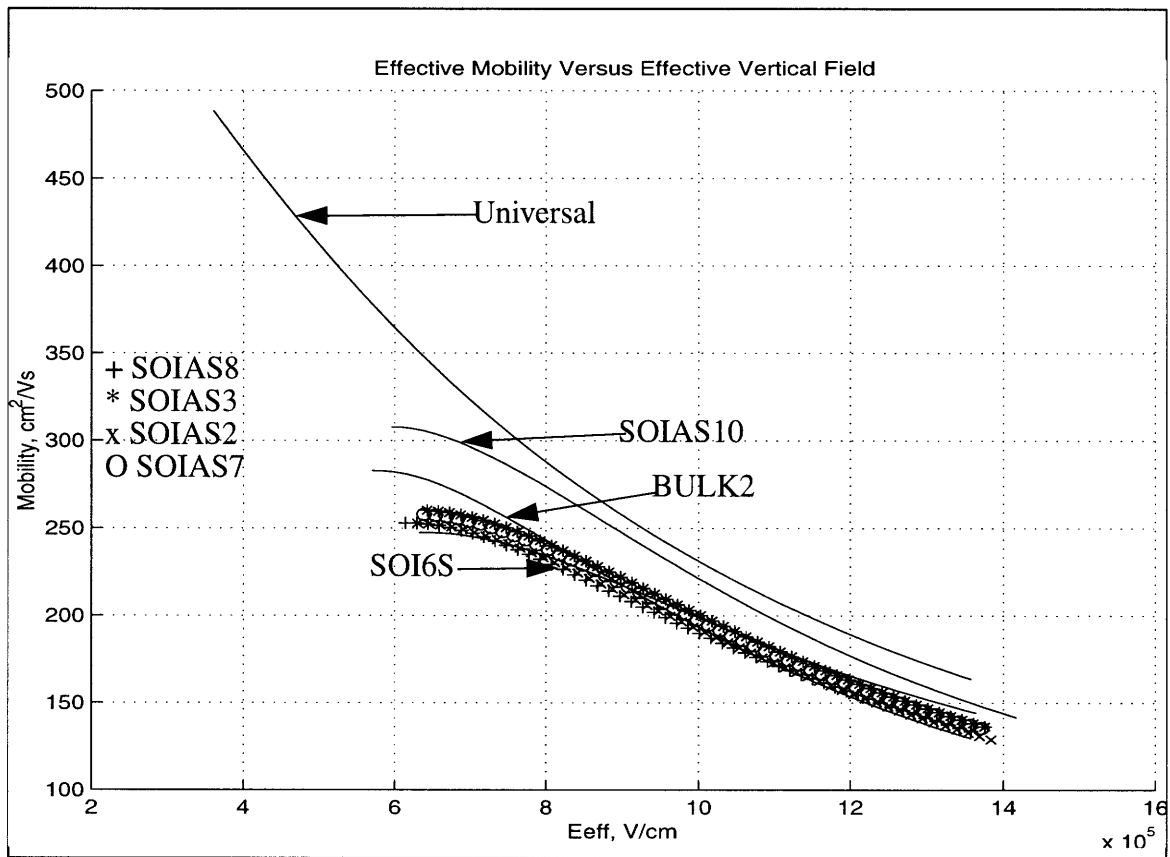
Figure 7.10: Effective Mobility Versus Effective Electric Field

The figure below plots the surface mobility (μ_{sr}) as a function of surface roughness for E_{eff}=0.8 MV/cm. Surface mobility is determined using Matthiessen's rule:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{sr}} + \frac{1}{\mu_{bulk}} \tag{7.10}$$

where μ_{eff} is given in the figure above and μ_{bulk} is given to be ~400 cm²/Vs for a doping of 4.71×10^{17}.
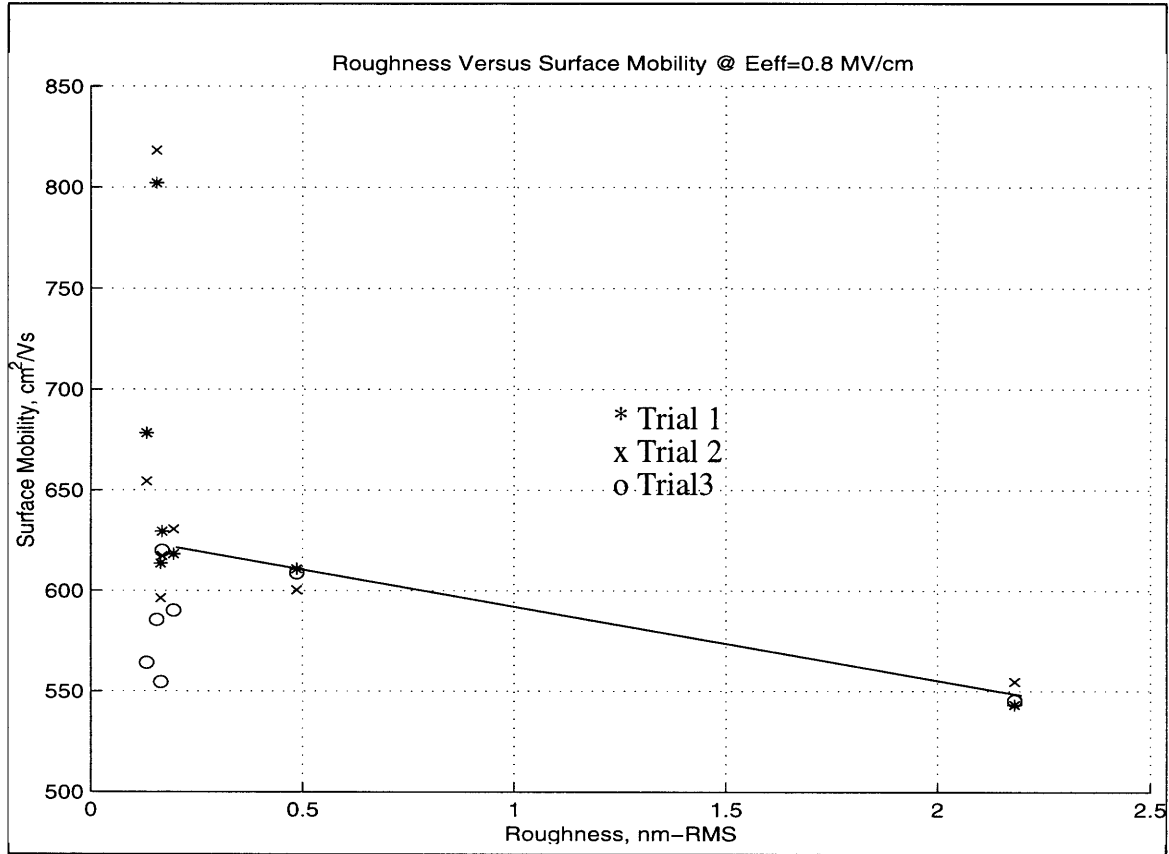
Figure 7.11: Surface Mobility Versus Surface Roughness For Eeff=0.8 MV/cm

The plot shows that there is a weak correlation between surface roughness and mobility. There is significant scatter of the data at low roughness which obscures any real correlation. The source of this scatter could not be determined in this work.

7.9 Analysis of Results

The results I obtained at first surprised me a great deal for many of them run contrary to what was found in previous research by others, but a critical analysis of these previous results demonstrate there are subtle difference and the conclusions made need more evidence. I conclude that there is no definite correlation between roughness and electrical

parameters. There are, however, advantages to polishing the surface compared to processing on rough surfaces such as less on-wafer D_{it} variation. I cannot give a physical reason behind this, but I will try to speculate. The roughness on the wafers might be changing a great deal from location to location. What might be thought to be a generally smooth surface, might actually have a spatially varying roughness. Recall that a 1 μm by 1 μm square is used in the calculation of the surface roughness.

Concerning the discrepancy of the literature with the finding of this work on the issue of D_{it} correlation with roughness, I must note that Hahn et al. [1] uses a different technique of surface characterization. His experiment occurred in 1983 well before the invention of AFM. He uses SPA-LEED (surface profile analysis of low energy electron diffraction). This technique senses differences in atomic step heights. It also gives the shape of the distribution. From these two, one can calculate a step density. It is this value that Hahn correlates with electrical parameters. This value can be quite different than the surface roughness since the beam size is much larger than 1 μm, the scan size used in the AFM resulting in loss of morphology information. It is also worth mentioning that Hahn's conclusion that mobility is reduced with an increase in roughness is from Hall mobility measurements that he performed at a temperature of 4.2 K. My experiment was at room temperature and was not a Hall measurement. Kimura et al [76]. performed a D_{it} measurement for two different substrate roughness measured by AFM, 24.3 nm-RMS and 18 nm-RMS. He found that D_{it} near the silicon midgap is higher for the rougher sample. Examining his data, the difference is very small, 2×10^{10} and 3×10^{10} cm^{-2}eV^{-1}. This difference is larger than the scatter I got in my experiments. Also, my experiments show that larger roughness samples have a larger deviation in roughness. Therefore, I believe that Kimura et al. may not have measured enough samples to unequivocally conclude that D_{it} in general decreases with reduced roughness.

The D_{it} variation decreases with decreased roughness perhaps because a sample that has seen a touch polish not only has its roughness reduced, but also the roughness becomes more uniform throughout the wafer so that different devices see similar roughness values.

There is no major change in D_{it} for different roughness samples perhaps due to the fact that surface roughness might not only be the only factor. Other indications of morphology might be important such as the periodicity of variation (lateral wavelength). Also, charges in the oxide can produce enough electric field to create states [25], so the D_{it} is dependent somewhat on the cleanliness of the process. All these issues could be superimposed upon the dependence on roughness. It is worth noting that the SOIAS wafers always have a higher D_{it} than bulk. This could be attributed to the fact that the SOIAS wafers saw extra processing steps, namely the TMAH substrate removal. That could have added ionics to the oxide, causing charges and states to be created.

It is difficult to state that the reason that SOIAS10 has a larger mobility than BULK is that its surface roughness is smaller than bulk. Other factors need to be examined. I examined the possibility that perhaps SOIAS10's doping was incorrect, hence, making the effective electric field wrong. I went back to determine the amount of doping necessary to make the SOIAS10 curve fall on top of Bulk. It turns out that 3×10^{17} less doping in SOIAS10 is needed to make them the same. This is a large number so it is unlikely that any doping difference can be attributed to SOIAS10 having a larger mobility than Bulk. One possible discrepancy is that the Bulk sample might have a larger fixed oxide charge. Sun et al. show that fixed oxide charge reduces mobility [37]. Sun et al. [37] explain that fixed oxide charge effects the surface mobility by:

$$\mu_{max} = \frac{\mu_o(N_A)}{1 + \alpha(N_A)Q_F} \tag{7.11}$$

Where:

$$\mu_o = 3490 - 164\log(N_A) \text{ and}$$

$$\alpha = -1.04 \times 10^{-1} + 1.93 \times 10^{-2}\log(N_A)$$

From the above, I determine that in order for the Bulk mobility curve to match the SOIAS10 curve, the fixed oxide charge density needs to be reduced from $Qf=4.64 \times 10^{11}$cm^{-2} to $Qf=3.89 \times 10^{11}$cm^{-2}. It is very possible that the two samples have different fixed oxide charge since it depends on the cleanliness of the process. On another note, it is worth mentioning that SOIAS10 did not have a linear response of the recombination charge with frequency until very high frequencies in the MHz regime. I am not sure what information that gives about the quality of the interface.

From the mobility plot (Figure 7.10) we observe that all the different roughness wafers are basically the same. This conclusion is backed up by Sherony et al. [33] who discovered that the mobility of fully depleted SOI devices were universal and identical to bulk MOSFET devices. I showed before that SIMOX wafers have ~ 2 times larger roughness than bulk wafers, so one can conclude that there is no correlation between roughness and mobility. It is also interesting to note that the value of the mobility is well below the universal mobility curve including the bulk wafer. A source of this discrepancy could be the fixed oxide charge. Plugging in numbers, using Eq. 7.11 above, I calculate that in order for the bulk mobility curve to match the universal curve, the fixed oxide charge density needs to be reduced from $Q_f=4.64 \times 10^{11}$ cm^{-2} to $Q_f=2.63 \times 10^{11}$ cm^{-2}. Yamanaka et al. [35] show that the correlation of morphology to electrical performance is reduced when the lateral wavelength of the morphology is larger compared with the electron mean path. This is the case for the wafers used in this work. Examining the morphology data from Table 5.2, we

see that the lateral wavelength is on the order of microns, much larger than the electron mean path. This might be a cause of why the roughness is not correlating well with the mobility.

The TZDB plot (Figure 7.5) demonstrates that oxide breakdown does not depend on roughness. From the plot, we can deduce that the source of breakdown is internal since the electric field for 50% cumulative failure is 12 MV/cm. This electric field agrees with literature which claims that the intrinsic breakdown of SiO_2 occurs at 12-13 MV/cm [34]. This then eliminates any external effects such as defects. Yang [10] came up with the same conclusion. She performed a TZDB measurement on different substrate SOIAS wafers and SIMOX wafers with different roughness and found that they all had approximately the same breakdown. This result is reinforced by Kimura et al. [36] who found that oxide breakdown did not change over the scale of roughness change in their experiments (.19 nm-RMS to .25 nm RMS).

Chapter 8

Conclusion

8.1 Final Remarks

This study has demonstrated that there is a weak correlation between surface roughness and electrical properties of MOS devices. It has been shown that polished SOIAS can be promoted to a level close to bulk with respect to oxide reliability and mobility, but the interface states still cannot be brought to the level of bulk silicon. Surface mobility has been demonstrated to decrease slightly with increase in surface roughness. High mobility is needed in modern VLSI chips in order to provide a sufficient drive current for high performance. In order for SOIAS wafers to be used for this application, this work has shown that the surface roughness needs to be reduced ten times in order to get results comparable with bulk wafers. In fact, comparing the roughest and smoothest SOIAS sample it is calculated that a 97% reduction in surface roughness leads to a 16% increase in mobility. It is also interesting to note that a SOIAS wafer reduced to a roughness slightly lower than a bulk wafer had a larger mobility with bulk. In fact, the polished SOIAS wafer had a 8% smaller roughness than the bulk wafer, and that translated into a 9% larger surface mobility at an effective electric field of 0.8 MV/cm.

In addition, this thesis has shown that D_{it} is weakly related to surface roughness. Comparing the roughest SOIAS sample to the smoothest, it is calculated that reduction of the roughness by a factor of 92% results in a 22% reduction in D_{it}. Unfortunately, this trend was not observed in all the wafers. The D_{it} of the polished samples that have roughness values comparable to their bulk counterparts have a six times larger D_{it}. This shows that improving D_{it} of SOIAS wafers is attainable through polishing, but we still can not get as good as bulk silicon even with polishing. It has also been shown that the oxide reliability

has a very weak relationship with surface roughness with the electric field for 50% cumulative failure being nearly independent of surface roughness, a rather surprising result.

8.2 Future Work

Determination of the underlying physics of why surface roughness is not a very important factor in electrical performance is a research challenge. Many physical questions are still unanswered, but the thesis has shed light on the topic and consequently has opened a path for future research.

The thesis has reinforced SOIAS as a possible substrate for use in microlectronics with the only major weakness being the consistently high D_{it}. Improving the D_{it} to match bulk is a serious challenge. D_{it} as explained in Chapter Two depends a great deal on the cleanliness of the process- a parameter very hard to control, and which might as well be out of our hands. Improving the process of perhaps cleaning after CMP, using a cleaner process for the TMAH substrate removal should be investigated to help pursue this new technology further and bring it into mainstream microelectronics.

References

[1] P.O. Hahn, "The Si-SiO$_2$ interface: Correlation of atomic structure and electrical properties", *J. Vac. Science Technology A.*, Apr-June 1984, 574-583.

[2] S.W. Crowder, P.B. Griffin, J. D. Plummer, "Characterization of interface topography of the buried Si-SiO$_2$ interface in silicon-on-insulator material by atomic force microscopy", *Applied Physics Letters*, Vol. 65, 1994, 1698-1699.

[3] H. Fusstetter, A. Schnegg, D. Graf, H. Kirschner, M. Brohl, P. Wagner, "Impact of Chemomechanical Polishing On The Chemical Composition and Morphology of the Silicon Surface", *Material Research Society Symposium (MRS)*, 1995.

[4] P.O. Hahn, M. Grudner, A. Schnegg, H. Jacob, "Correlation of Surface Morphology and Chemical State of Si Surfaces To Electrical Properties", *Applied Surface Science*.

[5] I. Yang, Vieri, A. Chandraksan, D.A. Antoniadis, "Back-Gated CMOS on SOIAS For Dynamic Threshold Voltage Control", *IEEE Transactions On Electron Devices*, Vol. 44, No. 5, May 1997.

[6] T. Ouisse, S. Cristoloveanu, T. Elewa, H. Haddara, "Adaptation of the Charge Pumping Technique To Gated p-i-n Diodes Fabricated on Silicon on Insulator, *IEEE Transactions On Electron Devices*, Vol. 38, No. 6, June 1991, 1432-1443.

[7] J.P. Colinge, "Silicon-On-Insulator Technology: Materials to VLSI, Kluwer Academic Publishers, 1991, 45.

[8] S. Cristoloveanu, S. Li, "Electrical Characterization of Silicon-On-Insulator Materials and Devices", Kluwer Academic Publishers, 1995.

[9] S. Lee, S. Cristoloveanu, "Accurate technique for C-V measurements on SOI structures excluding parasitic capacitance effects", *IEEE Electron Device Letters*, Vol. EDL-7, p. 537, 1986.

[10] I. Yang, PhD Thesis, "Study of Sub-0.5μm SOI-with-Active-Substrate (SOIAS) Technology for Ultra-Low Power Applications", Massachusettes Institute of Technology, September 1996.

[11] G. Pfeiffer, S. Fetheroff, S.S. Iyer, "Final Polish For SOI Wafers- Surface Roughness and TTV Degradation", *Proceeding of 1995 IEEE International SOI Conference,* Oct. 1995, p. 172-173

[12] M. Miyahsita, T. Tusga, K. Makihara, T. Ohmi, "Dependence of Surface Microroughness of CZ, FZ, and EPI Wafers on Wet Chemical Processing"*Journal of the Electrochemical Society,* Vol139, No.8, August 1992, 2133-2142.

[13] Z. Liliental, O.L. Krivanek, S.M. Goodnick, C.W. Wilmesen, "Correlation of Si-SiO2 Interface Roughness With MOSFET Carrier Mobility"*Materials Research Symposium Proceedings,* 1985. 193-197.

[14] J.P. Gambino, T.N. Nguyen, B. Cunningham, J.F. Shepard, "Dielectric Breakdown of SiO_2 Grown on Rough Si Substrates" *The Physics and Chemistry of the SiO_2 and the Si-SiO_2 interface,* 1988, 445-452.

[15] A. Chan, C. Nguyen, P. Simon, T.H. Chan, S. Wong, "Polished TFT's: Surface Roughness Reduction and Its Correlation to Device Performance Improvement" *IEEE Transactions on Electron Devices,* March 1997, Vol44, Number 3, 455-463.

[16] C.Guilhalmenc, H.Moriceau, B. Aspar, A.J. Auberton-Herve, J.M. Lamure, "Characterization by atomic force microscopy of the SOI layer topography in low-dose SIMOX materials" *Materials Science and Engineering* B46 1997, 29-32

[17] G.J. Pietsch, Y.J. Chabal, G.S. Higashi, "The atomic-scale removal mechanism during chemo-mechanical polishing of Si(100) and Si(111)", *Surface Science* 395-401, 1995

[18] F. Sugimoto, H. Horie, Y. Arimota, T. "A pH Controlled Chemical Mechanical Polishing Method For Ultra-Thin Bonded SOI Wafer"*1993 Symposium on VLSI Technology. Digest of Technical Papers,* 113-114

[19] A. Gilicinshki, R. Rynders, S. Beck, Y. Strausser, J. Stets, B. Felker, D. Bohling, "Study of Silicon Surface Roughness by Atomic Force Microscopy" *Materials Research Society Symposium Proceedings* Vol. 324, 391-396

[20] Bjorkman et al. "Influence of Surface Roughness on the Electrical Properties of Si-SiO_2 interfaces and on second-harmonic generation at these interfaces" J. Vac. Sci. Technology B, July 1993, 1521-1527

[21] J.M. Grant, L.R. Allen, "Characterization of Rapid Thermally Grown Dielectrics by Surface Charge Analysis and Atomic Force Microscopy" *SPIE* Vol. 2091, 51-61

[22] H. Abe, F. Kiyosumi, "Studies of Breakdown and Defects in Thin SiO2 Thermally Grown on Si substrates" *Proceedings of the Fifth International Symposium on Silicon Materials Science and Technology: Semiconductor Silicon 1986,* 1011-21

[23] H.C. Lin, E.C. Kan, T. Yamanaka, C.R. Helms, "Modeling and Characterization of Si/SiO_2 Interface Roughness" *1997 Symposium on VLSI Technology Digest of Technical Papers.* 43-44.

[24] M.J. Sherony, Phd Thesis, Design, Process, and Reliability Considerations in Silicon-On-Insulator (SOI) MOSFETs, Massachusetts Institute of Technology, Feb 1998.

[25] E.H. Nicollian, J.R. Brews, MOS (Metal Oxide Semiconductor) Physics and Technology, John Wiley and Sons, New York, 1982.

[26] Azzam, Ellipsometry and Polarized Light, North-Holland Publishing Company, 1977.

[27] Henry Smith class notes, "Submicron-and Nanometer Structures Technology"

[28] Weisendanger, Roland. Scanning Probe Microscopy and Spectroscopy.

[29] IBM at Zurich WEb site: http://www.zurich.ibm.com/Technology/Atomic/atomic.force.html

[30] Advanced Surface Microscopy, Inc. http://www.a1.com/asm/afmpage.htm

[31] Department of Physics, Berekeley University. http://www.physics.berkeley.edu/data/www/research/.

[32] Schroder, Semiconductor Material and Device Characterization, John Wiley and Sons Inc. 1990.

[33] M.J Sherony, L.T. Su, J.E Chung, D.A. Antoniadis, "SOI MOSFET effective channel mobility", *IEEE Transactions on Electron Devices*, vol.41, no.2, Feb. 1994, p. 276-8,

[34] Y. Satoh, T. Shiota, Y. Murakami, T. Shingyouji, and H. Furuya, Journal of Applied Physics, 79 (10), May 1996, 7944-7948.

[35] T. Yamanaka, S. J. Fang, H. C. Lin, J. P. Snyder, C. R. Helms, "Correlation Between Inversion Layer Mobility and Surface Roughness Measured by AFM", *IEEE Electron Device Letters*, Vol. 17 No. 4, April 1996, 178-180.

[36] M. Kimura, J. Mitsuhashi, H. Koyama, Si/SiO_2 "Interface States and neutral oxide traps induced by surface microroughness", *Journal of Applied Physics*, 77 (4), February 1995, 1569-1575.

[37] S.C. Sun, J. D. Plummer, "Electron Mobility in Inversion and Accumulation Layers on Thermally Oxidized Silicon Surfaces", *IEEE Transactions on Electron Devices,* Vol. ED-27, NO. 8, August 1980.

Appendix A

MTL NMOS Process Flow For Material Characterization Devices

A.1 PROCESS TRAVELER-MSOIAS1

I) Brief Description:

6 MASK N-MOSFET PROCESS WITH PIN DIODES with lengths: 0.5-5 microns and widths: 1-50 microns.

II) Lot Owner: Hasan Nayfeh

III) Wafers For MSOIAS1: (14 wafers)

III-a) 7 SOIAS Wafers

Wafer	Intial Roughness (nm RMS)	Final Roughness (nm RMS)	Tsi (Angstroms)
2	2.518	.165	1467
3	2.016	.486	1505
6	.333	.250	2403 (1263 after thinning)
7	2.931	.196	1457
8	2.181	2.181	1531
9	2.561	2.561	1524
10	3.406	.156	1377

Table 1.1: SOIAS Wafers

III-b) 4 SIMOX Wafers

Wafer	Initial nm RMS	Final nm RMS	Tsi initial(Angstroms)	Tsi final(Angstroms)
3s	0.22	0.132	2413	2238

Table 1.2: SOI Wafers

4s	0.22	0.134	2410	2269
5s	0.224	0.224	2431	2431
6s	0.222	0.222	2419	2419

Table 1.2: SOI Wafers

III-c) 2 Bulk Wafers- 1b, 2b

Wafer Description:

- P-type Si <100>

- 0.169 nm rms

- 10-20 ohm-cm

III-d) 1 SIMOX Reject- a check of the consequences of pirahna and oxide thinning on surface roughness.

Wafer Description:

Wafer 8c: Tsi=1991 angstroms, after thinning: 1003 angstroms remaining

Surface Roughness=0.090 nm RMS

IV) MASKS TO BE USED:

1. CD active

2. CP Poly

3. CNN Source/Drain Implants

4. CNN Complement

5. CC Contact Cuts

6. CM Metal Pattern

File Name: ~/hnayfeh/kic/final.kic

V) Physical Parameters of Devices:

1. tox=55 angstroms

2. Na=4.71×10^{17}

VI) Processing Steps:

Process Step	Description /Comments
CMP on all Wafers	Touch Polish <0.2 nm RMS, 50 A/min except 8,9,5s,6s
Si thinning	Wafer6 &Wafer8c 1910 angstroms of oxide removal of 988 angstroms) were grown. 1000C, 20 min in Dry O_2 Measured dummy SIMOX wafer8c at 1000C, 21 min in Wet O_2 Materials lab, and found that 1019 angstroms 1000C, 20 min in Dry O_2 of Si was removed. Thickness of 6 is ~1263. 1975 angstroms of O2 grown.
Stress Relief Oxide	275 angstroms of Oxide grown. 950C, 35min in Dry O_2 950C, 30min in N_2 recipe 230 Tube A1 target: 22 nm
LPCVD Silicon Nitride	1450 angstroms grown. (800C, 2hr) recipe 410 Tube A5 target: 150 nm (1.5 kA)
Active Area Pattern	No alignment (Mask: MSOIAS1 CD) * Dump rinse wafers in DI water to remove EBR edge bead remover from back before doing nitride etch.
Nitride Plasma Etch	150-215 angstroms of oxide (SF$_6$, 40 sec) in field area (nanospec). *Run bulk first -- can't check if remaining nitride on soi wafers

P-Field Implant	3×10^{13}, Boron, 25keV
Pirahna in TRL (brown-green)	Needed since wafers were taken outside the ICL.
Pre-Metal in ICL	This step will remove the resist
Field Oxide	*recipe 114*
	Bulk: target SiO_2: 340 nm
	SOI: target SiO_2: 1/0.44 tsi plus 10% over-oxidation
Nitride Wet Etch	*15 sec BOE dip prior to nitride etch*
Stress Relief Oxide Wet Etch	dip until dewet in scribe lanes
Dummy Gate Oxide Growth	(45A)800° C, 30 minutes O_2 800° C, 15 min, N_2
	recipe 110
Enhancement Channel Implant	BF_2 25kev 9×10^{11}
Gate Oxidation	(45A) 800C, 30 min in Dry O_2
	800C, 15 min in N_2 recipe 110
	dummy gate oxide etched in 50:1 HF after RCA SC-1
LPCVD Polysilicon (3kA)	625 ^{o}C, 45 min rec 428 (3k poly) rec 419 (2k poly)
	target: 300 nm
Poly Gate Pattern	Mask: msoias1 CP
	Align to mask CD
Plasma Poly Etch (CCl4	** First do 1sec dip in BOE and*
	rinsed in DI water
Resist Ash	
Reoxidation	900 ^{o}C, 10 min dry O_2, 15 min in N_2 Tube B5 Tar
	get SiO_2: 70 angstroms

N+ Poly/S/D Pattern

Mask: MSOIAS1 CNN
align to mask CP

Poly and S/D Implant   Arsenic: 25kev,4e15

                                    0 degree implant

Resist Ash

P+ Poly/S/D Pattern   *Mask: MSOIAS1 CNN comp align to mask CP*

P+ S/D Implant BF_2: *25kev,4e15*

Resist Ash

Poly And S/D Diffusion *RTA*   *1000C, 20sec in N_2*

LTO Deposition (4kA) 400° C $SiH_4/N_2/O_2$, 45 secs

                                    target: SiO_2: 400 nm

Resist Coat   * *Hardbake -- abort normal develop recipe 20*

                                    * *Assign hardbake recipe 82 to track 2*

                                    * *Re-assign temp 130° C to back module 86 for back*

                                    side etch, hardbake at 130 ^{o} C, 60 secs

Backside LTO Wet Etch   * *Dip in BOE till backside dewets* Approximately*

                                    30 secs

Backside Poly Plasma Etch   (SF_6, 1min) * *rec 12 -- timed etch*

Backside Oxide Wet Etch   * *dip till dewets 5 sec*

Resist Ash

Contact Pattern   *Mask: MSOIAS1 CCalign to mask CP*

LTO Plasma Etch CF_4,*timed etch*

                                    * *etcher-2 rec. 24*

	* don't endpoint! figure out a timed etch to leave about 500A of LTO
LTO Wet Etch	*BOE dip until de-wet*
	(~ 10 secs.)
Resist Ash	
Metal Deposition	(1 μm, Al,1%Si)
	Clean in 3:1 H_2SO_4/H_2O_2 dip in buffered oxide etch (3 secs) prior to loading wafers, no sputter etch.
Metal Pattern	*Mask: MSOIAS CM*
	align to mask MSOIAS1 CC ** Need to HARDBAKE after developing* *dev track 2, program 43 -- need to reprogram bake module 86 for 150C*
Metal Plasma Etch	* etcher-3 rec 32
	BCl3 / Cl2/ CHCl3
Resist Ash	** di rinse -- **VERY IMPORTANT** --*
	*since metal etch with Cl_2 is **CORROSIVE***
Sinter Metal	*425 °C, 15 min in H_2+N_2* tube B8 *rec 710*

A.2 Processing and Fabrication

A.2.1 Facility

The devices for the project were fabricated at the Integrated Circuits Laboratory (ICL). It

is a class 10 clean room (less than 10 0.5 μm particles within 100 cubic feet) located in

MIT at the Microelectronics Technology Laboratory (MTL). The wafers used were seven

Silicon on Insulator with Active Substrate (SOIAS), two Silicon on Insulator (SOI), and

two bulk Silicon wafers. The process used was the conventional NMOS process. The pro-

cedure for this follows from the Twin Well CMOS Process by Tedrow and Sodini, but eliminating the steps related to PMOS fabrication. I will now describe the steps in the process.

A.2.2 Touch Polish & AFM Imaging of Morphology
First, wafers were touch polished using the CMP tool in the ICL. Splits were created with the variable differing being the time of polish. Before polishing, the morphology of each wafer was determined by use of Atomic Force Microscopy (AFM), so to have knowledge of the effect of CMP on morphology. After the touch polish, the wafers are then cleaned in an automated instrument in the CMP room to remove any remnant slurry. The clean, however, does not eliminate all the ionics such as alkalines and so forth, that are in abundance during the touch polish process. Therefore, in order for the wafers to be classified as being clean enough to enter the ICL, they must undergo a pirahna clean in the Technology Research Laboratory (TRL). The pirahna clean consists of 2 steps: 10 minute immersion in 3:1 H_2SO_4:H_2O_2 solution and a 15 second 7:1 BOE (buffered oxide etch) dip. This is all done in fluoroware dedicated to deal with ionics so as not to contaminate other users processes.

A.2.3 Thinning of Film Thickness
The wafers were then taken into the ICL, where the Si film thicknesses were reduced by growing oxide thermally and then etching it off using 7:1 BOE solution. The target for the thicknesses ranged from 1256-1346 angstroms. That called for a removal of ~1000 angstroms of silicon. To determine the amount of oxide necessary to grow to convert that amount into SiO_2, one utilizes the rule that for every angstrom of oxide grown, 0.44 angstroms of Si are removed. With this target of amount of oxide necessary to grow, supreme simulations were done to determine the time necessary for the oxide growth. 1900 angstroms of oxide were grown at 1000°C. Since this oxide is only a means of silicon removal, we do not care much about the quality of it, so wet oxide was grown, but dry thin

oxide films sandwiched the wet so that the actual silicon surface was in contact with the higher quality dry oxide.

A.2.4 Defining Active Regions

The next step of the fabrication was to prepare for defining the active regions. The approach taken was to pattern Silicon Nitride (Si_3N_4). The problem with this is that Si_3N_4 is severely lattice mismatched with Si. Deposition of a silicon nitride film on Si would cause a great deal of stress. To counter this, we grow a stress relief oxide first of thickness ~22 nm. The silicon nitride is then grown using Low Pressure Chemical Vapor Deposition (LPCVD). The thickness is ~150 nm.

A.2.5 Lithography

The wafer then undergoes a lithography step to define the active area. This is done using a direct step-on-wafer GCA-4800 10X stepper located in the ICL. The radiation used is g-line UV radiation of wavelength ~260-330 nm. The steps in the lithography are first:

1. HMDS- this ensures photoresist adhesion. This is done by placing the wafers in an oven at 150° C. It uses nitrogen gas to drive off water vapor and uses hexamethyldisilizane to prepare the surface for resist coat.

2. Coat- ~1 μ m of photoresist on the wafer. Wafer moves on to the coater where a fixed volume of photoresist is dispensed onto the wafer. A puddle is put on the wafer and is then accelerated to high speeds to attain a target resist thickness of 1.15 μ m. The goal is to achieve a uniform, striation-free coat that is close to this target thickness. A bake follows the coat process to remove a percentage of solvents that cast the photoresist.

3. Pilot Wafer- A focus expo wafer is used to determine the best time and focus parameters.

4. Expose- The wafer is aligned and exposed. The 1:1 contact aligners view the wafer

target through the mask target and the wafer and mask can move independently. The 10:1 wafer steppers align the mask to the machine, then align the wafer target to the machine target by joystick movement of the stage and viewed on a tv monitor. Exposure energy comes from a mercury (Hg) lamp. An electronic shutter controls the energy dose. Visual inspection of a pilot wafer sets the dose. The mask features are then transferred to the resist by blocking the UV light.

5. Develop- Exposed resist is removed to complete pattern transfer from the mask.

6. Inspection- Visually inspect the mask using an optical microscope. Microscope inspection is done to fix focus and exposure parameters on pilot wafers and to scan the lots following the develop process.

A.2.6 Etch for final active region definition

After defining the active areas by patterning the resist, the nitride that is exposed is then removed by a plasma etch using SF_6 chemistry. Recipe 15 was used to perform the etch. The recipe goes as follows:

Table 1.1: SF_6 Nitride Etch

Pressure	Step #1 500 mtorr	Step #2 500 mtorr	Step #3 375 mtorr	Step #4 375 mtorr	Step #5 375 mtorr
RF top	0 Watts	300 Watts	0 Watts	250 Watts	100 Watts
Gap	1.5 cm	1.5 cm	1.0 cm	1.0 cm	1.35 cm
CCl_4	0 sccm	0 sccm	0 sccm	0 sccm	0 sccm
Oxygen	200 sccm	200 sccm	0 sccm	0 sccm	0 sccm
Helium	100 sccm	100 sccm	20 sccm	20 sccm	20 sccm
Cl_2	0 sccm	0 sccm	0 sccm	0 sccm	0 sccm
SF_6	0 sccm	0 sccm	50 sccm	50 sccm	60 sccm

The etch rate is ~2071 A/sec.

Next, we perform a p-field implant. The reason for this is to make the threshold voltage of the field area very large so the parasitic transistor will not turn on, and result in extra field leakage current. The implant was done in Implant Sciences. The material used to implant was Boron. The conditions were dose of $3x10^{13}$ ions/cm^2 and an energy of 25 keV.

Since the wafers were taken out of the ICL, in order for them to be classified as being clean enough, they had to undergo a pirahna clean as described above. It should be noted that the pirahna clean removes the resist on the wafer, so those areas after the pirahna have nitride over them.

A.2.7 Formation of Field Area
The next step was growth of the field oxide. For the SOI based wafers, the goal was to consume the entire silicon thin film. This was done by calculating the amount of oxide necessary to consume the thickest film. These parameters were then used for all the SOI based wafers. The bulk wafers had a standard growth of 340 nm of oxide. Next, the nitride is etched away in a wet etch. It is a timed etch. There is ~1450 angstroms of nitride. The wafers were in the transene solution for ~40 minutes giving an etch rate of ~36.25 angstroms/minute.

Next the stress relief oxide is etched away. There is ~270 angstroms. BOE etch rate is 250 angstroms for 15 seconds. The sign that the SRO is gone is that we get beading over the active areas. Dipped for 15 seconds and noticed beading. I then put it in for an additional 5 secs for security. That gives a total of 20 secs, ~ 333 angstroms of oxide removed. Total BOE time is 20+15=35 (15 secs when we started) to give Fox removal of ~585 angstroms. I have larger than 3000 angstroms of Fox to start with so it is a safe etch.

A.2.8 Gate Definition

We then prepare for the gate oxidation, and the channel implant by growing a dummy gate oxide. An important consideration in the science of implanting is the phenomena called channeling. It involves ions traveling along specific crystallographic directions. This can occur if the substrate is a single crystal. If ions are able to channel, then energy loss due to nuclear stopping is negligible or zero, so the ions travel much farther than they are supposed to. To counter this, we grow a very thin oxide on the wafer before we implant. Since oxide is amorphous, there is no preferred direction of travel, so channeling is prevented. Another advantage of growing a thin oxide before growing the gate oxide is that this oxide acts as a sacrificial oxide, and it has been shown that growing a thin oxide and then etching it away and then growing the actual gate oxide gives a much better Si-SiO_2 interface, so that the oxide integrity is better- the oxide breakdown voltage is larger.

A.2.9 Channel Implant

We then were ready to perform the channel implant so that we can give the transistors a certain threshold voltage. The goal of this project is to study the back interface of the Separation by Implantation by Oxidation (SIMOX) wafer which turns out to be the front interface of the SOIAS wafer. So, we do not want any effects from the back interface that would perturb our results. Therefore, we want to ensure that the transistors are partially depleted. To do that, we use the constraint that the maximum depletion width be equal to approximately half the silicon film thickness. The worst case to examine is the thinnest film wafer. The thinnest one has a thickness of 1248 angstroms after the SRO growth. In order for the project to most closely follow industry, we decided to make our gate oxide thickness 50 angstroms. This thin thickness is best to study since the current drive in industry is to utilize very thin films. So, the dummy and gate oxide amount to 100 angstroms. The reoxidation that is planned ahead is 70 angstroms, so the total is 170 ang-

stroms. That translates into 75 (170x0.44) angstroms of silicon removed. Subtracting that from the thinnest film thickness gives- 1173 angstroms. So, a reasonable number for the maximum depletion width is ~500 angstroms.

We need to determine the doping level that will give this value for the maximum depletion width. The depletion width is given by:

$$W = \sqrt{\frac{-2\varepsilon_s \phi_s}{eN_a}}$$ (1.1)

The maximum depletion width is achieved when the transistor is in the onset of inversion. This is the case when $\phi_s = -2|\phi_f|$. Giving the maximum depletion width:

$$W_{max} = \sqrt{\frac{4\varepsilon_s |\phi_f|}{eN_a}}$$ (1.2)

where

$$\phi_f = \frac{k_b T}{e} \ln\left(\frac{N_a}{n_i}\right)$$ (1.3)

n_i is the intrinsic carrier density for silicon. We now solve the equation above for $W_{max} = 500A$ and get $N_a = 4.71 \times 10^{17}$.

We can now calculate what the threshold voltage for this is from:

$$V_T = V_{FB} + 2|\phi_f| + \frac{\sqrt{2\varepsilon_s eN_a |2\phi_p|}}{C_{ox}}$$ (1.4)

(1.5)

where $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ and $V_{FB} = \phi_{poly} - \phi_{bulkSi}$. For our case, the poly is doped very heavily, so we may assume that the fermi level in the poly is at the conduction band-

edge. Setting the valence band edge to zero, $\phi_{poly} = \dfrac{E_g}{2}$ where E_g is the bandgap of

Si, 1.1 eV. Using the equation for ϕ_F we get that $\phi_{bulkSi} = -0.45eV$ so that

$V_{FB} = -1\,Volt$. From knowledge that the oxide thickness $t_{ox} = 50A$, we calculate

that $V_T = 0.4467\,Volts$

Next, supreme simulations were performed in order to determine the dose necessary to achieve the required doping level. This was done by including all the heat cycles that the wafer undergoes during furnace operations. The dopant material was Boron di-fluoride BF_2. The energy was 25 keV and the dose was 7.75×10^{12} ions/cm^2 at an angle of 7°. The implant was performed at implant sciences.The supreme program is given in Appendix A.

We then perform the usual pirahna clean in the TRL so that the wafers can reenter the ICL. The dummy gate oxide was then etched, and the gate oxide was grown. Before this step, an RCA clean was performed on the wafers which consisted of 10 minutes in SC1, 15 sec HF dip (this removes the dummy gate oxide) and 15 minutes in SC2. (SC1 is 5:1:1 DI:NH$_4$OH:H$_2$O$_2$ and SC2 is 5:1:1 DI:HCL:H$_2$O$_2$). The growth recipe used was 35 minutes at 800° C. The species was dry oxygen. In order to determine the correct parameters for the growth, we had to first characterize the growth in the tube by running some dummy wafers. Using supreme simulation, we predict that to grow 50 angstroms of SiO$_2$, we need to perform 30 minutes in dry O$_2$ at 800° C. However, ellipsometry measurements showed that the thickness grown was 47 angstroms. So, in the real run I used a time of 32 minutes. Table 7.2 below outlines the usual furnace growth recipe:

Table 1.2: Oxidation Furnace Schedule

Interval	Description	Temperature (celsius)	Time (minutes)	Gas
1	Push-In	800	20	N_2(high)
2	Stabilization	800	10	N_2(high)
3	Ramp-Up	800-T	10/min	N_2(low)
4	Stabilization	T	10	N_2(low)
5	Oxidation	T	t_1	Gas
n	More Oxidation	T	t_2	Gas
n+1	Anneal	T	t_3	N_2
n+2	Ramp-down	T-800	2.5/min	N_2(low)
n+3	Pull-out	800	20	N_2(high)

We then grow the polysilicon using Low Pressure Chemical Vapor Deposition (LPCVD). The target thickness was 2000 angstroms of polysilicon. The polysilicon is then patterned to define the gates using a lithography step. The remaining polysilicon is then etched using plasma etching. The tool used was the AME5000. The etch is a timed etch, so several dummies were ran in order to determine 1) an etch rate, and 2) a delay time for the plasma to form. Two points were taken, and a linear model was created. The fast etch rate was determined to be 111.1 a/sec with a 24 sec delay and the slow etch rate was 24.56 A/s with a 3.47 second delay. Test experiments were performed finding that the

rates were off. The actual recipe used to remove 2200 angstroms was 18.6 secs fast and 53.8 secs slow. Table 7.3 shows the recipe for etching polysilicon:

Table 1.3: CCl₄ Poly Si etch

Pressure	Step1 500 mTorr	Step2 200 mTorr	Step3 200 mTorr	Step4 200 mTorr	Step5 200 mTorr
RF top	0 Watts	300 Watts	0 Watts	300 Watts	200 Watts
Gap	1.5 cm	1.5 cm	1.5 cm	1.5 cm	1.5 cm
CCl₄	0 sccm	0 sccm	130 sccm	130 sccm	130 sccm
Oxygen	200 sccm	200 sccm	20 sccm	20 sccm	20 sccm
Helium	100 sccm	100 sccm	70 sccm	70 sccm	130 sccm
Cl₂	0 sccm	0 sccm	0 sccm	0 sccm	0 sccm
SF₆	0 sccm	0 sccm	0 sccm	0 sccm	0 sccm

How Plasma Etch Works:

Etching occurs by a chemical reaction between the substrate and the atoms or radicals produced in the plasma. The advantage of using gas phase material to etch compared to liquid is that one can make the plasma etch anistropic if you add ion bombardment to the substrate.

Etching requires three steps:

1. Chemisorption: A gas in the form of a molecule or radical is adsorbed (sticks) on the surface and forms a chemical bond.

2. Rearrangement: Atoms on the surface rearrange to form a product molecule.

3. Desorption: The product molecule desorbs.

In the experiment using the AME5000, we use CCl_4 as our etching gas. The plasma produces Cl_2 molecules that can etch silicon with the product being $SiCl_4$. For our case the poly-si rests on top of a oxide layer so the selectivity is very important so our gate oxide

will be protected. The selectivity has been measured to be about 40:1. The reason is that the reaction SiO_2 ->$SiCl_4$ is thermodynamically unfavorable- the Gibbs Free energy is greater than zero $\Delta G > 0$.

A.2.10 Source Drain Regions
After that, we grow a reoxidation. The purpose of it is to prevent the source/drain and polysilicon doped implant from channeling. Approximately 70 angstroms of oxide are grown. Before that, an RCA clean was performed, but the standard HF dip for 15 seconds was not performed in order to protect the remaining gate oxide. The reoxidation was done for 5 minutes dry O_2 at 900°C and was followed by a 15 min N_2 anneal at 900°C.

We then perform a lithography step in order to block off certain regions of sources and drains. For regular NMOS transistors, the source and drains are left open, but p-i-n diodes had to have the source blocked off so that it can act as the "substrate" in a bulk situation. This step is a non-self aligned process. Mask CNN was used to perform this step. Misalignment can result in p-i-n diodes not operating correctly. There are two scenarios for the blocking off of the n^+ implant. One is that we don't block off then entire source region. We would then create an nmos transistor instead of a p-i-n. The P^+ will not be able to contact the channel, so the carriers that are trapped will not be pumped. The other scenario is that we block off everything, but we also block off part of the gate. That would result in regions of the gate not being doped. This is not perfect, but the rapid thermal anneal might be able to distribute the doping so we might be safe. So, the first case is the one that is most dangerous. The second case will result in devices not working if we completely cover the gate. That is why I expect the shorter channel p-i-n diodes to not work.

The n+ implant was then performed. The species is Arsenic, As, at an energy of 25 keV, and a dose of 4×10^{15} ions/cm^2 at 0 degrees.

The wafers were then pirahna cleaned without performing the standard HF dip in the TRL, so that they could enter the ICL.

Now, the complement of the CNN mask was applied in order to prepare for the P^+ implant. So, all devices were covered, and the p-i-n diodes were covered in regions that received the n+ implant. The misalignment issue here is that if we are not completely covering, then we will have a n-type region as a buffer to the channel so that when we need to pump, the holes will have to travel through this region so great care has to be taken to make sure this region is as small as possible. One way we can destroy the devices is not to cover the entire gate. That would counter-dope the n^+ doping of the poly, and the transistors will not work as we want.

The P^+ implant was then performed at implant sciences. The species was BF_2 at an energy of 25 keV, and a dose of 4×10^{15} ions/cm^2.

The wafers then where pirahna cleaned in TRL, so that they could get back into the ICL. Next, a rapid thermal anneal was performed so that the polysilicon and source/drain diffusions would spread out uniformly. It was done at 1000°C for 20 secs under N_2 gas.

A.2.11 Final Steps

Next, we deposited LTO (low thermal oxide) all over the wafer. It consists of the gases: $SiH_4/N_2/O_2$. Approximately 400 nm were deposited.

We now begin the phase of cleaning out the backend. The entire top is covered by resist. We then etch away the LTO on the backside using a wet etch in BOE. After that, the polysilicon is etched away using SF_6. The oxide is then etched away in a wet etch. We then remove the resist from the top, and get back to processing.

We now prepare for the contact cuts. A lithography step is done in order to define the cuts. Mask CC is used, and we align to mask CP. Exposed regions then have their LTO

etched away in a plasma etch using CF_4. The plasma produces two radicals- Fluorine and $CF3^+$ in the following ionization reaction:

$CF_4+e^- -> F+CF_3^+ +2e^-$
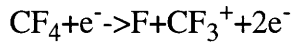
The CF_3^+ radical etches the oxide in the following reaction:

$SiO_2+CF_3^+ -> SiF_m+CO/CO_2$
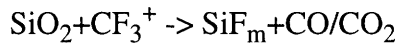
One problem is that atomic fluorine etches silicon:

$Si+4F->SiF_4$
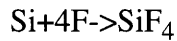
This shows that selectivity is an important issue. We perform the etch such that there is a remaining 500A of LTO remaining on the wafer. This is done since we do not want the plasma to attack the silicon wafer. It can result in damage to the morphology, a wet chemistry is needed. Next, we remove the leftover LTO using a wet etch (BOE). We then deposit the metal. It is $1\mu m$ of Aluminum with 1% silicon. The metal is then patterned using mask CM. We align to Mask CC (mask used to define the contact cuts). The aluminum is etched away using plasma, but using chlorides instead of fluorocarbons because of selectivity.

When aluminum is exposed to air a thin layer of about 30 angstroms of aluminum oxide grows at room temperature. This oxide is resistant to many chemicals, so it must be removed before we can start etching away the aluminum. The chloride CCl_4 will etch both the native oxide and the aluminum:

$2Al_2O_3+3CCl_4->4AlCl_3+CO_2$
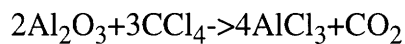
Free electrons in the plasma collide with the etchant gas to produce the radicals needed:

$CCl_4+e->Cl+CCl_3+2e$

$BCl_3+e->Cl+BCl_2+2e$
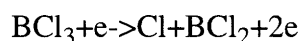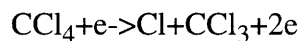
In both cases, atomic chlorine Cl etches the metal. The lifetime of the chlorine is very small, so, the wafer has to be in contact with the discharge, unlike etching of the LTO, where we use a barrel reactor. The resist is then removed, and the metal is then sintered.

A.3 Supreme Program Calculation of Dose and Energy of Vt Implant

TITLE   N-Channel and Backgate Implant S B2a_implant.inpimulation

$ base structure (1000 A Box and 600 A Si)

INITIALIZE SILICON <100> THICKNESS=1 DX=0.1 MIN.DX=0.001 XDX=0.01

+ BORON CONCENTR=1.0e15

VOL.RATION SILICON /OXIDE RATIO=0.5

$SILICON OEDK.0=0 OEDK.E=0 OED.RATE=0

$ Back oxide (Approximately 9000A)

DIFFUSION TEMPERAT=950 TIME=100 DTMIN=0.005 DTMAX=5.0 WETO2

DIFFUSION TEMPERAT=950 TIME=30 DTMIN=0.005 DTMAX=5.0 DRYO2

print layer

GRID   LAYER.2 DX=0.02 MIN.DX=0.0001 XDX=0.1 SPACES=30

$ Intrinsic Backgate Poly

DEPOSITION POLYSILI TEMPERAT=590 PRESSURE=1.0 THICKNES=0.25
DX=0.005

+ MIN.DX=0.00001 XDX=0.125 BORON CONCENTR=1.0e15 SPACES=100

$ Backgate oxide

DEPOSITION OXIDE THICKNES=0.1 DX=0.003 MIN.DX=0.0001 XDX=0.05
SPACES=70

$ Silicon Film

DEPOSITION THICKNES=0.140 SILICON <100> DX=.001 MIN.DX=0.00001 XDX=0.05

+ BORON CONCENTR=1.0e15 SPACES=200

$Wafer Bonding Anneal

DIFFUSION TEMPERAT=1000 TIME=60 NITROGEN

$Print Material Coefficients

$PRINT MATERIAL SILICON POLYSILI IMPURITY BORON OXIDATIO

$ Boron channel and backgate implant

$IMPLANT   BORON PEARSON DOSE=1.35e15 ENERGY=130

PRINT CONCENTR ACTIVE NET FILENAME=a.dat XMIN=0.0 XMAX=0.63

+COLUMNS=29 LINES/PAG=10000

$PRINT   LAYERS LINES/PAG=2000 COLUMNS=80

$PLOT   ACTIVE NET XMIN=0.0 XMAX=0.47

$PRINT   CONCENTR ACTIVE NET XMIN=0.0 XMAX=0.47

$+ FILENAME=B2_implant.sup LINES/PAG=2000 COLUMNS=80

$Stress Relief Oxide

DIFFUSION TEMPERAT=800 TIME=25 NITROGEN

DIFFUSION TEMPERAT=950 TIME=10 NITROGEN

DIFFUSION   TEMPERAT=950   TIME=185   DTMINXS=0.0001   DTMAX=5.0 DRYO2

$GRID LAYER.6 DX=0.001 MIN.DX=0.0001 XDX=0.015 SPACES=120

DIFFUSION TEMPERAT=950 TIME=30 NITROGEN

DIFFUSION TEMPERAT=800 TIME=60 NITROGEN

COMMENT PRINT LAYERS

$Nitride Deposition

DIFFUSION TEMPERAT=800 TIME=97 NITROGEN

$Field Oxidation

DIFFUSION TEMPERAT=800 TIME=10 NITROGEN

DIFFUSION TEMPERAT=950 TIME=130 NITROGEN

DIFFUSION TEMPERAT=800 TIME=70 NITROGEN

$Stress Relief Oxide Etch

ETCH   OXIDE ALL

$Dummy Gate Oxide Growth

GRID LAYER.5 DX=0.0008 MIN.DX=0.00001 XDX=0.04 SPACES=100

DIFFUSION TEMPERAT=800 TIME=30 DRYO2

DIFFUSION TEMPERAT=800 TIME=20 NITROGEN

$GRID LAYER.6 DX=0.0003 MIN.DX=0.00001 XDX=0.003 SPACES=30

IMPLANT BF2 PEARSON DOSE=7.75e12 ENERGY=25

ETCH OXIDE ALL

PRINT CONCENTR ACTIVE NET FILENAME=b2.dat XMIN=0.0 XMAX=0.25

+COLUMNS=29 LINES/PAG=10000

PLOT ACTIVE NET XMIN=0.0 XMAX=0.5

$ Front gate oxide

GRID LAYER.5 DX=0.0008 MIN.DX=0.00001 XDX=0.04 SPACES=100

DIFFUSION TEMPERAT=800 TIME=10 NITROGEN

DIFFUSION TEMPERAT=900 TIME=20 NITROGEN

DIFFUSION TEMPERAT=900 TIME=17 DTMIN=0.0001 DTMAX=5.0 DRYO2

$GRID LAYER.6 DX=0.0003 MIN.DX=0.0001 XDX=0.003 SPACES=50

DIFFUSION TEMPERAT=900 TIME=15 NITROGEN

DIFFUSION TEMPERAT=800 TIME=40 NITROGEN

COMMENT PRINT LAYERS

$Poly Gate Deposition

$DEPOSITION POLYSILI TEMPERAT=625 PRESSURE=1.0 THICKNES=0.3

$Reox

DIFFUSION TEMPERAT=800 TIME=30 NITROGEN

DIFFUSION TEMPERAT=800 TIME=25 NITROGEN

$PRINT LAYERS

$Gate and S/D Implant Anneal

DIFFUSION TEMPERAT=1000 TIME=0.167 NITROGEN

$Cobalt Silicidation

DIFFUSION TEMPERAT=750 TIME=10 NITROGEN

$Etch Reox

$ETCH   OXIDE ALL

$Remove Gate Poly

$ETCH   POLYSILI ALL

$Remove Gate Oxide

ETCH   OXIDE ALL

$PRINT   LAYERS FILENAME=B2.out LINES/PAG=2000 COLUMNS=80

$PLOT   ACTIVE NET XMIN=0.0 XMAX=0.47

PRINT LAYERS

PRINT CONCENTR ACTIVE NET FILENAME=c.dat XMIN=0.0 XMAX=0.25

+COLUMNS=29 LINES/PAG=10000

$PRINT MINIMOS File=B2a_implantf.sav XMIN=0.0 XMAX=0.06

savefilefilename=nmos1000-400 all

print concentration net chemical xmin=0 xmax=.1035, LINES/PA=1000

+file=film.out

STOP   End of Suprem3 file

A.4 TMAH Etch For Silicon Substrate Removal

Laboratory: Prof. Marty Schmidt's Lab on the 5th floor (chemical hood)
Objective:
We will be etching the silicon substrates using TMAH (Tetramethyl Ammonium Hydroxide). The buried oxide of the SIMOX will be used as an etch stop. In addition, we will be removing the buried oxide of the original SIMOX wafer using a 7:1 BOE (Buffered Oxide Etch) solution. We will be using our own fluroware for this experiment.
Procedure:

1. **Native oxide Removal:** 50:1 H_2O:HF dip for ~2 minutes

2. **Silicon substrate removal (60 microns):** 25% wt. TMAH etch for 2 hours, 35 minutes @ 80° C (etch rate~ 23 microns/hour).

3. **Expose Silicon inclusions:** 50:1 H_2O:HF dip for 45 seconds

4. **Dissolve Silicon inclusions:** 25% wt. TMAH etch for 45 seconds @ 80^oC.

5. **SIMOX oxide removal:** 7:1 BOE dip for ~ 2 minutes.

A.5 AFM Operation

The AFM used was a Digital Instruments Nanoscope III Scanned Probe Microscope. Images were taken at the Nanostructures Laboratory (NSL), and the Central for Material Science Engineering (CMSE).

The instrument offers the following:

1. Contact mode and tapping mode AFM operation with variations (MFM, EFM,LFM, under fluid, etc.)

2. Phase imaging/surface potential imaging capability, plus signal access module for customized applications

3. Scanning tunneling (STM) mode operation

4. Dimension 3000 microscope (118 micron x 118 micron x 6 micron nominal maximum scan range, vacuum chuck for up to 8" wafer size, mechanized stage)

5. Small atomic-resolution-optimized AFM and STM microscopes as well

6. Optical microscope with color video monitor for analysis area selection

7. Digital image processing and analysis software, automatic tip approach

The following are the steps for operating the AFM:

Preparation of sample: The sample should be flat, level and dust free. The sample is then placed on the platen whereby a vacuum pump holds the sample down.

Aligning Laser and Photodiode Mirror: The laser is aligned so that it is on the tip of the cantilever and centered. The photodiode mirror is then aligned so that the laser spot give a sum of ~ 2 volts.

Tuning the Cantilever: The auto tune routine is used to find the dominant peak in the frequency response curve (natural resonance frequency). It displays a short frequency

range with the peak at the center. The software adjusts the drive amplitude so that the RMS voltage response of the cantilever is 3 volts which is the setpoint voltage. We operate the cantilever at a frequency slightly lower than the resonant frequency. This is done by shifting it ~4 kHz lower.

Positioning Sample Before Engaging: We first spiral the piezo tube near the surface. The tip is then focused with respect to the optical microscope. We then position the cantilever so that the tip is in focus.

Engaging the microscope: The entire system is then covered by an acoustic hood to prevent interference of acoustic vibrations. We then engage by having the motor move the SPM head within 200 μm of the surface. After that, the motor steps the SPM head down toward the surface in micron-sized steps until the RMS amplitude is damped such that the SPM recongizes it as a true engagement. It knows when to stop going down by having a setpoint voltage where the piezo begins scanning.

Optimizing Feedback Parameters: The user defines a box of certain length and width that will be scanned. The cantilever is then raster scanned. The fast axis is the trace and this path is repeated with a retrace. The slow scan axis allows one to move in the other direction so that a new line can be scanned. Ideally, the trace and retrace should be the same. If not, the main control parameters need to be adjusted so that they are. The parameters that can be changed are: scan rate, integral and proportional gains, and setpoint. It is best for the force on the sample to be as small as possible, so the setpoint should be decreased as a last resort. The rougher the sample and/or the larger the area being scanned, the slower the scan rate should be.

A.6 CMP Recipe
Equipment & Chemistry
Machine: Strausbaugh (Precision Free Wafer Polishmaster 6EC (226135))

Slurry: RODEL's ADVANSIL 2000 (*See Below)

Pad: Rodel's UR-100

Recipe

1) Down Force: 3 PSI

2) Quill Speed: 60 RPM

3) Table Speed: 60 RPM

4) Slurry: 193 mL/min

5) Pad Temperature: 36 Celsius

6) Back Pressure: 0 PSI

Etch Rate

20:1 diluted slurry (20 Deionized Water to 1 slurry)-> Rate: 200 Angstroms/minute

*Specifications of Slurry:

Particulate Size: 160 nm.

PH: 10.0

Sodium: < 1ppm (part per million)

Contaminants: Cu-> 50 ppb, Cr-> 40 ppb, Ni-> 80 ppb, Fe-> 200 ppb (parts per billion)

Experiment touch polish SIMOX reject wafers:

Name: Hasan Nayfeh, Tom Tackacs

Topic: CMP Experiment

Lab: ICL (Integrated Circuits Laboratory- CMP Room)

Title: Touch Polish of 4 SIMOX dummy wafers

Date: August 11, 1997

Equipment:

Strausbaugh Polish Master

Rodel's UR100 Pad

Rodel's Advancil 2000-> 20:1 diluted (D.I:slurry)

4 SIMOX wafers:

  -wafer 4c: 0.548 nm RMS, tsi=1921 angstroms

  -wafer 5c: 0.628 nm RMS, tsi=1952 angstroms

-wafer 7c: 0.733 nm RMS, tsi=1921 angstroms

-wafer 8c: 0.595 nm RMS, tsi=2260 angstroms

Procedure:

Down Force: 3PSI

Quill Speed: 60 RPM

Table Speed: 60 RPM

Slurry: 193 ml/min

Pad temp: 36 celsius

Back Pressure: 0 PSI

wafer4c-> 1 min @ conditions above

wafer5c-> 2 min @ conditions above

wafer7c-> 4 min @ conditions above

wafer8c-> 4 min @ conditions above

Expected: 200 Angstroms/minute removal rate, < 0.1 nm RMS roughness.

Touch Polish of SOIAS Wafers

Name: Hasan Nayfeh, Tom Tackacs

Topic: CMP Experiment

Lab: ICL (Integrated Circuits Laboratory- CMP Room)

Title: Touch Polish of 6 SOIAS wafers, and 2 prime SIMOX wafers

Date: August 18, 1997

Equipment:

Strausbaugh Polish Master

Rodel's UR100 Pad

Rodel's Advancil 2000-> 20:1 diluted (D.I:slurry)

8 SOIAS wafers:

-wafer 2: 2.518 nm RMS

-wafer 3: 2.016 nm RMS

-wafer 4: 3.962 nm RMS

-wafer 6: 0.333 nm RMS

-wafer 7: 2.931 nm RMS

-wafer 8: 2.181 nm RMS

-wafer 9: 2.561 nm RMS

-wafer 10: 3.406 nm RMS

4 Good SIMOX wafers Surface roughness~ 0.7 nm RMS

-wafer 3s: tsi=2413, tox=2034 Run 3590

-wafer 4s: tsi=2410, tox=2053 Run 3590

-wafer 5s: tsi=2431, tox=2036 Run 3591

-wafer 6s: tsi=2419. tox=2059 Run 3591

Procedure:

Down Force: 3PSI

Quill Speed: 60 RPM

Table Speed: 60 RPM

Slurry: 193 ml/min

Pad temp: 36 celsius

Back Pressure: 0 PSI

8&9->   NO CMP

3&6->   1 min @ conditions above

2&7->   2 min @ conditions above

4&10-> 4 min @ conditions above

3s&4s-> 4 min @ conditions above

5s&6s-> NO CMP

Expected: 50Angstroms/minute removal rate, < 0.1 nm RMS roughness

Appendix B

Electrical Measurements

B.1 IV Curves
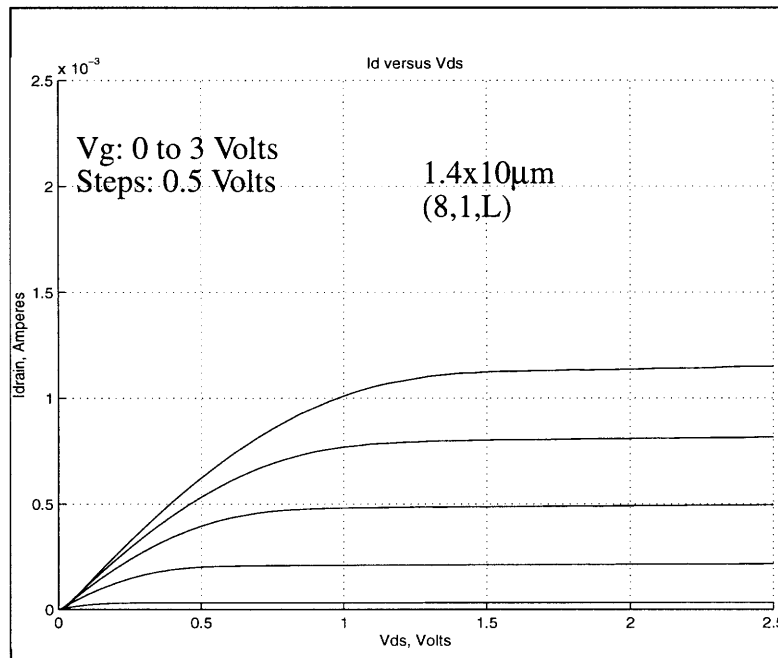
Figure 2.1: BULK IV
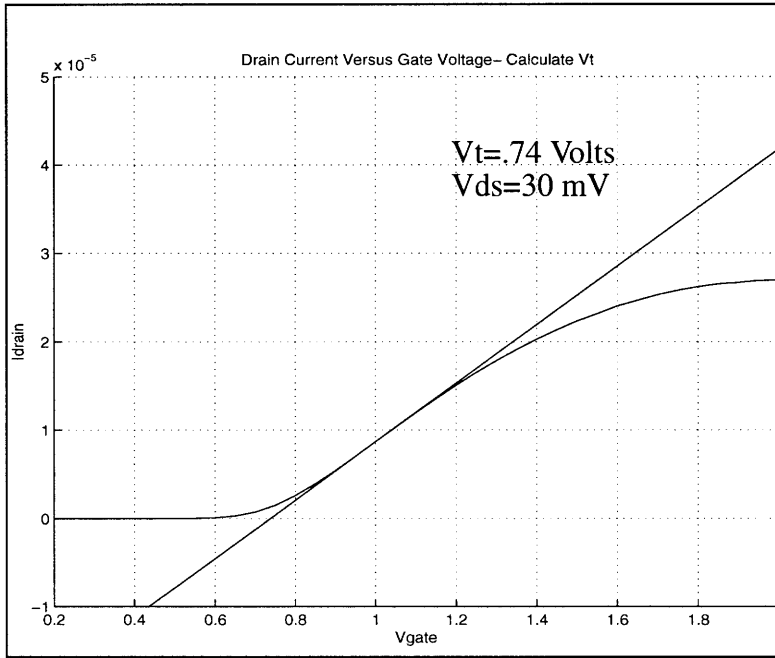
Figure 2.2: BULK Vt calculation
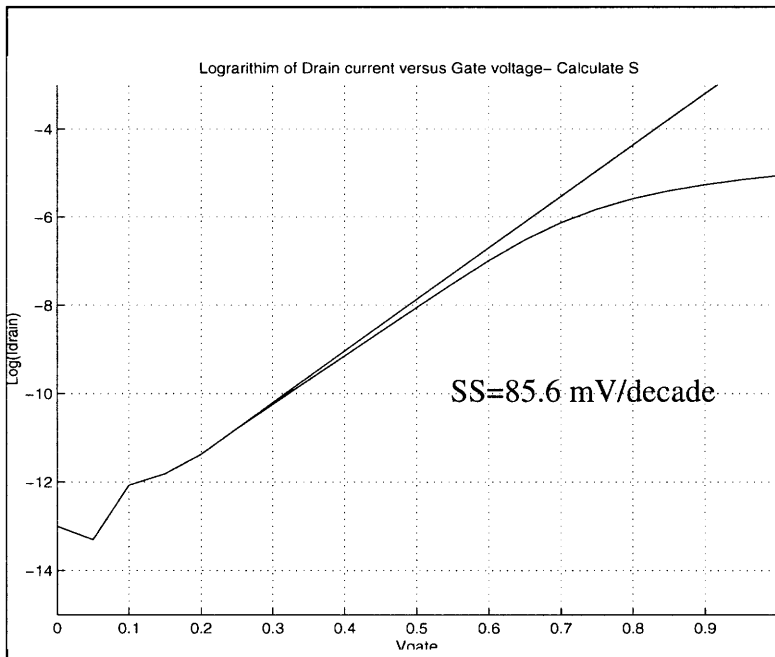
Figure 2.3: BULK2 SS Calculation

116

Id versus Vds

$\times 10^{-3}$

1.4x10μm
(8,2,L)
Vg-> 0 to 3 Volts
in steps of 0.5 Volts

Vds, Volts

Figure 2.4: IV SOI3S

Drain Current Versus Gate Voltage- Calculate Vt

$\times 10^{-5}$

Vt=0.341 Volts
Vds=30 mV

Idrain

Vgate
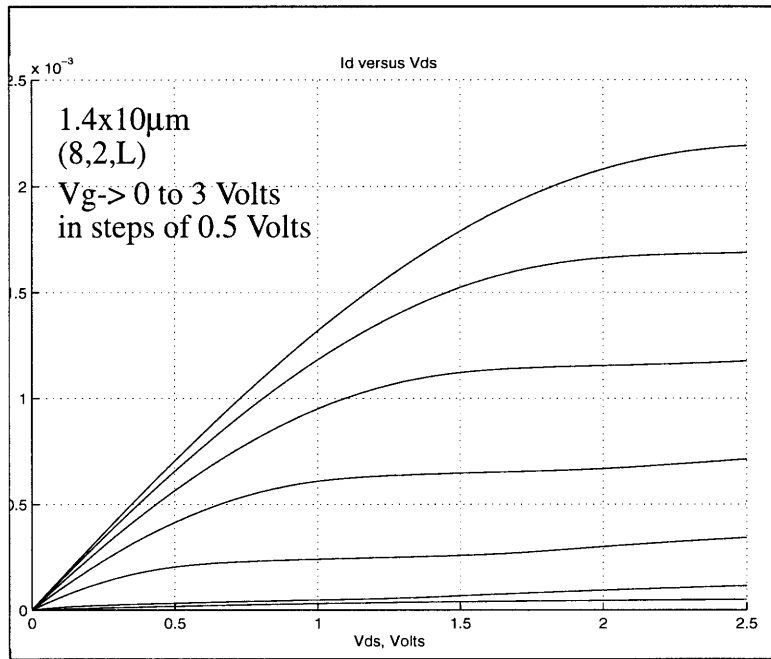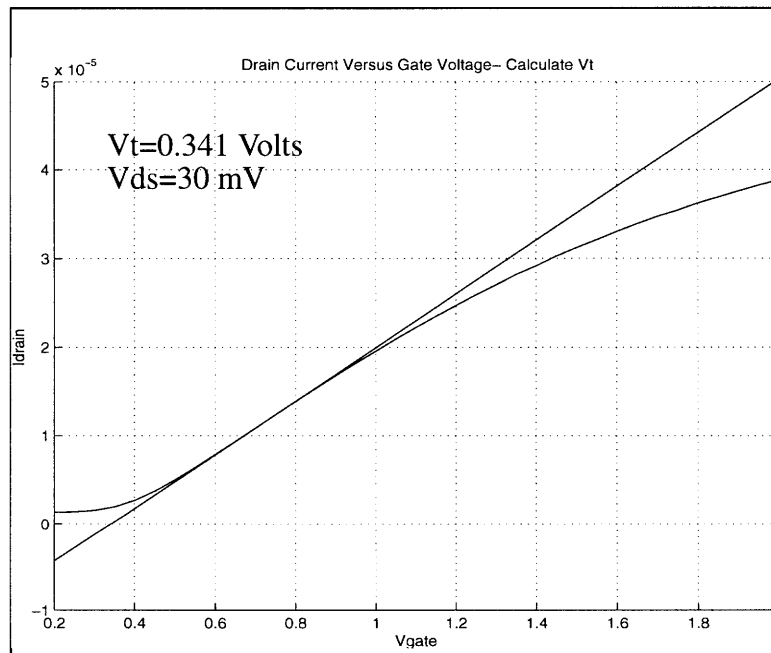
Figure 2.5: SOI3S Vt Calculation

117
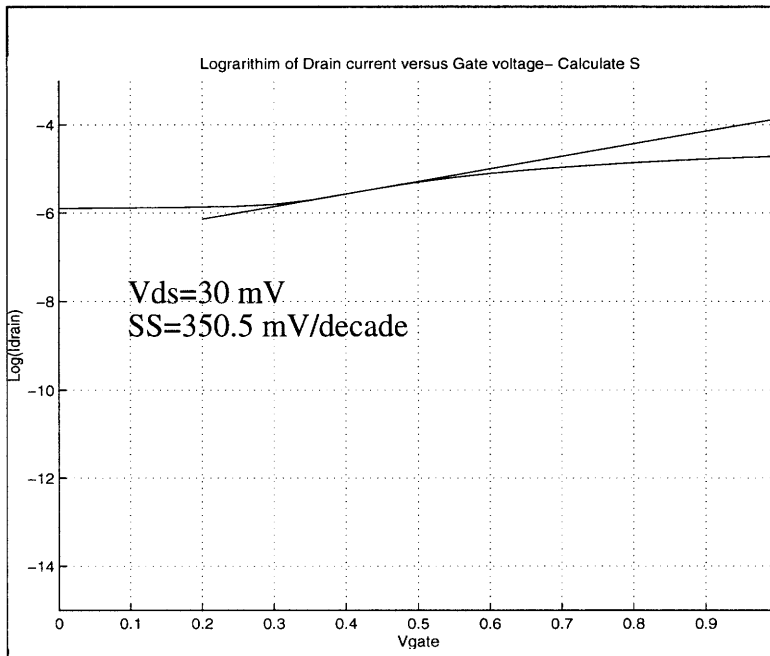
Figure 2.6: SOI3S SS Calculation
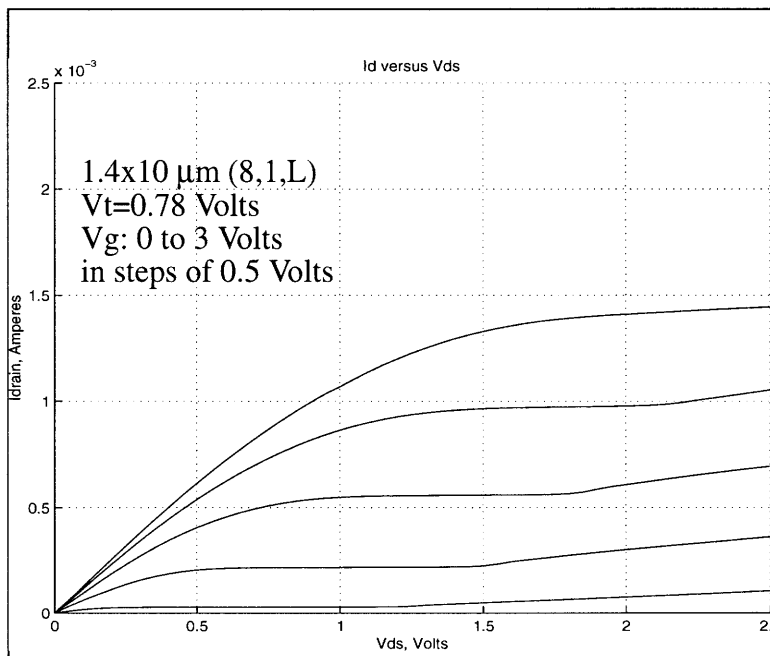
Figure 2.7: SOI6S IV Calculation
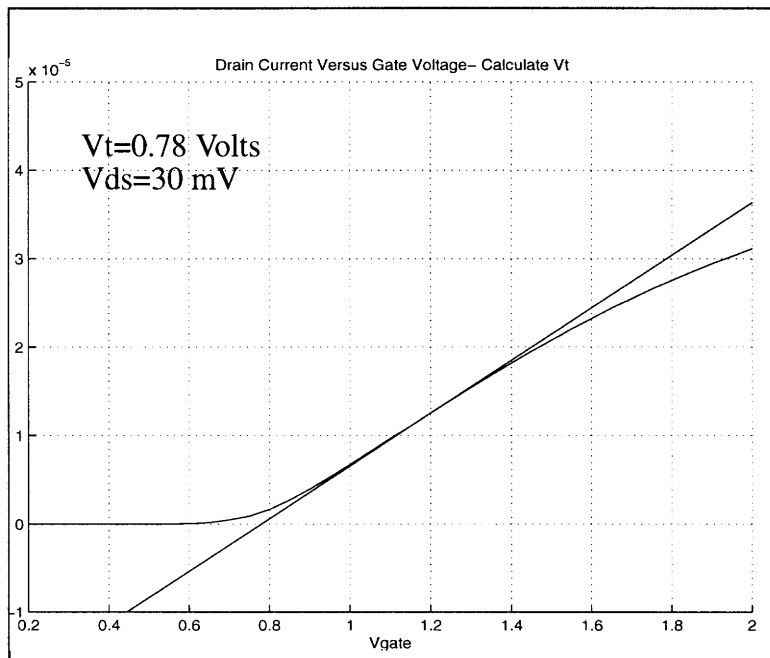
Figure 2.8: SOI6S Vt Calculation
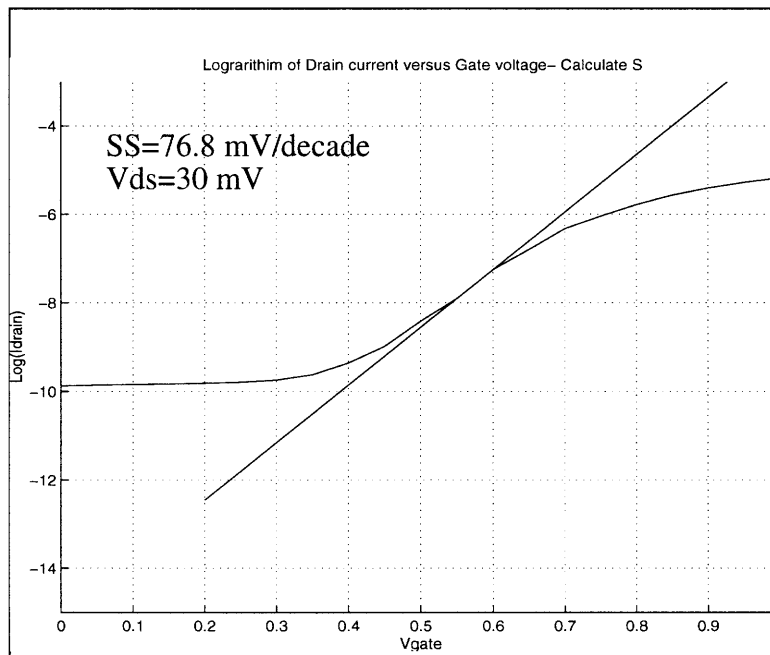
Figure 2.9: SOI6S SS Calculation
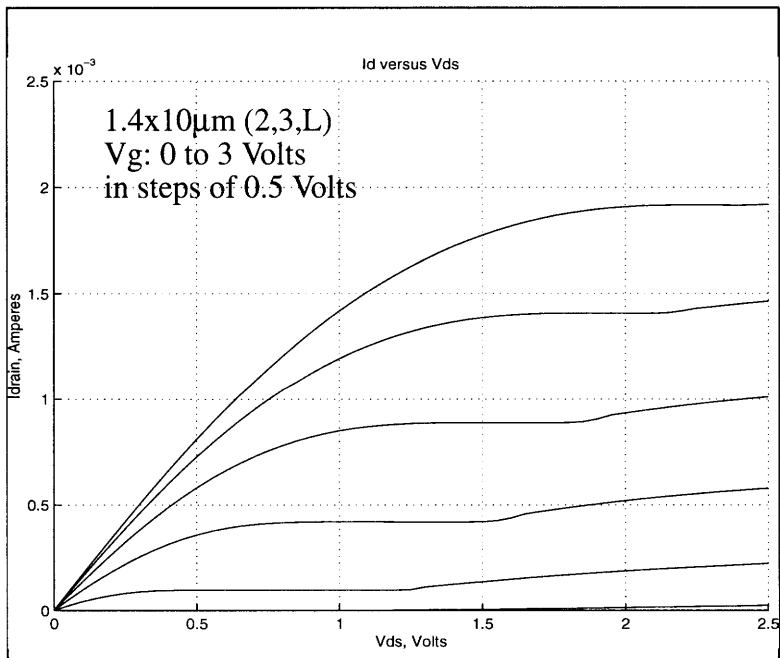
Figure 2.10: IV SOIAS10
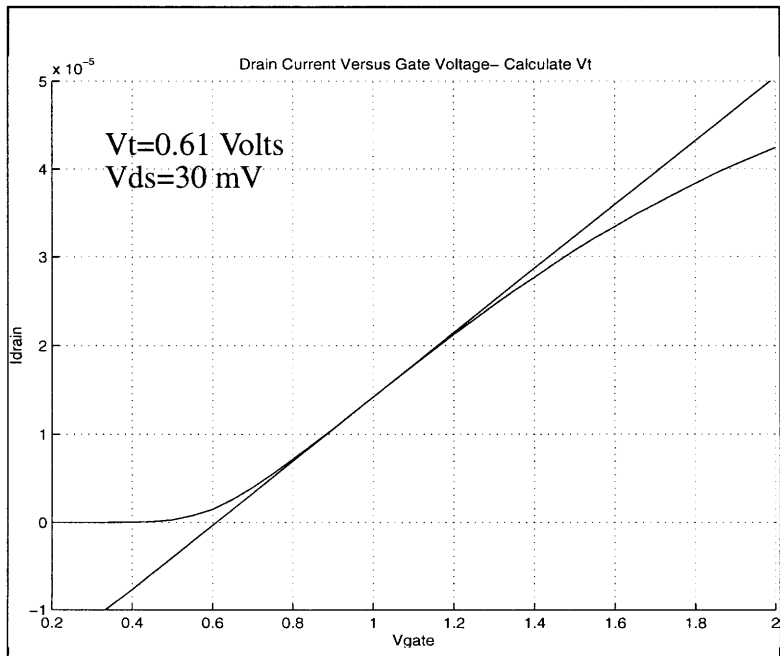
Figure 2.11: SOIAS10 Vt Calculation
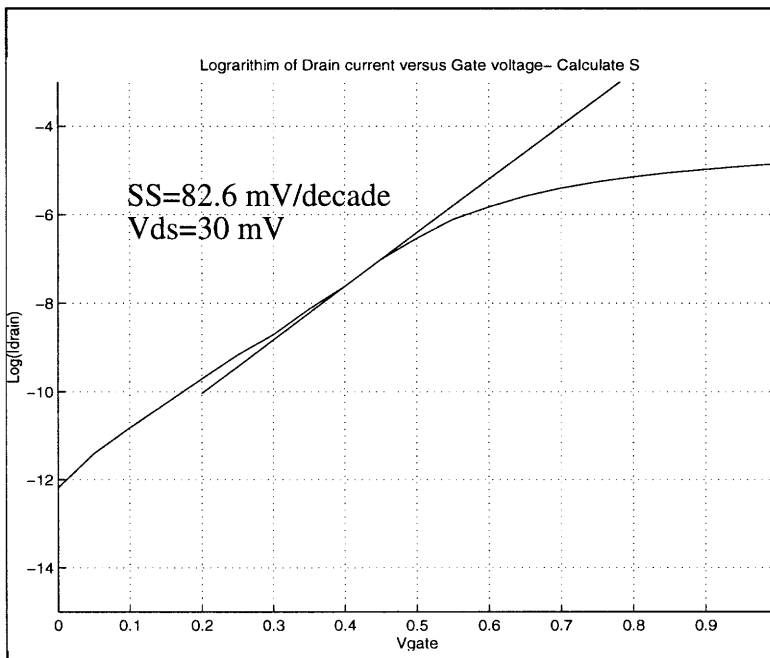
Figure 2.12: SOIAS10 SS Calculation
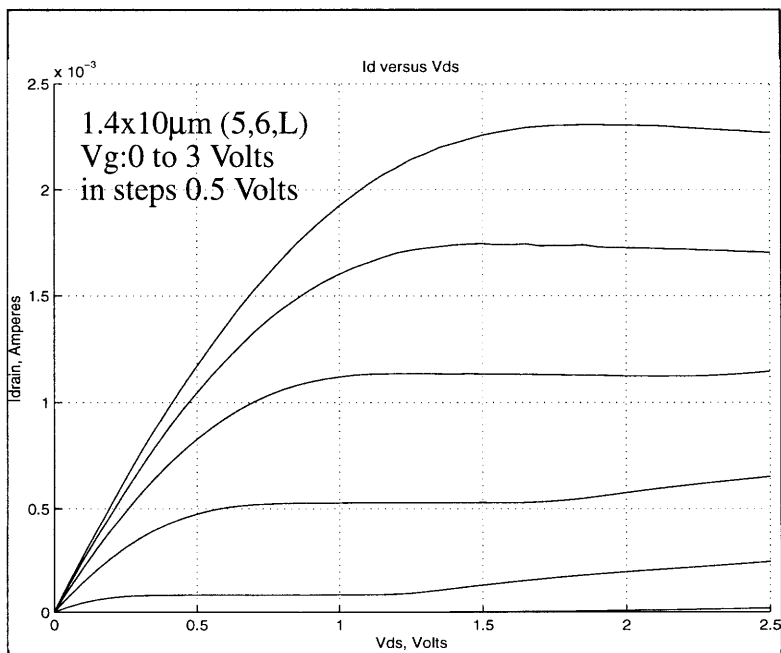
Figure 2.13: IV SOIAS2

121
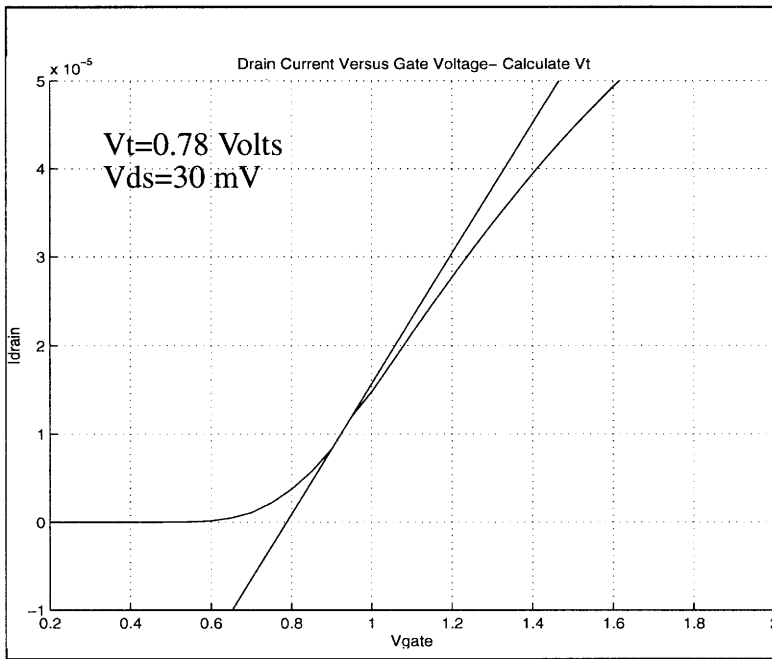
Figure 2.14: Vt Calculation SOIAS2
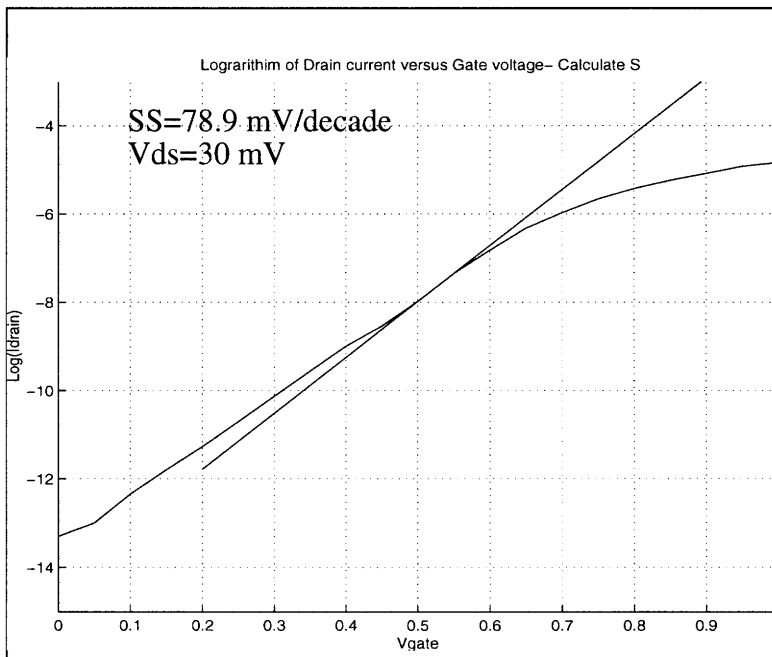
Figure 2.15: SOIAS2 SS Calculation
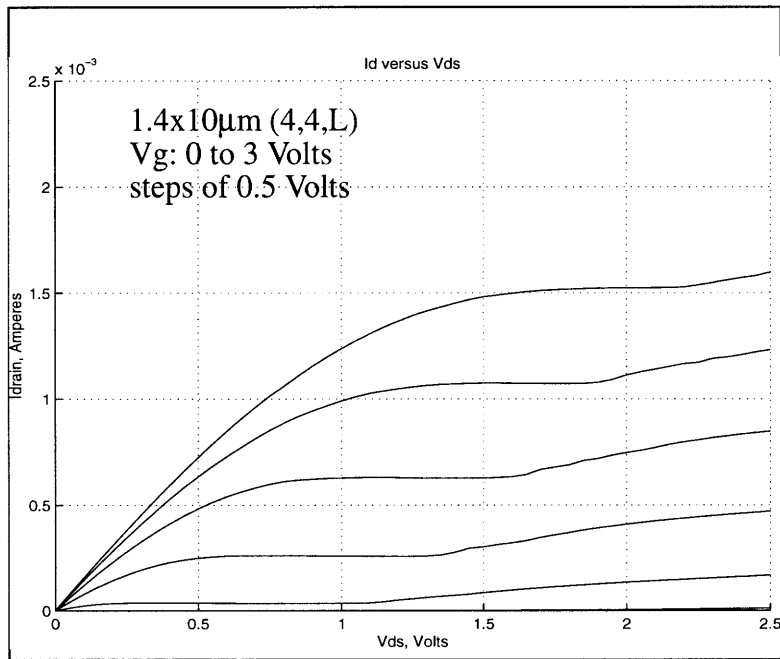
Figure 2.16: SOIAS3 IV Curves
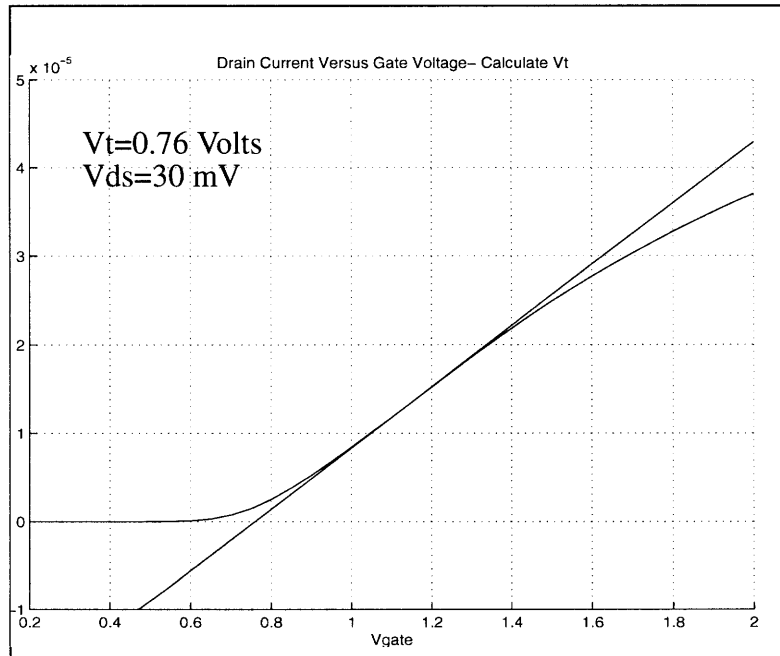
Figure 2.17: SOIAS3 Vt Calculation

123
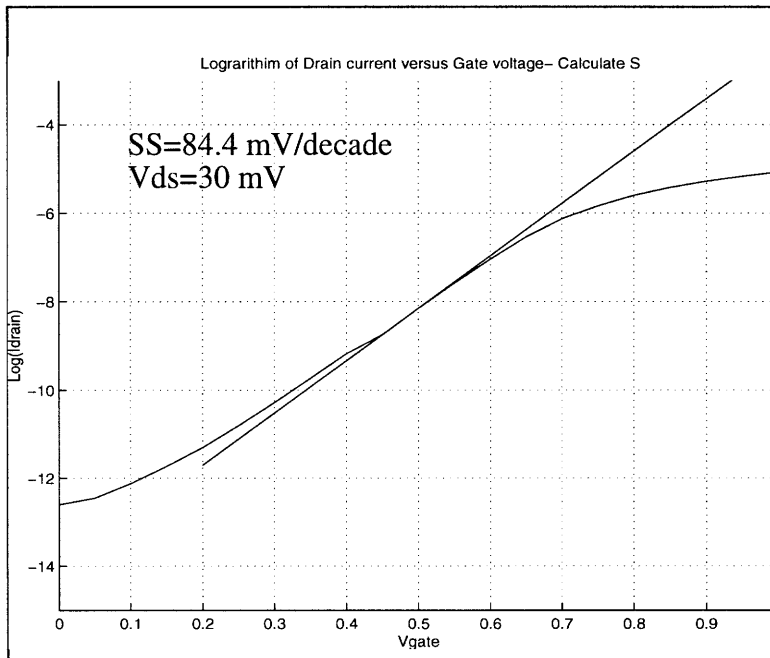
Figure 2.18: SOIAS3 SS Calculation
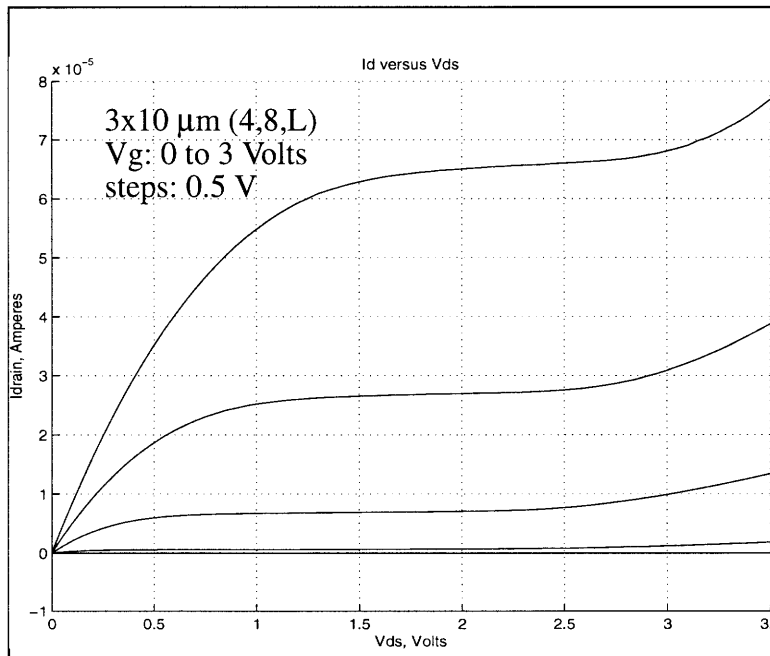
Figure 2.19: SOIAS6 IV Curves

124
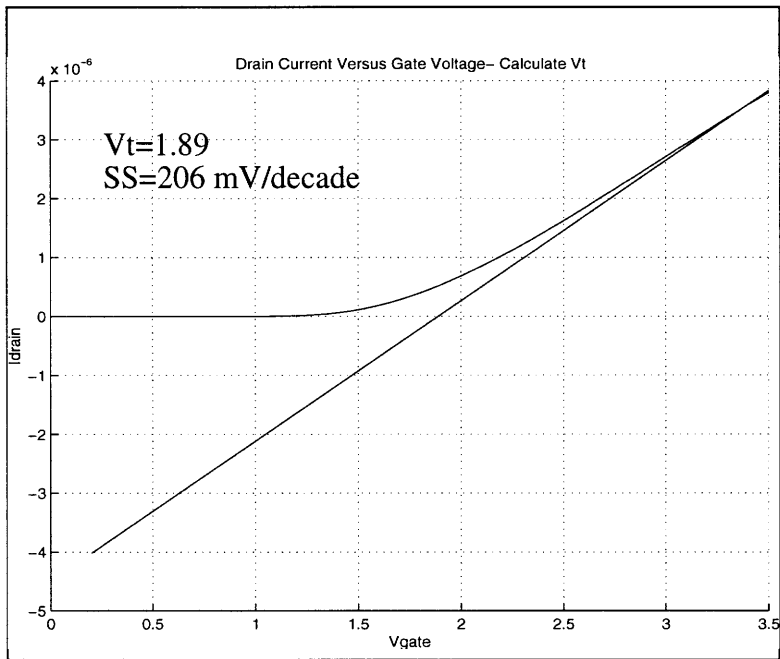
Figure 2.20: SOIAS6 Vt Calculation
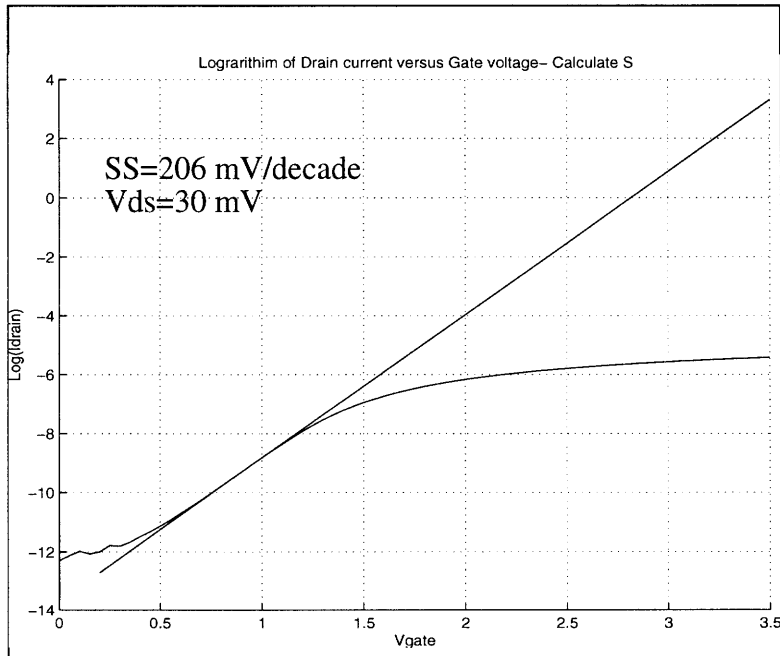
Figure 2.21: SOIAS6 SS Calculation
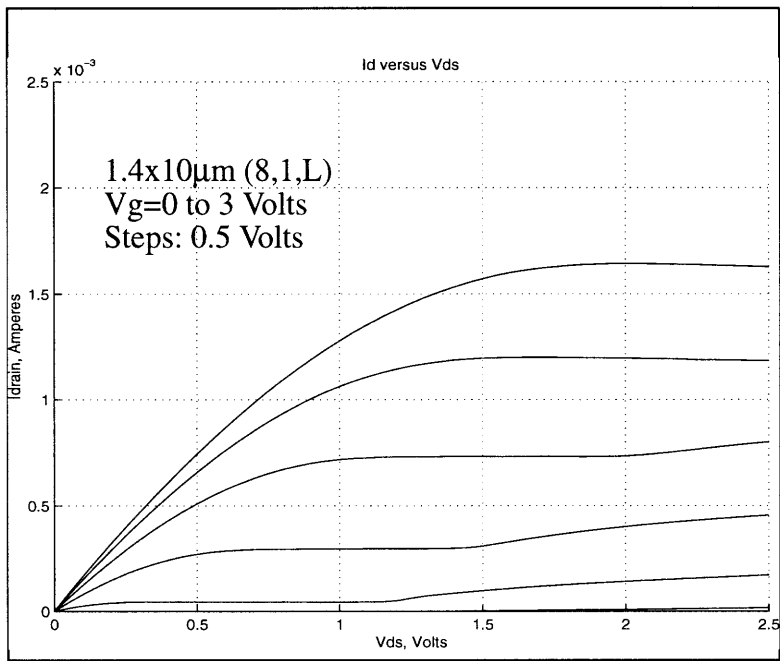
Figure 2.22: SOIAS7 IV Curves
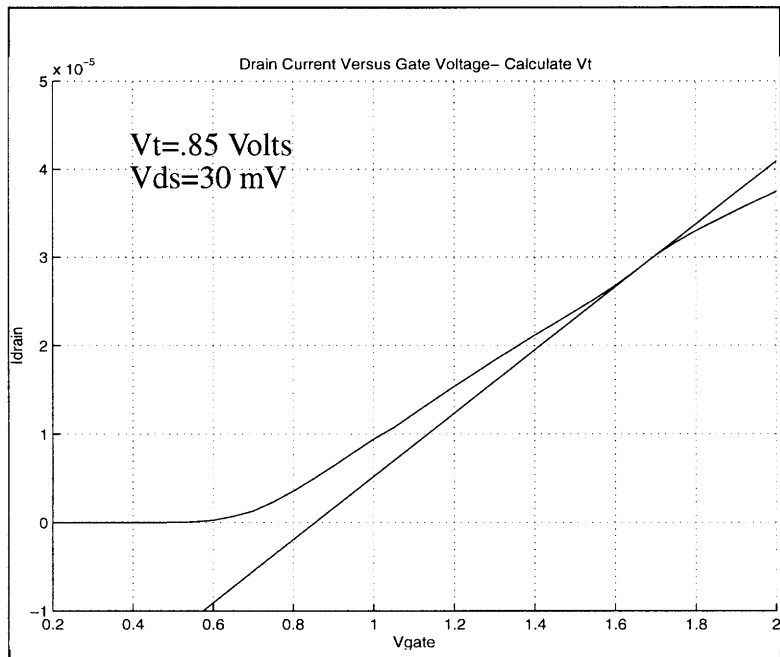
Table 2.1: SOIAS7 Vt Calculation
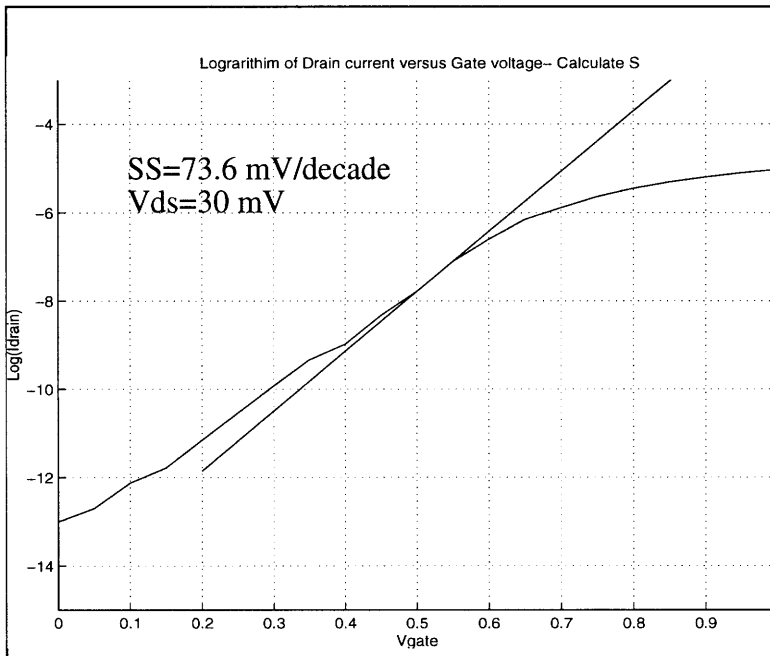
Figure 2.23: SOIAS7 SS Calculation
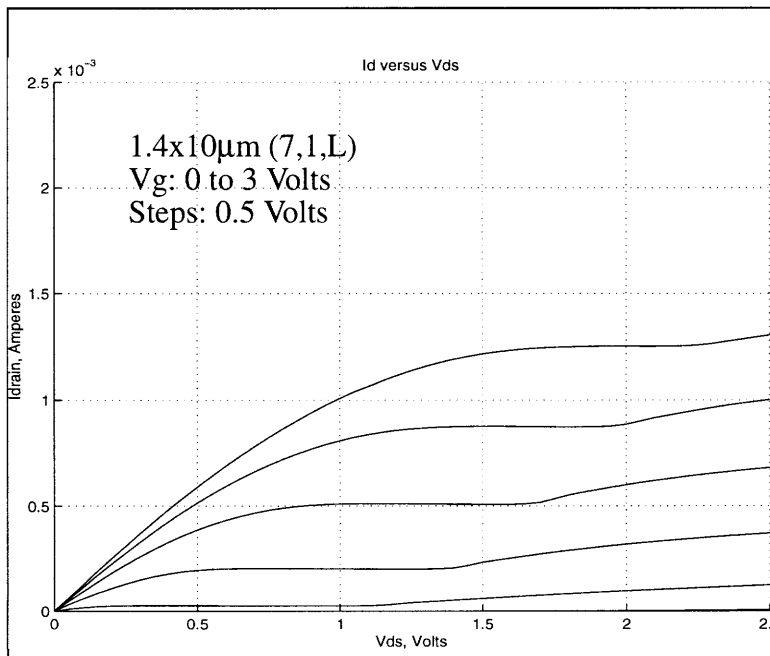
Figure 2.24: SOIAS8 IV Curves
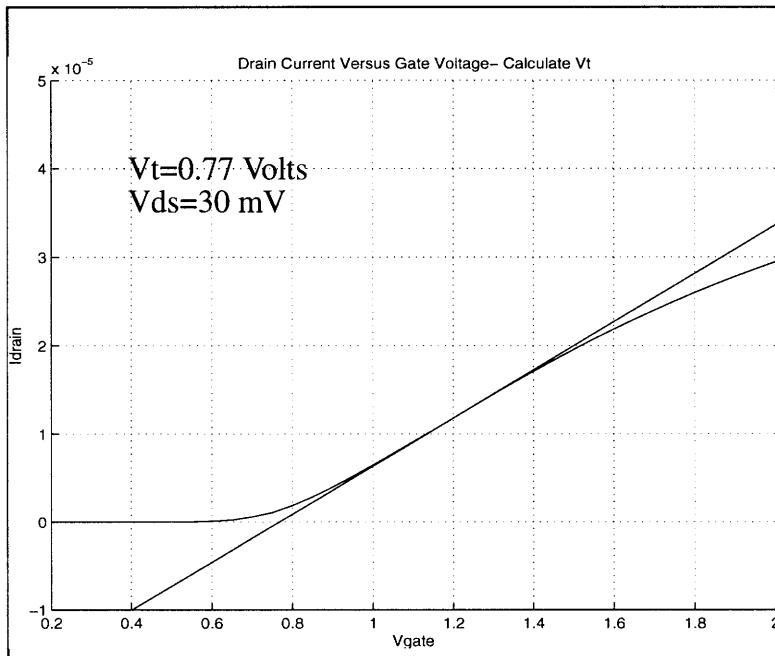
Figure 2.25: SOIAS8 Vt Calculation
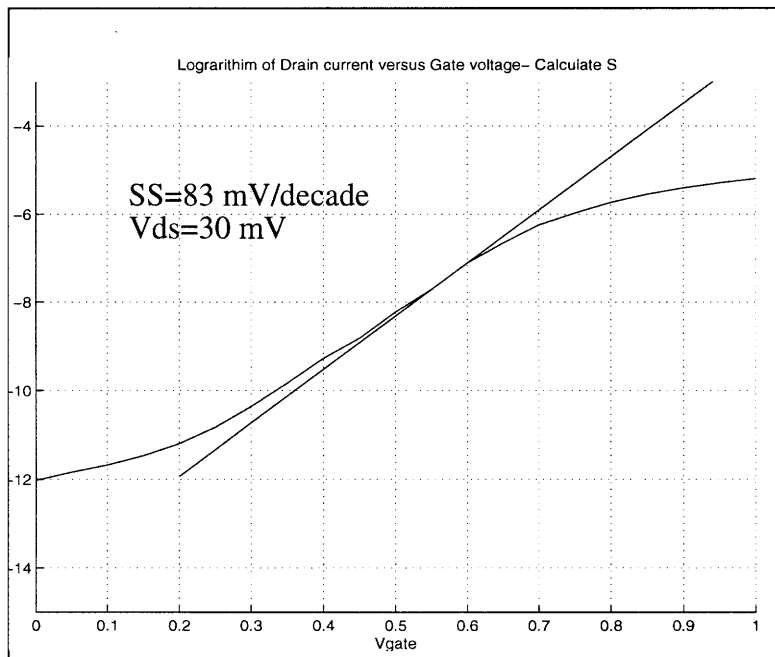
Figure 2.26: SOIAS8 SS Calculation

B.2 Charge Pumping Plots- Dit signature/Dit determination
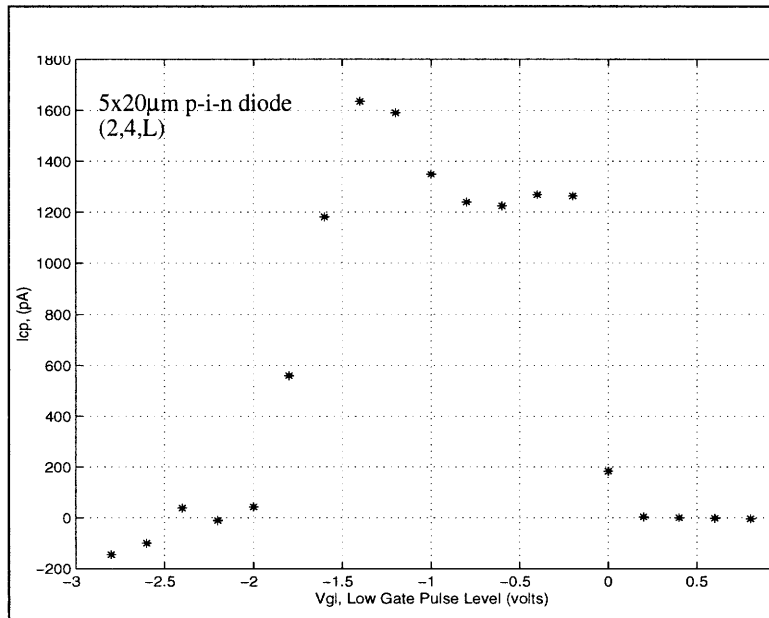
Figure 2.1: SOIAS2 Signature
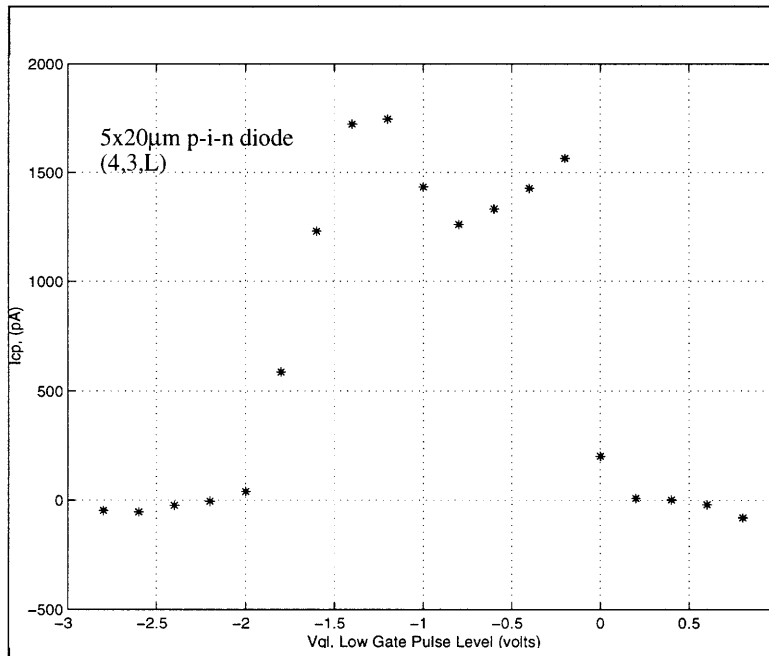
Figure 2.2: SOIAS3 Signature
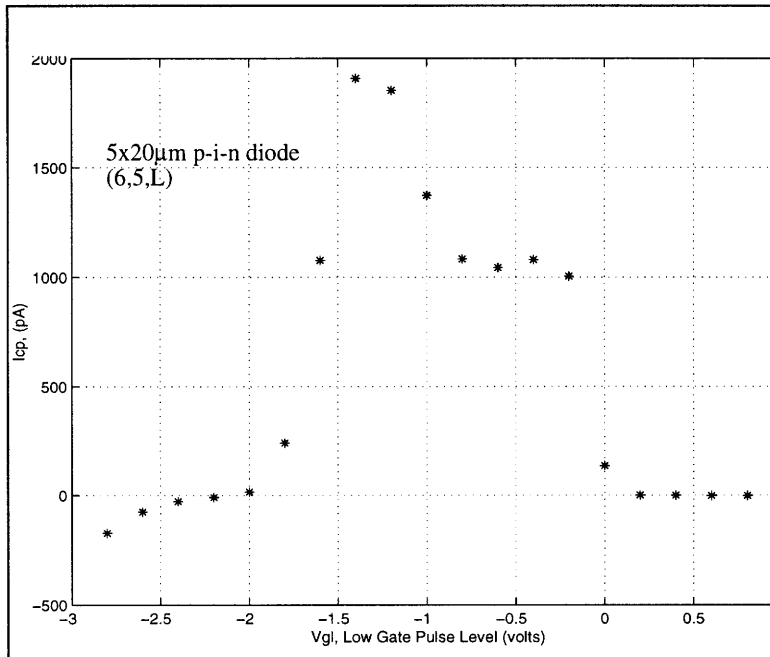
Figure 2.3: SOIAS7 Signature
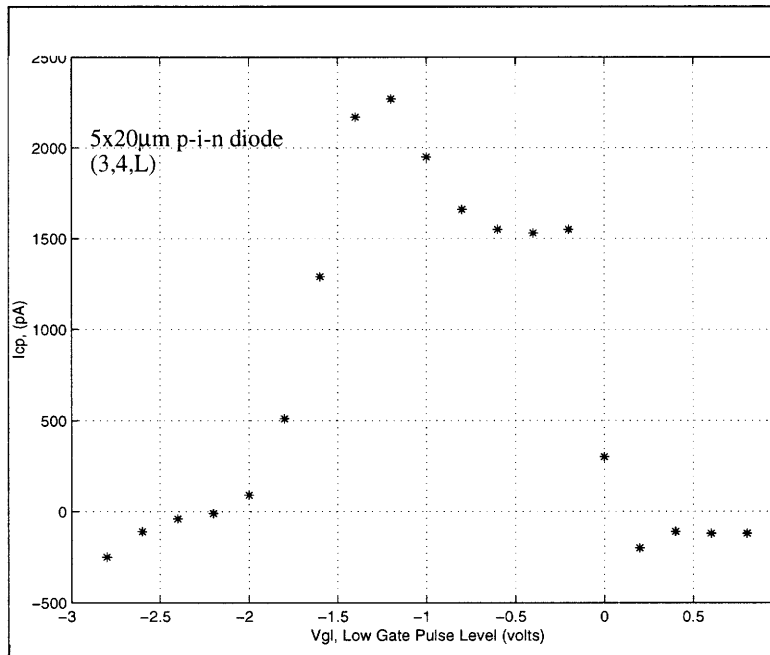
Figure 2.4: SOIAS8 Signature

130
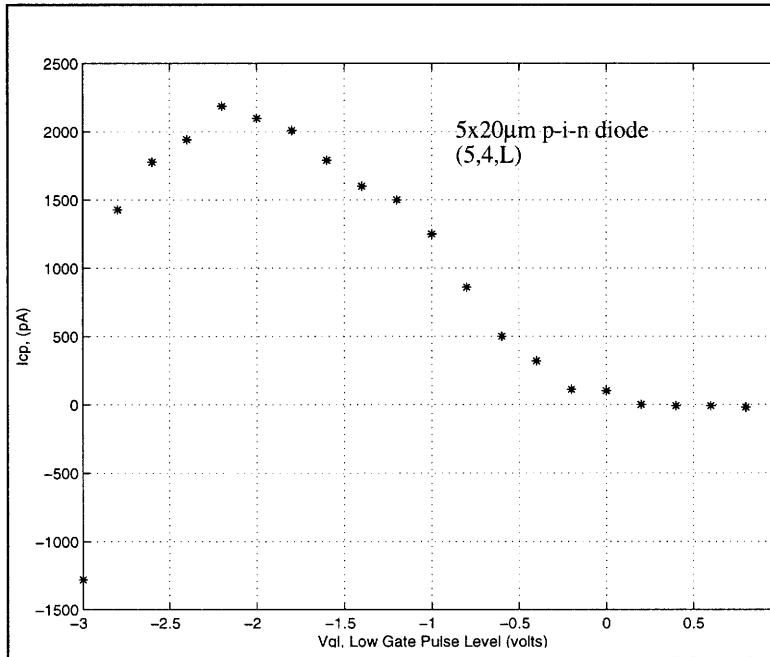
Figure 2.5: SOI3S Signature
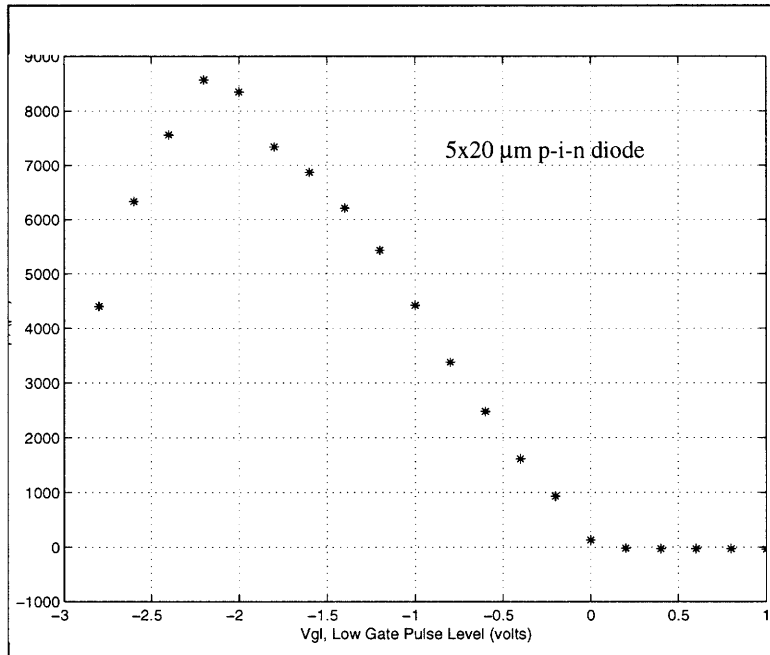
Figure 2.6: SOI6S Signature
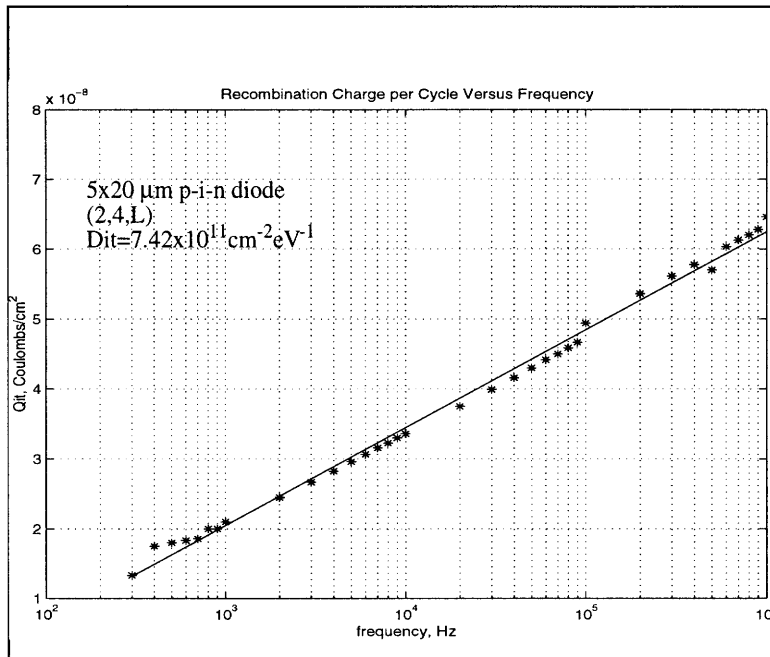
Figure 2.7: SOIAS2 D_{it} Determination
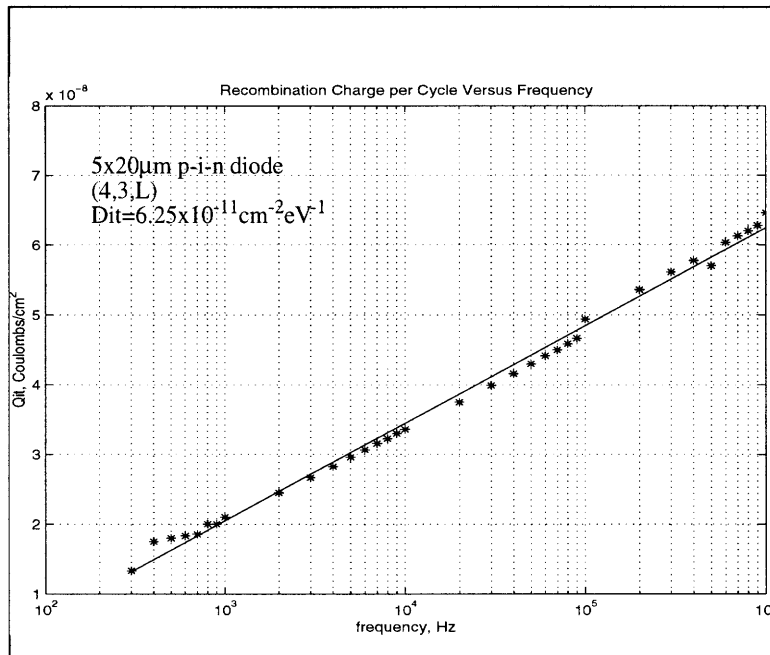
Figure 2.8: SOIAS3 D_{it} Determination
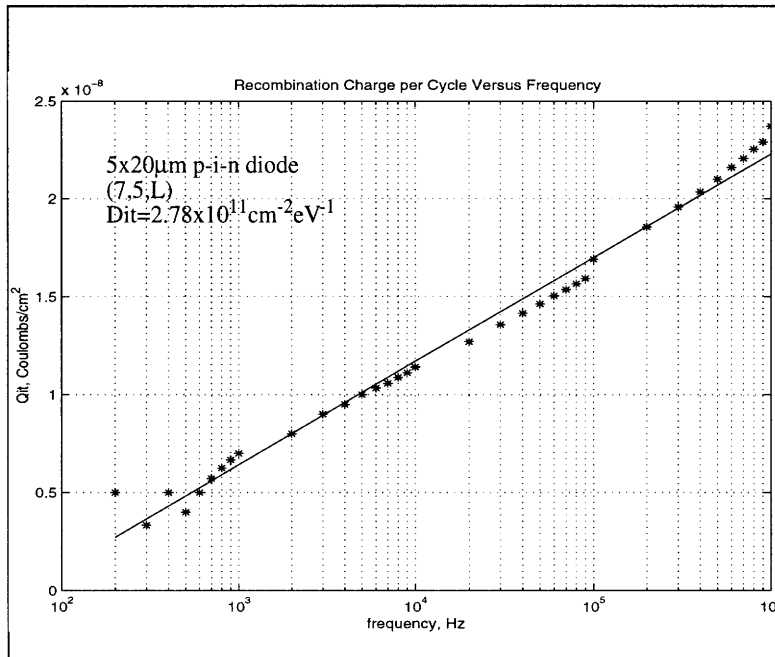
Figure 2.9: SOIAS7 D_{it} Determination
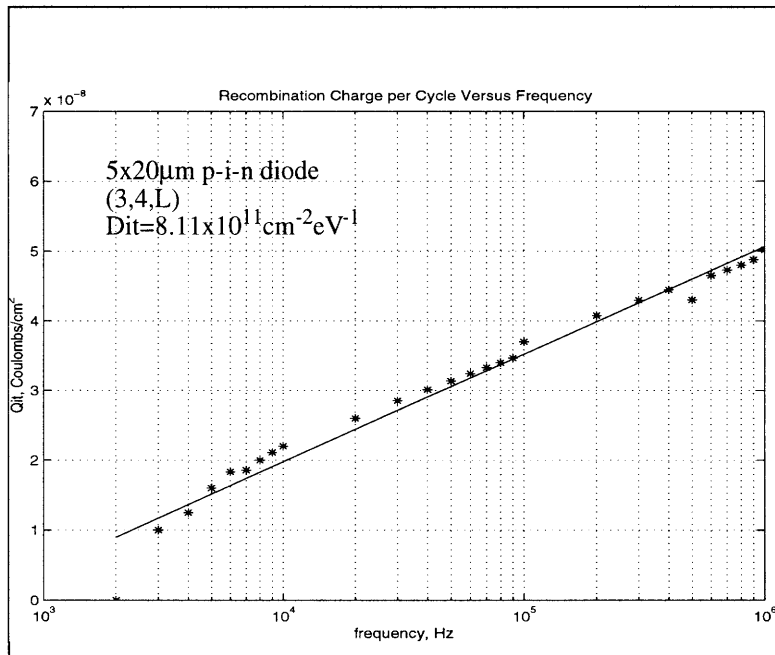
Figure 2.10: SOIAS8 D_{it} Determination
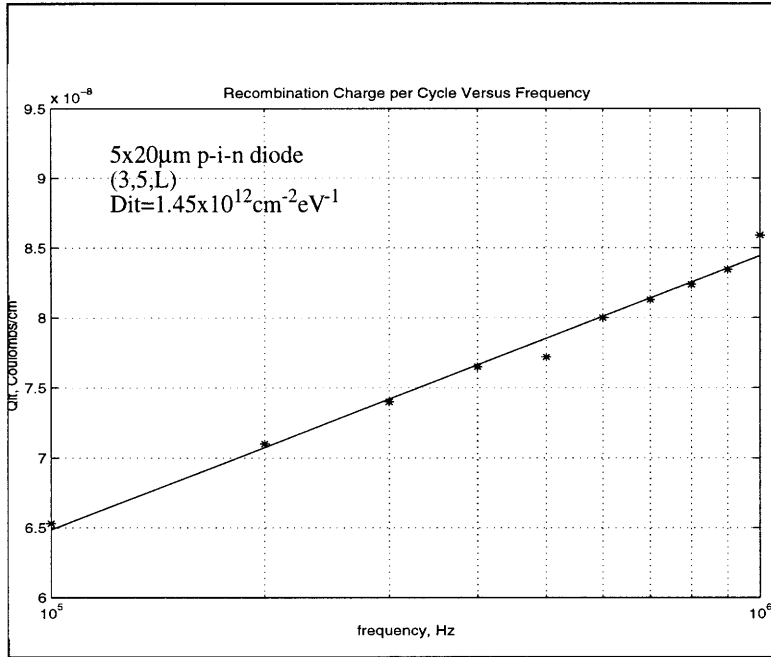
Figure 2.11: SOIAS10 D_{it} Determination
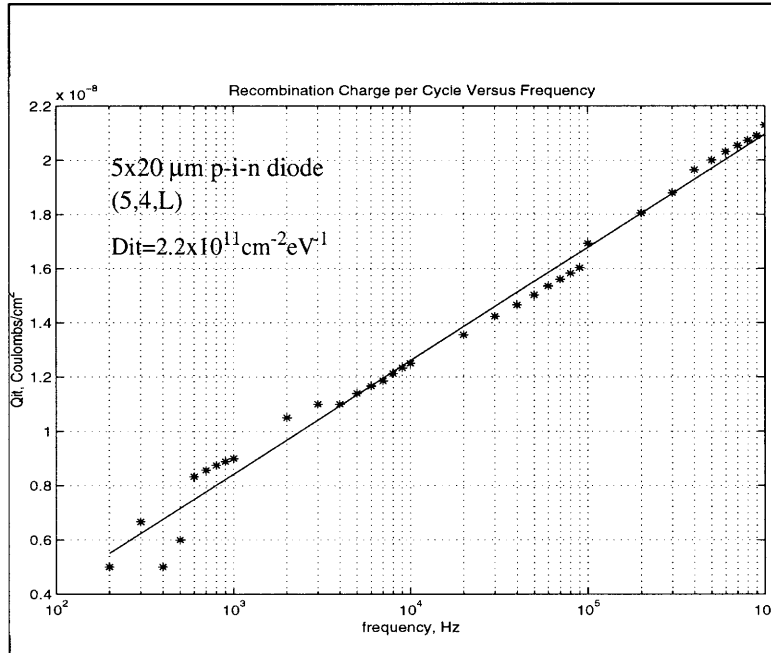
Figure 2.12: SOI3S D_{it} Determination

x 10⁻⁸

Recombination Charge per Cycle Versus Frequency
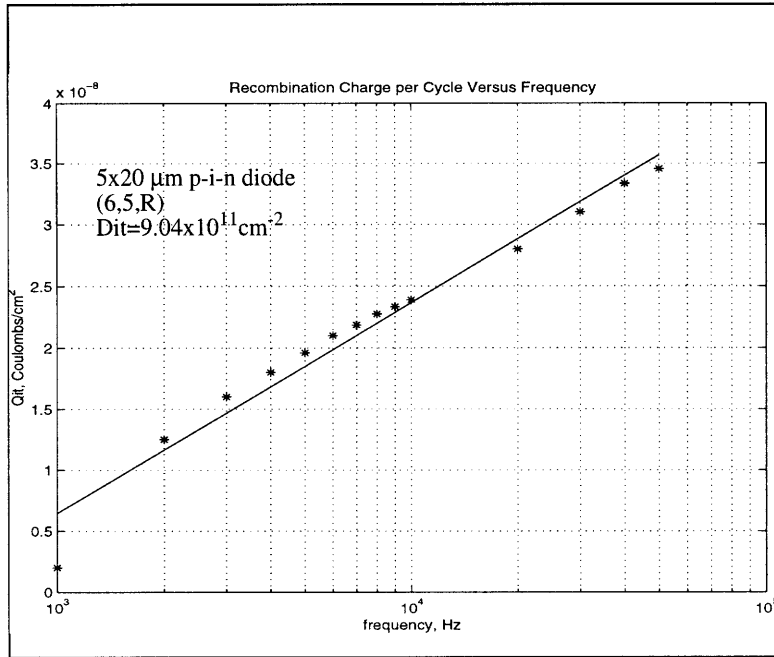
5x20 μm p-i-n diode
(6,5,R)
Dit=9.04x10¹¹cm⁻²

Qit, Coulombs/cm²

frequency, Hz

Figure 2.13: SOI6S D_{it} Determination